

## 3/2/1-Phase Synchronous-Rectified Buck Controller for Mobile GPU Power

### General Description

The uP9509S is a 3/2/1-phase synchronous-rectified buck controller specifically designed to work with 3V ~ 26V input voltage and deliver high quality output voltage for high-performance graphic processor power.

The uP9509S adopts proprietary RCOT™ technology, providing flexible selection of output LC filter and excellent transient response to load and line change.

The uP9509S supports NVIDIA Open Voltage Regulator-2+ with PWMVID feature. The PWMVID input is buffered and filtered to generate accurate reference voltage, and the output voltage is precisely regulated to the reference input.

The uP9509S integrates two bootstrapped MOSFET gate drivers and one PWM output achieving optimal balance between cost and flexibility. The uP9509S uses MOSFET  $R_{DS(ON)}$  current sensing for channel current balance.

Other features include accurate and reliable over current limit protection, adjustable on-time setting, power saving control input, and power good output. This part is available in a VQFN4x4 - 24L package.

### Ordering Information

Order Number	Package Type	Top Marking
uP9509SQAG	VQFN4x4 - 24L	uP9509S

Note:

(1) Please check the sample/production availability with uPI representatives.

(2) uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

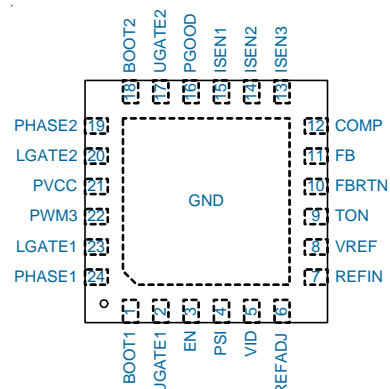
### Features

- Support NVIDIA's Open VReg Type-2+ PWMVID Technology
- Wide Input Voltage Range 3V ~ 26V
- Robust Constant On-Time Control
- 3/2/1 Phase Operation
- Two Integrated MOSFET Drivers with Shoot-Through Protection and Internal Bootstrap Schottky Diode
- Adjustable Current Balancing by  $R_{DS(ON)}$  Current Sensing
- Adjustable Operation Frequency
- External Compensation
- Dynamic Output Voltage Adjustment
- Adjustable Per-Phase Over Current Limit
- Adjustable Soft-Start Time
- Power Good Indication
- Over Voltage Protection
- Under Voltage Protection
- Over Temperature Protection
- RoHS Compliant and Halogen Free

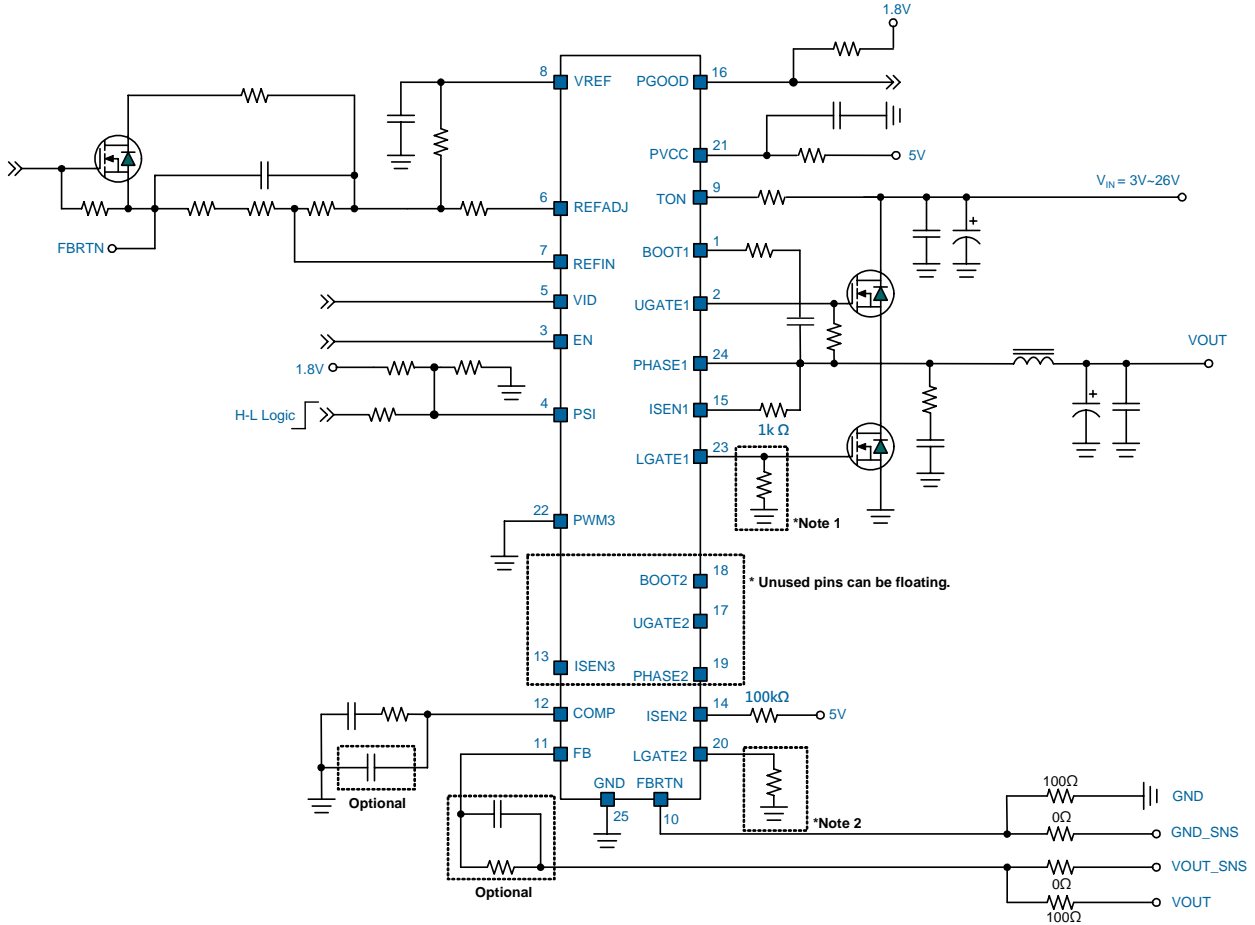
### Applications

- Middle-High End GPU Core Power
- High End Notebook PC Memory Core Power
- Low Output Voltage, High Power Density DC-DC Converters
- Voltage Regulator Modules

### Pin Configuration

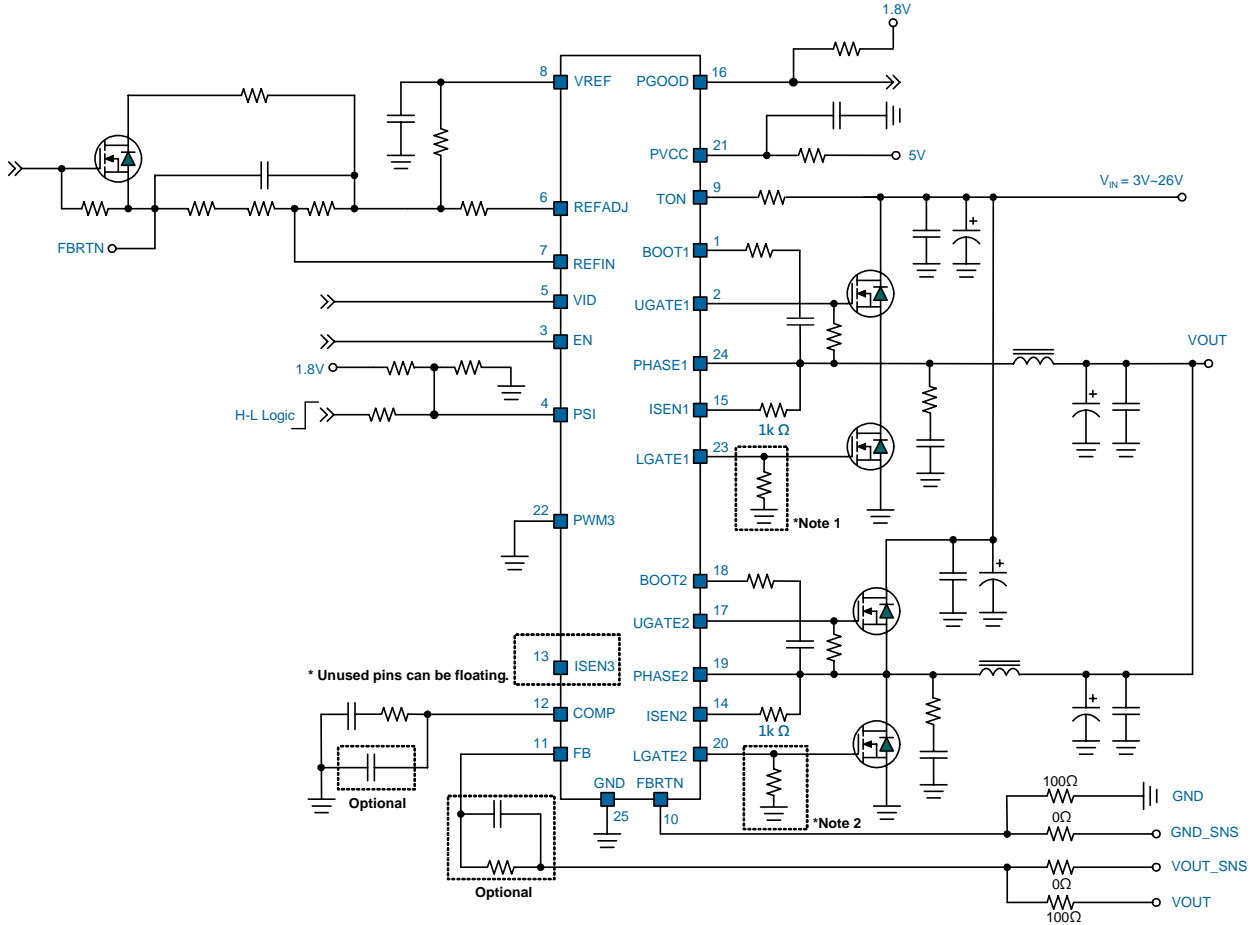


**1-Phase Mode**

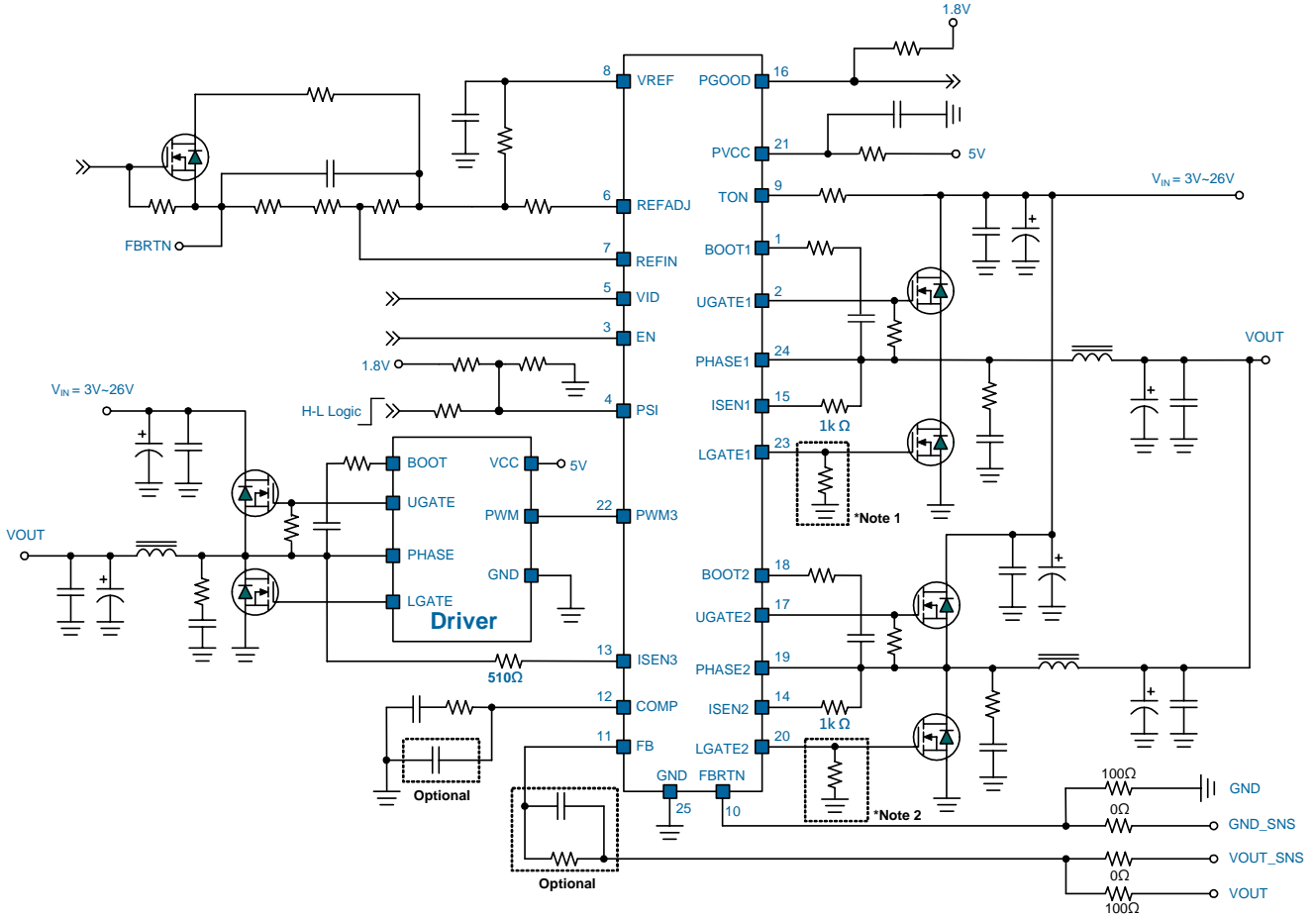


\*Note 1 : Programs per-phase over current limit threshold.  
\*Note 2 : Programs output ramp-up time during power on.

**2-Phase Mode**



**3-Phase Mode**

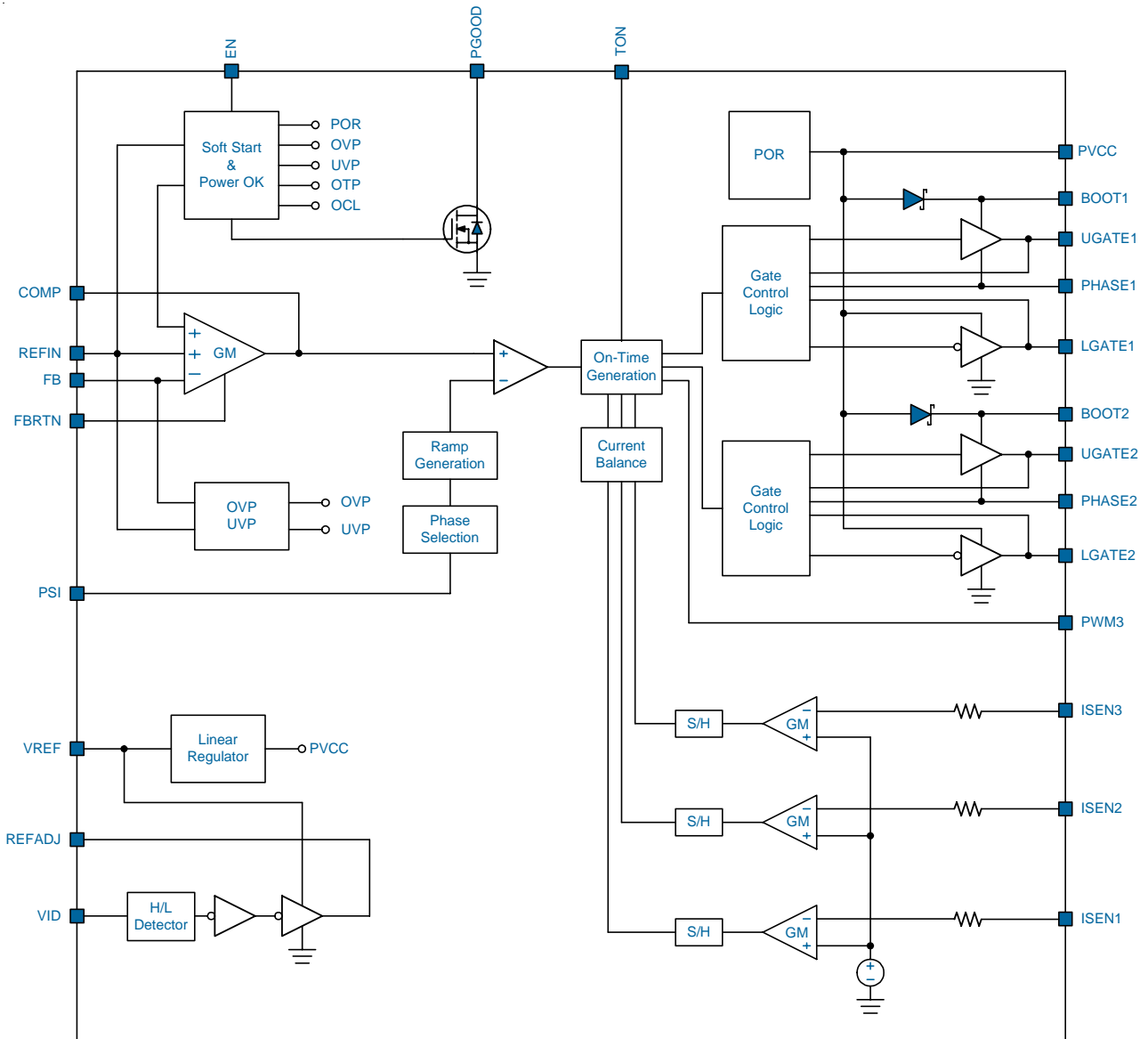


\*Note 1 : Programs per-phase over current limit threshold.  
\*Note 2 : Programs output ramp-up time during power on.

**Functional Pin Description**

No.	Name	Pin Function
1	BOOT1	<b>BOOT for Phase 1.</b> Connect a capacitor from this pin to PHASE1 to form a bootstrap circuit for upper gate driver of the phase 1.
2	UGATE1	<b>Upper Gate Driver for Phase 1.</b> Connect this pin to the gate of phase 1 upper MOSFET.
3	EN	<b>Enable.</b> Chip enable.
4	PSI	<b>Power Saving Input.</b> An input pin receiving power saving control signal from GPU. PSI input voltage determines the controller operating mode. Do not leave this pin open.
5	VID	<b>VID.</b> PWMVID input pin.
6	REFADJ	<b>Reference Adjustment.</b> PWMVID output pin. Connect this pin with an RC integrator to generate REFIN voltage.
7	REFIN	<b>Reference Input.</b> Connect this pin to an external reference voltage through a resistor or connect to the output of the REFADJ circuit.
8	VREF	<b>Reference Voltage.</b> 2V LDO voltage output pin. Connect an at least 1uF decoupling capacitor between this pin and GND.
9	TON	<b>On-time Setting Pin.</b> Connect a resistor from this pin to VIN to set the on-time of the upper MOSFET. Do not add any extra capacitor to this pin.
10	FBRTN	<b>Return for the Reference Circuit.</b> Connect this pin to the ground point where output voltage is to be regulated.
11	FB	<b>Feedback Pin.</b> This pin is the inverting input of the error amplifier.
12	COMP	<b>Compensation Output.</b> This pin is the output of the error amplifier. Connect an RC network from this pin to GND to compensate the voltage control loop.
13	ISEN3	<b>ISEN3.</b> Connect this pin to the PHASE3 pin <b>ONLY</b> with 510Ω to sense phase 3 output current. <b>DO NOT use other resistor.</b>
14	ISEN2	<b>ISEN2.</b> Connect this pin to the PHASE2 pin with a resistor to sense phase 2 output current.
15	ISEN1	<b>ISEN1.</b> Connect this pin to the PHASE1 pin with a resistor to sense phase 1 output current.
16	PGOOD	<b>Power Good Indication.</b> Open-drain structure. Connect this pin to a voltage source with a pull-up resistor.
17	UGATE2	<b>Upper Gate Driver for Phase 2.</b> Connect this pin to the gate of phase 2 upper MOSFET.
18	BOOT2	<b>BOOT for Phase 2.</b> Connect a capacitor from this pin to PHASE2 to form a bootstrap circuit for upper gate driver of the phase 2.
19	PHASE2	<b>Phase Pin for Phase 2.</b> This pin is the return path of upper gate driver for phase 2. Connect a capacitor from this pin to BOOT2 to form a bootstrap circuit for upper gate driver of the phase2.
20	LGATE2	<b>Lower Gate Driver for Phase 2.</b> Connect this pin to the gate of phase 2 lower MOSFET.
21	PVCC	<b>Supply Input for the IC.</b> Voltage power supply of the IC. Connect this pin to a 5V supply and decouple using at least a 1uF ceramic capacitor.
22	PWM3	<b>PWM Output of Phase 3.</b> Connect this pin to the PWM input pin of the companion gate driver. Connect this pin to GND to configure this device as a 2-phase controller.
23	LGATE1	<b>Lower Gate Driver for Phase 1.</b> Connect this pin to the gate of phase 1 lower MOSFET.
24	PHASE1	<b>Phase Pin for Phase 1.</b> This pin is the return path of upper gate driver for phase 1. Connect a capacitor from this pin to BOOT1 to form a bootstrap circuit for upper gate driver of the phase 1.
	Exposed Pad	<b>Ground.</b> Tie this pin to ground island/plane through the lowest impedance connection available.

**Functional Block Diagram**



## Functional Description

### Supply Input and Power On Reset

The uP9509S receives supply input from PVCC pin to provide current to gate drivers and internal control circuit. PVCC is continuously monitored for power on reset. The POR level is typical 4.1V at rising. The TON pin voltage is used for on-time calculation and should be connected to the supply input of power stage.

The uP9509S integrates floating MOSFET gate driver that are powered from the PVCC pin. A bootstrap Schottky diode is embedded to facilitates PCB design and reduce the total BOM cost. No external Schottky diode is required in real applications.

### Phase Number of Operation (Hardware Setting)

The uP9509S supports 3/2/1 phase operation. The maximum phase number of operation is determined by checking the PWM3 and ISEN2 status when POR. Connect PWM3 pin to GND and ISEN3 floating for maximum 2-phase operation; Connect ISEN2 pin to PVCC with 100kΩ resistor and connect PWM3 to GND for maximum 1-phase operation. When configured to 1-phase operation, the components of PHASE2/PHASE3 can be unstuffed. Once selected, the maximum phase number of operation is latched and can only be changed at the next POR.

Table 1. Operation Phase Number Settings

Configuration	Pin Connection, Pull High/Low to Target			
	PWM3	ISEN3	ISEN2	ISEN1
2+1 phase	--	--	--	--
2 phase	GND	Floating	--	--
1 phase	GND	Floating	PVCC	--

Note 1: "--" denotes normal connection.  
 Note 2: Use 100kΩ pull up resistor when pull up to PVCC  
 Note 3: Strictly follow the table for phase disable. Incorrect pin pull up/down connection may cause catastrophic fault during start up.

### Constant On-Time Setting

The uP9509S adopts a compensated constant-on-time control scheme. A resistor  $R_{TON}$  connected to TON pin programs the constant on time according to the equation:

$$T_{ON}(ns) = \frac{V_{OUT}}{V_{IN}} \times \frac{R_{TON}}{9} \times 100 \quad (ns)$$

where  $R_{TON}$  is in kΩ,  $V_{IN}$  is the supply input voltage and  $V_{OUT}$  is the output voltage.

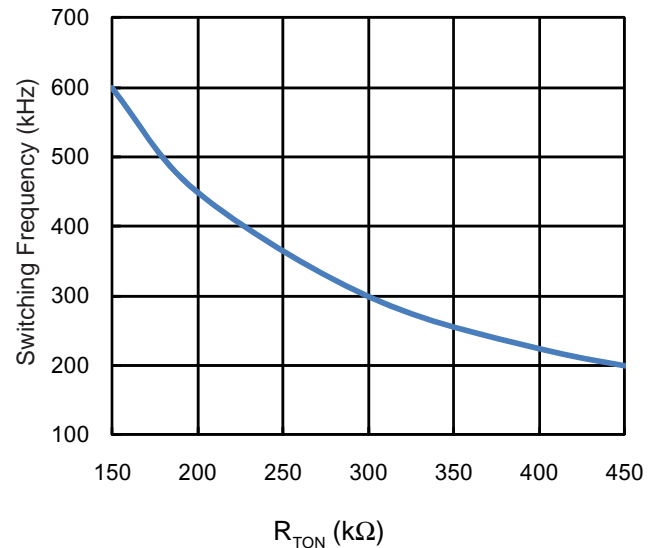


Figure 1. Switching Frequency vs.  $R_{TON}$

### Voltage Control Loop and PWMVID Function

Figure 2 illustrates the voltage control loop of the uP9509S. FB and REFIN are negative and positive inputs of the Error Amplifier respectively. The Error Amplifier modulates the COMP voltage  $V_{COMP}$  of buck converter to force FB voltage  $V_{FB}$  follows  $V_{REFIN}$ .

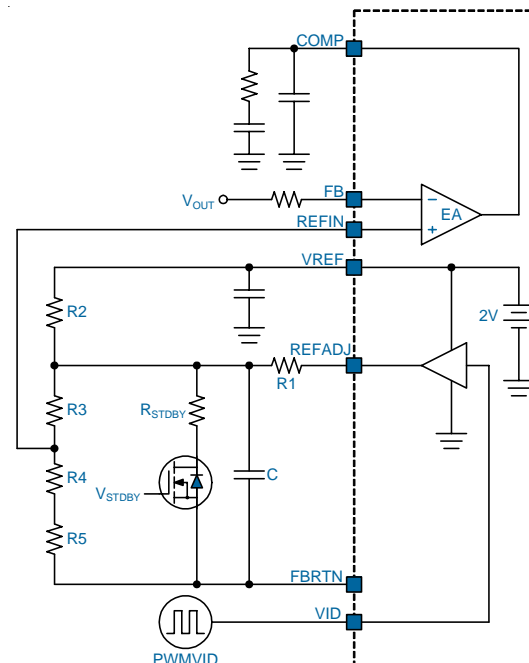


Figure 2. Voltage Control Loop

## Functional Description

The PWMVID signal from GPU is applied to the VID pin, which is the input pin of the internal buffer. This buffer plays the role of level shifting, and the output of this buffer is injected into the external RC integrator to generate REFIN voltage, which can be calculated as:

$$V_{REFIN} = V_{VREF} \times D \times \frac{R2 // (R3 + R4 + R5)}{R1 + R2 // (R3 + R4 + R5)} \times \frac{R4 + R5}{R3 + R4 + R5} + V_{VREF} \times \frac{R1 // (R3 + R4 + R5)}{R2 + R1 // (R3 + R4 + R5)} \times \frac{R4 + R5}{R3 + R4 + R5}$$

where  $V_{REFIN,DC}$  is the DC voltage of REFIN,  $V_{VREF}$  is the voltage of VREF (typically 2V), and D is the duty cycle of PWMVID input.

### Boot Voltage and Standby Mode

The new generation PWMVID structure includes two operation modes other than normal operation: boot mode and standby mode. During boot mode, the GPU stops sending PWMVID signal and the input of the PWMVID buffer is floating. The REFADJ pin enters high impedance state after the VID pin enters tri-state region, and the REFIN voltage can then be calculated as:

$$V_{REFIN,BOOT} = V_{VREF} \times \frac{R4 + R5}{R2 + R3 + R4 + R5}$$

During standby mode, other than GPU stopping the PWMVID transaction, an external system standby signal additionally controls the entry of standby mode. An additional external switch should be connected in parallel with the original PWMVID resistors as shown in Figure 3 to generate the standby mode voltage:

$$V_{REFIN,STDBY} = V_{VREF} \times \frac{(R3 + R4 + R5) // R_{STDBY}}{R2 + (R3 + R4 + R5) // R_{STDBY}} \times \frac{R4 + R5}{R3 + R4 + R5}$$

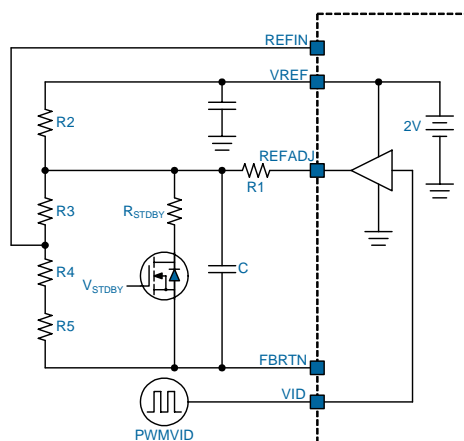


Figure 3. Standby Mode Configuration

### Channel Current Balance

The uP9509S senses phase currents for current balance by the means of on-resistance of power stage low-side MOSFET as shown in Figure 4.

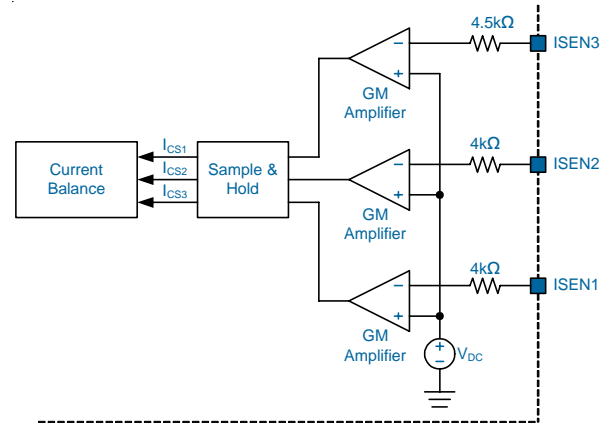


Figure 4.  $R_{DS(ON)}$  Current Sensing Scheme

The GM amplifier senses the voltage drop across the low-side MOSFET and converts it into current signal each time it turns on. The sampled and held current is expressed as:

$$I_{CSX} = \frac{(I_{LX} \times R_{DS(ON)} + V_{DC})}{R_{ISENX}}$$

where  $I_{LX}$  is the phase N current in Ampere,  $R_{DS(ON)}$  is the on-resistance of low-side MOSFET of the power stage in  $m\Omega$ ,  $V_{DC}$  is an internal 30mV voltage source, and  $R_{ISENX}$  is the external sensing resistor connected at ISENx pins plus the internal resistor to ISENx pins. In this current sense mechanism, the valley of the inductor current is sampled and held. Therefore, the equivalent sensed current can be described by the following equation:

$$I_{LX\_SH} = I_{LX\_AVG} - \frac{1}{2} \times \Delta I_{LX}$$

The sensed current  $I_{LX\_SH}$  is mirrored to the current balance circuit, comparing between each other, and generating current adjusting signals for each phase. These current adjusting signals are fed to the on-time circuit of the uP9509S to separately adjust each phase on-time for the purpose of adjusting current balance.

The external  $R_{ISEN}$  resistor connected at ISEN3 pin should be 510 $\Omega$ . It can **NOT** use other resistor due to the limitation of Multi-Phase DCM and Phase3 OCL functions. If the phase current unbalance exist in actual application. Fine adjusts the  $R_{ISEN1}$  and  $R_{ISEN2}$  is allowed for phase current adjustment. However, the resistance of  $R_{ISEN1}/R_{ISEN2}$  can **NOT** be lower than 510 $\Omega$ .



**Soft-Start and Power Good**

A built-in soft-start is used to prevent surge current from power supply input during turn on. The error amplifier is a three-input device. Reference voltage  $V_{REFIN}$  or the internal soft-start voltage SS whichever is smaller dominates the behavior of the non-inverting inputs of the error amplifier. SS internally ramps up to 5VCC with a slew rate determined by  $V_{REFIN}$  after the soft start cycle is initiated. Accordingly, the output voltage will follow the SS signal and ramp up smoothly to its target level. The output voltage ramp-up time can be selected through a resistor which is connected from LGATE2 to GND. To keep LGATE2 functional setting work normally, the total capacitance from LGATE2 to GND can **NOT** larger than 12nF (including  $C_{ISS}$  capacitance of Low Side MOSFET). The output ramp-up time selection table shown as following table. Figure 5 shows the Soft Start Sequence.

Table 2. Output Ramp Up Time Setting

$R_{LG2}$	Output Voltage Ramp Up Time ( $T_{ramp}$ )
10k $\Omega$	150us
22k $\Omega$	500us
51k $\Omega$	1ms
Open	1.5ms

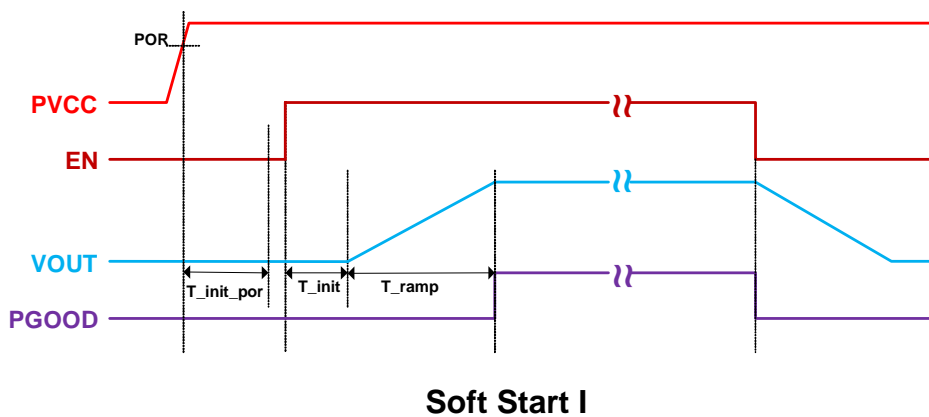
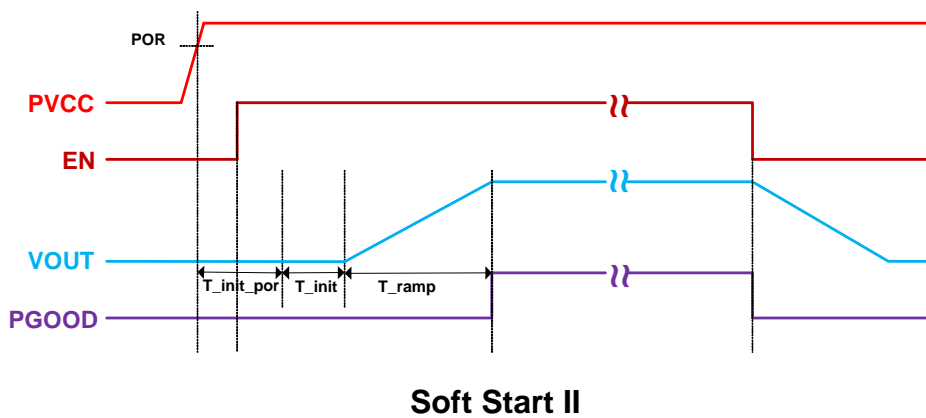


Figure 5. Soft-Start Sequence

Functional Description

Power Saving Mode

The uP9509S provides power saving features for platform designers to program platform specific power saving configuration. There are four operation modes: multi-phase CCM, multi-phase DCM, single-phase CCM, and single-phase DCM. The uP9509S switches between these four operation modes according to the input voltage level of the PSI pin. Figure 6 shows typical PSI application circuit, and Table 3 shows recommended PSI setting voltage level of four operation modes. In single-phase operation, the uP9509S auto-selects phase 1 to be the operating phase. DCM operation mode is activated by two conditions:

1. PSI voltage stays at "Single-Phase DCM" or "Multi-Phase DCM" operation mode.
2. After PGOOD goes high, VID pin has received a high or low input signal.

Once the DCM mode activated, the uP9509S automatically reduces switching frequency at light load to maintain high efficiency. As the load current decreases, the rectifying MOSFET is turned off when zero inductor current is detected, and the converter runs in discontinuous conduction mode.

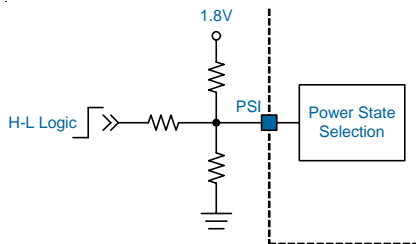


Figure 6. PSI application circuit

Table 3. Recommended PSI Setting

Operation Mode	Recommended Voltage Setting at PSI
Multi-Phase CCM	1.8V
Multi-Phase DCM	1.2V
Single-Phase CCM	0.6V
Single-Phase DCM	GND

Over Current Limit

The uP9509S monitors the inductor valley current by low side MOSFET  $R_{DS(ON)}$  when it turns on. The over current limit is triggered once the sensing current level is higher than  $V_{OC}$ . When triggered, the over current limit will keep high side MOSFET off even the voltage loop commands it to turn on.

The output voltage will decrease if the load continuously demands more current than current limit level. The current limit threshold is set by connecting a resistor ( $R_{OC}$ ) from LGATE1 to GND. To keep OCL function work normally, the total capacitance from LGATE1 to GND can **NOT** larger than 12nF(including  $C_{ISS}$  capacitance of Low Side MOSFET). The voltage across PHASE and GND pins is compared with  $V_{OC}$  for current limit. The current limit threshold is calculated as:

$$I_{LIM}(A) = \frac{V_{OC}(mV)}{R_{DS(ON)}} + \frac{I_{RIPPLE}}{2}$$

And ,  $R_{OC}$  resistance can be calculated as:

$$R_{OC}(k\Omega) = \frac{500mV}{\frac{V_{OC}(mV) - 20mV}{180mV} \times \frac{255}{8}(uA) + 5uA}$$

$V_{OC}$  is the per-phase GND-PHASE voltage when the power stage low-side MOSFETs is turned-on;  $R_{DS(ON)}$  is the on-resistance of equivalent per-phase power stage low side MOSFET and  $I_{RIPPLE}$  is the peak-to-peak inductor ripple current at steady state. The minimum  $V_{OC}$  is 20mV and the maximum  $V_{OC}$  is 200mV. **Controller will keep the minimum  $V_{OC}$  level even if designer sets the VOC level lower than 20mV, and vice versa.**

Over Voltage Protection (OVP)

The OVP is triggered if  $V_{FB} > 1.5 \times V_{REFIN}$  sustained 6us. When OVP is activated, the uP9509S turns on all low-side MOSFET(s) and turns off all high-side MOSFET(s). The over voltage protection is a latch-off function and can only be reset by PVCC re-POR or EN restart.

Under Voltage Protection (UVP)

The under voltage protection is triggered if  $V_{FB} < 0.5 \times V_{REFIN}$  sustained 10us. When UVP is activated, the uP9509S turns off all high-side and low-side MOSFET. The under voltage protection is a latch-off function and can only be reset by PVCC re-POR or EN restart.

Over Temperature Protection (OTP)

The uP9509S monitors the temperature of itself. If the temperature exceeds typical 150°C, the uP9509S is forced into shutdown mode. The over temperature protection is a latch-off function and can only be reset by PVCC re-POR or EN restart.

## Absolute Maximum Rating

(Note 1)

Supply Input Voltage, PVCC	-----	-0.3V to +6.5V
BOOTx to PHASEx		
DC	-----	-0.3V to +6V
PHASEx to GND		
DC	-----	-0.7V to +28V
< 100ns	-----	-8V to +36V
BOOTx to GND		
DC	-----	-0.3V to +34V
< 100ns	-----	-5V to +42V
UGATEx to PHASEx		
DC	-----	-0.3V to +6V
< 100ns	-----	-5V to +7V
LGATEx to GND		
DC	-----	-0.3V to +6V
< 100ns	-----	-5V to +7V
Other Pins	-----	-0.3V to +6V
Storage Temperature Range	-----	-65°C to +150°C
Junction Temperature	-----	150°C
Lead Temperature (Soldering, 10 sec)	-----	260°C
ESD Rating (Note 2)		
HBM (Human Body Mode)	-----	2kV

## Thermal Information

Package Thermal Resistance (Note 3)

VQFN4x4 - 24L $\theta_{JA}$	-----	40°C/W
VQFN4x4 - 24L $\theta_{JC}$	-----	4°C/W
Power Dissipation, $P_D$ @ $T_A = 25^\circ\text{C}$		
VQFN4x4 - 24L	-----	2.5W

## Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range	-----	-40°C to +125°C
Operating Ambient Temperature Range	-----	-40°C to +85°C
Input Voltage, $V_{IN}$	-----	3V to 26V
Control Voltage, $V_{PVCC}$	-----	4.5V to 5.5V

**Note 1.** Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

**Note 2.** Devices are ESD sensitive. Handling precaution recommended.

**Note 3.**  $\theta_{JA}$  is measured in the natural convection at  $T_A = 25^\circ\text{C}$  on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

**Note 4.** The device is not guaranteed to function outside its operating conditions.

**Electrical Characteristics**

 (PVCC = 5V, T<sub>A</sub> = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
<b>Supply Input</b>						
Quiescent Current	I <sub>Q</sub>	V <sub>REFIN</sub> = 0.9V, EN = 1.8V, V <sub>FB</sub> = 1V, no switching	--	3	--	mA
Shutdown Current	I <sub>SHDN</sub>	EN = 0V	--	2	--	uA
PVCC POR Threshold	V <sub>PVCCRTH</sub>	V <sub>PVCC</sub> rising	3.9	4.1	4.3	V
PVCC POR Hysteresis	V <sub>PVCCHYS</sub>		--	0.3	--	V
VREF Voltage Accuracy	V <sub>REF</sub>		1.98	2	2.02	V
VREF Sourcing Current	I <sub>REF</sub>		10	--	--	mA
<b>Control Input: EN</b>						
Logic Low Threshold	V <sub>EN_L</sub>		--	--	0.6	V
Logic High Threshold	V <sub>EN_H</sub>		1.2	--	--	V
Internal Pull-down Resistance	R <sub>EN</sub>		--	150	--	kΩ
<b>Reference Voltage</b>						
REFIN Disable Threshold			--	0.1	--	V
External Reference Voltage Range	V <sub>REFIN</sub>		0.2	--	2	V
<b>On Time</b>						
One Shot Width	T <sub>ON</sub>	V <sub>IN</sub> = 12V, V <sub>OUT</sub> = 1.2V, F <sub>SW</sub> = 300kHz	--	333	--	ns
Minimum Off Time	T <sub>OFF_MIN</sub>		--	300	--	ns
Minimum On Time	T <sub>ON_MIN</sub>		--	80	--	ns
<b>Error Amplifier</b>						
Open Loop DC Gain	AO	Guaranteed by Design	--	70	--	dB
Gain Bandwidth Product	G <sub>BW(EA)</sub>	Guaranteed by Design	--	10	--	MHz
Offset Voltage	V <sub>OS(EA)</sub>		-1	--	1	mV
Trans-conductance	GM		--	2020	--	uA/V
Maximum Current (Source & Sink)	I <sub>COMP</sub>		--	300	--	uA
<b>Current Sense Amplifier (Current Balance)</b>						
Input Offset Voltage	V <sub>OFF_CSA</sub>		-1	--	1	mV
Max Sourcing Current	I <sub>SRC_CSA</sub>		100	--	--	uA
ISENx Voltage	V <sub>DC_CSA</sub>		25	30	35	mV
Internal Current Sense Resistance	R <sub>ISENX_INT</sub>	Internal R <sub>ISEN1</sub> & R <sub>ISEN2</sub>	--	4	--	kΩ
		Internal R <sub>ISEN3</sub>	--	4.5	--	

**Electrical Characteristics**

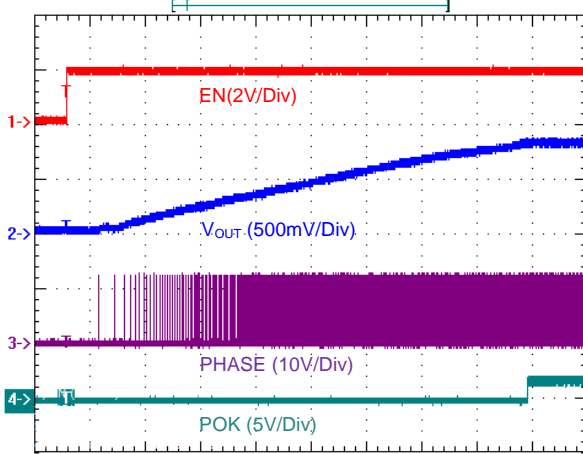
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
<b>FBRTN</b>						
FBRTN Current	$I_{FBRTN}$	EN = 1.4V, no switching	--	--	500	uA
<b>Soft Start</b>						
Initialization Time at POR	$T_{INIT\_POR}$	Refer to Fig. 5	--	--	350	us
Initialization Time	$T_{INIT}$	Refer to Fig. 5	--	--	250	us
Output Voltage Ramp-Up Time	$T_{ramp}$	Refer to Figure 5, $R_{LG2}$ = Open	--	1.5	--	ms
<b>PWMVID Buffer</b>						
VID Input Low Level	$V_{IL\_VID}$		--	--	0.6	V
VID Input High Level	$V_{IH\_VID}$		1.2	--	--	V
VID Tri-state Delay	$T_{TRL\_VID}$		--	100	--	ns
REFADJ Source Resistance	$R_{BF\_SRC}$	$I_{SRC} = 1mA$	--	20	--	$\Omega$
REFADJ Sink Resistance	$R_{BF\_SNK}$	$I_{SNK} = 1mA$	--	20	--	$\Omega$
<b>PWM3 Output</b>						
Output Low Voltage	$V_{PWM\_L}$	$I_{SNK} = 4mA$	--	--	0.2	V
Output High Voltage	$V_{PWM\_H}$	$I_{SRC} = 4mA$	4.7	--	--	V
High Impedance State Leakage		$V_{PWM} = 0V$	-1	--	0	uA
		$V_{PWM} = 5V$	0	--	1	
<b>PSI</b>						
Power Saving Mode Logic	$V_{PSI}$	Multi-Phase CCM	1.6	--	--	V
		Multi-Phase DCM	1	--	1.4	V
		Single-Phase CCM	0.4	--	0.8	V
		Single-Phase DCM	--	--	0.2	V
<b>Gate Drivers</b>						
Upper Gate Source	$R_{UG\_SRC}$	$I_{UG} = -80mA$	--	0.7	1	$\Omega$
Upper Gate Sink	$R_{UG\_SNK}$	$I_{UG} = 80mA$	--	0.3	0.5	$\Omega$
Lower Gate Source	$R_{LG\_SRC}$	$I_{LG} = -80mA$	--	0.7	1	$\Omega$
Lower Gate Sink	$R_{LG\_SNK}$	$I_{LG} = 80mA$	--	0.3	0.5	$\Omega$
Dead Time	$T_{DT}$		--	30	--	ns
<b>Internal Bootstrap Schottky Diode</b>						
Forward Voltage	$V_F$	Forward Bias Current = 3.5mA	--	0.33	--	V
<b>Zero Current Detection Threshold</b>						
Zero Current Threshold	$V_{ZC}$	Measure $V_{PHASE}$ -GND	-0.5	--	0.5	mV

**Electrical Characteristics**

Parameter	Symb-ol	Test Conditions	Min	Typ	Max	Units
<b>Protection</b>						
Minimum Over Current Threshold	$V_{OC\_min}$	$R_{LG1} = \text{Open}$ , measure GND- $V_{PHASE}$	--	20	--	mV
Maximum Over Current Threshold	$V_{OC\_max}$	$R_{LG1} = 12k\Omega$ , measure GND- $V_{PHASE}$	--	200	--	mV
Over Voltage Protection Threshold	$V_{OVP}$	$V_{FB}/V_{REFIN}$	--	150	--	%
Over Voltage Delay Time	$T_{OVP}$		--	6	--	us
Under Voltage Protection Threshold	$V_{UVP}$	$V_{FB}/V_{REFIN}$	--	50	--	%
Under Voltage Delay Time	$T_{UVP}$		--	10	--	us
Over Temperature Protection Threshold			--	150	--	°C
<b>Power Good Indicator</b>						
PGOOD Output Low Level		$I_{SINK} = 4mA$	--	--	0.3	V
PGOOD Leakage Current		$V_{PGOOD} = 5V$	--	--	0.1	uA

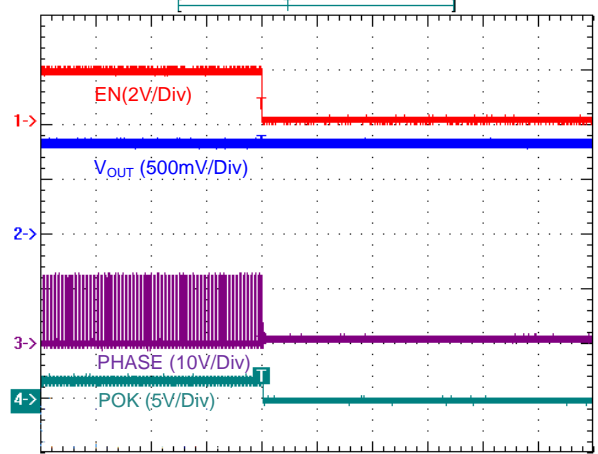
## Typical Operation Characteristics

**EN Power On**



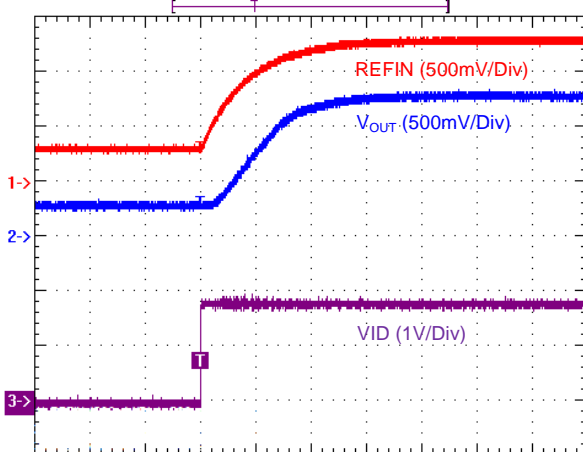
Time : 200us/Div  
 $V_{IN} = 12V, V_{OUT} = 0.8V, I_{OUT} = 0A$

**EN Power Off**



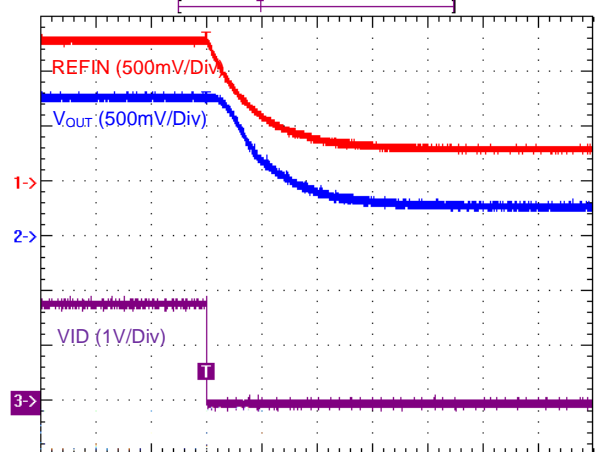
Time : 200us/Div  
 $V_{IN} = 12V, V_{OUT} = 0.8V, I_{OUT} = 0A$

**VID: 0% to 100%**



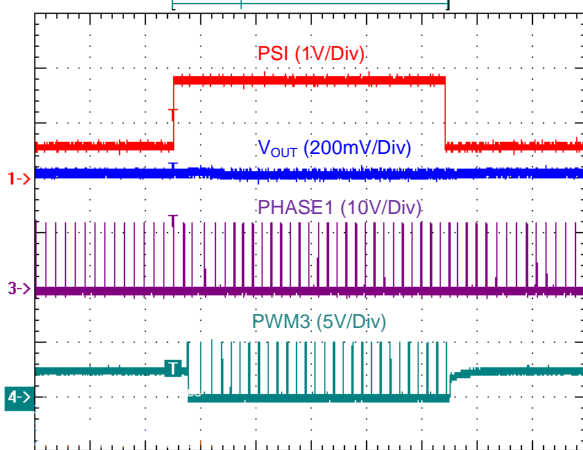
Time : 20us/Div  
 $V_{IN} = 12V, \text{No Load}$

**VID: 100% to 0%**



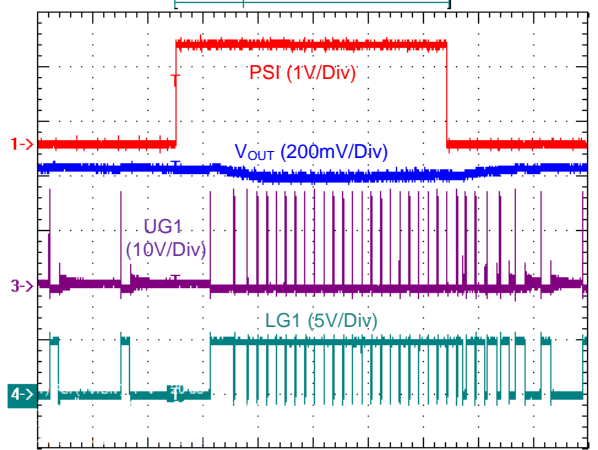
Time : 20us/Div  
 $V_{IN} = 12V, \text{No Load}$

**PSI Transition: 0.6V  $\leftrightarrow$  1.8V**



Time : 20us/Div  
 $V_{IN} = 12V, V_{OUT} = 0.8V, I_{OUT} = 0.5A$

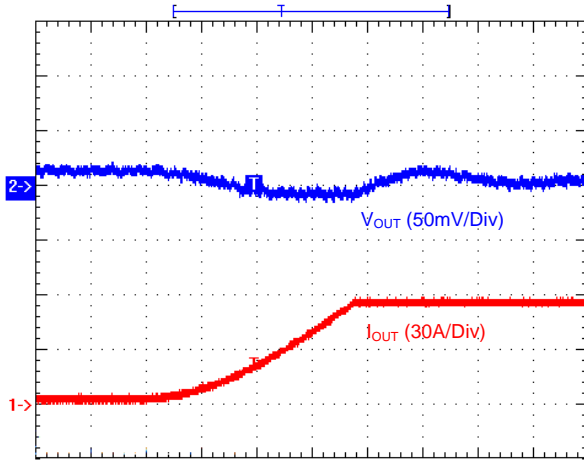
**PSI Transition: 0V  $\leftrightarrow$  1.8V**



Time : 20us/Div  
 $V_{IN} = 12V, V_{OUT} = 0.8V, I_{OUT} = 1A$

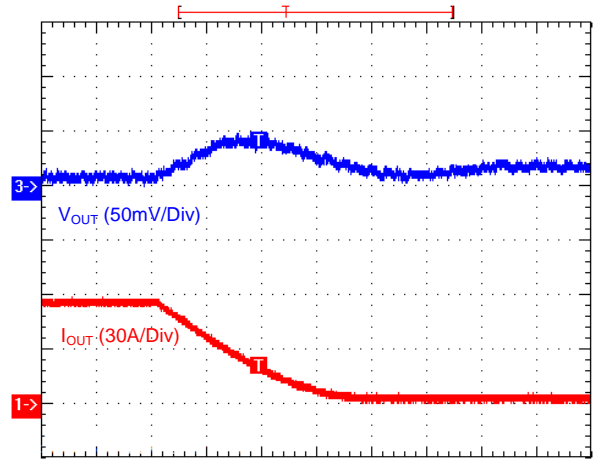
## Typical Operation Characteristics

**Load Transient: Undershoot**



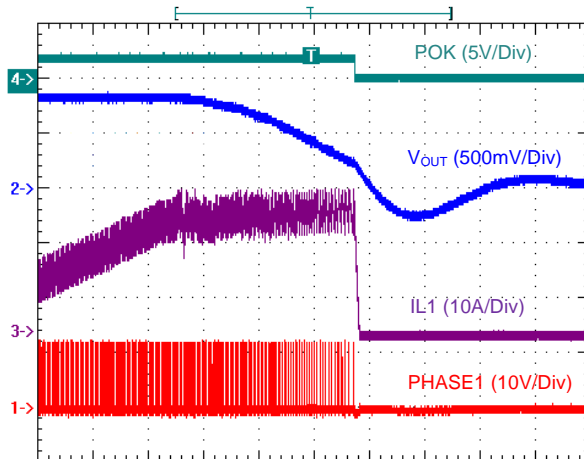
Time : 4us/Div  
 $V_{IN} = 12V, V_{OUT} = 0.8V, I_{OUT} = 0A \text{ to } 60A$

**Load Transient: Overshoot**



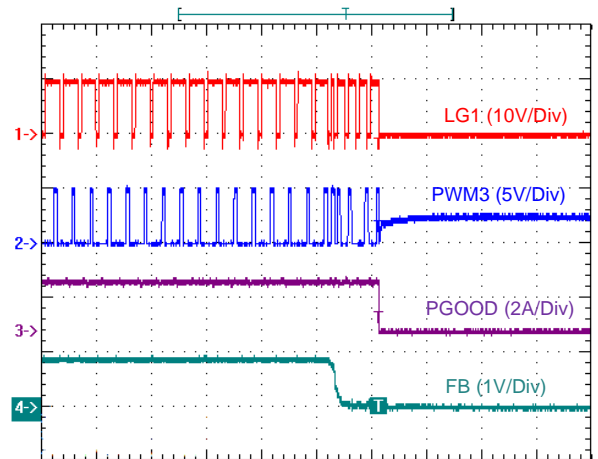
Time : 4us/Div  
 $V_{IN} = 12V, V_{OUT} = 0.8V, I_{OUT} = 60A \text{ to } 0A$

**Over Current Limit**



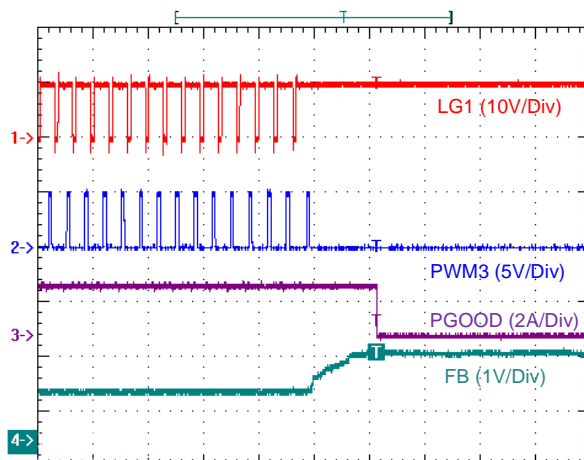
Time : 100us/Div  
 $V_{IN} = 12V, V_{OUT} = 0.8V, R_{OC} = 47k\Omega$

**UVP**



Time : 10us/Div  
 $V_{IN} = 12V, V_{OUT} = 0.8V, \text{No load}$

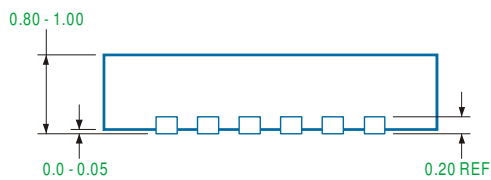
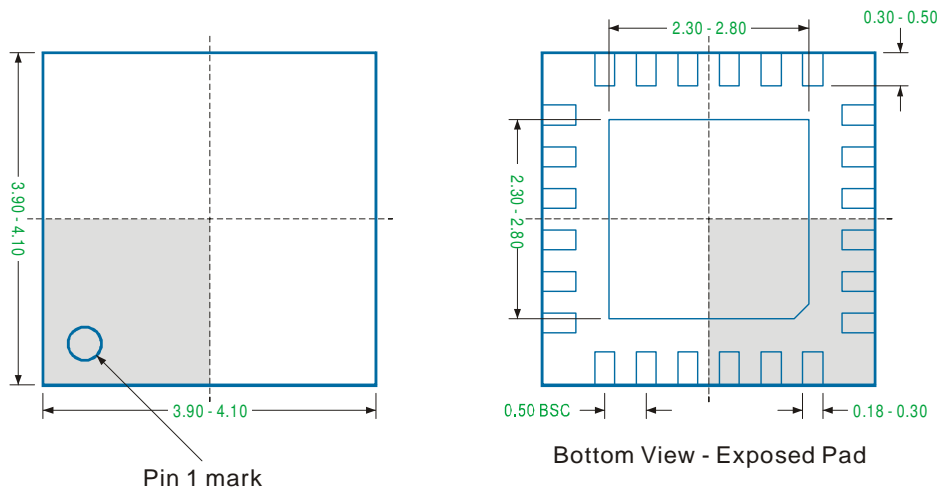
**OVP**



Time : 10us/Div  
 $V_{IN} = 12V, V_{OUT} = 0.8V, \text{No load}$



### VQFN4x4 - 24L



#### Note

##### 1. Package Outline Unit Description:

BSC: Basic. Represents theoretical exact dimension or dimension target

MIN: Minimum dimension specified.

MAX: Maximum dimension specified.

REF: Reference. Represents dimension for reference use only. This value is not a device specification.

TYP: Typical. Provided as a general value. This value is not a device specification.

##### 2. Dimensions in Millimeters.

##### 3. Drawing not to scale.

##### 4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

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