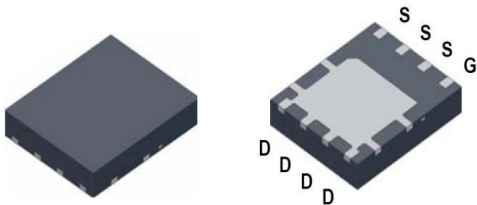


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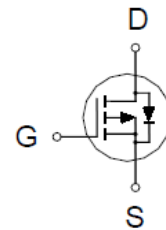
P-Channel Logic Level Enhancement Mode MOSFET

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
-30V	7m Ω @ $V_{GS} = -10V$	-43A



PDFN 5x6P



ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	± 25	
Continuous Drain Current	$T_C = 25\text{ }^\circ\text{C}$	I_D	-43	A
	$T_C = 100\text{ }^\circ\text{C}$		-27	
	$T_A = 25\text{ }^\circ\text{C}$		-13	
	$T_A = 70\text{ }^\circ\text{C}$		-10	
Pulsed Drain Current ¹		I_{DM}	-110	
Avalanche Current		I_{AS}	-38	
Avalanche Energy	L = 0.1mH	E_{AS}	72	mJ
Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	P_D	25	W
	$T_C = 100\text{ }^\circ\text{C}$		10	
	$T_A = 25\text{ }^\circ\text{C}$		2.2	
	$T_A = 70\text{ }^\circ\text{C}$		1.4	
Operating Junction & Storage Temperature Range		T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

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P-Channel Logic Level Enhancement Mode MOSFET

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient ²	$R_{\theta JA}$		56	°C / W
Junction-to-Case	$R_{\theta JC}$		5	

¹Pulse width limited by maximum junction temperature.

²The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ\text{C}$. The value in any given application depends on the user's specific board design.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-1	-1.5	-3	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 25V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -24V, V_{GS} = 0V$			-1	uA
		$V_{DS} = -20V, V_{GS} = 0V, T_J = 125^\circ\text{C}$			-10	
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = -10V, I_D = -13A$		5.7	7	mΩ
		$V_{GS} = -4.5V, I_D = -13A$		8.4	12	
Forward Transconductance ¹	g_{fs}	$V_{DS} = -5V, I_D = -13A$		40		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = -15V, f = 1\text{MHz}$		2822		pF
Output Capacitance	C_{oss}			452		
Reverse Transfer Capacitance	C_{rss}			364		
Gate Resistance	R_g	$V_{GS} = 0V, V_{DS} = 0V, f = 1\text{MHz}$		4		Ω
Total Gate Charge ²	$Q_{g(VGS=-10V)}$	$V_{DS} = -15V, I_D = -13A$		60		nC
	$Q_{g(VGS=-4.5V)}$			30		
Gate-Source Charge ²	Q_{gs}			6.1		
Gate-Drain Charge ²	Q_{gd}			14		
Turn-On Delay Time ²	$t_{d(on)}$		$V_{DS} = -15V, I_D \cong -13A, V_{GS} = -10V, R_{GS} = 6\Omega$		39	
Rise Time ²	t_r			26		
Turn-Off Delay Time ²	$t_{d(off)}$			161		
Fall Time ²	t_f			100		

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SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_J = 25 °C)

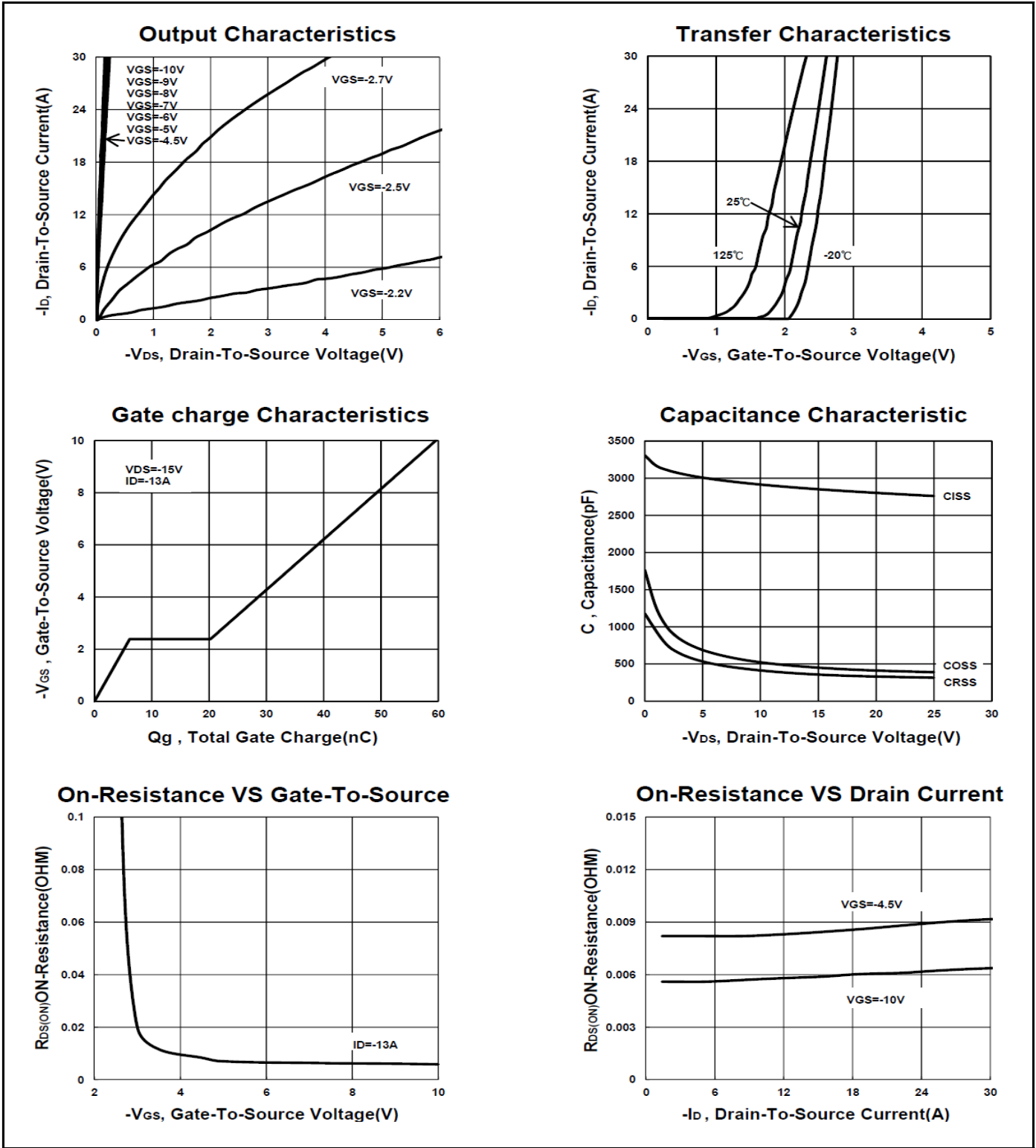
Continuous Current	I _S			19	A
Forward Voltage ¹	V _{SD}	I _F = -13A, V _{GS} = 0V		-1.3	V
Reverse Recovery Time	t _{rr}	I _F = -13A, dI _F /dt = 100A / μS		23	nS
Reverse Recovery Charge	Q _{rr}			6	nC

¹Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

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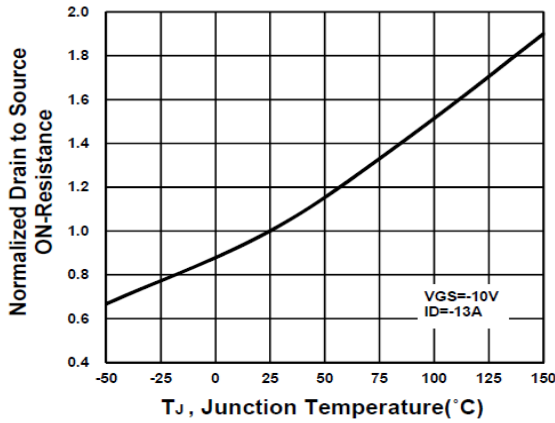
P-Channel Logic Level Enhancement Mode MOSFET



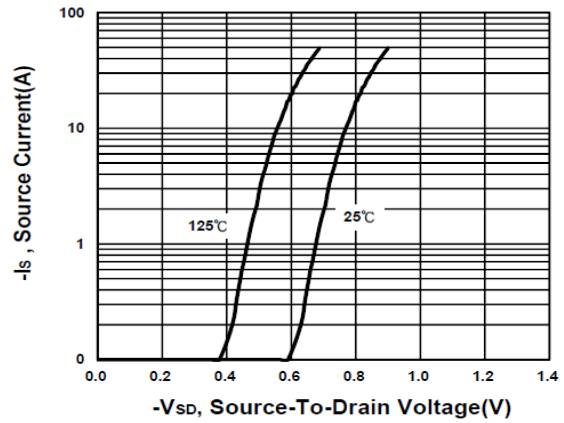
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P-Channel Logic Level Enhancement Mode MOSFET

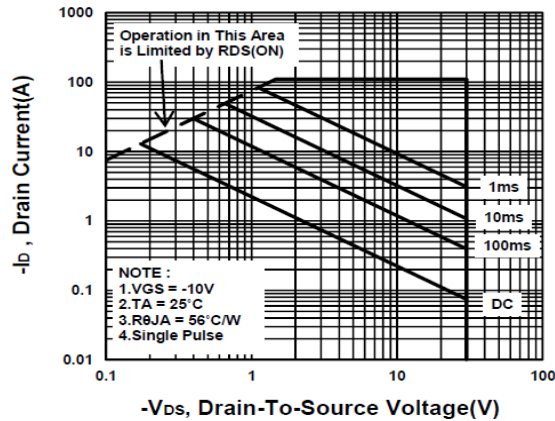
On-Resistance VS Temperature



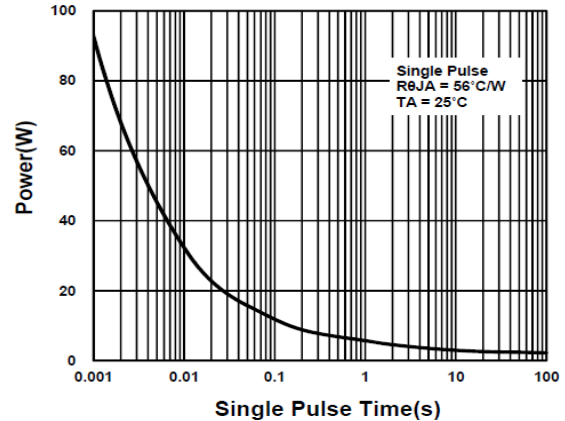
Source-Drain Diode Forward Voltage



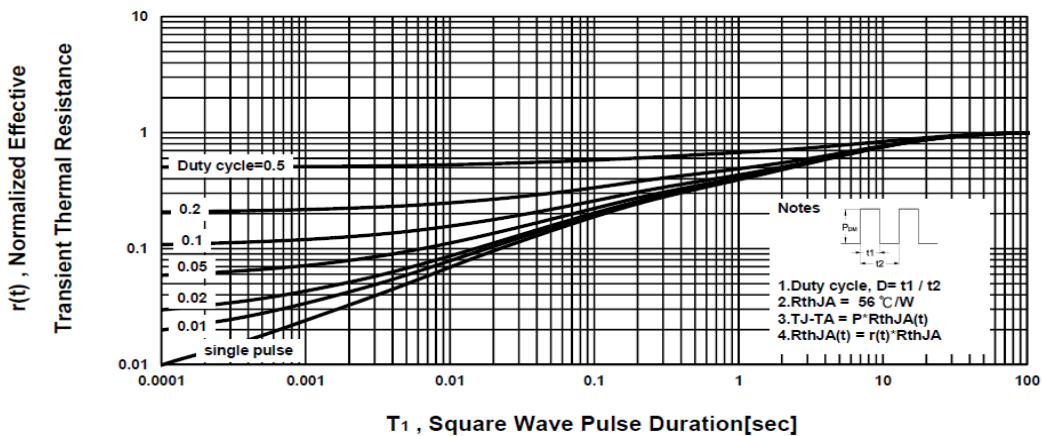
Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve



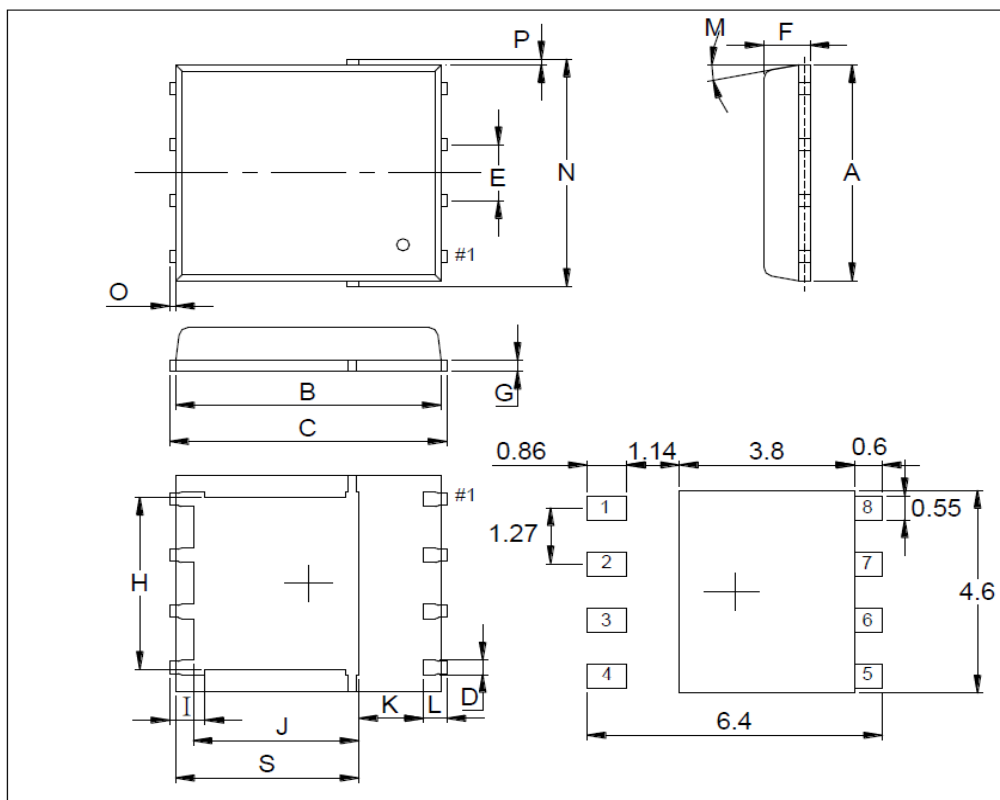
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Package Dimension

PDFN 5x6P MECHANICAL DATA

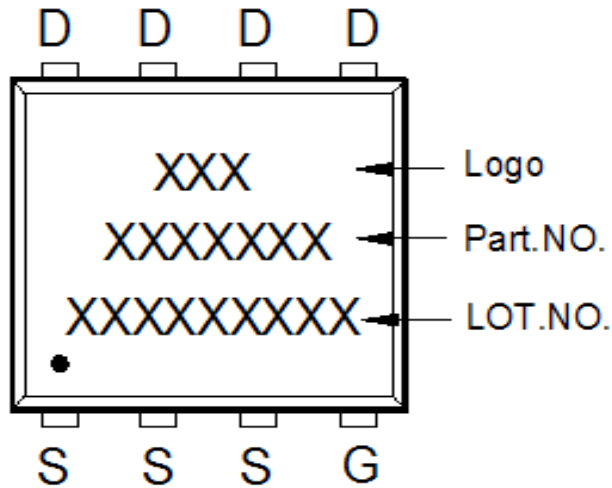
Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	4.8		5.15	J	3.34		3.9
B	5.42		5.9	K	0.9		
C	5.9		6.35	L	0.38		0.711
D	0.3		0.51	M	0°		12°
E	1.17	1.27	1.37	N	4.8		5.4
F	0.8	1	1.2	O	0.05		0.36
G	0.15		0.35	P	0.05		0.25
H	3.67		4.31	S	3.73		4.19
I	0.38		0.71				



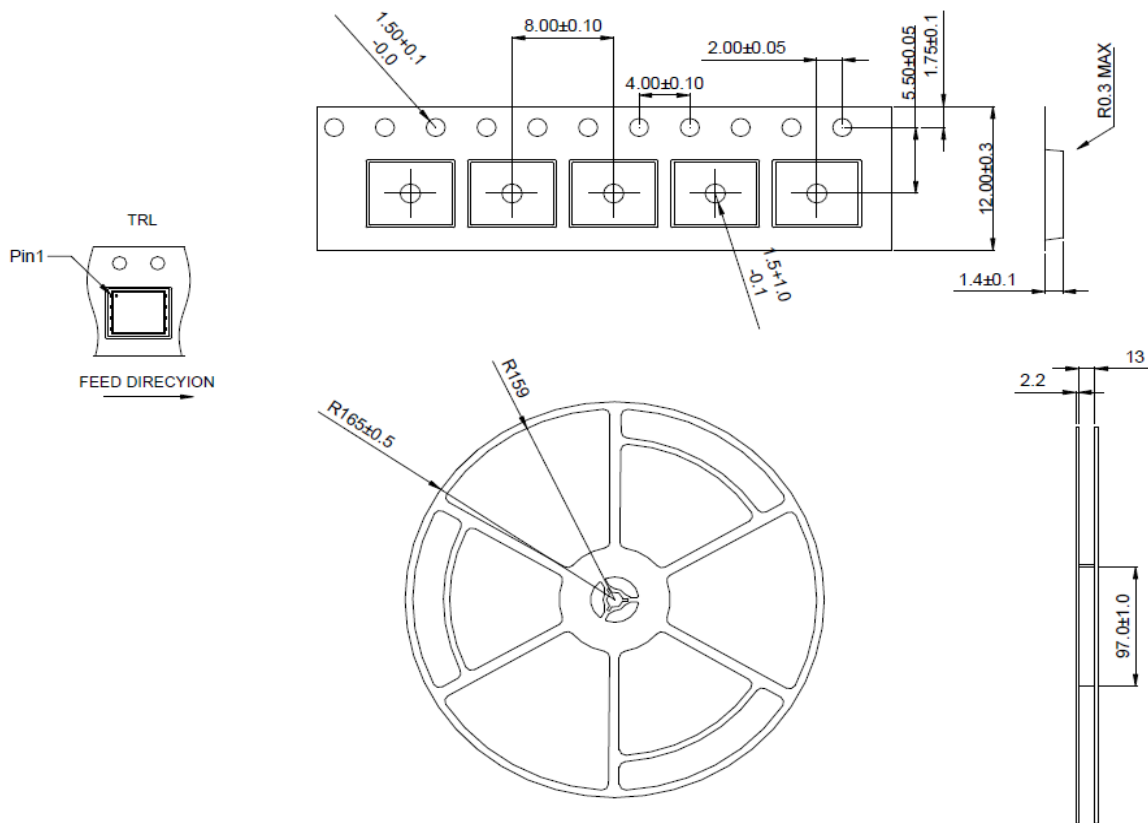
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A. Marking Information



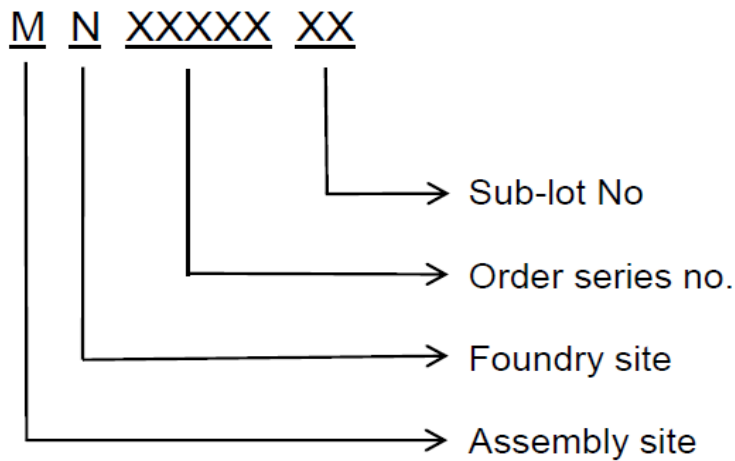
B. Tape & Reel Information: 3000pcs/Reel



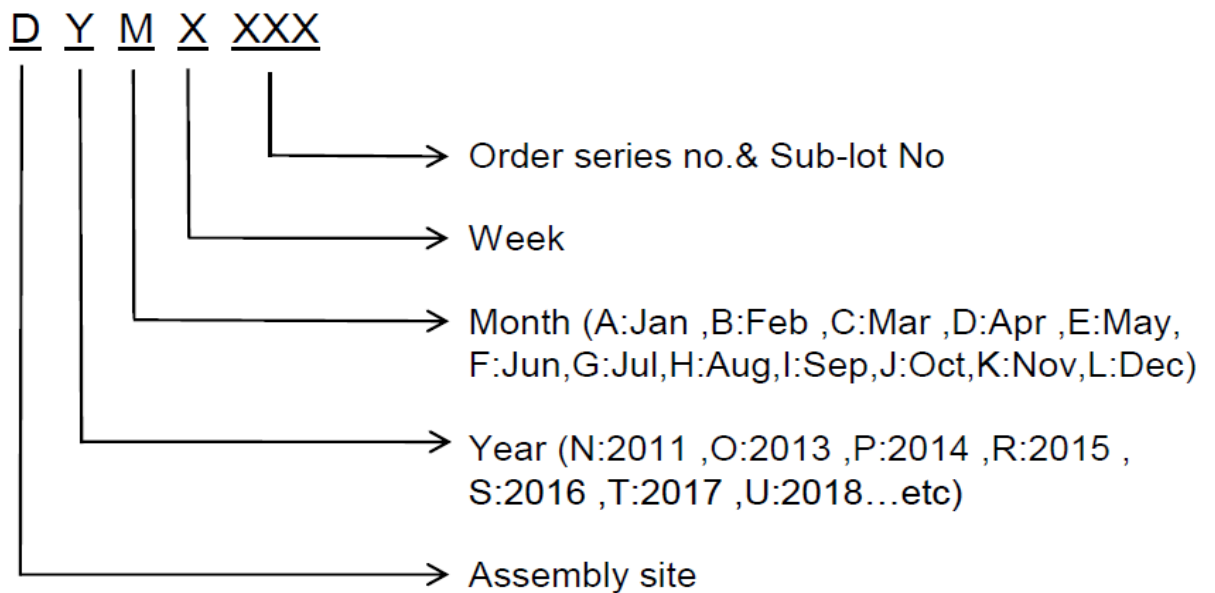
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P-Channel Logic Level Enhancement Mode MOSFET

C. Lot No.&Date Code rule

1. Lot No.



2. Date Code





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D.Label rule

标签内容(Label content)



1	Label Size	30 * 90 mm
2	Font style	Times New Roman or Arial (或可区分英文"0"和数字"0", "G"和"Q"的字型即可)
3	U-NIKC	Height: 4 mm
4	Package	Height: 2 mm
5	Date	Height: 2 mm Shipping date: YYYY/MM/DD, ex. 2008/09/12
6	Device	Height: 3 mm (Max: 16 Digit)
7	Lot	Height: 3 mm (Max: 9 Digit) Sub lot
8	D/C	Height: 3 mm (Max: 7 Digit)
9	QTY	Height: 3 mm (Max: 6 Digit) Thousand mark is no needed
10	RoHS label	 long axis: 12 mm minor axis: 6 mm bottom color: White Font color: Black Font style: Arial
11	Halogen Free label	 Diameter: 10 mm bottom color: Green Font color: Black Font style: Arial
12	Scan information	Device / Lot / D/C / QTY , Insert "/" between every parts. for example: P3055LDG/G12345601/GGG2301/2000 DPI (Dots per inch): Over 300 dpi Code : Code 128 Height: 6 mm at least