4A, 26V, 380kHz, Asynchronous Step-Down Converter

Features

- **Wide Input Voltage from 4.5V to 26V**
- **Output Current up to 4A**
- **Adjustable Output Voltage from 0.8V to 90% V_{IN}**
  - **0.8V Reference Voltage**
  - **±2.5% System Accuracy**
- **80mΩ Integrated P-Channel Power MOSFET**
- **High Efficiency up to 91%**
  - **Pulse-Skipping Mode (PSM) / PWM Mode Operation**
- **Current-Mode Operation**
  - **Stable with Ceramic Output Capacitors**
  - **Fast Transient Response**
- **Power-On-Reset Monitoring**
- **Fixed 380kHz Switching Frequency in PWM Mode**
- **Built-in Digital Soft-Start**
- **Output Current-Limit Protection with Frequency Foldback**
- **70% Under-Voltage Protection**
- **Over-Temperature Protection**
- **<5mA Quiescent Current During Shutdown**
- **Thermal-Enhanced SOP-8P Package**
- **Lead Free and Green Devices Available (RoHS Compliant)**

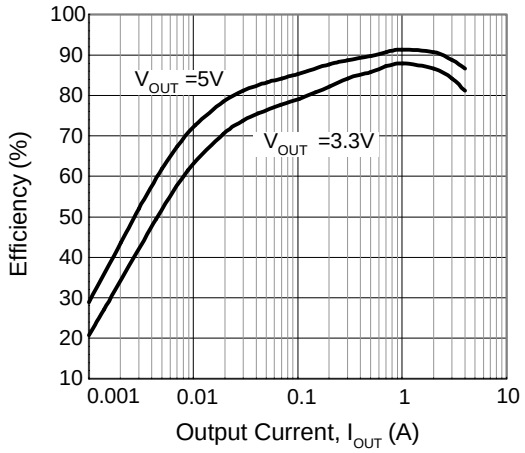
Applications

- **LCD Monitor / TV**
- **Set-Top Box**
- **Portable DVD**
- **Wireless LAN**
- **ADSL, Switch HUB**
- **Notebook Computer**
- **Step-Down Converters Requiring High Efficiency and 4A Output Current**

General Description

The APW7089 is a 4A, asynchronous, step-down converter with integrated 80mΩ P-channel MOSFET. The device, with current-mode control scheme, can convert 4.5~26V input voltage to the output voltage adjustable from 0.8 to 90% V_{IN} to provide excellent output voltage regulation.

The APW7089 regulates the output voltage in automatic PSM/PWM mode operation, depending on the output current, for high efficiency operation over light to full load current. The APW7089 is also equipped with power-on-reset, soft-start, and whole protections (under-voltage, over-temperature, and current-limit) into a single package. In shutdown mode, the supply current drops below 5μA. This device, available in a 8-pin SOP-8P package, provides a very compact system solution with minimal external components and good thermal conductance.



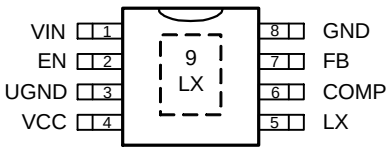
ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Ordering and Marking Information

APW7089 □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code KA : SOP-8P Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APW7089 KA : APW7089 XXXXX	XXXXX - Date Code

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

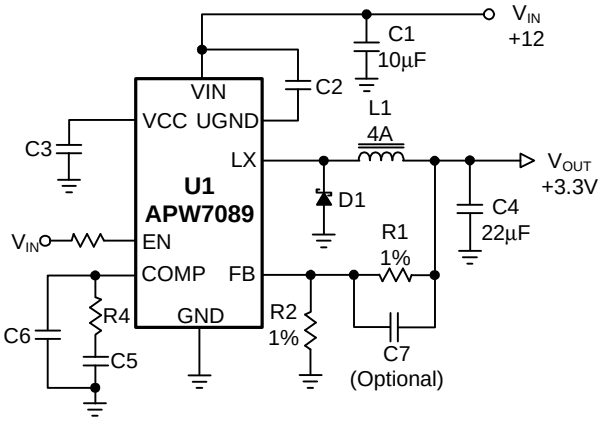
Pin Configuration



SOP-8P
(Top View)

The Pin 5 must be connected to the Exposed Pad

Simplified Application Circuit



Absolute Maximum Ratings (Note 1)

Symbol	Parameter		Rating	Unit
V_{IN}	VIN Supply Voltage (VIN to GND)		-0.3 ~ 30	V
V_{LX}	LX to GND Voltage	> 100ns	-2 ~ V_{IN}+0.3	V
		< 100ns	-5 ~ V_{IN}+6	
V_{CC}	VCC Supply Voltage (VCC to GND)	V_{IN} > 6.2V	-0.3 ~ 6.5	V
		V_{IN} ≤ 6.2V	< V_{IN}+0.3	
V_{UGND_GND}	UGND to GND Voltage		-0.3 ~ V_{IN}+0.3	V
V_{VIN_UGND}	VIN to UGND Voltage		-0.3 ~ 7V	V
	EN to GND Voltage		-0.3 ~ 20	V
	FB, COMP to GND Voltage		-0.3 ~ V_{CC} +0.3	V
	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature		-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds		260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in Free Air (Note 2) SOP-8P	50	°C/W
θ_{JC}	Junction-to-Case Resistance in Free Air (Note 3) SOP-8P	10	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of SOP-8P is soldered directly on the PCB.

Note 3: The case temperature is measured at the center of the exposed pad on the underside of the SOP-8P package.

Recommended Operating Conditions (Note 4)

Symbol	Parameter	Range	Unit
V_{IN}	VIN Supply Voltage	4.5 ~ 26	V
	VCC Supply Voltage	4.0 ~ 5.5	V
V_{OUT}	Converter Output Voltage	0.8 ~ 90% V_{IN}	V
I_{OUT}	Converter Output Current	0 ~ 4	A
	VCC Input Capacitor	0.22 ~ 2.2	µF
	VIN-to-UGND Input Capacitor	0.22 ~ 2.2	µF
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 4: Refer to the typical application circuits.

Electrical Characteristics

Refer to the typical application circuits. These specifications apply over V_{IN}=12V, V_{OUT}=3.3V and T_A= -40 ~ 85°C, unless otherwise specified. V_{CC} is regulated by an internal regulator. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW7089			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
I_{VIN}	VIN Supply Current	V_{FB} = 0.85V, V_{EN}=3V, LX=Open	-	1.0	2.0	mA
I_{VIN_SD}	VIN Shutdown Supply Current	V_{EN} = 0V, V_{IN}=26V	-	-	5	µA
I_{VCC}	VCC Supply Current	V_{EN} = 3V, V_{CC} = 5.0V, V_{FB}=0.85V	-	0.7	-	mA
I_{VCC_SD}	VCC Shutdown Supply Current	V_{EN} = 0V, V_{CC} = 5.0V	-	-	1	µA
VCC 4.2V LINEAR REGULATOR						
	Output Voltage	V_{IN} = 5.2 ~ 26V, I_O = 0 ~ 8mA	4.0	4.2	4.5	V
	Load Regulation	I_O = 0 ~ 8mA	-60	-40	0	mV
	Current-Limit	V_{CC} > POR Threshold	8	-	30	mA
VIN-TO-UGND 5.5V LINEAR REGULATOR						
	Output Voltage ($V_{VIN-UGND}$)	V_{IN} = 6.2 ~ 26V, I_O = 0 ~ 10mA	5.3	5.5	5.7	V
	Load Regulation	I_O = 0 ~ 10mA	-80	-60	0	mV
	Current-Limit	V_{IN} = 6.2 ~ 26V	10	-	30	mA

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Electrical Characteristics (Cont.)

Refer to the typical application circuits. These specifications apply over V_{IN}=12V, V_{OUT}=3.3V and T_A= -40 ~ 85°C, unless otherwise specified. V_{CC} is regulated by an internal regulator. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW7089			Unit
			Min.	Typ.	Max.	
POWER-ON-RESET (POR) AND LOCKOUT VOLTAGE THRESHOLDS						
	VCC POR Voltage Threshold	V_{CC} rising	3.7	3.9	4.1	V
	VCC POR Hysteresis		-	0.15	-	V
	EN Lockout Voltage Threshold	V_{EN} rising	2.3	2.5	2.7	V
	EN Lockout Hysteresis		-	0.2	-	V
	VIN-to-UGND Lockout Voltage Threshold	$V_{VIN-UGND}$ rising	-	3.5	-	V
	VIN-to-UGND Lockout Hysteresis		-	0.2	-	V
REFERENCE VOLTAGE						
V_{REF}	Reference Voltage		-	0.8	-	V
	Output Voltage Accuracy	T_J = 25°C, I_{OUT}=0A, V_{IN}=12V	-1.0	-	+1.0	%
		T_J = -40 ~ 125°C, I_{OUT} = 0 ~ 4A, V_{IN} = 4.5 ~ 26V	-2.5	-	+2.5	
	Line Regulation	V_{IN} = 4.5V to 26V, I_{OUT} = 0A	-	0.36	-	%
	Load Regulation	I_{OUT} = 0 ~ 4A	-	0.4	-	%
OSCILLATOR AND DUTY						
F_{OSC}	Free Running Frequency	V_{IN} = 4.5 ~ 26V	340	380	420	kHz
	Foldback Frequency	V_{FB} = 0V	-	80	-	kHz
	Maximum Converter's Duty Cycle		-	93	-	%
	Minimum Pulse Width of LX	V_{IN} = 4.5 ~ 26V	-	200	-	ns
CURRENT-MODE PWM CONVERTER						
Gm	Error Amplifier Transconductance		-	400	-	µA/V
	Error Amplifier DC Gain	COMP = Open	60	80	-	dB
	Current-Sense Resistance		-	0.12	-	Ω
	P-channel Power MOSFET Resistance	Between VIN and Exposed Pad, T_J=25°C	-	80	100	mΩ
PROTECTIONS						
I_{LIM}	P-channel Power MOSFET Current-limit	Peak Current	5.0	6.5	8.0	A
V_{UV}	FB Under-Voltage Threshold	V_{FB} falling	66	70	74	%
	FB Under-Voltage Hysteresis		-	40	-	mV
	FB Under-Voltage Debounce		-	2	-	µs
T_{OTP}	Over-Temperature Trip Point		-	150	-	°C
	Over-Temperature Hysteresis		-	50	-	°C
SOFT-START, ENABLE, AND INPUT CURRENTS						
t_{SS}	Soft-Start Interval		9	10.8	12	ms
	Preceding Delay before Soft-Start		9	10.8	12	ms
	EN Logic Low Voltage	V_{EN} falling, V_{IN} = 4 ~ 26V	-	-	0.8	V

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Electrical Characteristics (Cont.)

Refer to the typical application circuits. These specifications apply over V_{IN}=12V, V_{OUT}=3.3V and T_A= -40 ~ 85°C, unless otherwise specified. V_{CC} is regulated by an internal regulator. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW7089			Unit
			Min.	Typ.	Max.	
SOFT-START, ENABLE, AND INPUT CURRENTS (CONT.)						
	EN Logic High Voltage	V_{EN} rising, V_{IN} = 4 ~ 26V	2.1	-	-	V
	EN Pin Clamped Voltage	I_{EN}=10mA	12	-	17	V
	P-channel Power MOSFET Leakage Current	V_{EN} = 0V, V_{LX} = 0V, V_{IN} = 26V	-	-	4	μA
I_{FB}	FB Pin Input Current	V_{FB} = 0.8V	-100	-	+100	nA
I_{EN}	EN Pin Input Current	V_{EN} < 3V	-500	-	+500	nA

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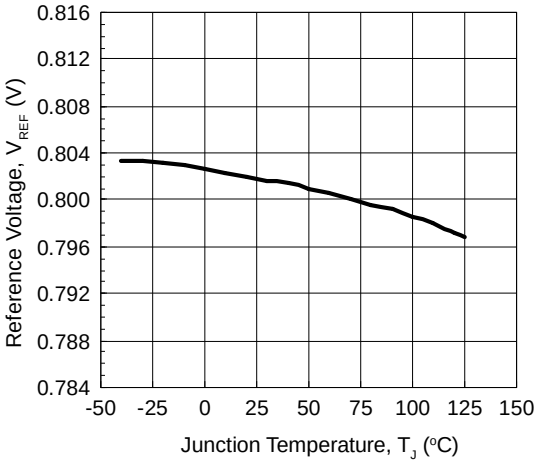
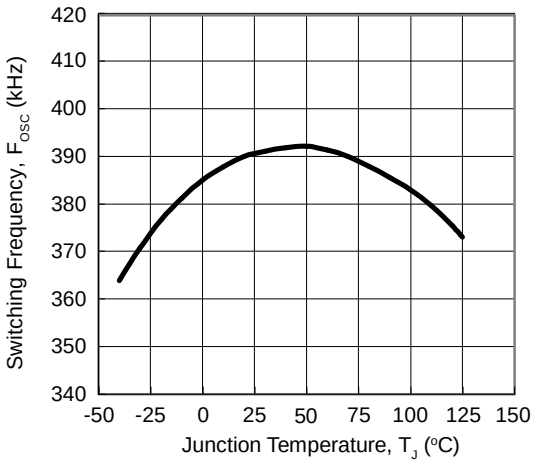
Typical Operating Characteristics

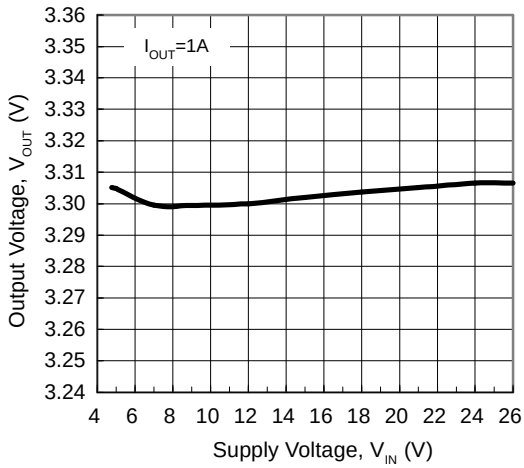
Reference Voltage vs. Junction Temperature



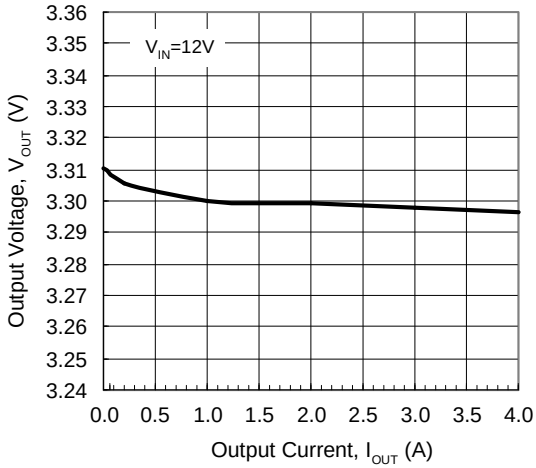
Switching Frequency vs. Junction Temperature



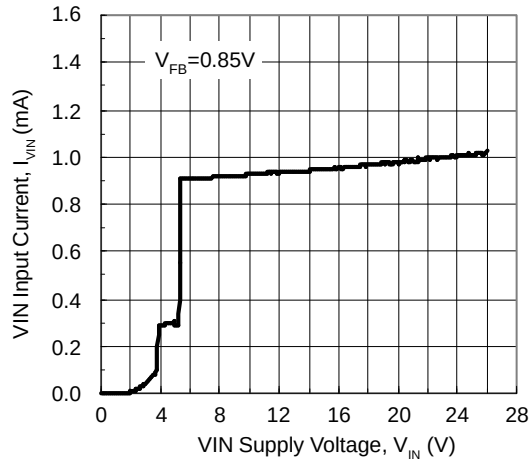
Output Voltage vs. Supply Voltage



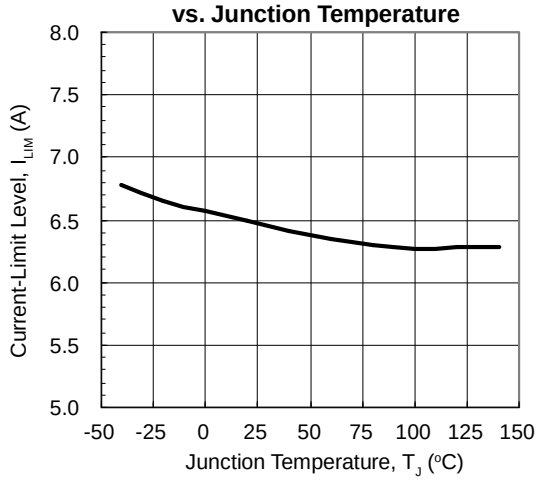
Output Voltage vs. Output Current



VIN Input Current vs. Supply Voltage



Current-Limit Level (Peak Current) vs. Junction Temperature



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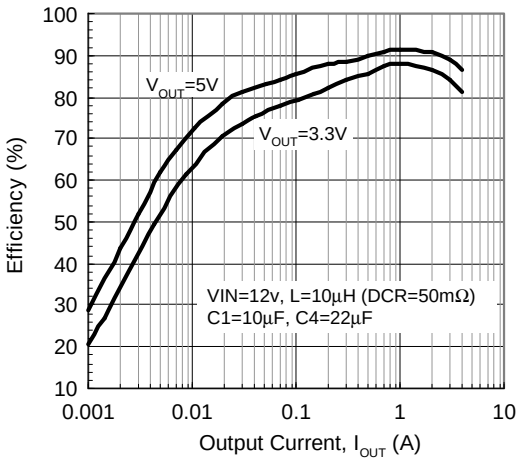
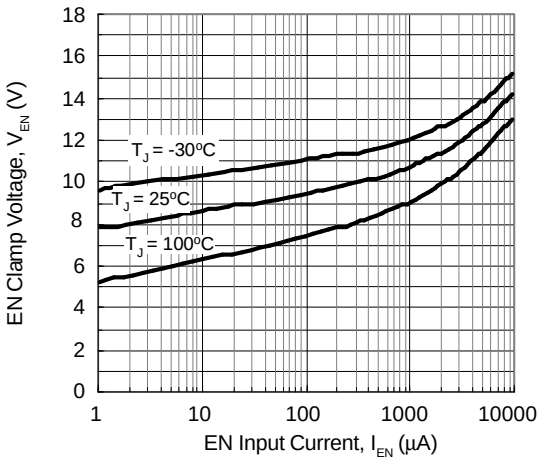
Typical Operating Characteristics (Cont.)

Efficiency vs. Output Current



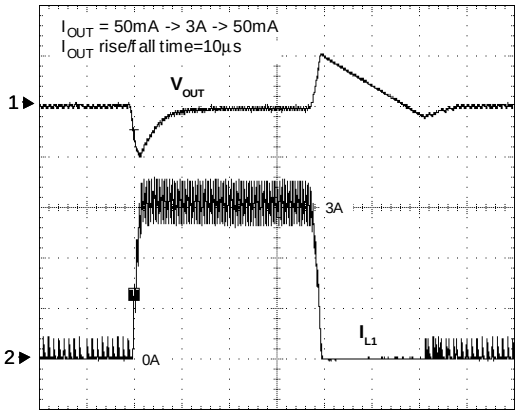
EN Clamp Voltage vs. EN Input Current



Operating Waveforms

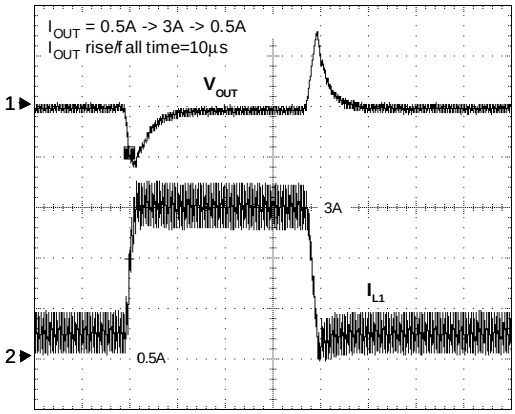
(Refer to the application circuit 1 in the section “Typical Application Circuits”, V_{IN}=12V, V_{OUT}=3.3V, L1=10µH)

Load Transient Response



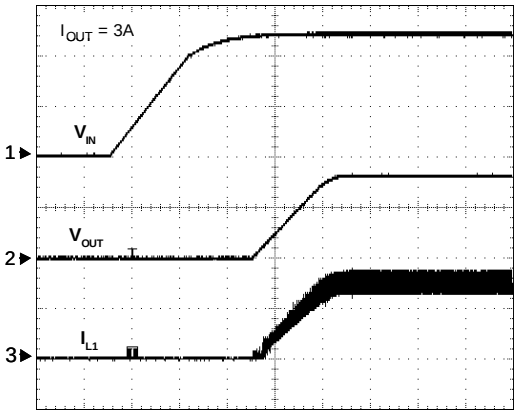
Ch1: V_{OUT}, 200mV/Div, DC,
Voltage Offset = 3.3V
Ch2: I_{L1}, 1A/Div, DC
Time: 50µs/Div

Load Transient Response



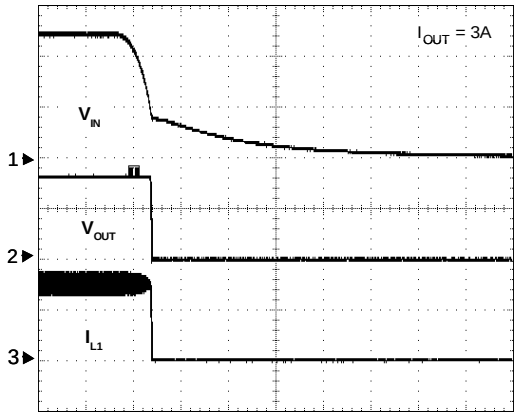
Ch1: V_{OUT}, 100mV/Div, DC,
Voltage Offset = 3.3V
Ch2: I_{L1}, 1A/Div, DC
Time: 50µs/Div

Power On



Ch1: V_{IN}, 5V/Div, DC
Ch2: V_{OUT}, 2V/Div, DC
Ch3: I_{L1}, 2A/Div, DC
Time: 5ms/Div

Power Off



Ch1: V_{IN}, 5V/Div, DC
Ch2: V_{OUT}, 2V/Div, DC
Ch3: I_{L1}, 2A/Div, DC
Time: 5ms/Div

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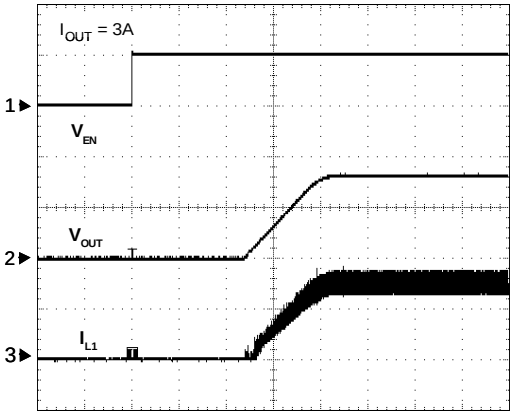
Operating Waveforms (Cont.)

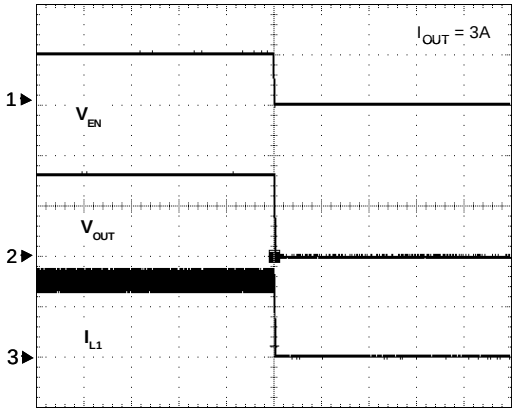
(Refer to the application circuit 1 in the section "Typical Application Circuits", V_{IN}=12V, V_{OUT}=3.3V, L1=10µH)

Enable Through EN Pin



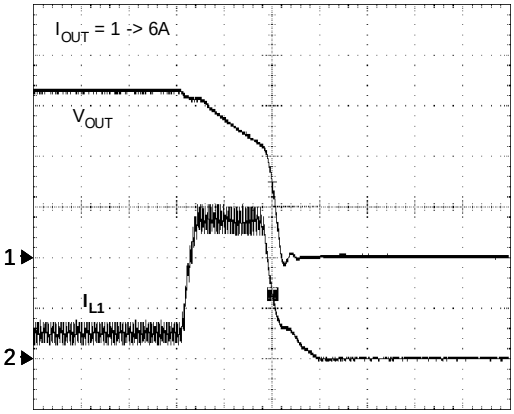
Ch1: V_{EN}, 5V/Div, DC
Ch2: V_{OUT}, 2V/Div, DC
Ch3: I_{L1}, 2A/Div, DC
Time: 5ms/Div

Shutdown Through EN Pin



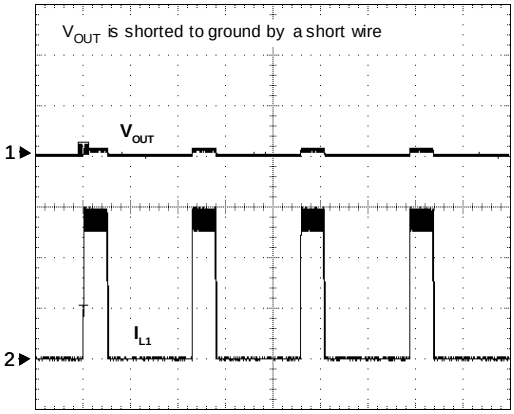
Ch1: V_{EN}, 5V/Div, DC
Ch2: V_{OUT}, 2V/Div, DC
Ch3: I_{L1}, 2A/Div, DC
Time: 5ms/Div

Over Current



Ch1: V_{OUT}, 1V/Div, DC
Ch2: I_{L1}, 2A/Div, DC
Time: 50µs/Div

Short Circuit

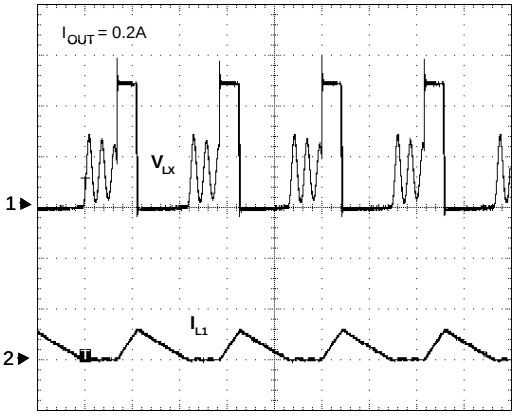


Ch1: V_{OUT}, 1V/Div, DC
Ch2: I_{L1}, 2A/Div, DC
Time: 50ms/Div

Operating Waveforms (Cont.)

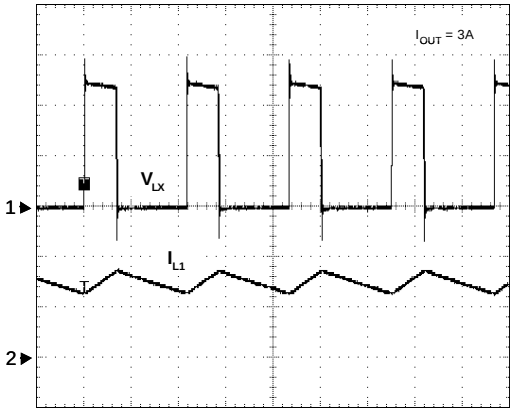
(Refer to the application circuit 1 in the section “Typical Application Circuits”, V_{IN}=12V, V_{OUT}=3.3V, L1=10µH)

Switching Waveform



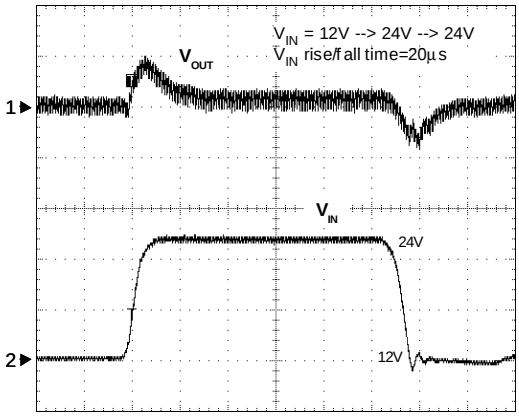
Ch1: V_{LX}, 5V/Div, DC
Ch2: I_{L1}, 1A/Div, DC
Time: 1.25µs/Div

Switching Waveform



Ch1: V_{LX}, 5V/Div, DC
Ch2: I_{L1}, 2A/Div, DC
Time: 1.25µs/Div

Line Transient Response

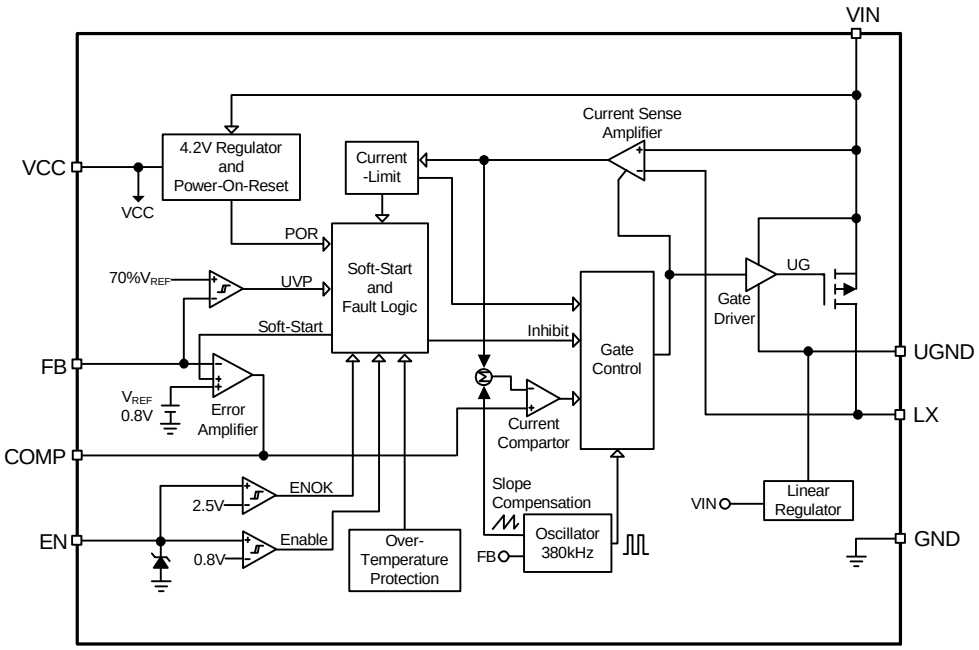


Ch1: V_{OUT}, 50mV/Div, DC,
Voltage Offset = 3.3V
Ch2: V_{IN}, 5V/Div, DC,
Voltage Offset = 12V
Time: 50µs/Div

Pin Description

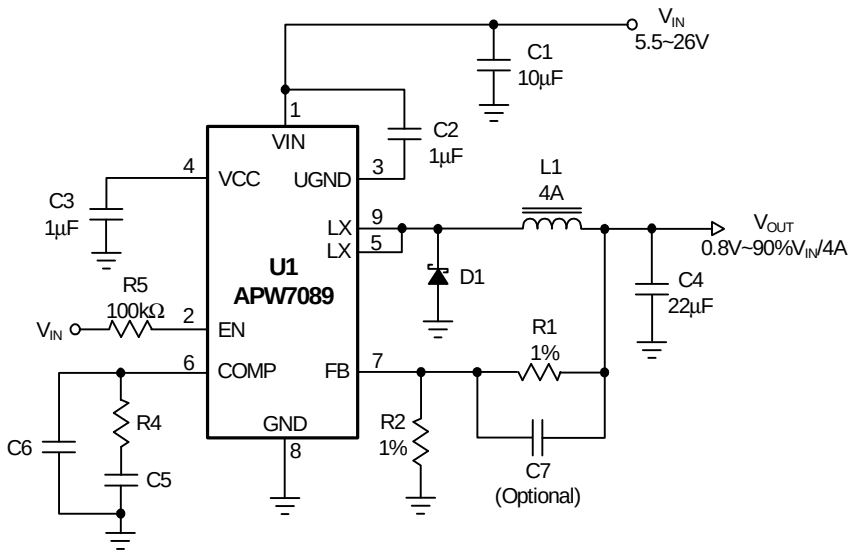
PIN		FUNCTION
NO.	NAME	
1	VIN	Power Input. VIN supplies the power (4.5V to 26V) to the control circuitry, gate driver and step-down converter switch. Connecting a ceramic bypass capacitor and a suitably large capacitor between VIN and GND eliminates switching noise and voltage ripple on the input to the IC.
2	EN	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator, drive it low to turn it off. Pull up with 100kΩ resistor for automatic start-up.
3	UGND	Gate driver power ground of the P-channel Power MOSFET. A linear regulator regulates a 5.5V voltage between VIN and UGND to supply power to P-channel MOSFET gate driver. Connect a ceramic capacitor (1μF typ.) between VIN and UGND for noise decoupling and stability of the linear regulator.
4	VCC	Bias input and 4.2V linear regulator's output. This pin supplies the bias to some control circuits. The 4.2V linear regulator converts the voltage on VIN to 4.2V to supply the bias when no external 5V power supply is connected with VCC. Connect a ceramic capacitor (1μF typ.) between VCC and GND for noise decoupling and stability of the linear regulator.
5	LX	Power Switching Output. Connect this pin to the underside Exposed Pad.
6	COMP	Output of error amplifier. Connect a series RC network from COMP to GND to compensate the regulation control loop. In some cases, an additional capacitor from COMP to GND is required for noise decoupling.
7	FB	Feedback Input. The IC senses feedback voltage via FB and regulate the voltage at 0.8V. Connecting FB with a resistor-divider from the output set the output voltage in the range from 0.8V to 90% V_{IN}.
8	GND	Power and Signal Ground.
9 (Exposed Pad)	LX	Power Switching Output. LX is the Drain of the P-channel MOSFET to supply power to the output. The Exposed Pad provides current with lower impedance than Pin 5. Connect the pad to output LC filter via a top-layer thermal pad on PCBs. The PCB will be a heat sink of the IC.

Block Diagram



Typical Application Circuit

1. 5.5~26V Single Power Input Step-down Converter (with Ceramic Input/Output Capacitors)



Recommended Feedback Compensation Network Components List:

V_{IN} (V)	V_{OUT} (V)	L1 (µH)	C4 (µF)	C4 ESR (mΩ)	R1 (kΩ)	R2 (kΩ)	C7 (pF)	R4 (kΩ)	C5 (pF)	C6 (pF)
24	12	15	22	5	140	10	22	62	820	22
24	12	15	44	3	140	10	22	120	820	22
24	5	10	22	5	63.4	12	33	24	1500	22
24	5	10	44	3	63.4	12	33	51	1500	22
12	5	10	22	5	63.4	12	68	24	820	22
12	5	10	44	3	63.4	12	68	51	820	22
12	3.3	10	22	5	47	15	82	15	1000	22
12	3.3	10	44	3	47	15	82	33	1000	22
12	2	4.7	22	5	30	20	56	10	2200	22
12	2	4.7	44	3	30	20	56	20	2200	22
12	1.2	3.3	22	5	7.5	15	150	6.2	3300	22
12	1.2	3.3	44	3	7.5	15	150	12	3300	22
5	3.3	3.3	22	5	47	15	68	15	560	22
5	3.3	3.3	44	3	47	15	68	33	560	22
5	1.2	2.2	22	5	7.5	15	270	5.6	1500	22
5	1.2	2.2	44	3	7.5	15	270	12	1500	22
5	0.8	2.2	22	5	0	NC	NC	2.7	2700	22
5	0.8	2.2	44	3	0	NC	NC	6.2	2700	22

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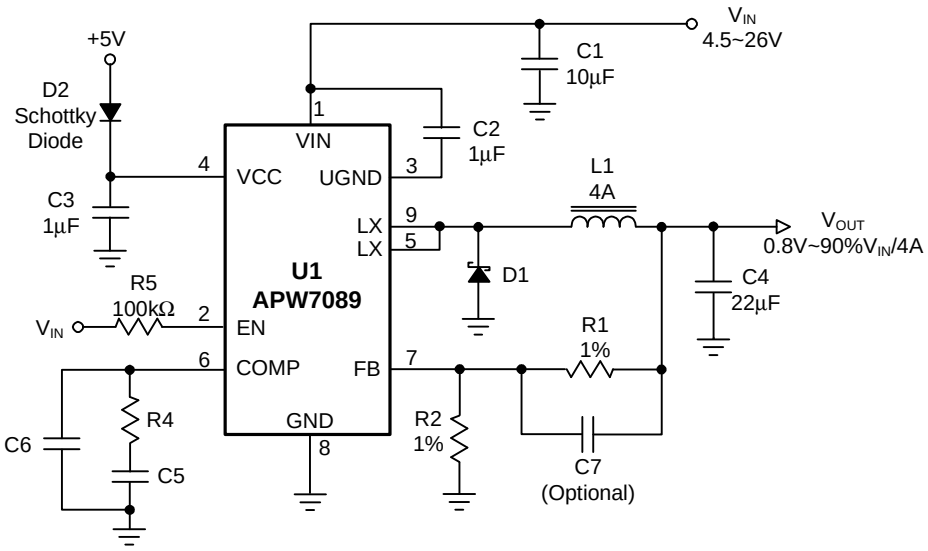
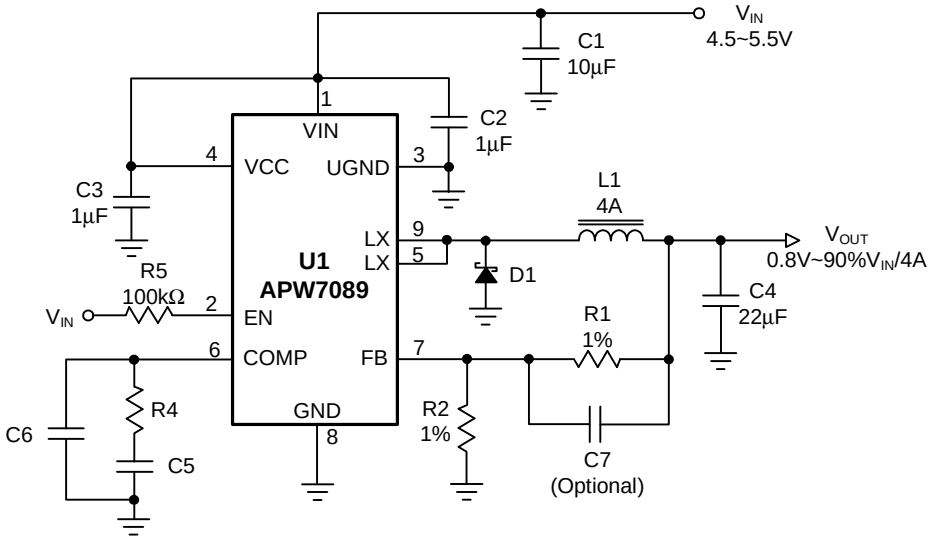
Typical Application Circuit (Cont.)

2. Dual Power Inputs Step-down Converter (V_{IN}=4.5~26V)

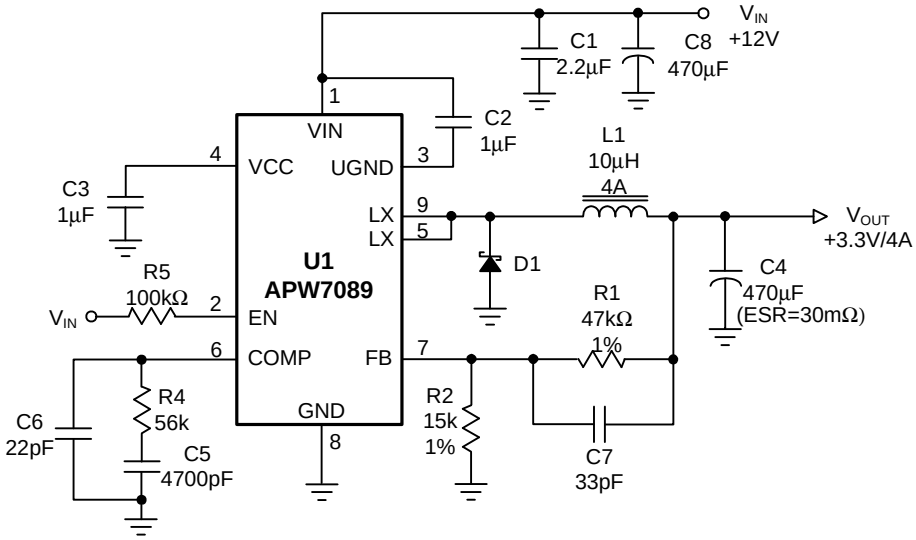


3. 4.5~5.5V Single Power Input Step-down Converter

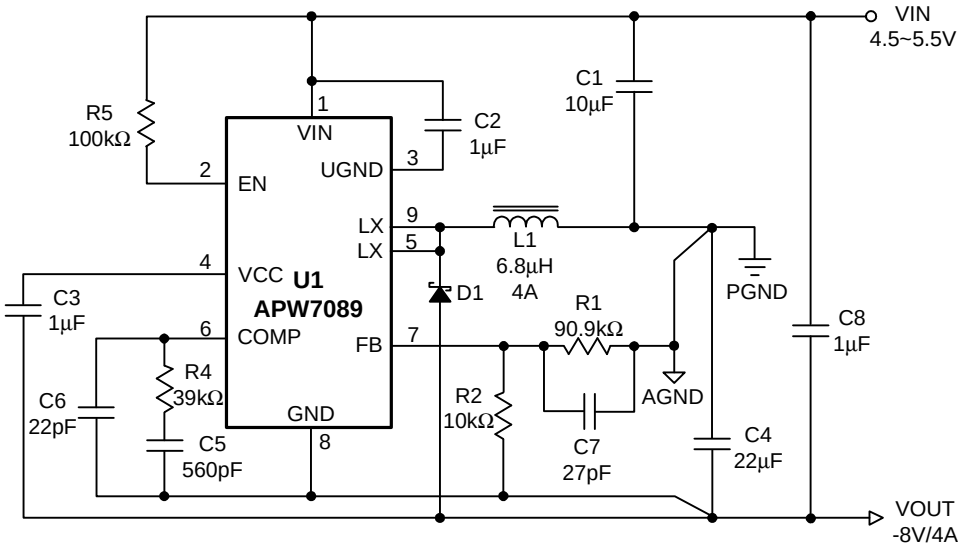


Typical Application Circuit (Cont.)

4. +12V Single Power Input Step-down Converter (with Electrolytic Input/Output Capacitors)



5. -8V Inverting Converter with 4.5~5.5V Single Power Input



Function Description

Main Control Loop

The APW7089 is a constant frequency current mode switching regulator. During normal operation, the internal P-channel power MOSFET is turned on each cycle when the oscillator sets an internal RS latch and would be turned off when an internal current comparator (ICMP) resets the latch. The peak inductor current at which ICMP resets the RS latch is controlled by the voltage on the COMP pin, which is the output of the error amplifier (EAMP). An external resistive divider connected between V_{OUT} and ground allows the EAMP to receive an output feedback voltage V_{FB} at FB pin. When the load current increases, it causes a slight decrease in V_{FB} relative to the 0.8V reference, which in turn causes the COMP voltage to increase until the average inductor current matches the new load current.

VCC Power-On-Reset(POR) and EN Under-voltage Lockout

The APW7089 keeps monitoring the voltage on VCC pin to prevent wrong logic operations which may occur when VCC voltage is not high enough for the internal control circuitry to operate. The VCC POR has a rising threshold of 3.9V (typical) with 0.15V of hysteresis.

An external under-voltage lockout (UVLO) is sensed and programmed at the EN pin. The EN UVLO has a rising threshold of 2.5V with 0.2V of hysteresis. The EN UVLO should be programmed by connecting a resistive divider from VIN to EN to GND.

After the VCC, EN, and VIN-to-UGND voltages exceed their respective voltage thresholds, the IC starts a start-up process and then ramps up the output voltage to the setting of output voltage. Connect a RC network from EN to GND to set a turn-on delay that can be used to sequence the output voltages of multiple devices.

VCC 4.2V Linear Regulator

VCC is the output terminal of the internal 4.2V linear regulator which is powered from VIN and provides power to the APW7089. The linear regulator is designed to be stable with a low-ESR ceramic output capacitor powers the internal control circuitry. Bypass VCC to GND with a ceramic capacitor of at least 0.22µF. Place the capacitor physically close to the IC to provide good noise decoupling. The linear regulator is not intended for powering up any external loads. Do not connect any external loads to VCC. The linear regulator is also equipped with current-limit protection to protect itself during over-load or short-circuit conditions on VCC pin.

VIN-to-UGND 5.5V Linear Regulator

The built-in 5.5V linear regulator regulates a 5.5V voltage between VIN and UGND pins to supply bias and gate charge for the P-channel Power MOSFET gate driver. The linear regulator is designed to be stable with a low-ESR ceramic output capacitor of at least 0.22µF. It is also equipped with current-limit function to protect itself during over-load or short-circuit conditions between VIN and UGND.

The APW7089 shuts off the output of the converters when the output voltage of the linear regulator is below 3.5V (typical). The IC resumes working by initiating a new soft-start process when the linear regulator's output voltage is above the undervoltage lockout voltage threshold.

Digital Soft-Start

The APW7089 has a built-in digital soft-start to control the output voltage rise and limit the input current surge during start-up. During soft-start, an internal ramp, connected to the one of the positive inputs of the error amplifier, rises up from 0V to 1V to replace the reference voltage (0.8V) until the ramp voltage reaches the reference voltage.

The device is designed with a preceding delay about 10.8ms (typical) before soft-start process.

Output Under-Voltage Protection

In the process of operation, if a short-circuit occurs, the output voltage will drop quickly. Before the current-limit circuit responds, the output voltage will fall out of the required regulation range. The under-voltage continually monitors the FB voltage after soft-start is completed. If a load step is strong enough to pull the output voltage lower than the under-voltage threshold, the IC shuts down converter's output.

The under-voltage threshold is 70% of the nominal out-

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Function Description (Cont.)

Output Under-Voltage Protection (Cont.)

put voltage. The under-voltage comparator has a built-in 2μs noise filter to prevent the chips from wrong UVP shut-down caused by noise. The under-voltage protection works in a hiccup mode without latched shutdown. The IC will initiate a new soft-start process at the end of the preceeding delay.

Over-Temperature Protection (OTP)

The over-temperature circuit limits the junction temperature of the APW7089. When the junction temperature exceeds T_J = +150°C, a thermal sensor turns off the power MOSFET, allowing the devices to cool. The thermal sensor allows the converter to start a start-up process and regulate the output voltage again after the junction temperature is cooled by 50°C. The OTP is designed with a 50°C hysteresis to lower the average T_J during continuous thermal overload conditions, increasing lifetime of the IC.

Enable/Shutdown

Driving EN to ground places the APW7089 in shutdown. When in shutdown, the internal power MOSFET turns off, all internal circuitry shuts down and the quiescent supply current of VIN reduces to <1μA (typical).

Current-Limit Protection

The APW7089 monitors the output current, flowing through the P-channel power MOSFET, and limits the current peak at current-limit level to prevent loads and the IC from damages during overload or short-circuit conditions.

Frequency Foldback

When the output is shortened to ground, the frequency of the oscillator will be reduced to about 80kHz. This lower frequency allows the inductor current to safely discharge, thereby preventing current runaway. The oscillator's frequency will gradually increase to its designed rate when the feedback voltage on FB again approaches 0.8V.

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Application Information

Power Sequencing

The APW7089 can operate with sigle or dual power input(s). In dual-power applications, the voltage (V_{CC}) applied at VCC pin must be lower than the voltage (V_{IN}) on VIN pin. The reason is the internal parasitic diode from VCC to VIN will conduct due to the forward-voltage between VCC and VIN. Therefore, V_{IN} must be provided before V_{CC}.

Setting Output Voltage

The regulated output voltage is determined by:

$$V_{OUT} = 0.8 \cdot (1 + \frac{R1}{R2}) \quad (V)$$

Suggested R2 is in the range from 1K to 20kΩ. For portable applications, a 10kΩ resistor is suggested for R2. To prevent stray pickup, locate resistors R1 and R2 close to APW7089.

Input Capacitor Selection

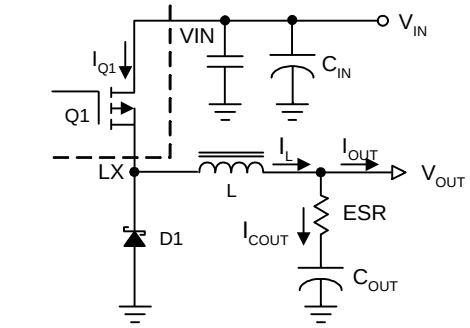
It is necessary to turn on the P-channel power MOSFET (Q1) each time when using small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the surge current. Place the small ceramic capcaitors physically close to the VIN and between VIN and the anode of the Schottky diode (D1)

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The RMS current (I_{RMS}) of the bulk input capacitor is calculated as the following equation:

$$I_{RMS} = I_{OUT} \cdot \sqrt{D \cdot (1-D)} \quad (A)$$

where D is the duty cycle of the power MOSFET.

For a through hole design, several electrolytic capacitors may be needed. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating.



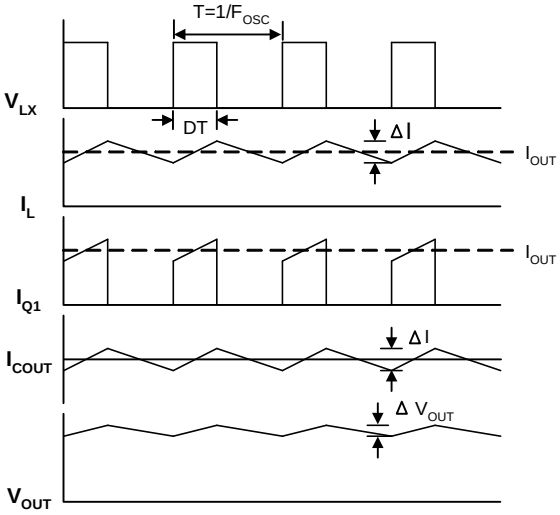


Figure 1. Converter Waveforms

Output Capacitor Selection

An output capacitor is required to filter the output and supply the load transient current. The filtering requirements are the function of the switching frequency and the ripple current (ΔI). The output ripple is the sum of the voltages, having phase shift, across the ESR and the ideal output capacitor. The peak-to-peak voltage of the ESR is calculated as the following equations:

$$D = \frac{V_{OUT} + V_D}{V_{IN} + V_D} \quad \text{..... (1)}$$

$$\Delta I = \frac{V_{OUT} \cdot (1-D)}{F_{OSC} \cdot L} \quad \text{..... (2)}$$

$$V_{ESR} = \Delta I \cdot ESR \quad (V) \quad \text{..... (3)}$$

where V_D is the forward voltage drop of the diode.

The peak-to-peak voltage of the ideal output capacitor is calculated as the following equation:

Application Information (Cont.)

Output Capacitor Selection (Cont.)

$$\Delta V_{COUT} = \frac{\Delta I}{8 \cdot F_{OSC} \cdot C_{OUT}} \text{ (V)} \quad \text{..... (4)}$$

For the applications using bulk capacitors, the ΔV_{COUT} is much smaller than the V_{ESR} and can be ignored. Therefore, the AC peak-to-peak output voltage (ΔV_{OUT}) is shown as below:

$$\Delta V_{OUT} = \Delta I \cdot ESR \quad \text{(V)} \quad \text{..... (5)}$$

For the applications using ceramic capacitors, the V_{ESR} is much smaller than the ΔV_{COUT} and can be ignored. Therefore, the AC peak-to-peak output voltage (ΔV_{OUT}) is close to ΔV_{COUT}.

The load transient requirements are the function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout. High frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (Effective Series Resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes. However, the Equivalent Series Inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading.

Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies permit the use of a smaller inductor for the same amount of inductor ripple current. However, this is at the expense of efficiency due to an increase in MOSFET gate charge losses. The equation (2) shows that the inductance value has a direct effect on ripple current.

Accepting larger values of ripple current allows the use of low inductances but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I \le 0.4 \cdot I_{OUT(MAX)}$. Remember, the maximum ripple current occurs at the maximum input voltage. The minimum inductance of the inductor is calculated by using the following equation:

$$\frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{380000 \cdot L \cdot V_{IN}} \le 1.6$$

$$L \ge \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{608000 \cdot V_{IN}} \quad \text{(H)} \quad \text{..... (6)}$$

where $V_{IN} = V_{IN(MAX)}$

Output Diode Selection

The Schottky diode carries load current during the off-time. The average diode current is therefore dependent on the P-channel power MOSFET duty cycle. At high input voltages, the diode conducts most of the time. As V_{IN} approaches V_{OUT}, the diode conducts only a small fraction of the time. The most stressful condition for the diode is when the output is short-circuited. Therefore, it is important to adequately specify the diode peak current and average power dissipation so as not to exceed the diode ratings.

Under normal load conditions, the average current conducted by the diode is:

$$I_D = \frac{V_{IN} - V_{OUT}}{V_{IN} + V_D} \cdot I_{OUT}$$

The APW7089 is equipped with whole protections to reduce the power dissipation during short-circuit condition. Therefore, the maximum power dissipation of the diode is calculated from the maximum output current as:

$$P_{DIODE(MAX)} = V_D \cdot I_{D(MAX)}$$

where $I_{OUT} = I_{OUT(MAX)}$

Remember to keep lead length short and observe proper grounding to avoid ringing and increased dissipation.

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Application Information (Cont.)

Layout Consideration

In high power switching regulator, a correct layout is important to ensure proper operation of the regulator. In general, interconnecting impedance should be minimized by using short, wide printed circuit traces. Signal and power grounds are to be kept separating and finally combined using ground plane construction or single point grounding. Figure 2 illustrates the layout, with bold lines indicating high current paths. Components along the bold lines should be placed close together. Below is a checklist for your layout:

1. Begin the layout by placing the power components first. Orient the power circuitry to achieve a clean power flow path. If possible, make all the connections on one side of the PCB with wide, copper filled areas.
2. In Figure 2, the loops with same color bold lines conduct high slew rate current. These interconnecting impedances should be minimized by using wide and short printed circuit traces.
3. Keep the sensitive small signal nodes (FB, COMP) away from switching nodes (LX or others) on the PCB. Therefore, place the feedback divider and the feedback compensation network close to the IC to avoid switching noise. Connect the ground of feedback divider directly to the GND pin of the IC using a dedicated ground trace.
4. The VCC decoupling capacitor should be right next to the VCC and GND pins. Capacitor C2 should be connected as close to the VIN and UGND pins as possible.

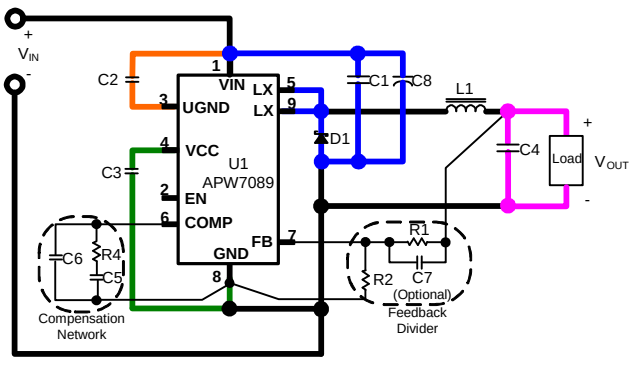


Figure 2. Current Path Diagram

5. Place the decoupling ceramic capacitor C1 near the VIN as close as possible. The bulk capacitors C8 are also placed near VIN. Use a wide power ground plane to connect the C1, C8, C4, and Schottky diode to provide a low impedance path between the components for large and high slew rate current.

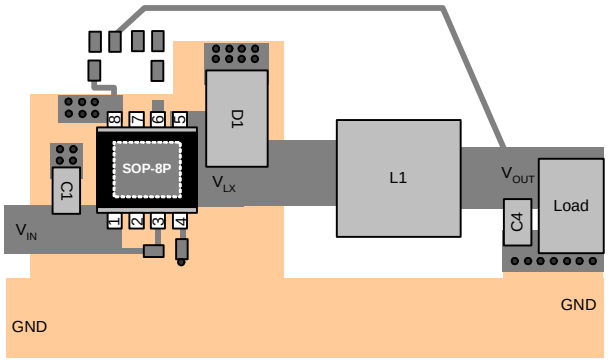


Figure 3. Recommended Layout Diagram

Thermal Consideration

In Figure 4, the SOP-8P is a cost-effective package featuring a small size, like a standard SOP-8, and a bottom exposed pad to minimize the thermal resistance of the package, being applicable to high current applications. The exposed pad must be soldered to the top V_{LX} plane. The copper of the V_{LX} plane on the Top layer conducts heat into the PCB and air. Please enlarge the area of V_{LX} plan to reduces the case-to-ambient resistance (θ_{CA}).

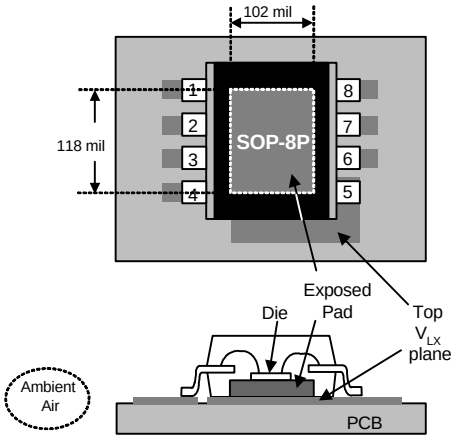
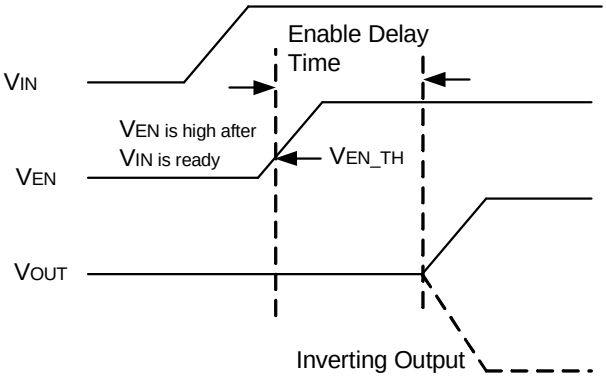


Figure 4.

Application Information (Cont.)

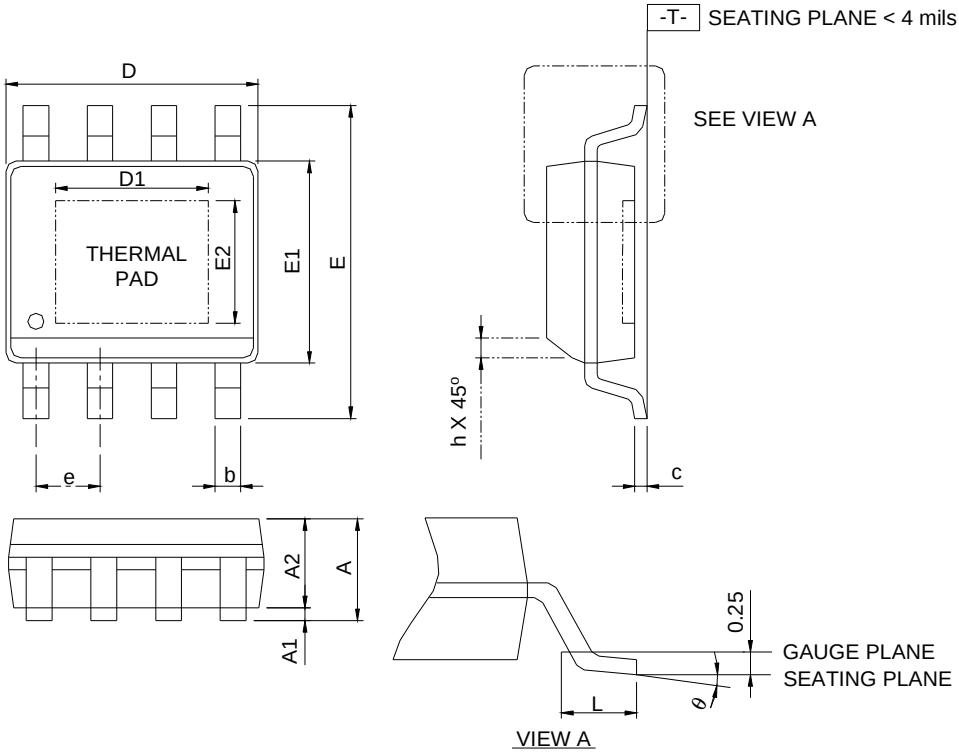
Power-on Sequencing

The VIN voltage and EN signal should have the correct power-up sequence to avoid triggering UVP or incorrect soft start at startup. The recommended power-on sequencing should be to provide the EN signal after the VIN voltage is ready. The recommended power-on sequence is shown in below figure.



Package Information

SOP-8P



SYMBOL	SOP-8P			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.60		0.063
A1	0.00	0.15	0.000	0.006
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
D1	2.50	3.50	0.098	0.138
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
E2	2.00	3.00	0.079	0.118
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°C	8°C	0°C	8°C

Note : 1. Followed from JEDEC MS-012 BA.
2. Dimension "D" does not include mold flash, protrusions or gate burrs.
Mold flash, protrusion or gate burrs shall not exceed 6 mil per side .
3. Dimension "E" does not include inter-lead flash or protrusions.
Inter-lead flash and protrusions shall not exceed 10 mil per side.

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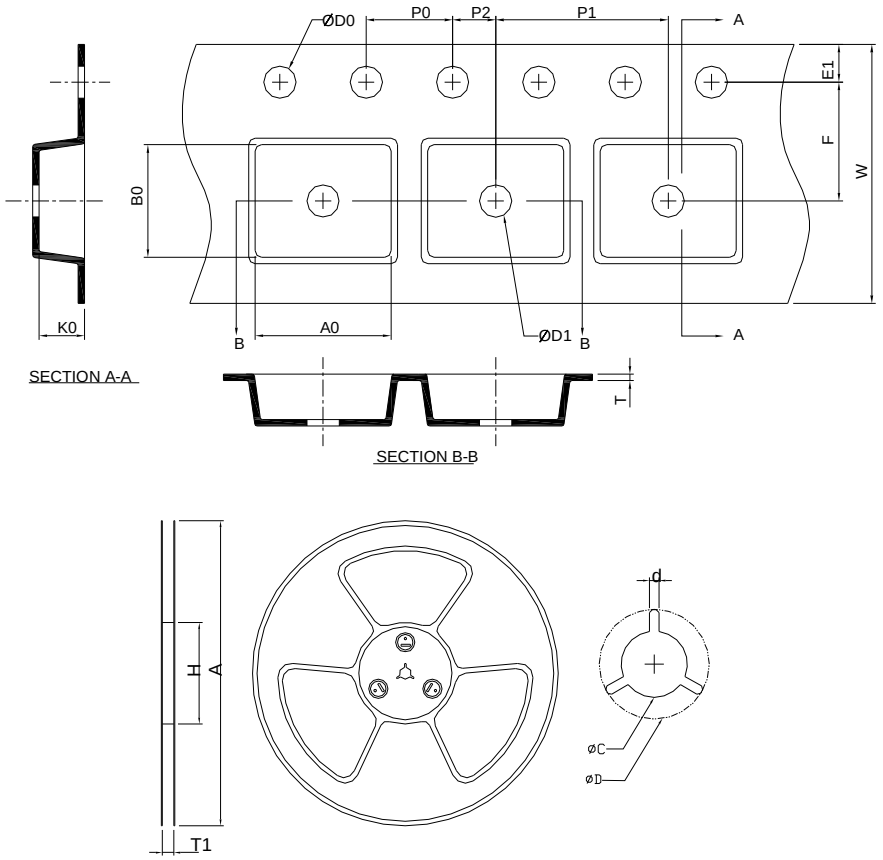
Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
SOP- 8P	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	5.20±0.20	2.10±0.20

(mm)

Devices Per Unit

Package Type	Unit	Quantity
SOP- 8P	Tape & Reel	2500

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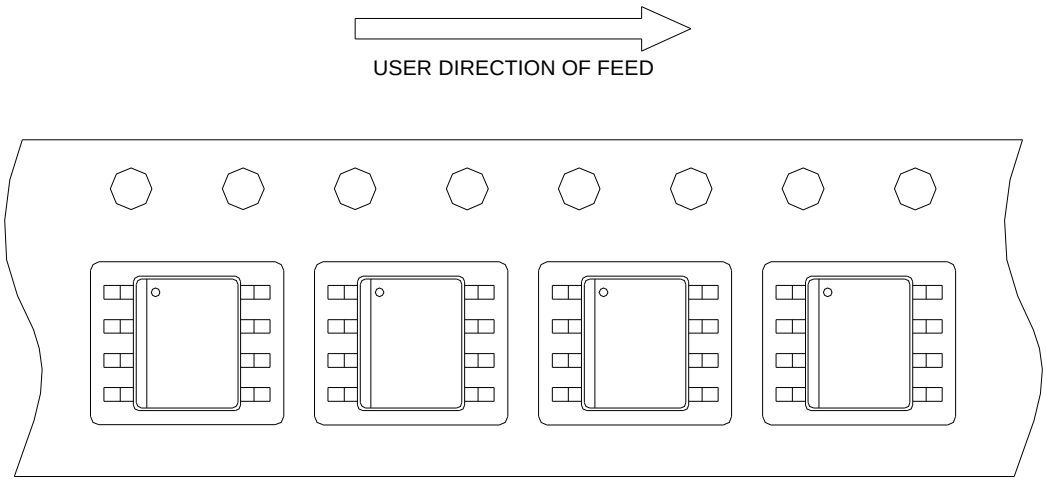
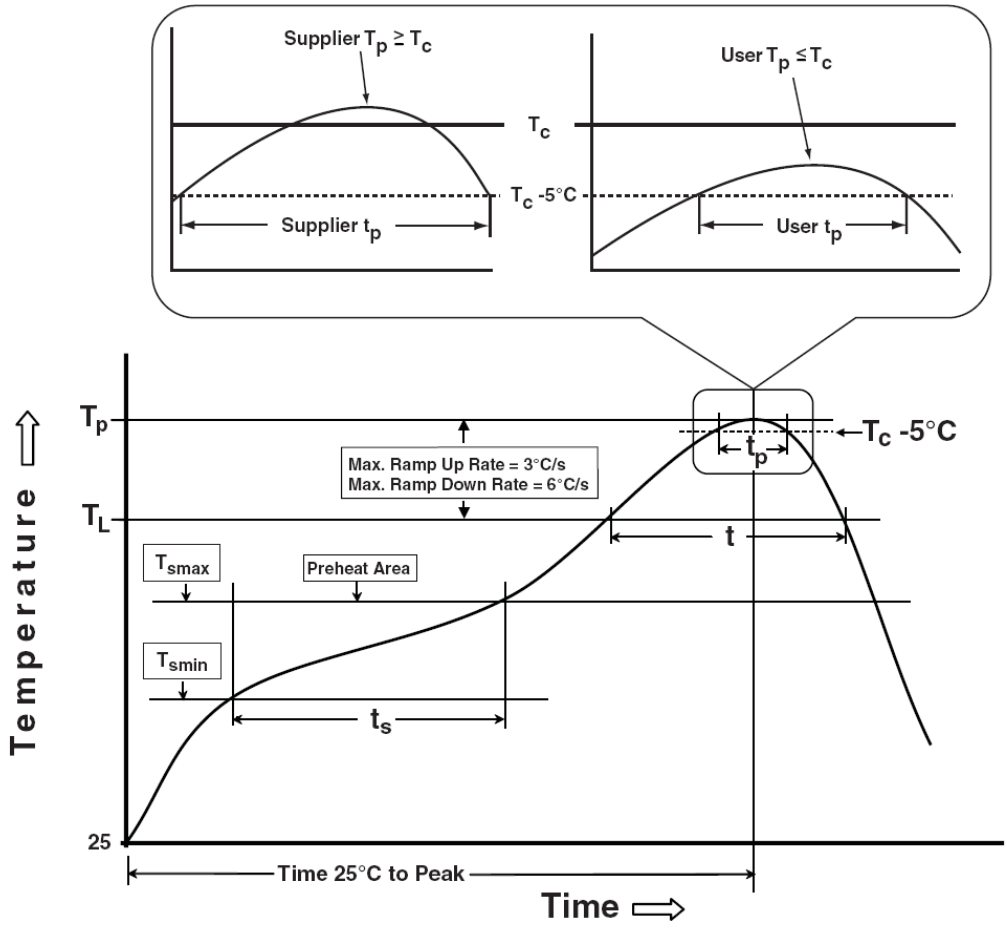
Taping Direction Information

SOP-8P



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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