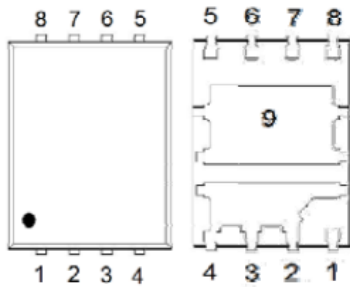


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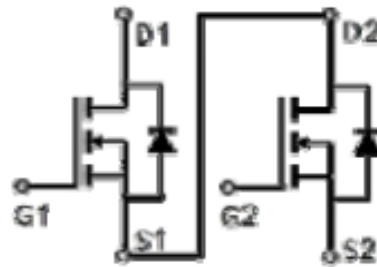
N-Channel Enhancement Mode MOSFET

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D	Channel
30V	7m Ω @ $V_{GS}=10V$	50A	Q1
30V	5.5m Ω @ $V_{GS}=10V$	58A	Q2



1 : G1
2,3,4 : D1
5,6,7 : S2
8 : G2
9 : S1/D2



PDFN 5X6P

ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	CH.	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	Q1	30	V
			Q2	30	
Gate-Source Voltage		V_{GS}	Q1	± 20	V
			Q2	± 20	
Continuous Drain Current ³	$T_C = 25\text{ }^\circ\text{C}$	I_D	Q1	50	A
			Q2	58	
	$T_C = 100\text{ }^\circ\text{C}$		Q1	31	
			Q2	36	
Pulsed Drain Current ¹		I_{DM}	Q1	81	A
			Q2	104	
Continuous Drain Current	$T_A = 25\text{ }^\circ\text{C}$	I_D	Q1	12	A
			Q2	15	
	$T_A = 70\text{ }^\circ\text{C}$		Q1	10	
			Q2	12	
Avalanche Current		I_{AS}	Q1	22	A
			Q2	30	
Avalanche Energy	L = 0.1mH	E_{AS}	Q1	24	mJ
			Q2	45	
Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	P_D	Q1	28	W
			Q2	35	
	$T_C = 100\text{ }^\circ\text{C}$		Q1	11	
			Q2	14	

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Power Dissipation	$T_A = 25\text{ }^\circ\text{C}$	P_D	Q1	2.1	W
			Q2	2.4	
	$T_A = 70\text{ }^\circ\text{C}$		Q1	1.3	
			Q2	1.5	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150		$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL		TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient ²	$R_{\theta JA}$	Q1		59	$^\circ\text{C} / \text{W}$
	$R_{\theta JA}$	Q2		52	
Junction-to-Case	$R_{\theta JC}$	Q1		4.4	
	$R_{\theta JC}$	Q2		3.5	

¹Pulse width limited by maximum junction temperature $T_{J(\text{MAX})}=150^\circ\text{C}$.

²The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ\text{C}$. The value in any given application depends on the user's specific board design.

³Package limitation current :Q1=25A,Q2=34A.

ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	CH.	LIMITS			UNITS	
				MIN	TYP	MAX		
STATIC								
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu\text{A}$	Q1	30			V	
			Q2	30				
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	Q1	1.3	1.6	2.3	V	
			Q2	1.3	1.7	2.3		
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$	Q1			± 100	nA	
			Q2			± 100		
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 24V, V_{GS} = 0V$	Q1			1	μA	
			Q2			1		
		$V_{DS} = 20V, V_{GS} = 0V, T_J = 55\text{ }^\circ\text{C}$	Q1			10		
			Q2			10		
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = 4.5V, I_D = 12A$	Q1		6.3	9.5	m Ω	
			Q2		4.3	8		
			$V_{GS} = 10V, I_D = 12A$	Q1		4.8		7
				Q2		3.3		5.5
Forward Transconductance ¹	g_{fs}	$V_{DS} = 5V, I_D = 12A$	Q1		67		S	
			Q2		80			

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DYNAMIC							
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 15V, f = 1MHz$	Q1		852	pF	
			Q2		1395		
Output Capacitance	C_{oss}		Q1		162		
			Q2		275		
Reverse Transfer Capacitance	C_{rss}		Q1		103		
			Q2		167		
Gate Resistance	R_g	$V_{GS} = 0V, V_{DS} = 0V, f = 1MHz$	Q1		2.1	Ω	
			Q2		1.3		
Total Gate Charge ²	$Q_g(V_{GS} = 10V)$	Q1 $V_{DS} = 15V, V_{GS} = 10V,$ $I_D = 12V,$ Q2 $V_{DS} = 15V, V_{GS} = 10V,$ $I_D = 15A$	Q1		18.6	nC	
	$Q_g(V_{GS} = 4.5V)$		Q2		29.6		
Gate-Source Charge ²			Q_{gs}	Q1			10
	Q2				15.7		
Gate-Drain Charge ²	Q_{gd}		Q1		2		
			Q2		4.1		
Turn-On Delay Time ²	$t_{d(on)}$	Q1 $V_{DS} = 15V, I_D \cong 12A,$ $V_{GS} = 10V, R_{GEN} = 6\Omega$ Q2 $V_{DS} = 15V, I_D \cong 15A,$ $V_{GS} = 10V, R_{GEN} = 6\Omega$	Q1		18	nS	
			Q2		27		
Rise Time ²	t_r		Q1		13		
			Q2		16		
Turn-Off Delay Time ²	$t_{d(off)}$		Q1		33		
			Q2		66		
Fall Time ²	t_f	Q1		15			
		Q2		23			
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_J = 25^\circ C$)							
Continuous Current ³	I_S		Q1		23	A	
			Q2		29		
Forward Voltage ¹	V_{SD}		$I_F = 12A, V_{GS} = 0V$	Q1		1.2	V
			$I_F = 15A, V_{GS} = 0V$	Q2		1.2	
Reverse Recovery Time	t_{rr}		Q1 $I_F = 12A, di_F/dt = 100A / \mu S$ Q2 $I_F = 15A, di_F/dt = 100A / \mu S$	Q1		15.8	nS
				Q2		21.3	
Reverse Recovery Charge	Q_{rr}	Q1			5.1	nC	
		Q2			8.8		

¹Pulse test : Pulse Width $\leq 300 \mu sec$, Duty Cycle $\leq 2\%$.

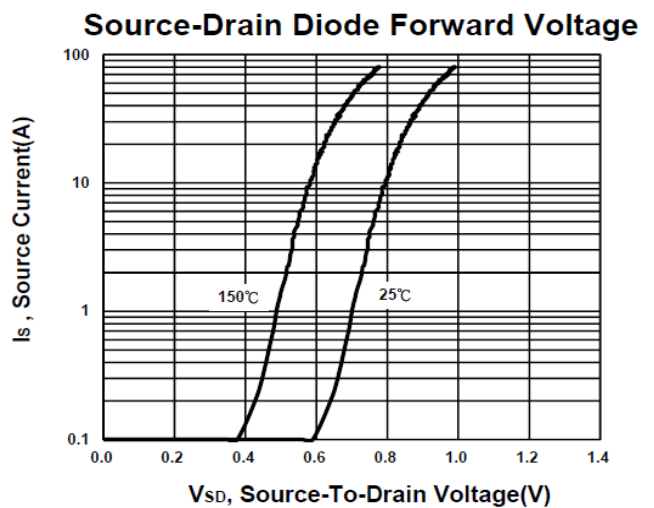
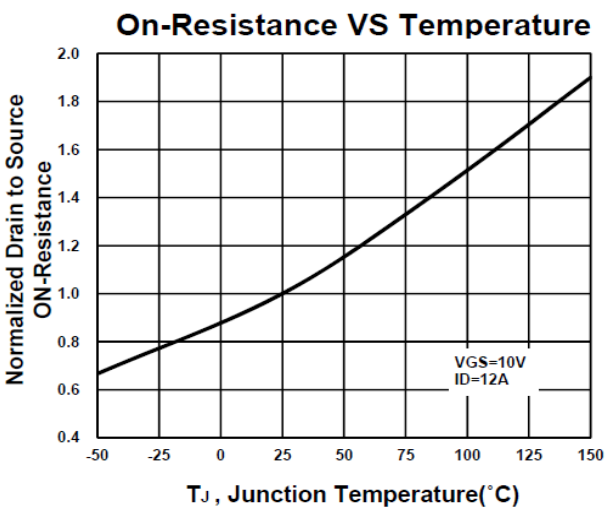
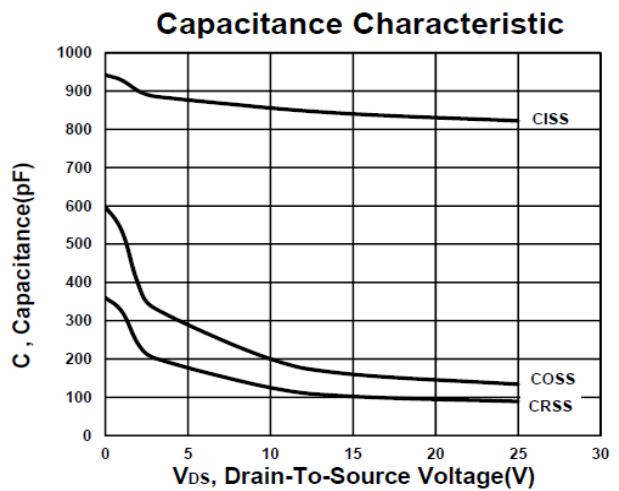
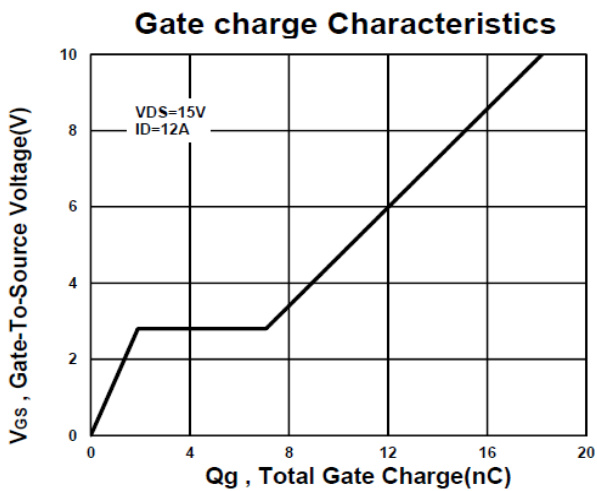
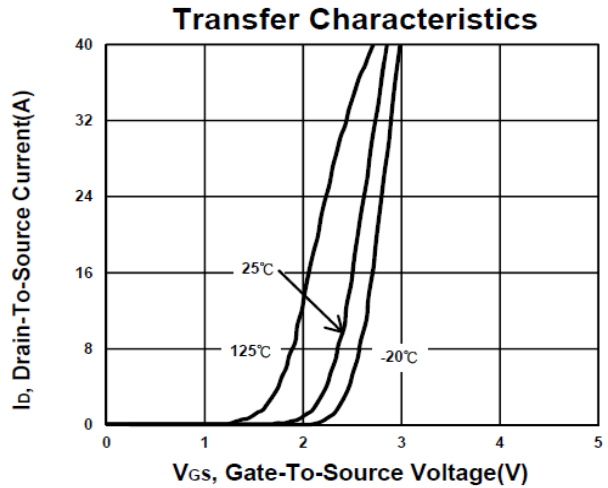
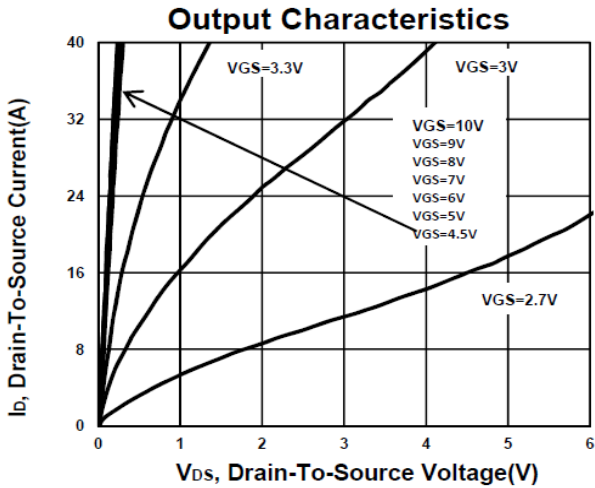
²Independent of operating temperature.

³Package limitation current : Q1=25A, Q2=34A.

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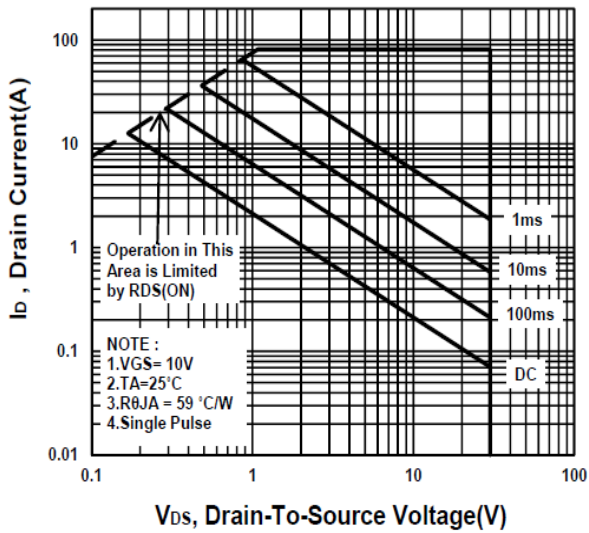
Q1



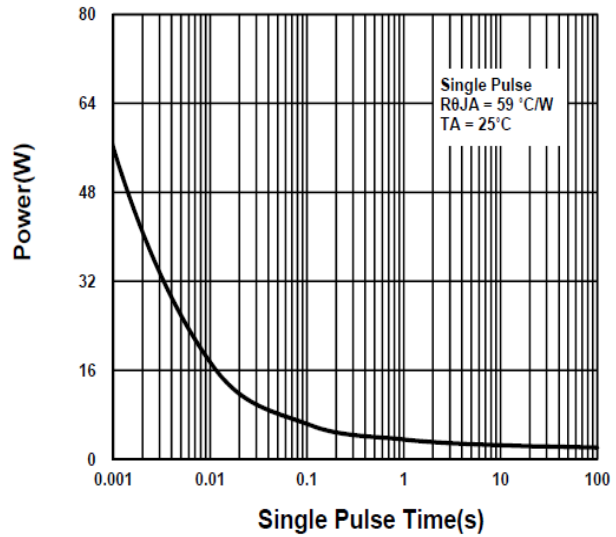
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N-Channel Enhancement Mode MOSFET

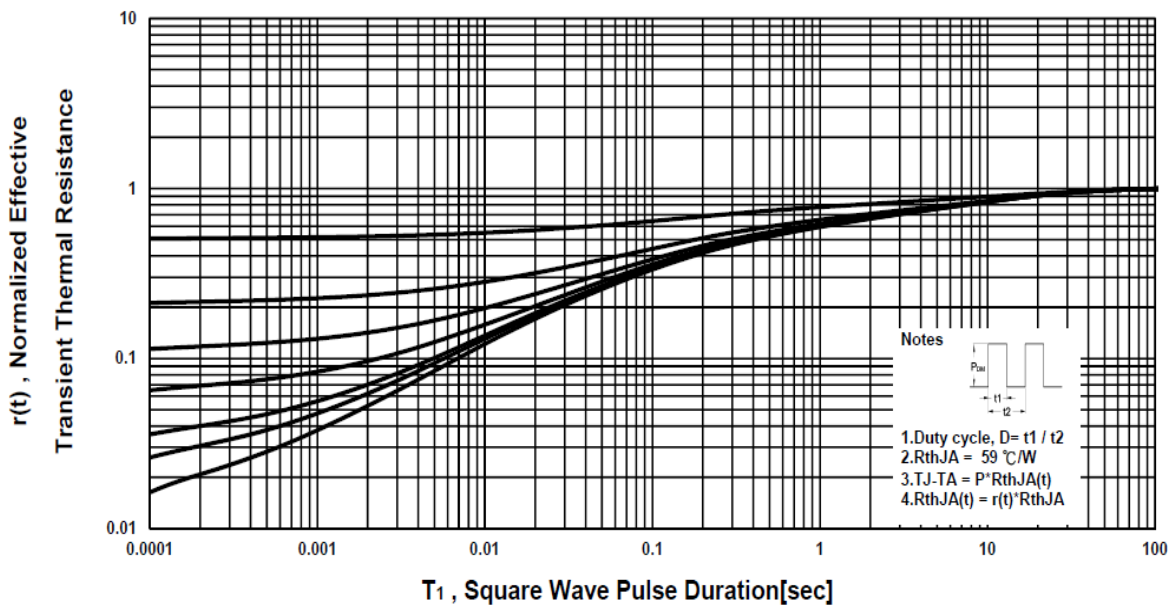
Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve

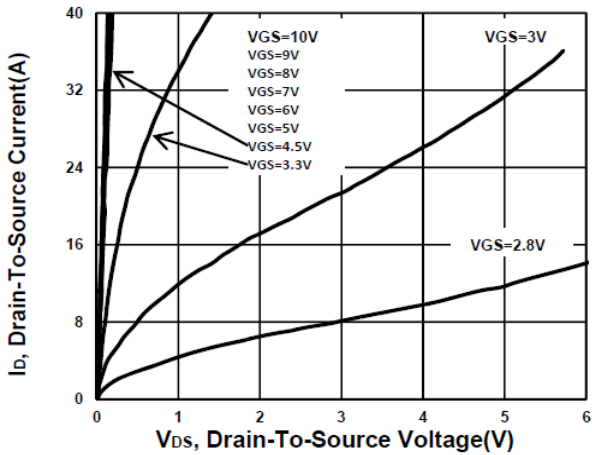


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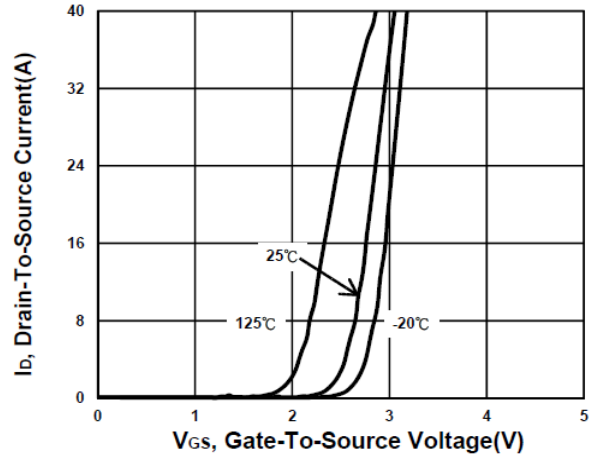
N-Channel Enhancement Mode MOSFET

Q2

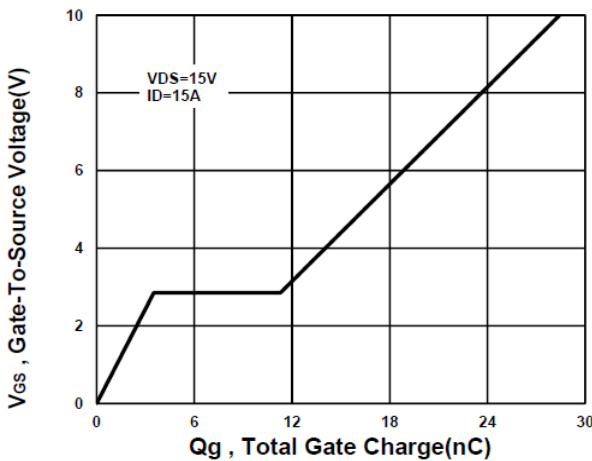
Output Characteristics



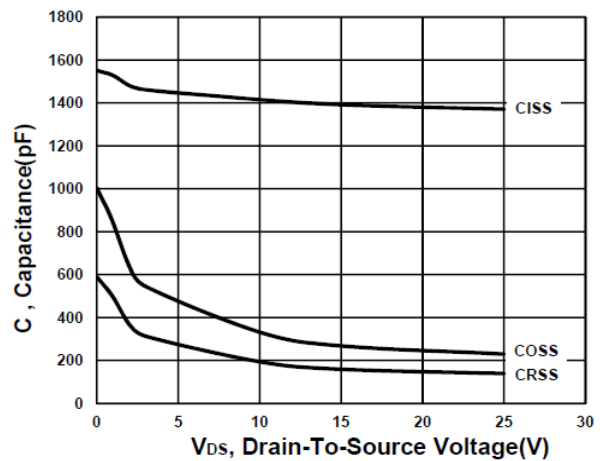
Transfer Characteristics



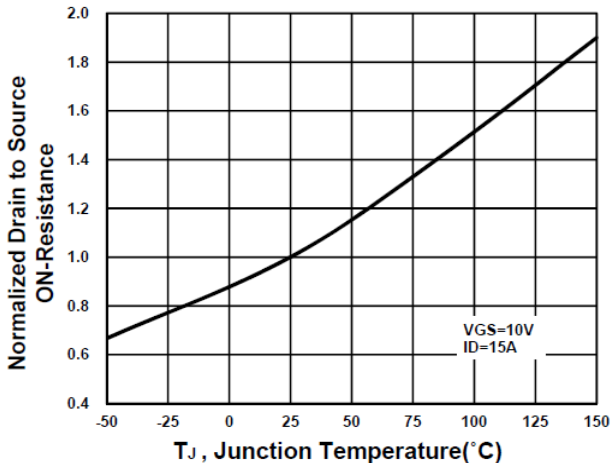
Gate charge Characteristics



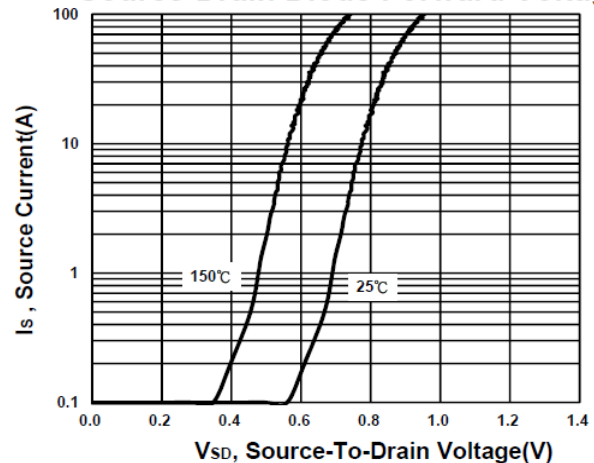
Capacitance Characteristic



On-Resistance VS Temperature



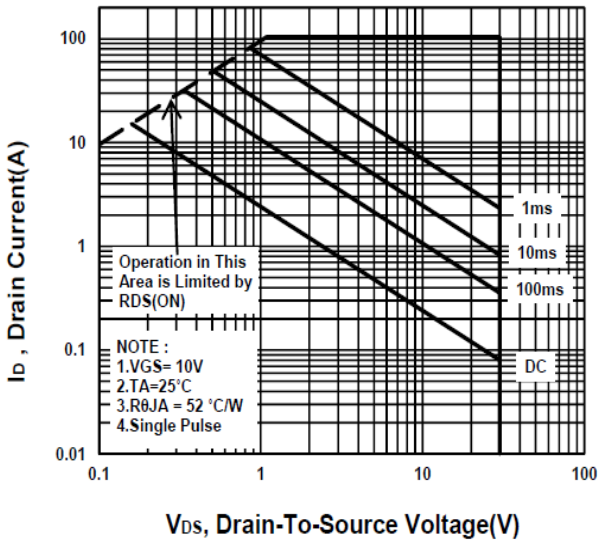
Source-Drain Diode Forward Voltage



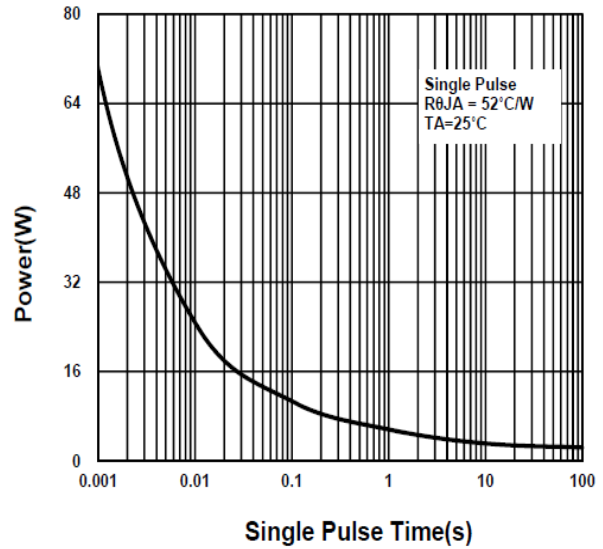
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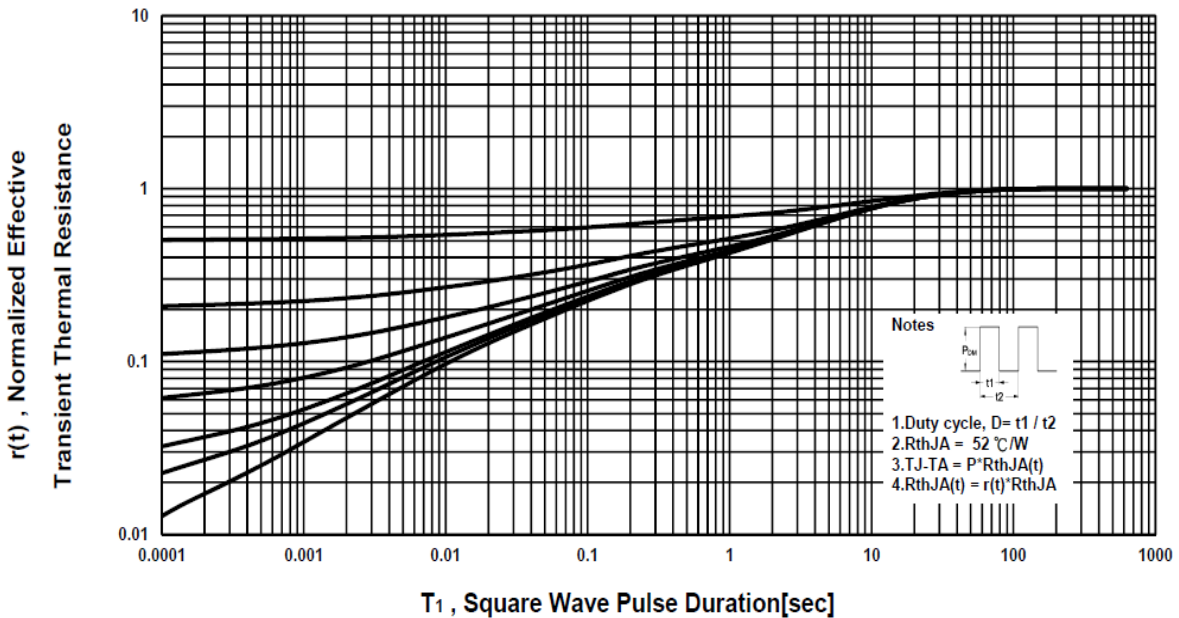
Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve



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N-Channel Enhancement Mode MOSFET

Package Dimension

PDFN 5x6P(上下 Dual) MECHANICAL DATA

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	4.8	5	5.4	K	0.82	1.06	1.3
B	5.9	6.15	6.35	L	0.4	0.5	0.6
C	0.9	1	1.18	M	2.0	2.21	2.42
D	5.42	5.59	5.85	N	0.5	1	
E	0.15	0.25	0.35	O	0.42	0.56	0.71
F	0°	6°	12°	P	0.3	0.4	0.51
G	1.17	1.27	1.37	Q	3.61	4.05	4.5
H	0.06	0.21	0.36				
J	0.41	0.55	0.7				

