



## 3A DDR Bus Termination Regulator

### Features

- $V_{CNTL}$  Supply Voltage: 3.3V to 5.5V
- Termination Supply Voltage: 1.8V to 3.6V
- Support Both DDR I (1.25V<sub>TT</sub>) and DDR II (0.9V<sub>TT</sub>) Requirements
- Requires Only 20μF Ceramic Output Capacitor
- Low Output Offset
- 3A Source and Sink Current
- Low External Component Count
- No Inductor Required
- Thermal Shutdown Protection
- Over Current Protection
- Suspend to RAM (STR) Function with High-impedance output
- SOP-8 (FD) Package

### Applications

- DDR-SDRAM Termination Voltage
- DDR I / DDR II Termination Voltage
- SSTL-18
- SSTL-2
- SSTL-3

### General Description

The G2992 is a linear regulator designed to meet the JEDEC SSTL-18, SSTL-2 and SSTL-3 (Series Stub Termination Logic) specifications for termination of DDR I / II -SDRAM. It contains a high-speed operational amplifier that provides excellent response to the load transients. This device can deliver 3A continuous current in the application such as required for DDR I / II SDRAM termination. The G2992 can easily provide the accurate V<sub>TT</sub> voltage with two external resistors generating reference voltage. The quiescent current is as low as 750μA @ V<sub>CNTL</sub> = 3.3V. So the power consumption can meet the low power consumption applications. The G2992 also has a shutdown function by setting V<sub>REF</sub> smaller than 0.2V, that provides Suspend to RAM (STR) functionality. When in the shutdown mode, the V<sub>TT</sub> output (on V<sub>OUT</sub> pin) will be tri-state providing a high impedance. A power saving advantage can be obtained in this mode through lowering the quiescent current to 50μA @ V<sub>CNTL</sub> = 3.3V.

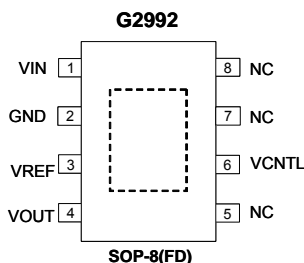
### Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Pb free)
G2992F1U	G2992	-40°C to +85°C	SOP-8 (FD)

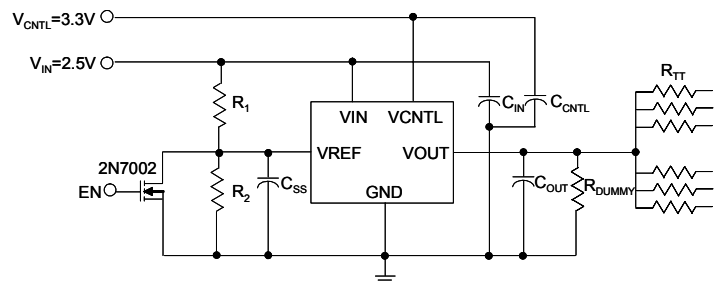
Note: U: Tape & Reel

(FD): Thermal Pad

### Pin Configuration



### Typical Application Circuit



**Absolute Maximum Ratings** <sup>(1)</sup>

Supply Voltage	
V <sub>CNTL</sub> to GND. . . . .	-0.3V to +7V
Maximum Junction Temperature, T <sub>J</sub> . . . . .	150°C
Storage Temperature Range, T <sub>STG</sub> . . . . .	-65°C to +150°C
Reflow Temperature (soldering, 10sec) . . . . .	260°C
Thermal Resistance Junction to Ambient, ( $\theta_{JA}$ )	
SOP-8 (FD). . . . .	50°C/W
Electrostatic Discharge, V <sub>ESD</sub>	
Human body mode. . . . .	2000V <sup>(2)</sup>

**Recommend Operation Range** <sup>(3)</sup>

Operating Ambient Temperature Range	
T <sub>A</sub> . . . . .	-40°C to +85°C
V <sub>CNTL</sub> to GND. . . . .	3.3V to 5.5V
V <sub>IN</sub> to GND. . . . .	1.8V to 3.6V
V <sub>REF</sub> to GND . . . . .	.0 to V <sub>CNTL</sub>

**Note:**

<sup>(1)</sup> : Absolute maximum rating indicates limits beyond which damage to the device may occurs.

<sup>(2)</sup> : Human body model : C = 100pF, R = 1500Ω, 3 positive pulses plus 3 negative pulses.

<sup>(3)</sup> : V<sub>IN</sub> and V<sub>REF</sub> mustn't be higher than V<sub>CNTL</sub>.

**Electrical Characteristics**

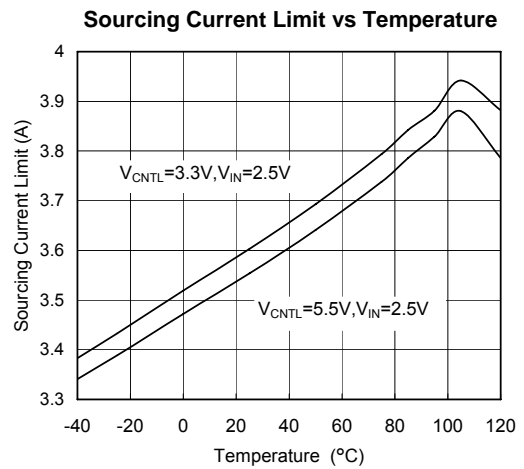
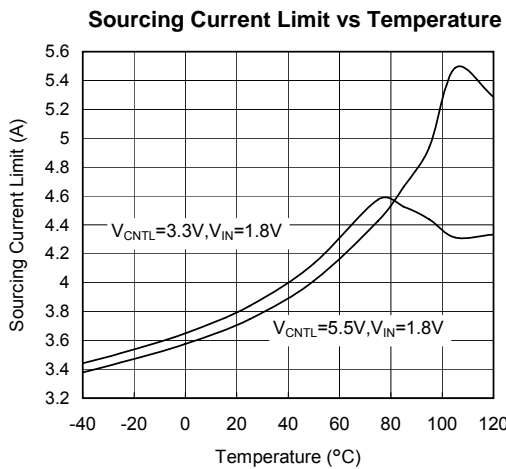
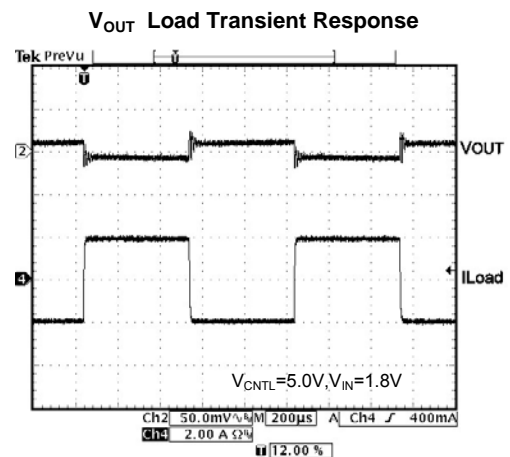
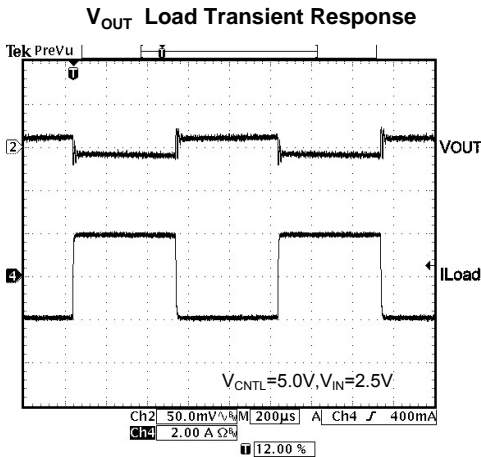
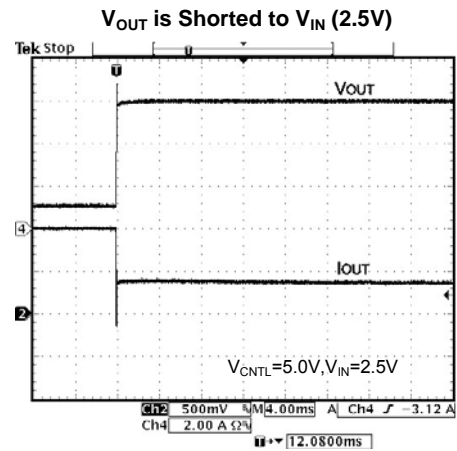
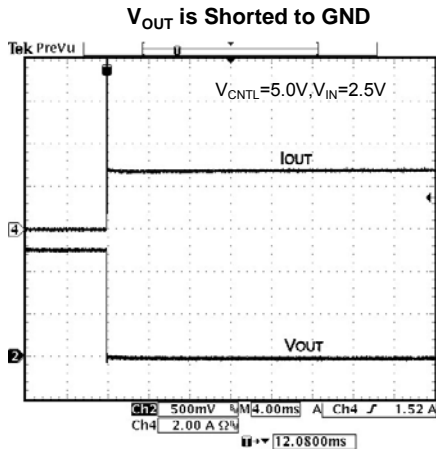
Specifications with standard typeface are for T<sub>A</sub>=25°C, V<sub>IN</sub>=2.5V, V<sub>CNTL</sub>=3.3V, V<sub>REF</sub>=1.25V, C<sub>OUT</sub>=20μF. Unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Output Offset Voltage	V <sub>OS</sub>		-20	0	20	mV
VTT output voltage	V <sub>TT</sub>	(DDR I/DDR II)	---	1.25/0.9	---	V
VTT Output Voltage Load Regulation (DDR I/DDR II)	ΔV <sub>TT</sub>	I <sub>VTT</sub> =0, V <sub>REF</sub> =1/2V <sub>IN</sub>	-20	---	20	mV
		I <sub>VTT</sub>  <1.5A, V <sub>REF</sub> =1/2V <sub>IN</sub>	-30	---	30	
		I <sub>VTT</sub>  <3A, V <sub>REF</sub> =1/2V <sub>IN</sub>	-40	---	40	
Input Voltage Range (DDR I/DDR II)	V <sub>IN</sub>		1.8	2.5/1.8	3.6	V
Control Voltage Range (DDR I/DDR II)	V <sub>CNTL</sub>		---	3.3	5.5	V
Quiescent Current	I <sub>CNTL</sub>	I <sub>OUT</sub> =0A	---	750	1500	μA
Quiescent Current in Shutdown	I <sub>SD</sub>	V <sub>REF</sub> <0.2V	---	50	90	μA
Current Limit	I <sub>LIMIT</sub>		3	---	---	A
Thermal Shutdown Temperature	T <sub>TS</sub>	3.3V ≤ V <sub>CNTL</sub> ≤ 5.5V	---	160	---	°C
Thermal Shutdown Hysteresis	T <sub>HYS</sub>		---	20	---	°C
Shutdown High Trigger Level Output	V <sub>IH</sub>	Output active	0.8	---	---	V
Shutdown Low Trigger Level Output	V <sub>IL</sub>	Output disable	---	---	0.2	V



Typical Performance Characteristics

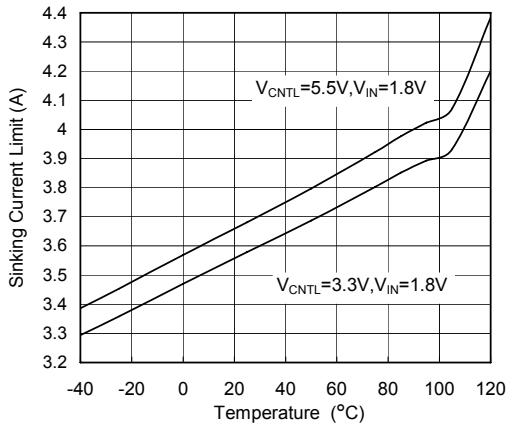
$C_{CNTL}=1\mu\text{F}/\text{MLCC}/\text{X5R}$ ,  $C_{IN}=22\mu\text{F}/\text{MLCC}/\text{X7R}$ ,  $C_{SS}=1\mu\text{F}/\text{MLCC}/\text{X5R}$ ,  $C_{OUT}=20\mu\text{F}/\text{X5R}/\text{MLCC}$  unless otherwise noted.



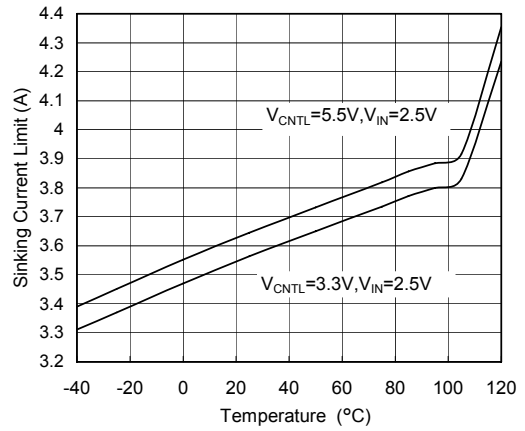


Typical Performance Characteristics (continued)

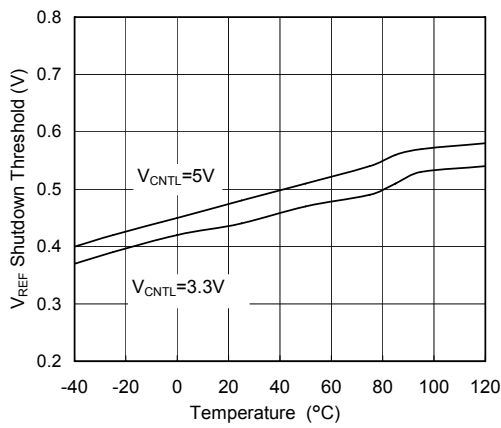
Sinking Current Limit vs Temperature



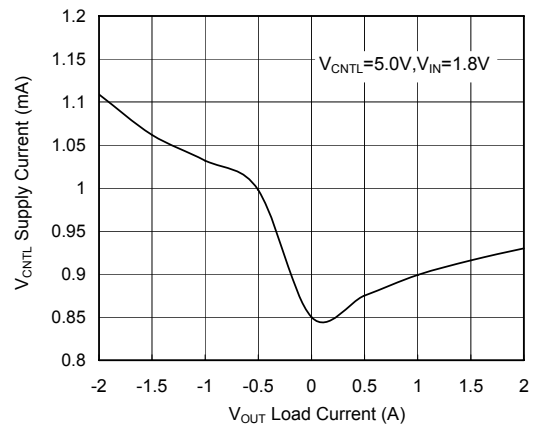
Sinking Current Limit vs Temperature



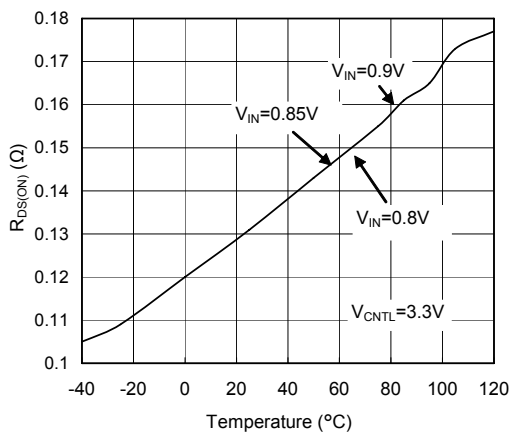
$V_{REF}$  Shutdown Threshold vs Temperature



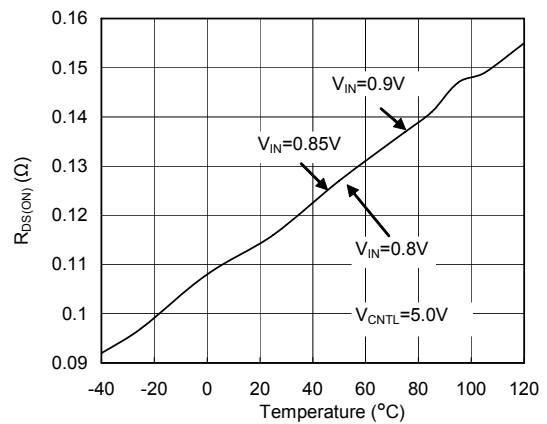
$V_{CNTL}$  Supply Current vs  $V_{out}$  Load Current



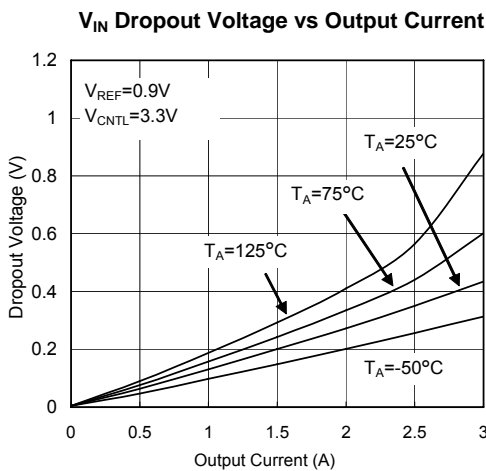
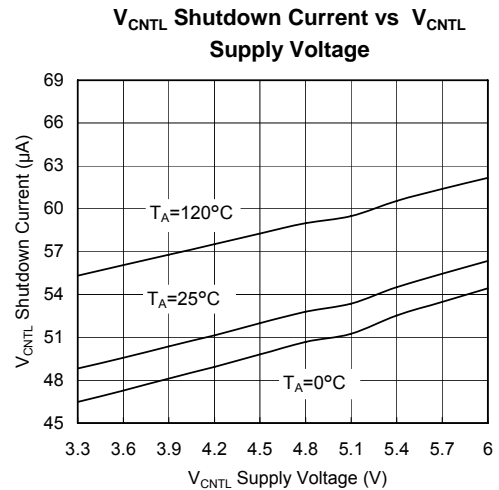
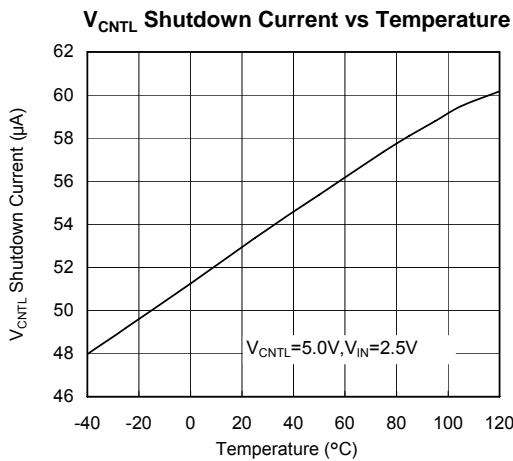
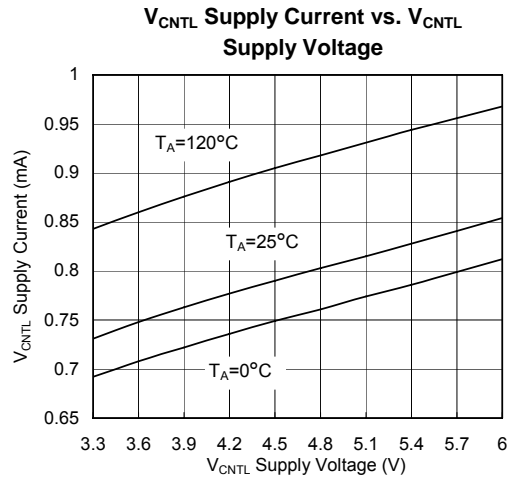
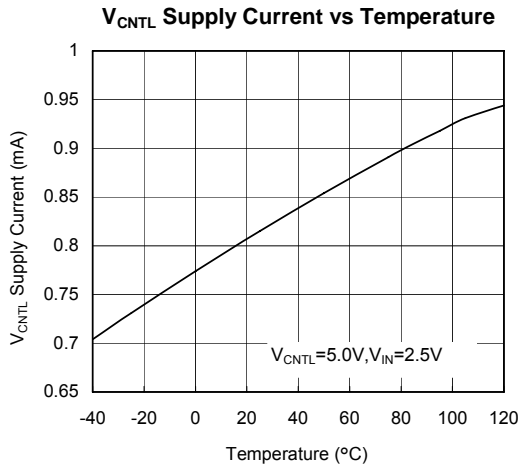
$R_{DS(ON)}$  vs Temperature



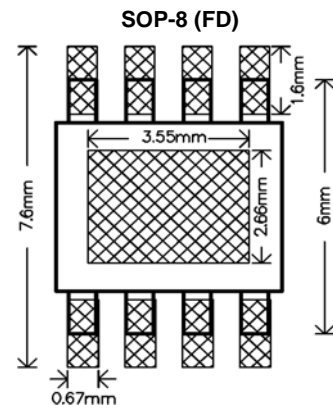
$R_{DS(ON)}$  vs Temperature



Typical Performance Characteristics (continued)



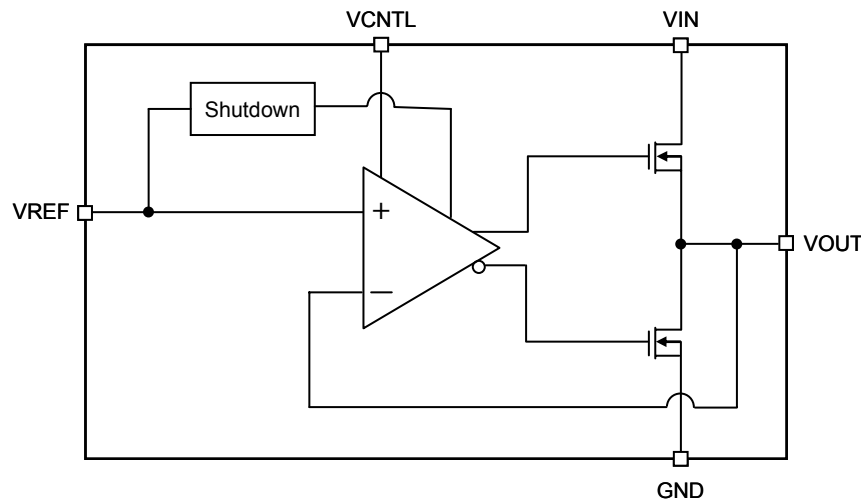
Recommended Minimum Footprint



## Pin Description

PIN	NAME	FUNCTION
1	VIN	Terminator Power pin.
2	GND	Ground
3	VREF	Terminator reference input voltage, 1.25V for DDR I, 0.9V for DDR II. Below 0.2V, the chip will be shutdown.
4	VOUT	Terminator output pin ( $V_{TT}$ voltage supplied)
5,7,8	NC	No Connection
6	VCNTL	Internal circuit power pin, at least 3.3V

## Block Diagram



## Application Information

### Output Capacitor

For stable operation, total capacitance of the  $V_{TT}$  output terminal can be equal or greater than  $20\mu\text{F}$ . The output capacitor should be located near  $V_{TT}$  output terminal as close as possible to minimize the effect of ESR and ESL.

### Power on sequence

For safely operation, The G2992 must keep  $V_{CNTL}$  voltage larger than  $V_{IN}$ , this condition is due to the internal parasitic diodes between  $V_{IN}$  to  $V_{CNTL}$ . The G2992 will consume large current when  $V_{IN}$  voltage is larger than  $V_{CNTL}$ .

### Consideration of the $V_{REF}$ Voltage

The  $V_{REF}$  voltage is applied by a buffered mid-rail

voltage which is generated by a resistor divider between  $V_{IN}$  and GND. Using a capacitor tapped to the voltage divider can form a low-pass filter. It can increase both the soft-start interval and the noise immunity.

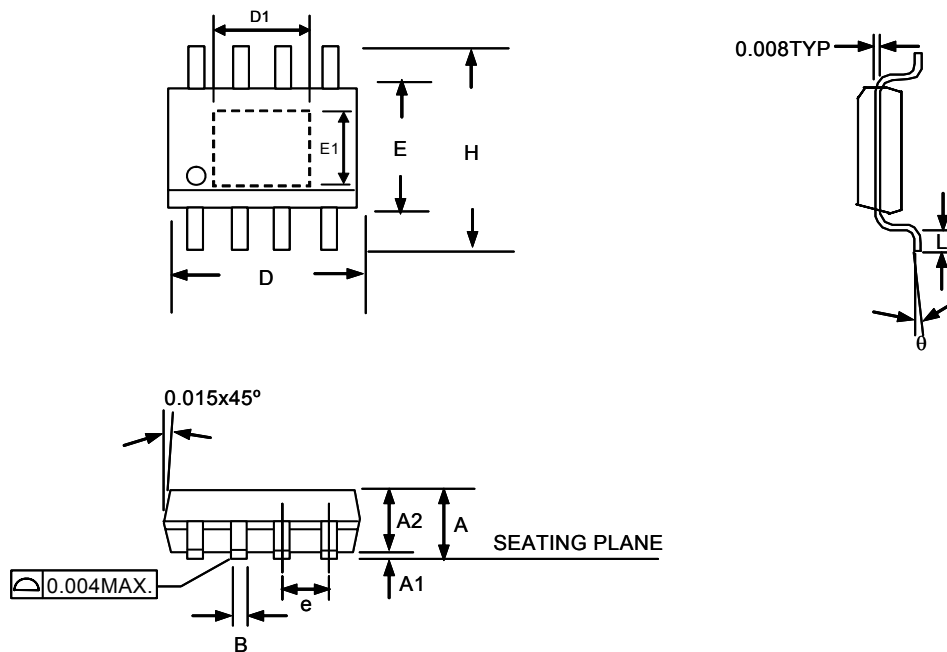
### Input Capacitor

Adding a capacitance close to  $V_{IN}$  pin can improve the  $V_{TT}$  performance when fast load-transient. In general,  $1/2 C_{OUT}$  is recommended for the  $V_{IN}$  capacitance. Separating the  $V_{IN}$  and  $V_{CNTL}$  pins will get better transient performance.

A ceramic capacitance with a value between  $1.0\mu\text{F}$  and  $4.7\mu\text{F}$  close to the  $V_{CNTL}$  pin is recommended to stabilize the  $V_{CNTL}$  voltage.



Package Information



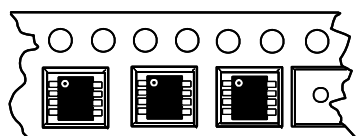
SOP- 8 (F1) Package

Note:

1. JEDEC Outline: MS-012 AA/E.P. Version: N/A
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions and gate burrs shall not exceed .15mm (.006in) per side.
3. Dimensions "E" does not include inter-lead flash, or protrusions inter-lead flash and protrusions shall not exceed .25mm (.010in) per side.

SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN.	MAX.	MIN.	MAX.
A	1.35	1.75	0.053	0.069
A1	0.00	0.13	0.000	0.005
A2	----	1.50	----	0.059
B	0.41TYP		0.016TYP	
D	4.80	4.98	0.189	0.196
E	3.81	3.99	0.150	0.157
e	1.27TYP		0.05TYP	
H	5.80	6.20	0.228	0.244
L	0.41	1.27	0.016	0.050
$\theta$	0°	8°	0°	8°
D1	----	2.29	----	0.090
E1	----	2.29	----	0.090

Taping Specification



Feed Direction  
Typical SOP Package Orientation

PACKAGE	Q'TY/REEL
SOP-8 (FD)	2,500 ea

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