FEATURES

- Dual MOSFET drivers in single 16 pin QFN package
- Buck Converter Driver Vin 4.0 to 13.2Vdc
- Multimode operation to configure the driver as either dual or doubler/interleaved mode drivers
- Variable Gate drive from 4V to 13V to optimize system efficiency
- 5V VCC and VDRV capability for sleep states where only 5V is available
- Large drivers designed to drive 3nF in ≤ 12ns with any voltage from 5V to 12V (typ) supplied to the VDRV pin
  - Low side driver – 0.85Ω source/0.38Ω sink
  - High side driver – 1.1Ω source/0.60Ω sink
  - Propagation delays ≤ 20ns
- Integrated bootstrap diode on both drivers
- Capable of high output switching frequencies from 150kHz up to greater than 1MHz
- Compatible with IR's patented Active Tri-Level (ATL) PWM for fastest response to transient overshoot as well as industry standard 3.3V and 5V Tri-State signals in most modes
- Non-overlap and under voltage protection
- Thermally enhanced 16 pin QFN package
- Lead free RoHS compliant package
- Low Quiescent power to optimize efficiency

DESCRIPTION

The IR3598 is a high-efficiency dual driver capable of switching a pair of high and low side N-channel MOSFETs in synchronous buck converters and is optimized for use with IR's Digital PWM controllers to provide a total voltage regulator solution for today's advanced computing applications. In a space saving 16-pin QFN package, the IR3598 can significantly improve density in high phase count voltage regulators saving over 50% board space versus conventional drivers.

The IR3598 can be configured as two independent drivers in DUAL mode with individual PWM signals, or as an interleaved DOUBLER driver where one PWM signal is internally split to drive the two pairs of MOSFETs 180° out of phase. The inter-leaving action is optimized internally to manage the tri-state action of multiple phases during transients, low current single phase operation, and PS2 operation (see Figs. 8 and 9.) The DOUBLER mode can double the effective maximum phase count from the controller, enabling a well-controlled, high phase count voltage regulator.

The IR3598 has a proprietary circuit which maintains the MOSFET drive strength throughout the 4.0V to 13.2V drive voltage range thus insuring fast switching even with 5V standby drive operation during system sleep modes. The integrated boot diodes reduce external component count. The IR3598 also features an adaptive non-overlap control for shoot-through protection.

The IR3598 PWM inputs are compatible with IR's fast Active Tri-Level (ATL) PWM signals as well as 3.3V and 5V Tri-State PWM signals.

APPLICATIONS

- Desktop CPU and GPU solutions
- Performance overclocking CPU and GPU VR solutions
- Optimized for Sleep state S3 systems using +5VSB

BASIC APPLICATION

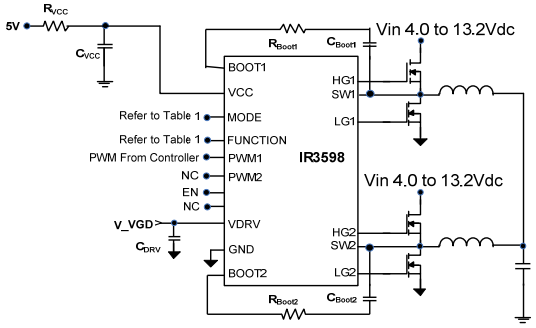


Figure 1: IR3598 Typical DOUBLER Mode Application Circuit

PIN DIAGRAM

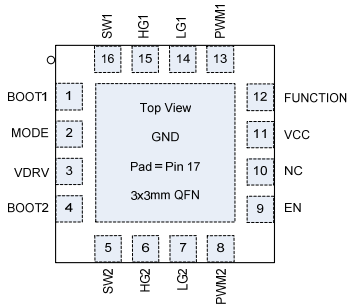
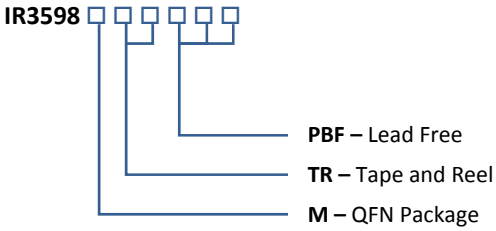


Figure 2: IR3598 Package Top View

ORDERING INFORMATION



Package	Tape & Reel Qty	Part Number
QFN	3000	**IR3598MTRPBF**
QFN	100	**IR3598MPBF**

FUNCTIONAL BLOCK DIAGRAM

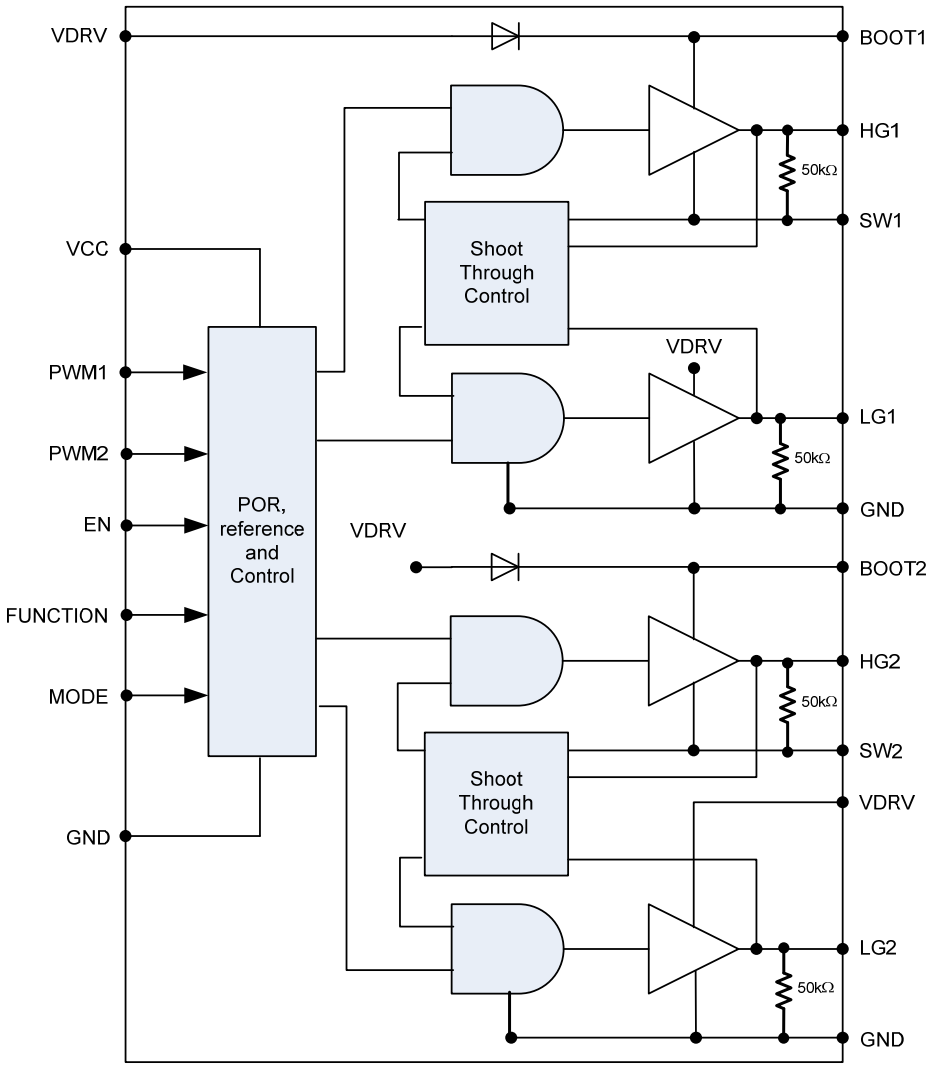


Figure 3: IR3598 Simplified Functional Block Diagram

TABLE 1: MODE CONFIGURATION TABLE

Function	Mode	PWM Mode	Phase Mode
0	1	IR ATL	Dual
1	1	IR ATL	Doubler
0	0	Tri-State	Dual
1	0	Tri-State	Doubler

TYPICAL APPLICATIONS

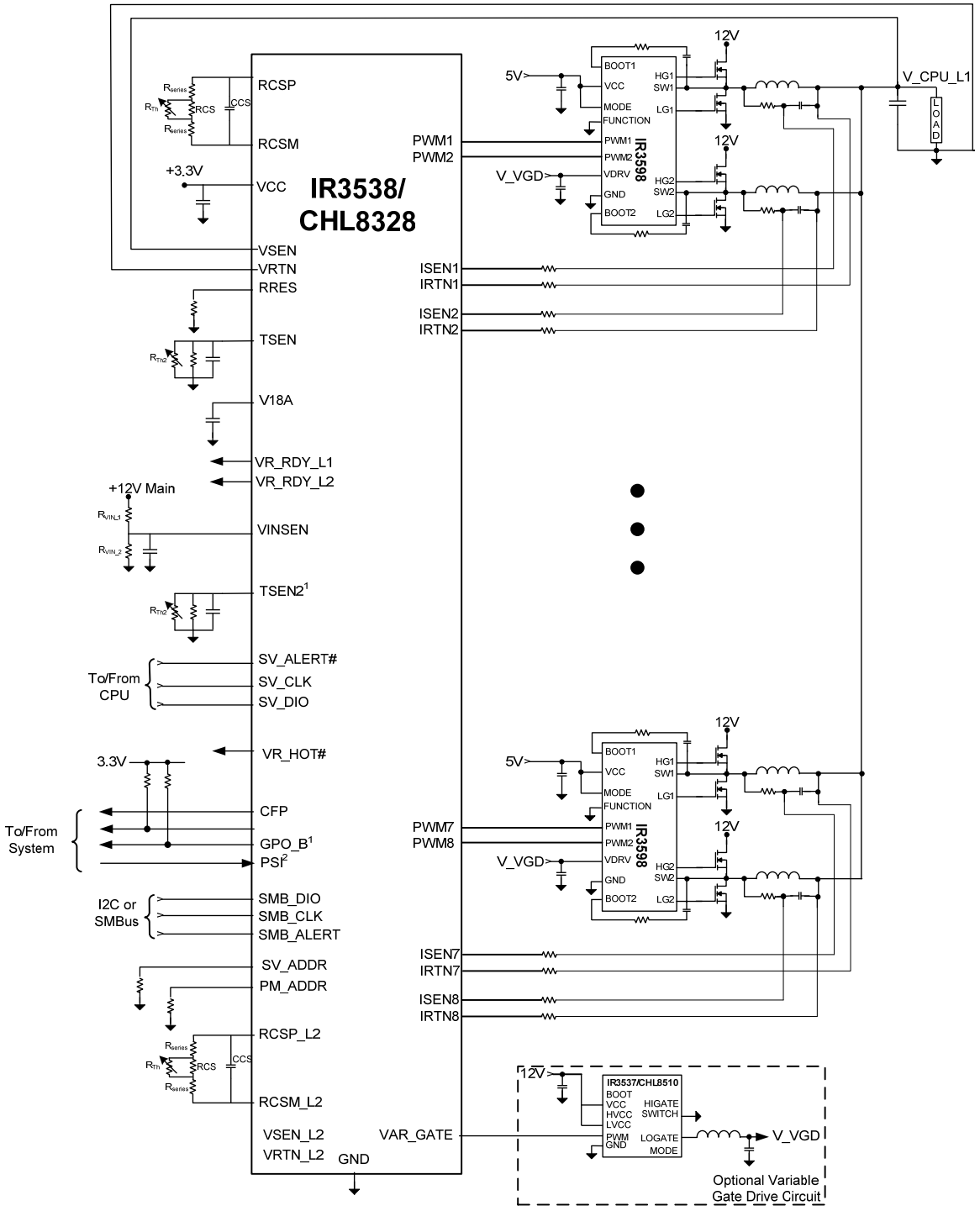


Figure 4: 8-Phase CPU VR solution using IR3598 MOSFET drivers in DUAL mode & IR3538/CHL8328 Controller with the IR3537/CHL8510 as a VGD Driver

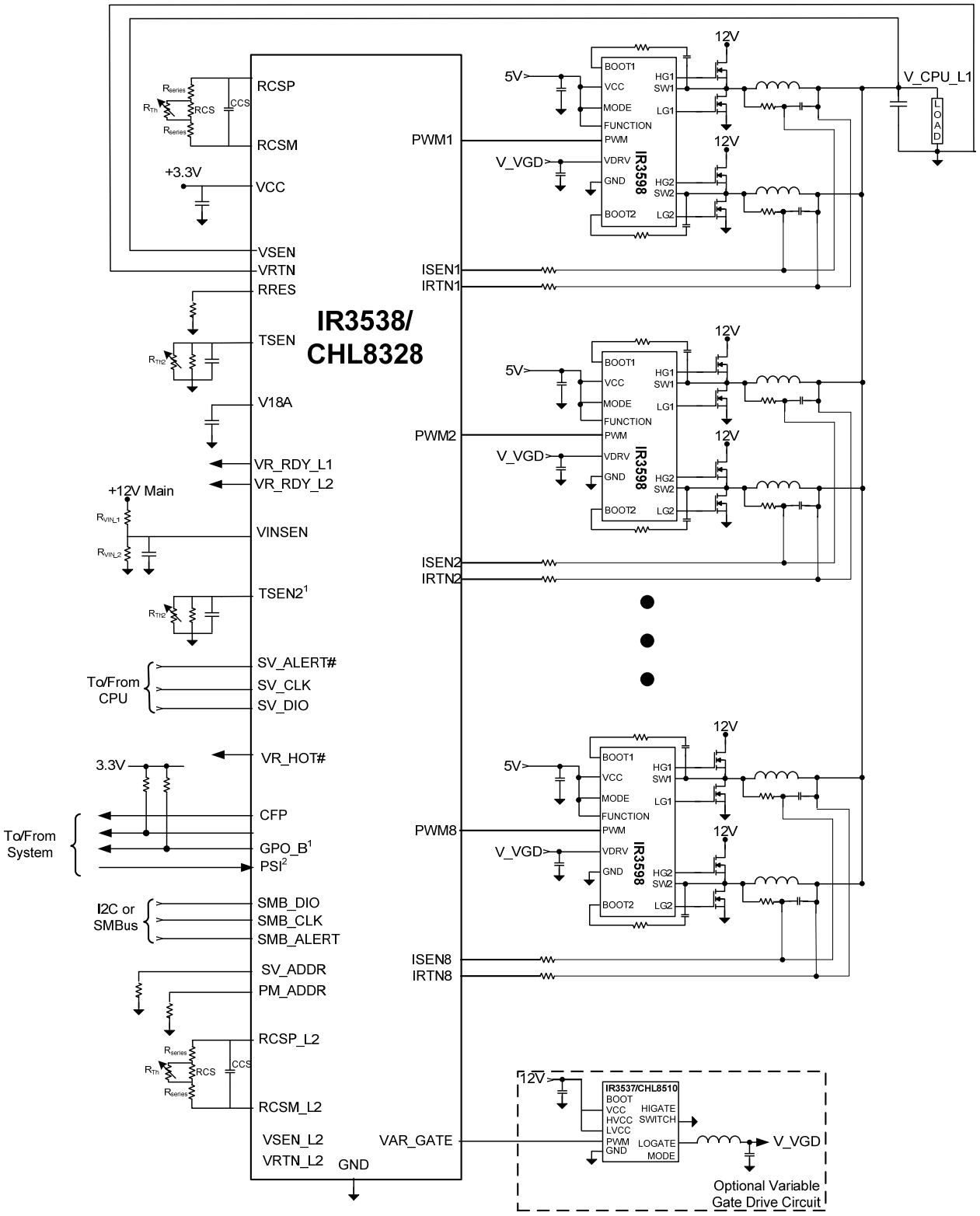


Figure 5: 16-Phase VR solution using IR3598 MOSFET drivers in DOUBLER mode & IR3538/CHL8328 Controller with the IR3537/CHL8510 as a VGD

PIN DESCRIPTIONS

PIN #	PIN NAME	PIN DESCRIPTION
1	BOOT1	Floating bootstrap supply pin for the upper gate drive HG1. Connect the bootstrap capacitor between this pin and the SW1 pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET. See the Internal Bootstrap Device section under DESCRIPTION for guidance in choosing the capacitor value.
2	MODE	The MODE pin is an input signal used to set the PWM MODE (Tri-State or IR ATL) of the drivers. The MODE pin levels are controlled by connecting the MODE pin to Ground or connecting to VCC. Refer to the configuration instructions in Table 1 to program the mode pin. Do not let this pin float. The mode pin must be directly connected to ground when this is the connection. Do not connect through a resistor when connecting to ground. The mode pin is low when the pin voltage is below 0.8Vdc and high when the pin voltage is above 2Vdc.
3	VDRV	Connect this pin to a separate supply voltage between 4.0V and 13.2V to vary the drive voltage on both the high side and low side MOSFET's. Place a high quality low ESR ceramic capacitor from this pin to GND. Note that on the high side MOSFET's, the gate drive voltage will be VDRV less the boot strap diode voltage drop.
4	BOOT2	Floating bootstrap supply pin for the upper gate drive HG2. Connect the bootstrap capacitor between this pin and the SW2 pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET. See the Internal Bootstrap Device section under DESCRIPTION for guidance in choosing the capacitor value.
5	SW2	Connect this pin to the SOURCE of the upper MOSFET and the DRAIN of the lower MOSFET of the second power stage, driven by HG2 and LG2. This pin provides a return path for the upper gate drive.
6	HG2	Upper gate drive output of Driver 2. Connect to gate of high-side power N-Channel MOSFET of the second power stage.
7	LG2	Lower gate drive output of Driver 2. Connect to gate of the low-side power N-Channel MOSFET of the second power stage.
8	PWM2	The PWM2 signal is the control input for the second driver from either an IR ATL compatible source or an industry standard Tri-State source. Connect this pin to the PWM output of the controller. As a DUAL driver, PWM2 controls the behavior of Gate Driver 2 (HG2, LG2). In DOUBLER mode this pin is not used and must be left open.
9	EN	The chip will be enabled with the EN pin left open, or pulled high to VCC. The enable is low when the pin voltage is below 0.8Vdc and high when the pin voltage is above 2Vdc.
10	NC	This pin must be left open.
11	VCC	Connect this pin to a +5V bias supply. Place a high quality low ESR 0.1uF ceramic capacitor from this pin to the IR3598 GND.
12	FUNCTION	The FUNCTION pin controls the Phase Mode (Dual or Doubler Modes). The FUNCTION pin levels are controlled by connecting the FUNCTION pin to Ground or VCC. Refer to the configuration instructions in Table 1 to program the FUNCTION pin. At power up, the function pin selection is latched into the IR3598, and therefore cannot be changed after initial power up. The function pin is low when the pin voltage is below 1 Vdc and high when the pin voltage is above 4.2Vdc.
13	PWM1	The PWM1 signal is the control input for the first driver from either an IR ATL compatible source or an industry standard Tri-State source. Connect this pin to the PWM output of the controller. As a DUAL driver, PWM1 controls the behavior of Gate Driver 1 (HG1, LG1). In DOUBLER mode PWM1 controls the behavior of Gate Drive 1 (HG1, LG1) and Gate Drive 2 (HG2, LG2).
14	LG1	Lower gate drive output of Driver 1. Connect to gate of the low-side power N-Channel MOSFET of the first power stage.
15	HG1	Upper gate drive output of Driver 1. Connect to gate of high-side power N-Channel MOSFET of the first power stage.
16	SW1	Connect this pin to the SOURCE of the upper MOSFET and the DRAIN of the lower MOSFET of the first power stage. This pin provides a return path for the upper gate drive.
(PAD) 17	GND	Bias and reference ground. All signals are referenced to this node. It is also the power ground return of the driver.

ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

Voltage Regulator Vin	4.0 to 13.2Vdc
VCC	-0.3V to +7.0V
VDRV	-0.3V to +15.0V
PWM1, PWM2, EN, MODE, FUNCTION	-0.3V to VCC +0.3V
BOOTx-GND, BOOTx – SWx	-0.3V to +35V, -0.3V to +15.0V
LG1, LG2	DC -0.3V to VDRV + 0.3V, <200ns: -5V to VDRV + 0.3V
HG1, HG2	SWx – 0.3V to VBOOT + 0.3V, <20ns: SWx – 5V to VBOOT + 0.3V
SW1, SW2	-0.3V to +35V, <200nS, -8V
ESD	750V HBM
Thermal Information	
Thermal Resistance (ΘJC)	3°C/W
Thermal Resistance (ΘJA)[1]	45°C/W
Maximum Junction Temperature	150°C
Maximum Storage Temperature Range	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s)	300°C

Note 1: θJA is measured with the component mounted on a high effective thermal conductivity test board in free air.

ELECTRICAL SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS FOR RELIABLE OPERATION WITH MARGIN

Recommended Voltage Regulator Vin Range	4.5 to 13.2Vdc
Recommended Operating Ambient Temperature Range	0°C to 85°C
Maximum Operating Junction Temperature	125°C
VCC Supply Voltage Range	+5V ± 10%
VDRV	4.0V to 13.2V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, these specifications were tested at +25°C. VCC = VDRV = 5.0V.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply						
Supply Bias Current Shutdown – Dual Mode	$I_{VCC} + I_{VDRV}$	ENABLE LOW	1.8	2.1	2.7	mA
Supply Bias Current Idle – Dual Mode	$I_{VCC} + I_{VDRV}$	Tri-stated Gate Driver	2.6	3.3	4.0	mA
Supply Bias Current Idle – Doubler Mode	$I_{VCC} + I_{VDRV}$	Tri-stated Gate Driver	2.1	2.9	3.6	mA
Supply Bias Current —Note 1	$I_{VCC} + I_{VDRV}$	f_{PWM} = 300kHz, no load	-	4.5	-	mA
VCC Rising Threshold for POR			3.55	3.80	3.98	V
VCC Falling Threshold for POR			3.20	3.50	3.80	V
Vdrive Rising Threshold for POR			3.55	3.80	3.98	V
Vdrive Falling Threshold for POR			2.50	2.75	3.00	V
PWM Input IR ATL Mode						
PWM Input Pull-Up Voltage	VPWM_pull up	PWM Input Floating	-	4.0	-	V
PWM Input High Threshold	$V_{IH(C\_PWM)}$		0.9	1.15	1.3	V
PWM Input Low Threshold	$V_{IL(C\_PWM)}$		0.7	0.95	1.1	V
PWM Tri-level High Threshold	$V_{TL(C\_PWM)}$		2.4	2.65	2.9	V
PWM Tri-level Low Threshold	$V_{TH(C\_PWM)}$		2.2	2.5	2.7	V
PWM Input Current Low	I_{C_PWM}	V_{PWM} = 0V	0.7	1.0	1.4	mA
PWM Input Current High		V_{PWM} = 1.8V	0.7	1.0	1.4	mA
PWM Input Current Tri-state		V_{PWM} = 3.3V	60	125	190	uA
PWM Input Tri-State Mode (+3.3V or +5V signal level)						
PWM Input Rising Threshold, Note 1	$V_{IH(C\_PWM)}$		-	1.65	-	V
PWM Input Falling Threshold, Note 1	$V_{IL(C\_PWM)}$		-	1.3	-	V
Tri-State LO_GATE Threshold			0.7	0.95	1.1	V
Tri-State LO_GATE Hysteresis			100	200	300	mV
Tri-State HI_GATE Threshold			2.4	2.65	2.9	V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Tri-State HI_GATE Hysteresis			100	200	300	mV
Tri-State Hold Off Time, Note 1			-	80	-	ns
PWM Input Pull-Up Voltage	VPWM_pull up	PWM Input Floating	1.3	1.55	1.9	V
PWM Input Resistance, Note 1	RPWM	PWM Input Floating	-	3.75	-	kΩ
Minimum Recognized PWM Pulse Width, Note 1		ATL (IR) and Tri-State Modes	-	40	-	nSec
High Side Gate Drivers						
Transition Time — Rise, Note1	$t_{R(HS)}$	3nF Load, VDRV = 5-12V	-	15	-	ns
Transition Time — Fall, Note1	$t_{F(HS)}$	3nF Load, VDRV = 12V	-	12	-	ns
Transition Time — Fall, Note1	$t_{F(HS)}$	3nF Load, VDRV = 5V	-	17	-	ns
Propagation Delay — Turn-on all modes, Note 1	$t_{PDH(HS)}$	3nF Load, VDRV = 5-12V	-	23	-	ns
Propagation Delay — Turn-off Dual, Note 1	$t_{PDL(HS)}$	3nF Load, VDRV = 5-12V	-	17	-	ns
Propagation Delay — Turn-off Doubler, Note 1	$t_{PDL(HS)}$	3nF Load, VDRV = 5-12V	-	24	-	ns
Propagation Delay — Exit Tri-State Dual, Note 1	$t_{PDTS(HS\_en)}$	3nF Load	-	40	-	ns
Propagation Delay — Exit Tri-State Doubler, Note 1	$t_{PDTS(HS\_en)}$	3nF Load	-	40	-	ns
Propagation Delay — Enter Tri-State Dual, Note 1	$t_{PDTS(HS\_dis)}$	3nF Load	-	19	-	ns
Propagation Delay — Enter Tri-State Doubler, Note 1	$t_{PDTS(HS\_dis)}$	3nF Load	-	19	-	ns
Output Impedance Source, Note 1	R_{HS_SOURCE}	VDRV = 12V, 100mA	-	1.1	-	Ω
Output Impedance Source, Note 1	R_{HS_SOURCE}	VDRV = 5V, 100mA	-	1.4	-	Ω
Output Impedance — Sinking, Note 1	R_{HS_SINK}	VDRV = 12V, 100mA	-	0.60	-	Ω
Output Impedance — Sinking	R_{HS_SINK}	VDRV = 5V, 100mA	0.70	0.90	1.20	Ω
Low Side Gate Drivers						
Transition Time — Rise, Note 1	$t_{R(LS)}$	3nF Load, VDRV = 5-12V	-	14	-	ns
Transition Time — Fall, Note 1	$t_{F(LS)}$	3nF Load, VDRV = 12V	-	7	-	ns
Transition Time — Fall, Note 1	$t_{F(LS)}$	3nF Load, VDRV = 5V	-	8.5	-	ns
Propagation Delay — Turn-on all modes, Note 1	$t_{PDH(LS)}$	3nF Load, VDRV = 5-12V	-	20	-	ns
Propagation Delay — Turn-off Dual, Note 1	$t_{PDL(LS)}$	3nF Load, VDRV = 5-12V	-	18	-	ns
Propagation Delay — Turn-off Doubler, Note 1	$t_{PDL(LS)}$	3nF Load, VDRV = 5-12V	-	24	-	ns
Propagation Delay — Exit Tri-State Dual, Note 1	$t_{PDTS(LS\_en)}$	3nF Load	-	24	-	ns
Propagation Delay — Exit Tri-State	$t_{PDTS(LS\_en)}$	3nF Load	-	30	-	ns

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Doubler, Note 1						
Propagation Delay — Enter Tri-State Dual, Note 1	$t_{PDTS(LS\_dis)}$	3nF Load	-	15	-	ns
Propagation Delay — Enter Tri-State, Doubler, Note 1	$t_{PDTS(LS\_dis)}$	3nF Load	-	23	-	ns
Output Impedance Source, Note 1	R_{LS_SOURCE}	VDRV = 12V, 100mA	-	0.85	-	Ω
Output Impedance Source, Note 1	R_{LS_SOURCE}	VDRV = 5V, 100mA	-	1.0	-	Ω
Output Impedance — Sinking, Note 1	R_{LS_SINK}	VDRV = 12V, 100mA	-	0.38	-	Ω
Output Impedance — Sinking	R_{LS_SINK}	VDRV = 5V, 100mA	0.45	0.55	0.75	Ω

Note 1: Guaranteed by design but not tested in production.

MODE AND TIMING DIAGRAMS

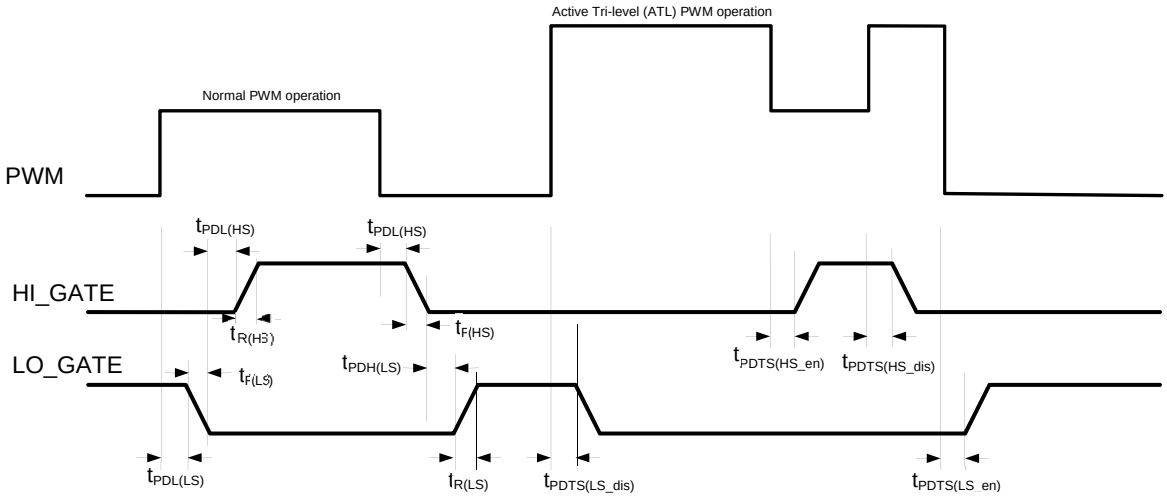


Figure 6: IR Active Tri-Level (ATL) mode PWM, HI_GATE and LO_GATE signals

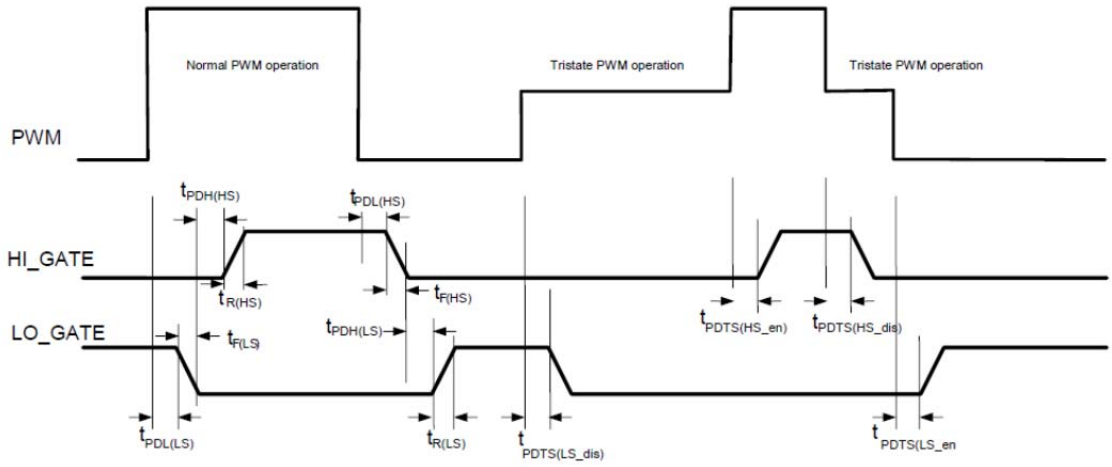


Figure 7: Tri-State mode PWM, HI_GATE and LO_GATE signals

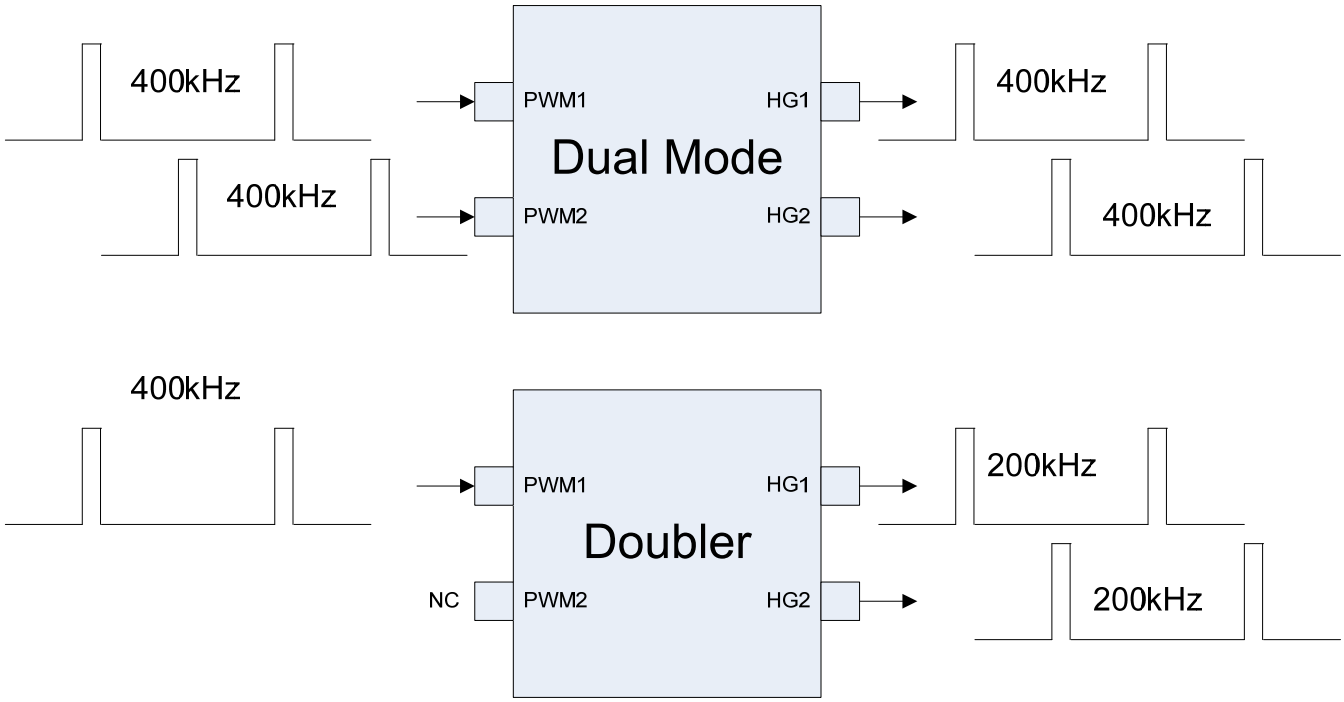


Figure 8: IR3598 Phase Modes

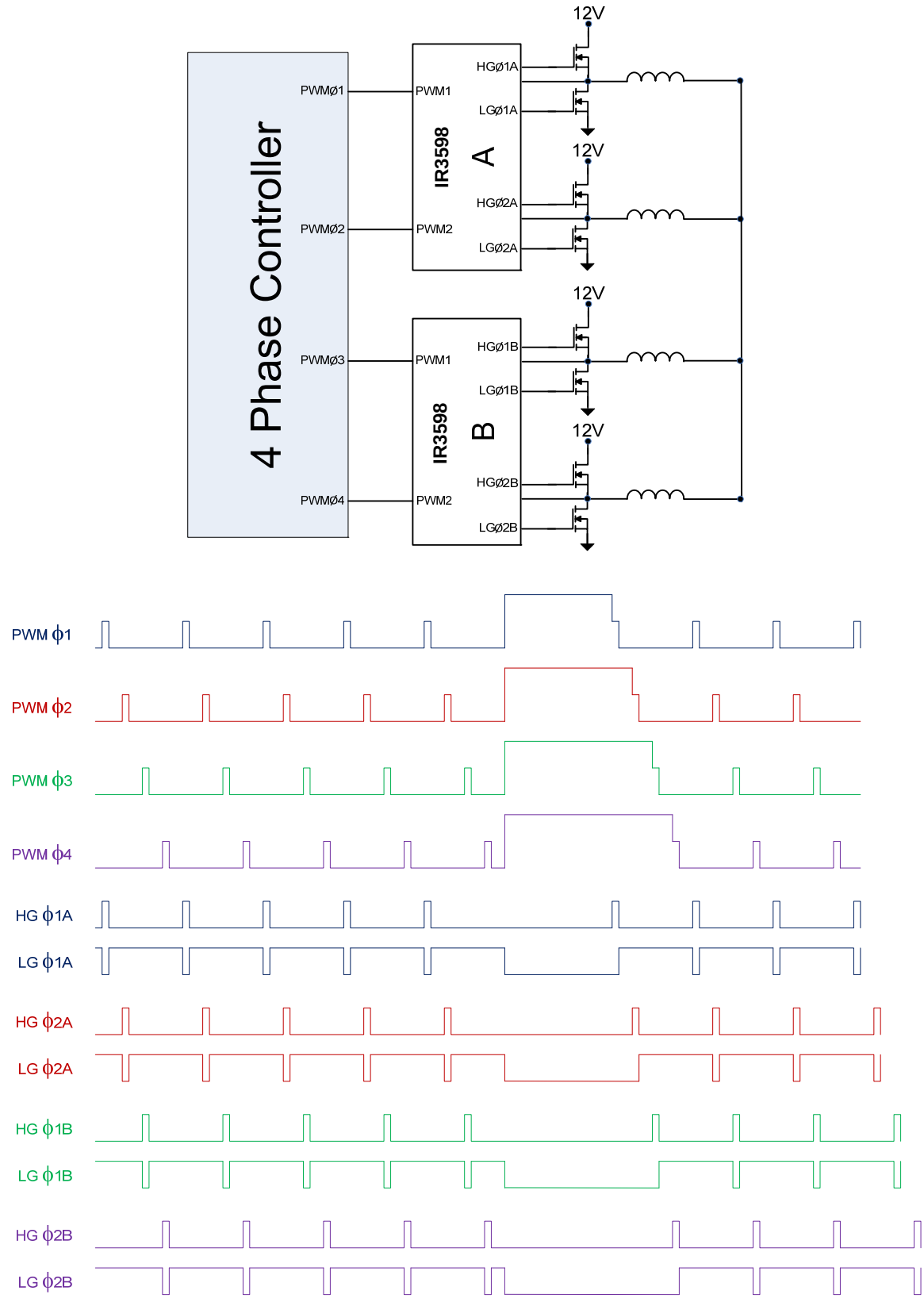


Figure 9: IR3598 timing when configured in DUAL mode (IR ATL PWM signals at input)

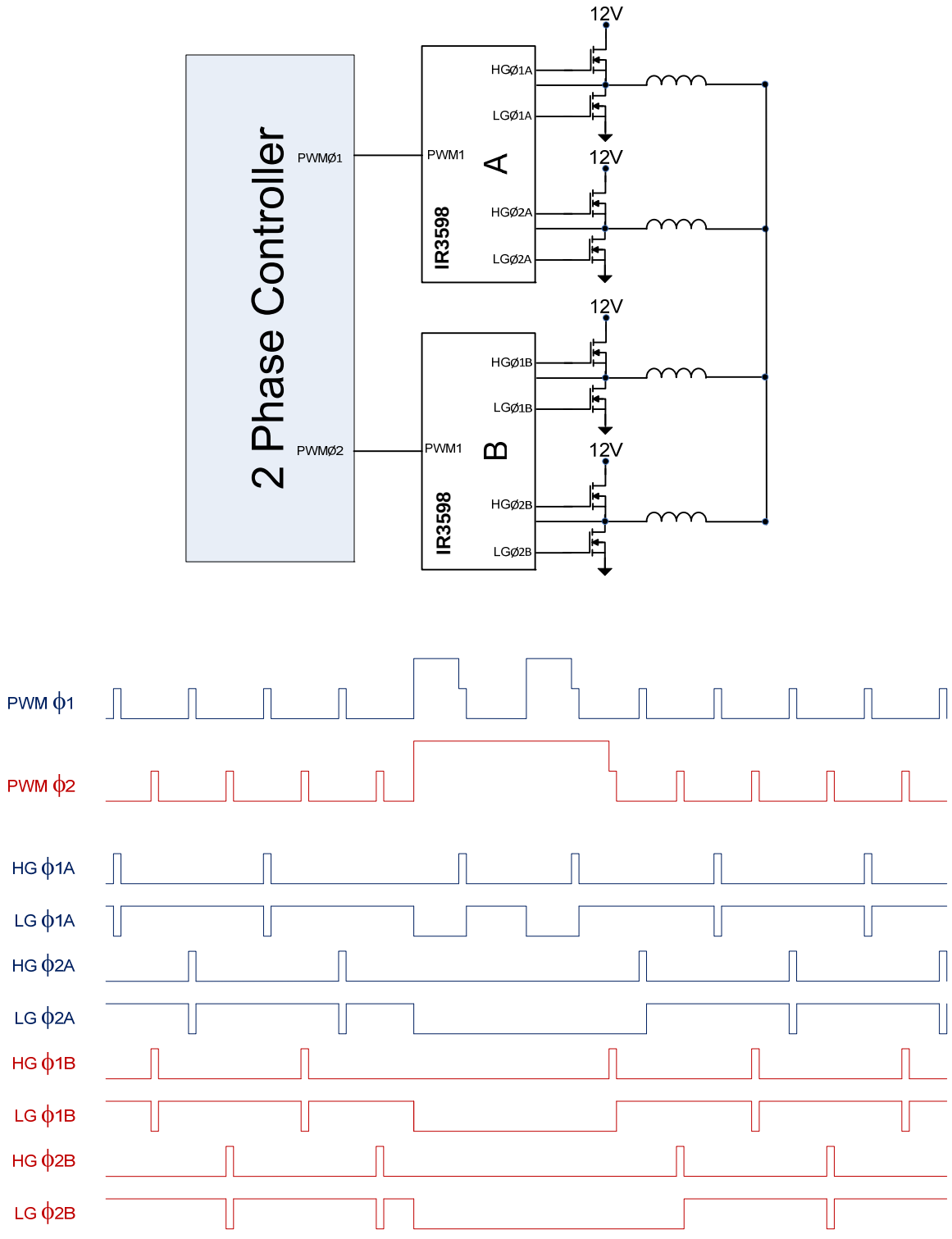


Figure 10: IR3598 timing when configured in DOUBLER mode (IR ATL PWM signals at input)

GENERAL DESCRIPTION

The IR3598 contains two high-efficiency, fast High and Low side MOSFET drivers with large source and sink current capability. It can reliably drive the external high- and low-side N-channel MOSFETs with large input capacitance at switching frequencies up to 1MHz.
The patented IR Active Tri-Level (ATL) feature allows complete control over enable and disable of both MOSFETs using the PWM input signal from the controller. The timing and voltage levels of ATL are shown in Figure 6.

Each IR3598 can be operated to drive two independent pairs of MOSFETs in one of two operating modes which are dual mode and doubler mode. In dual mode, two independent PWM inputs control two separate and independent gate drive outputs. Each driver functions in a similar way to a single high-low MOSFET driver such as the CHL8515. In doubler mode, the two independent drivers are controlled by a single input signal at PWM1.
In normal switching modes, they operate 180° out of phase with each other. The phase modes for dual and doubler are shown in Figure 8. Detailed timing diagrams can be seen in Figures 9 and 10.

During normal operation the PWM transitions between low and high voltage levels to drive the low- and high-side MOSFETs. The PWM signal falling edge transition to a low voltage threshold initiates the high side driver turn off after a short propagation delay, $t_{PDL(HS)}$. The dead time control circuit monitors the High Gate signals and switch voltages to ensure the high side MOSFET is turned off before the Low Gate voltages are allowed to rise to turn on the low-side MOSFET.

The PWM rising edge transition through the high-side turn on threshold, initiates the turn off of the low-side MOSFET after a small propagation delay, $t_{PDL(LS)}$. The adaptive dead time circuit provides the appropriate dead time by determining if the falling Low Gate voltage threshold has been crossed before allowing the High Gate voltage to rise and turn on the high-side MOSFET, $t_{PDH(HS)}$.

THEORY OF OPERATION

POWER-ON RESET (POR)

The IR3598 incorporates a power-on reset feature. This ensures that both the high and low side output drivers are made active only after the device supply voltage Vcc and Vdrive both have exceeded a certain minimum operating threshold. The V_{cc} and Vdrive supplies are monitored and both the drivers are set to the low state, holding both external MOSFETs off. Once both V_{cc} and VDRV cross the rising POR threshold, the IR3598 (if in IR ATL mode) is reset and the outputs are held in the low state until a transition from tri-state to active operation is detected at the PWM input. For Tri-state mode, the POR operation is the same except the driver does not look for an input tri-state before functioning. During normal operation the drivers continue to remain active until the V_{cc} falls below the falling POR threshold.

INTEGRATED BOOTSTRAP DIODE

The IR3598 features an integrated bootstrap diode to reduce external component count. This enables the IR3598 to be used effectively in cost and space sensitive designs.

The bootstrap circuit is used to establish the gate voltage for the high-side driver. It consists of a diode and capacitor connected between the SW and BOOT pins of each device. Integrating the diodes within the IR3598, results in the need for an external boot capacitor only. The bootstrap capacitor is charged through the diode and injects this charge into the high-side MOSFET input capacitance when PWM signal goes high.

IR ACTIVE TRI-LEVEL (ATL) PWM INPUT SIGNAL

The IR3598 gate drivers are driven by a patented active tri-level PWM control signal provided by the IR digital PWM controllers. During normal operation, the rising and falling edges of the PWM signal transitions between 0V and 1.8V to switch the LO_GATE and HI_GATE. To force both driver outputs low simultaneously, the PWM signal crosses a tri-state voltage level higher than the tri-state HI_GATE threshold. This threshold based tri-state results in a very fast disable for both the drivers, with only a small tri-state propagation delay. MOSFET switching resumes when the PWM signal falls below the tri-state threshold into the normal operating voltage range.

This fast tri-state operation eliminates the need for any tri-state hold-off time of the PWM signal to dwell in the shutdown window. Dedicated disable or enable pins are not required which simplifies the routing and layout in applications with a limited number of board layers. It also provides switching free of shoot through for slow PWM transition times of up to 20ns. The IR3598 is therefore tolerant of stray capacitance on the PWM signal lines.

The IR3598 provides a 1.0mA typical pull-up current to drive the PWM input to the tri-state condition of 3.3V when the PWM controller output is in its high impedance state. The 1.0mA typical current is designed for driving worst case stray capacitances and transition the IR3598 into the tri-state condition rapidly to avoid a prolonged period of conduction of the high or low side MOSFETs during faults. Immediately after the driver is driven into the tri-state mode, the 1mA current is disables such that power is conserved.

START UP

During initial startup, the IR3598 holds both high- and low-side drivers low even after POR threshold is reached if the device is in IR ATL mode. This mode is maintained while the PWM signal is pulled to the tri-state threshold level greater than the tri-state HI_GATE threshold and until it transitions out of tri-state. It is this initial transition out of the tri-state which enables both drivers to switch based on the normal PWM voltage levels.

This startup also ensures that any undetermined PWM signal levels from a controller in pre-POR state will not result in high or low-side MOSFET turn on until the controller is out of its POR.

For Tri-state mode, the POR operation is the same except the driver does not look for an input tri-state before functioning.

HIGH SIDE DRIVER

The high-side driver drives an external floating N-channel MOSFET. An external bootstrap circuit referenced to the SWITCH node, consisting of a boot diode and capacitor is used to bias the external MOSFET gate. When the SWITCH node is at ground, the boot capacitor is charged to near the supply voltage using the boot diode and this stored charge is used to turn on the external MOSFET when the PWM signal goes high. Once the high-side MOSFET is turned on, the SWITCH voltage rises to the supply voltage and the boot voltage rises to equal to the supply voltage plus the VDRV voltage less the diode forward voltage.

When the PWM signal goes low, the MOSFET is turned off by pulling the MOSFET gate to the SWITCH voltage.

LOW SIDE DRIVER

The IR3598 low-side driver is designed to drive an external N-channel MOSFET referenced to ground. The low-side driver is connected internally to the supply voltage to turn the MOSFET on.

When the low-side MOSFET is turned on the SWITCH node is pulled to ground. This allows charging of the boot capacitor to the supply voltage ready to drive the high-side MOSFET based on the PWM signal level.

ADAPTIVE DEAD TIME ADJUSTMENT

In a synchronous buck configuration dead time between the turn off of one MOSFET and turn on of the other is necessary to prevent simultaneous conduction.
This prevents a shoot-through condition which would result in a short of the supply voltage to ground. A fixed dead time does not provide optimal performance over a variety of MOSFETs, converter duty cycles and board layouts.

The IR3598 provides an ‘adaptive’ dead time adjustment. This feature minimizes dead time to an optimum duration which allows for maximum efficiency. The ‘break before make’ adaptive design is achieved by monitoring gate and SWITCH voltages to determine OFF status of a MOSFET.
It also provides zero-voltage switching (ZVS) of the low side MOSFET with minimum current conduction through its body-diode.

When operating in IR ATL mode, and the PWM is switching between 1.8V and 0V, its falling edge transition from high to low will turn off the high side gate driver. The adaptive dead time circuit monitors the HI_GATE and the SWITCH node voltages during the high side MOSFET turn off. When the HI_GATE falls below 1.25V above the SWITCH node potential or the SWITCH node voltage drops below 1.38 V the high side MOSFET is determined to be turned off and the LO_GATE turn on is initiated. This turns on the external low-side MOSFET. The rising edge transition of the PWM signal from low to high voltage causes the low-side gate driver to turn off. The adaptive circuit monitors the voltage at LO_GATE and when it falls below 1.38V, the low-side MOSFET is determined to be turned off and the high-side MOSFET turn on is initiated.

FREQUENCY RANGE

The IR3598 is designed to operate over a wide input and output frequency range. When operating in Dual Mode, the input and output frequencies are identical. When operating in Doubler mode, the input frequency at the PWM1 input is twice the output frequency.

The lower limit of the output frequency range is dictated by the size of the BOOT capacitor, which must provide charge to the HIGH side MOSFET during the entire on time. The upper limit of frequency is determined by thermal limitations as well as pulse width limitations. The IR3598 is designed to operate with input frequencies as low as 300kHz and output frequencies in excess of 1MHz.

ENABLE

When enable is low there are no High Gate or Low Gate outputs, both HGx and LGx are held low so that no MOSFET switching occurs. When enable goes high from a low, the driver passes the appropriate PWM signal as described previously in this datasheet. . The enable is low when the pin voltage is below 0.8Vdc and high when the pin voltage is above 2Vdc.

DOUBLER MODE REACTION TO TRI-STATE PWM INPUT

In Doubler mode, anytime there is a tri-state on the master PWM1, all outputs (HGx and LGx) are tri-stated. When the PWM1 transitions from a tri-state to a high and then from a high to a low, only the 0deg phase operates. This allows the VR to operate properly in PS2 mode and during load releases.

Once the PWM1 sees a transition from a low to a high, the doubler function starts again, with output on both sets of HGx and LGx. DUAL Mode Reaction to Tri-State PWM input

Anytime there is a tri-state on the PWMx, all outputs (HGx and LGx) associated with that PWMx are low.

USING A DUAL MODE DRIVER AS A SINGLE DRIVER

To use the Dual Mode driver as a single simply leave the unused input to float. With PWM floating, both HGx and LGx will be off. Alternatively you can ground the input which will sink 1 mAdc to ground. This will cause HGx to be off and LGx to be on.

APPLICATION INFORMATION

Figure 1 shows the typical applications circuit for the IR3598.

CONFIGURING THE PWM AND PHASE MODES

The IR3598 can operate in 2 separate Phase modes which are Dual and Doubler. Also, the IR3598 can accept either an IR ATL input PWM signal or a Tri-State PWM signal (3.3V or 5V).

Table 1 shows the user how to configure both the PWM mode as well as the Phase Modes utilizing the FUNCTION and MODE pins. The FUNCTION selection (pin 12) is latched into the IR3598 at power up, and cannot be changed after power on reset.

BOOT STRAP CIRCUIT

Once the high-side MOSFET selection is made, the bootstrap circuit can be defined. The integrated boot diode of the IR3598 reduces the external component count for use in cost and space sensitive designs.

The bootstrap capacitor C_{Boot} stores the charge and provides the voltage required to drive the external high side MOSFET gate. The minimum capacitor value can be defined by:

$$C_{Boot} = Q_{HS\ MOSFET\_gate} / \Delta V_{Boot}$$

Where:

$Q_{HS\ MOSFET\_gate}$ is the total gate charge of the high-side external MOSFET(s)

ΔV_{Boot} is the droop allowed on the boot capacitor voltage (at the high-side MOSFET gate)

A series resistor, 1Ω to 2Ω, should be added to customize the rise time of the high-side output. Slowing down this output allows setting the phase node rising slew rate and limits the surge current into the boot capacitor on start-up.

SUPPLY DECOUPLING CAPACITOR

VCC decoupling to the IR3598 is provided by a 0.1uF bypass capacitor C_{Vcc} located close to the supply input pin. A series resistor Rvcc, typically 10Ω, is added in series with the supply voltage to filter high frequency ringing and noise. A 1.0uF or higher capacitor is recommended for the VDRV decoupling capacitor, CDRV.

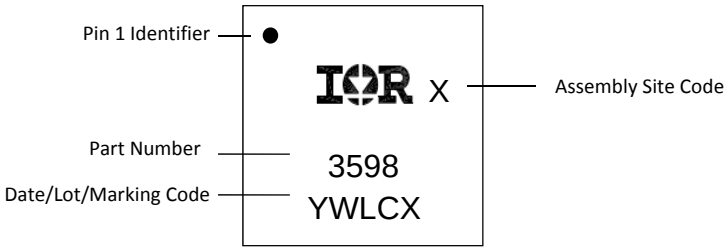
PCB LAYOUT CONSIDERATIONS

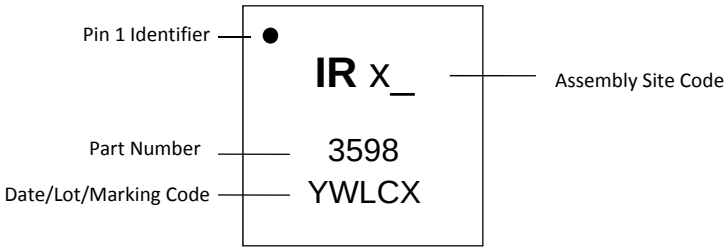
PCB layout and design is important to driver performance in voltage regulator circuits due to the high current slew rate (di/dt) during MOSFET switching.

- Locate all power components in each phase as close to each other as practically possible in order to minimize parasitics and losses, allowing for reasonable airflow.
- Input supply decoupling and bootstrap capacitors should be physically located close to their respective IC pins.
- High current paths like the gate driver traces should be as wide and short as practically possible.
- Trace inductances to the high and low side MOSFETs should be minimized.
- The ground connection of the IC should be as close as possible to the low side MOSFET source.
- Use of a copper plane under and around the IC and thermal vias to connect to buried copper layers improves the thermal performance.

MOSFET stages should be well bypassed with capacitors placed between the drain of the HIGH side MOSFET and the source of the LOW side MOSFET.

MARKING INFORMATION





Alternate marking

PACKAGE INFORMATION

QFN 3 x 3mm, 16 pin

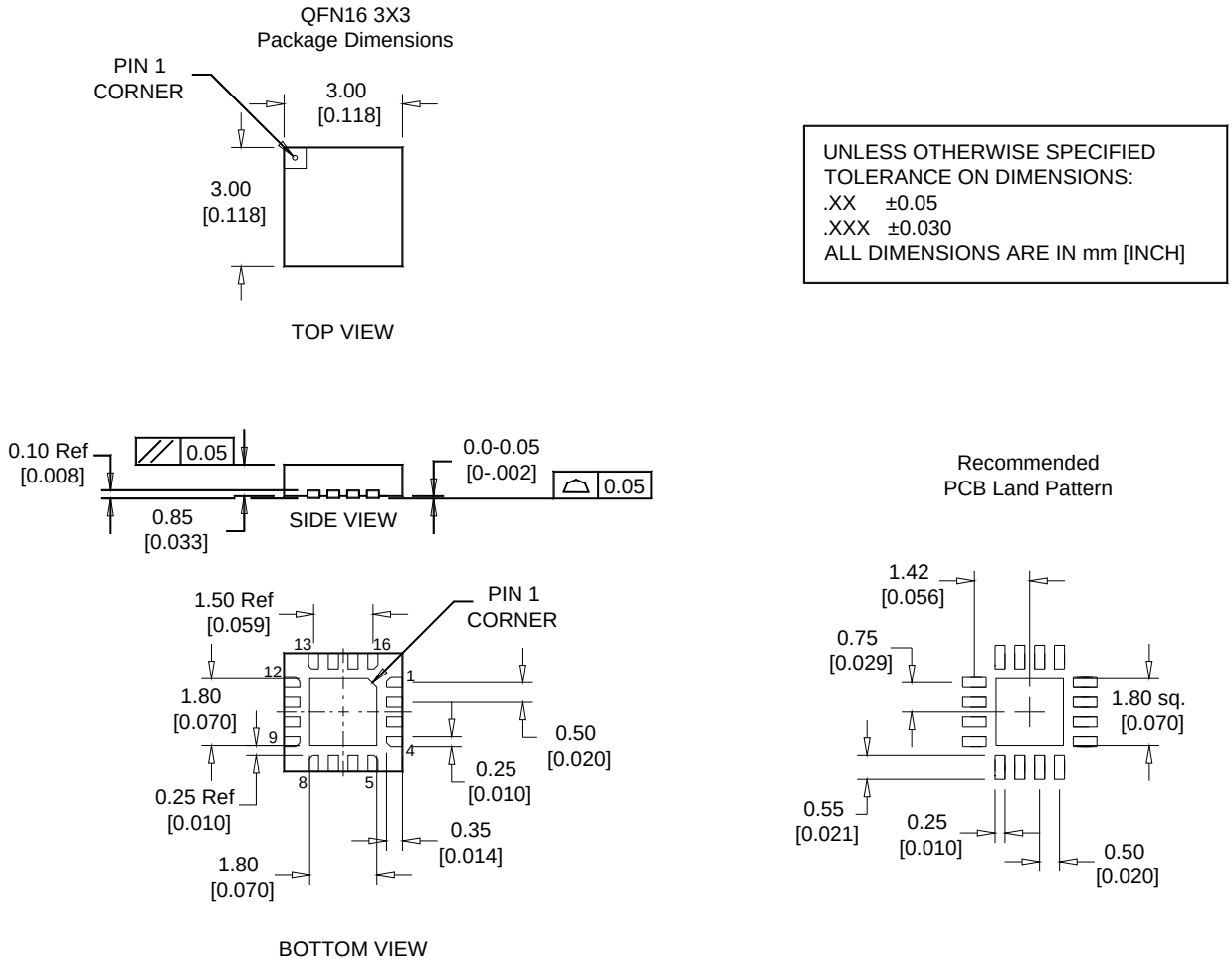


Figure 11: Package Dimensions

Data and specifications subject to change without notice.
This product will be designed and qualified for the Consumer market.
Qualification Standards can be found on IR's Web site.

International
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