3A, 2MHz, Synchronous Step-Down Converter

General Description

The RT8015B is a high efficiency synchronous, step down DC/DC converter. Its input voltage range is from 2.6V to 5.5V and provides an adjustable regulated output voltage from 0.8V to 5V while delivering up to 3A of output current.

The internal synchronous low on resistance power switches increase efficiency and eliminate the need for an external Schottky diode. The switching frequency is set by an external resistor. The 100% duty cycle provides low dropout operation extending battery life in portable systems. Current mode operation with external compensation allows the transient response to be optimized over a wide range of loads and output capacitors.

The RT8015B is operated in forced continuous PWM Mode which minimizes ripple voltage and reduces the noise and RF interference.

The 100% duty cycle in Low Dropout Operation further maximize battery life.

The RT8015B is available in the WDFN-10L 3x3 and SOP-8 (Exposed Pad) packages.

Ordering Information

RT8015B□□

- Package Type
  - QW : WDFN-10L 3x3
  - SP : SOP-8 (Exposed Pad-Option 2)
- Lead Plating System
  - G : Green (Halogen Free and Pb Free)

Note :

Richtek Green products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

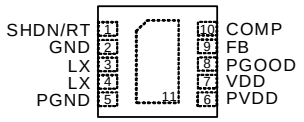
- **High Efficiency : Up to 95%**
- **Low $R_{DS(ON)}$ Internal Switches : 110mΩ**
- **Programmable Frequency : 300kHz to 2MHz**
- **No Schottky Diode Required**
- **0.8V Reference Allows for Low Output Voltage**
- **Forced Continuous Mode Operation**
- **Low Dropout Operation : 100% Duty Cycle**
- **Power Good Output Voltage Indicator**
- **RoHS Compliant and Halogen Free**

Applications

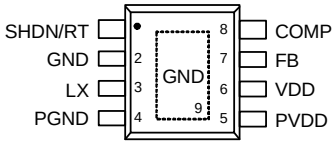
- Portable Instruments
- Battery-Powered Equipment
- Notebook Computers
- Distributed Power Systems
- IP Phones
- Digital Cameras

Pin Configurations

(TOP VIEW)



WDFN-10L 3x3

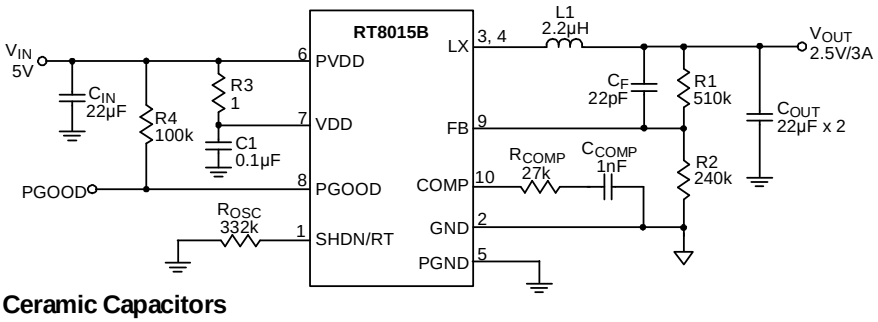


SOP-8 (Exposed Pad)

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area, otherwise visit our website for detail.

Typical Application Circuit



Note : Using all Ceramic Capacitors

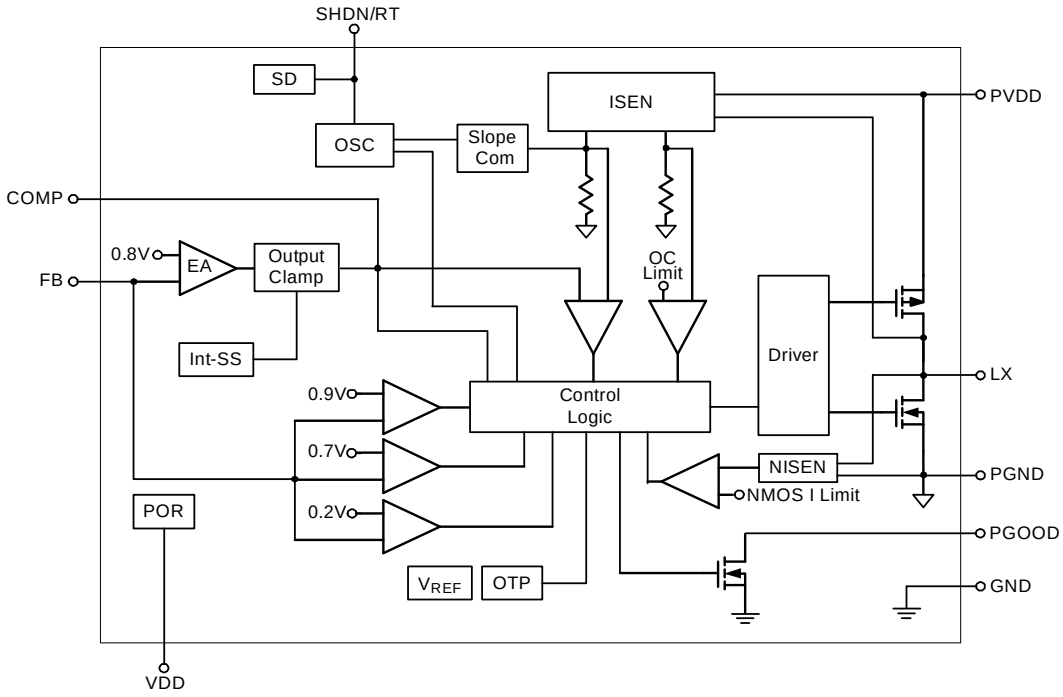
Table 1. Recommended Component Selection

V_{OUT} (V)	R1 (kW)	R2 (kW)	R_{COMP} (kW)	C_{COMP} (nF)	L1 (µH)	C_{OUT} (µF)
3.3	750	240	30	1	2.2	22 x 2
2.5	510	240	27	1	2.2	22 x 2
1.8	300	240	22	1	2.2	22 x 2
1.5	210	240	18	1	2.2	22 x 2
1.2	120	240	15	1	1.0	22 x 2
1.0	60	240	13	1	1.0	22 x 2

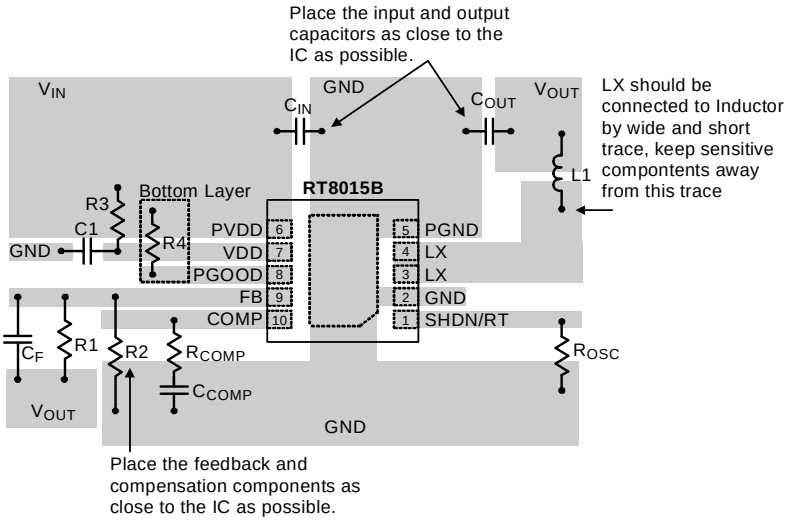
Functional Pin Description

Pin No.		Pin Name	Pin Function
WDFN -10L 3x3	SOP-8 (Exposed Pad)		
1	1	SHDN/RT	Oscillator Resistor Input. Connecting a resistor to ground from this pin sets the switching frequency. Forcing this pin to V_{DD} causes the device to be shut down.
2	2	GND	Signal Ground. All small signal components and compensation components should connect to this ground, which in turn connects to PGND at one point.
3, 4	3	LX	Internal Power MOSFET Switches Output. Connect this pin to the inductor.
5	4	PGND	Power Ground. Connect this pin close to the negative terminal of C_{IN} and C_{OUT}.
6	5	PVDD	Power Input Supply. Decouple this pin to PGND with a capacitor.
7	6	VDD	Signal Input Supply. Decouple this pin to GND with a capacitor. Normally V_{DD} is equal to PVDD.
8	--	PGOOD	Power Good Indicator. This pin is open drain logic output that is pulled to ground when the output voltage is not within ±12.5% of regulation point.
9	7	FB	Feedback Pin. This pin receives the feedback voltage from a resistive divider connected across the output.
10	8	COMP	Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. Connect external compensation elements to this pin to stabilize the control loop.
11	--	(Exposed Pad)	No Internal Connection. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
--	9	GND	The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Function Block Diagram



Layout Guide



Operation

Main Control Loop

The RT8015B is a monolithic, constant-frequency, current mode step-down DC/DC converter. During normal operation, the internal top power switch (P-Channel MOSFET) is turned on at the beginning of each clock cycle. Current in the inductor increases until the peak inductor current reach the value defined by the voltage on the COMP pin. The error amplifier adjusts the voltage on the COMP pin by comparing the feedback signal from a resistor divider on the FB pin with an internal 0.8V reference. When the load current increases, it causes a reduction in the feedback voltage relative to the reference. The error amplifier raises the COMP voltage until the average inductor current matches the new load current. When the top power MOSFET shuts off, the synchronous power switch (N-MOSFET) turns on until either the bottom current limit is reached or the beginning of the next clock cycle.

The operating frequency is set by an external resistor connected between the RT pin and ground. The practical switching frequency can range from 300kHz to 2MHz.

Dropout Operation

When the input supply voltage decreases toward the output voltage, the duty cycle increases toward the maximum on-time. Further reduction of the supply voltage forces the main switch to remain on for more than one cycle eventually reaching 100% duty cycle.

The output voltage will then be determined by the input voltage minus the voltage drop across the internal P-Channel MOSFET and the inductor.

Low Supply Operation

The RT8015B is designed to operate down to an input supply voltage of 2.6V. One important consideration at low input supply voltages is that the $R_{DS(ON)}$ of the P-Channel and N-Channel power switches increases. The user should calculate the power dissipation when the RT8015B is used at 100% duty cycle with low input voltages to ensure that thermal limits are not exceeded.

Slope Compensation and Inductor Peak Current

Slope compensation provides stability in constant frequency architectures by preventing sub-harmonic oscillations at duty cycles greater than 50%. It is accomplished internally by adding a compensating ramp to the inductor current signal. Normally, the maximum inductor peak current is reduced when slope compensation is added. In the RT8015B, however, separated inductor current signals are used to monitor over current condition. This keeps the maximum output current relatively constant regardless of duty cycle.

Short Circuit Protection

When the output is shorted to ground, the inductor current decays very slowly during a single switching cycle. A current runaway detector is used to monitor inductor current. As current increasing beyond the control of current loop, switching cycles will be skipped to prevent current runaway from occurring.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VDD, PVDD ---------- –0.3V to 6V
- LX Pin Switch Voltage ---------- –0.3V to (PVDD + 0.3V)
  <200ns ---------- –5V to 7.5V
- Other I/O Pin Voltages ---------- –0.3V to (VDD + 0.3V)
- LX Pin Switch Current ---------- 4A
- Power Dissipation, P_D @ T_A = 25°C
  SOP-8 (Exposed Pad) ---------- 1.333W
  WDFN-10L 3x3 ---------- 1.429W
- Package Thermal Resistance (Note 2)
  SOP-8 (Exposed Pad), θ_{JA} ---------- 75°C/W
  SOP-8 (Exposed Pad), θ_{JC} ---------- 15°C/W
  WDFN-10L 3x3, θ_{JA} ---------- 70°C/W
  WDFN-10L 3x3, θ_{JC} ---------- 8.2°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage ---------- 2.6V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{DD} = 3.3V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{DD}		2.6	--	5.5	V
Feedback Reference Voltage	V_{REF}		0.784	0.8	0.816	V
Feedback Leakage Current	I_{FB}		--	0.1	0.4	µA
DC Bias Current		Active , V_{FB} = 0.78V, Not Switching	--	460	--	µA
		Shutdown	--	--	1	µA
Output Voltage Line Regulation		V_{IN} = 2.7V to 5.5V	--	0.03	--	%/V
Output Voltage Load Regulation		Measured in Servo Loop, V_{COMP} = 0.2V to 0.7V (Note 5)	–0.2	±0.02	0.2	%
Error Amplifier Transconductance	g_m		--	800	--	µs
Current Sense Transresistance	R_T		--	0.4	--	Ω
Switching Leakage Current		SHDN/RT = VIN = 5.5V	--	--	1	µA

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Switching Frequency		R_{OSC} = 332k	0.8	1	1.2	MHz
		Switching Frequency	0.3	--	2	MHz
Switch On Resistance, High	R_{PMOS}	I_{SW} = 0.5A	--	110	160	mΩ
Switch On Resistance, Low	R_{NMOS}	I_{SW} = 0.5A	--	110	170	mΩ
Power Good Range			--	±12.5	±15	%
Power Good Pull-Down Resistance			--	--	120	Ω
Peak Current Limit	I_{LIM}		3.2	3.8	--	A
Under Voltage Lockout Threshold		V_{DD} Rising	--	2.4	--	V
		V_{DD} Falling	--	2.3	--	V
Shutdown Threshold			--	V_{IN} – 0.7	V_{IN} – 0.4	V

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured in natural convection at T_A = 25°C on a high-effective thermal conductivity four-layer test board of JEDEC 51-7 thermal measurement standard. The measurement case position of θ_{JC} is on the exposed pad of the packages.

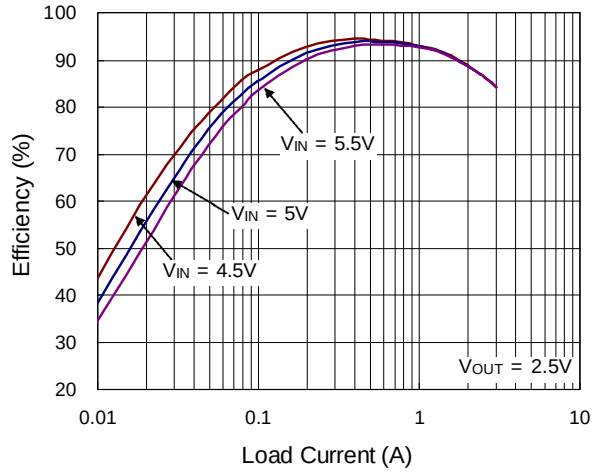
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

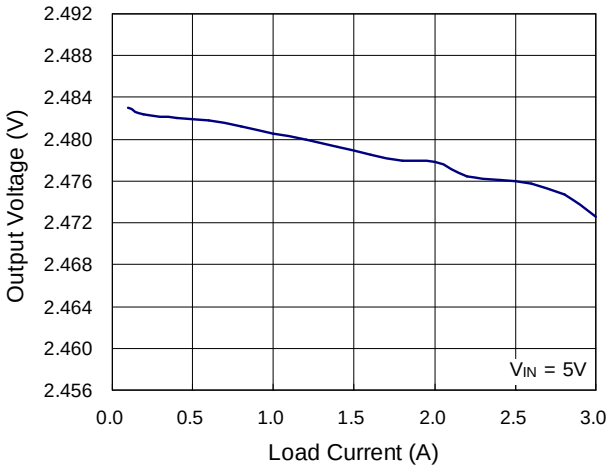
Note 5. The specifications over the -40°C to 85°C operation ambient temperature range are assured by design, characterization and correlation with statistical process controls.

Typical Operating Characteristics

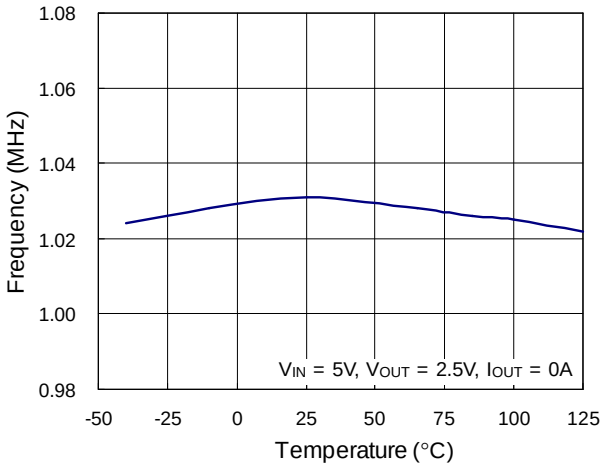
Efficiency vs. Load Current



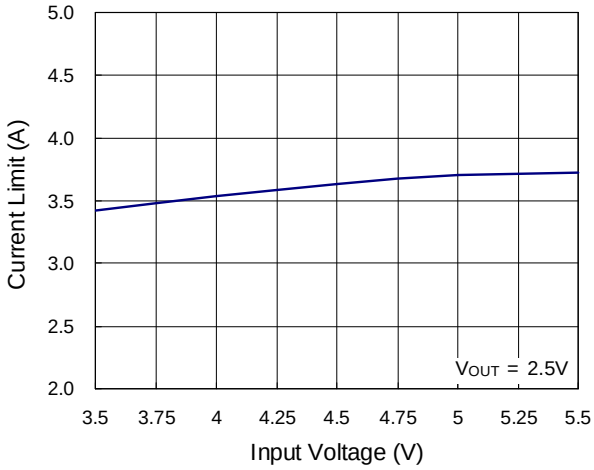
Output Voltage vs. Load Current



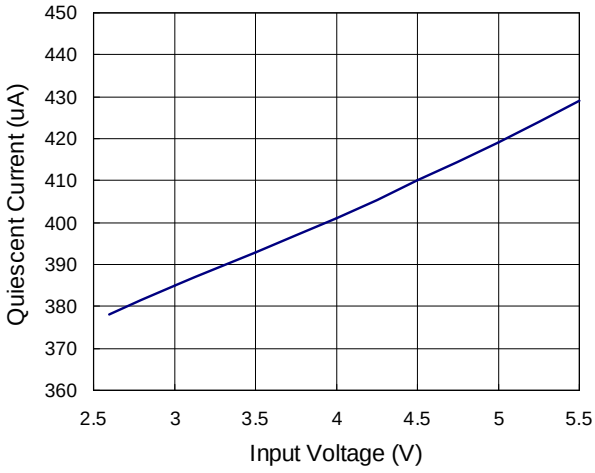
Frequency vs. Temperature



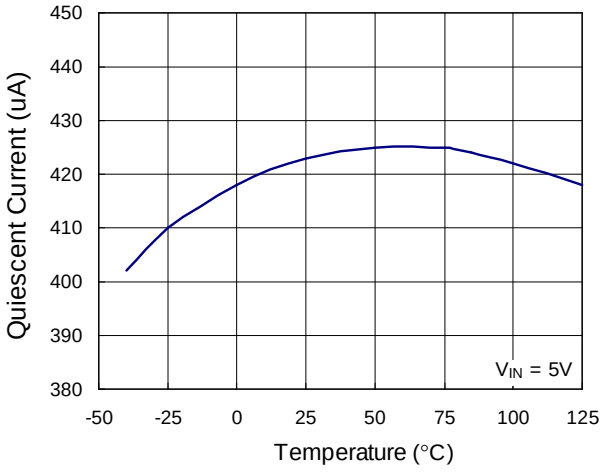
Peak Current Limit vs. Input Voltage



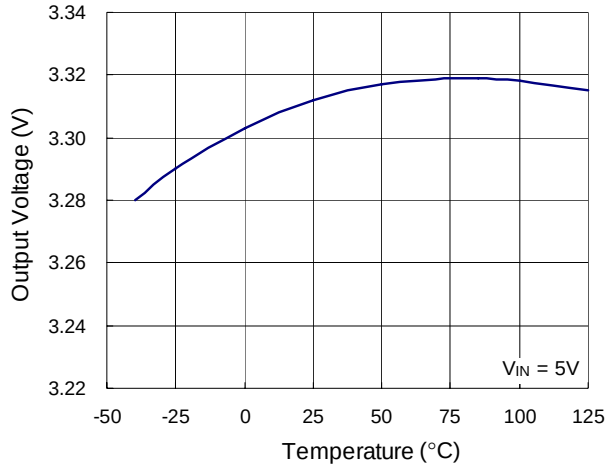
Quiescent Current vs. Input Voltage



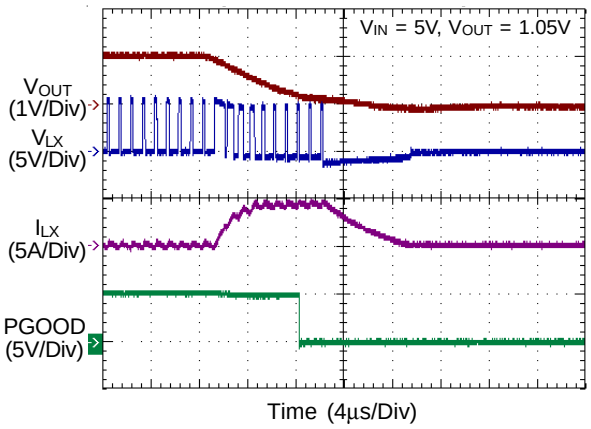
Quiescent Current vs. Temperature



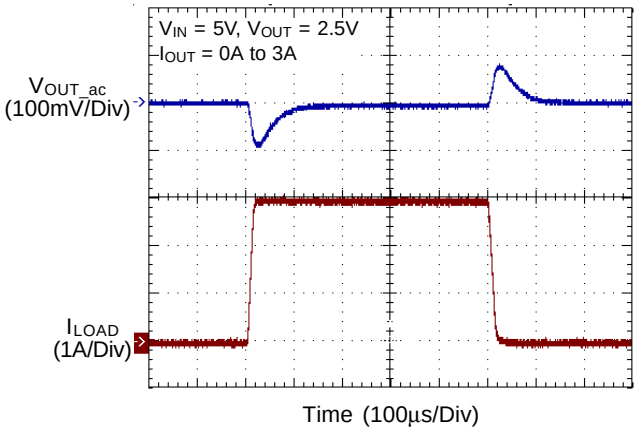
Output Voltage vs. Temperature



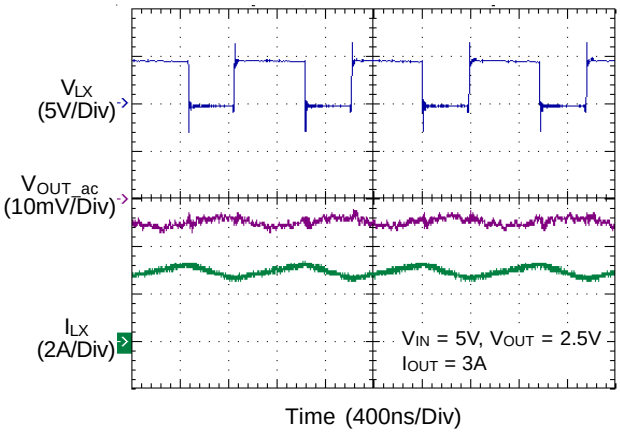
UVP



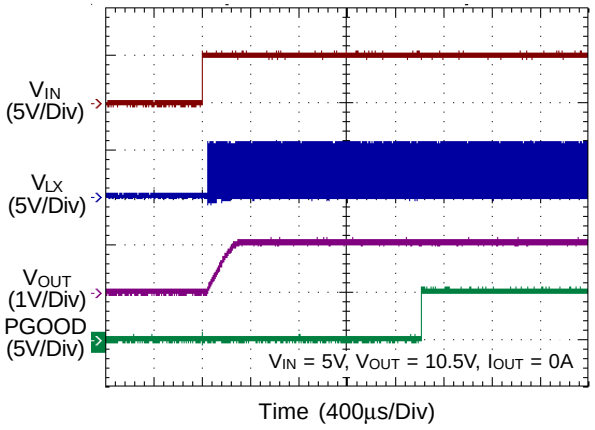
Load Transient Response



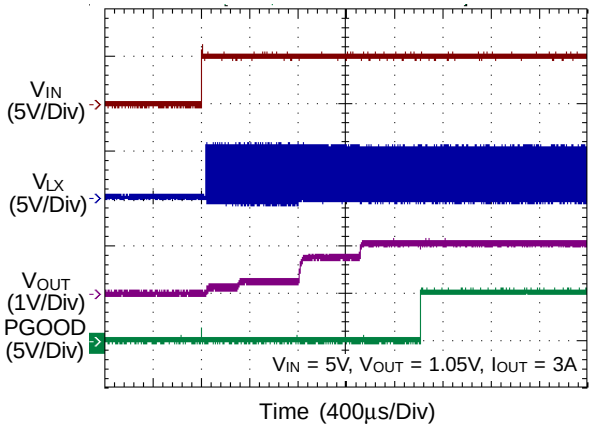
Output Ripple



Start up with No Load



Start up with Heavy Load



Application Information

The basic RT8015B application circuit is shown in Typical Application Circuit. External component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency followed by C_{IN} and C_{OUT}.

Output Voltage Programming

The output voltage is set by an external resistive divider according to the following equation :

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

where V_{REF} equals to 0.8V typical.

The resistive divider allows the FB pin to sense a fraction of the output voltage as shown in Figure 1.

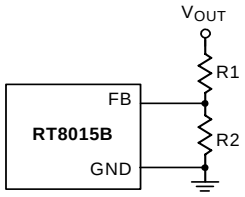


Figure 1. Setting the Output Voltage

Soft-Start

The RT8015B contains an internal soft-start clamp that gradually raises the clamp on the COMP pin. The full current range becomes available on COMP after 2048 switching cycles as shown in Figure 2.

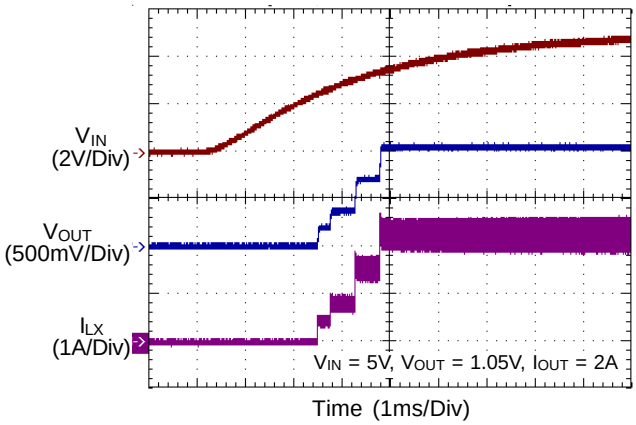


Figure 2. Soft-Start

Power Good Output

The power good output is an open-drain output and requires a pull up resistor. When the output voltage is 12.5% above or 12.5% below its set voltage, PGOOD will be pulled low. It is held low until the output voltage returns to within the allowed tolerances once more. In soft start, PGOOD is actively held low and is allowed to transition high until soft start finished over and the output voltage reaches 87.5% of its set voltage.

Operating Frequency

Selection of the operating frequency is a tradeoff between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequency improves efficiency by reducing internal gate charge and switching losses but requires larger inductance and/or capacitance to maintain low output ripple voltage.

The operating frequency of the RT8015B is determined by an external resistor that is connected between the RT pin and ground. The value of the resistor sets the ramp current that is used to charge and discharge an internal timing capacitor within the oscillator. The RT resistor value can be determined by examining the frequency vs. RT curve. Although frequencies as high as 2MHz are possible, the minimum on-time of the RT8015B imposes a minimum limit on the operating duty cycle. The minimum on-time is typically 110ns. Therefore, the minimum duty cycle is equal to 100 x 110ns x f(Hz).

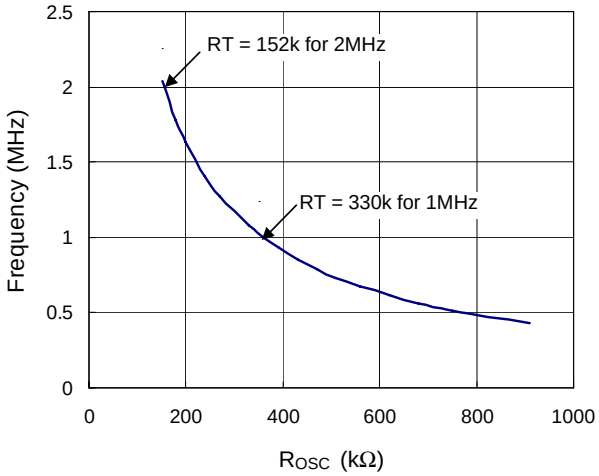


Figure 3

Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the ripple current. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance.

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right]\left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

Having a lower ripple current reduces the ESR losses in the output capacitors and the output voltage ripple. Highest efficiency operation is achieved at low frequency with small ripple current. This, however, requires a large inductor. A reasonable starting point for selecting the ripple current is $\Delta I = 0.4(I_{MAX})$. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right]\left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite or mollypermalloy cores. Actual core loss is independent of core size for a fixed inductor value but it is very dependent on the inductance selected. As the inductance increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard", which means that inductance collapses abruptly when the peak design current is exceeded.

This result in an abrupt increase in inductor ripple current and consequent output voltage ripple.

Do not allow the core to saturate!

Different core materials and shapes will change the size/ current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate energy but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price vs. size requirements and any radiated field/EMI requirements.

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple voltage, a low ESR input capacitor sized for the maximum RMS current should be used. RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Choose a capacitor rated at a higher temperature than required.

Several capacitors may also be paralleled to meet size or height requirements in the design.

The selection of C_{OUT} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients, as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section. The output ripple, ΔV_{OUT}, is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8fC_{OUT}}\right]$$

The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR but can be used in cost sensitive

applications provided that consideration is given to ripple current ratings and long term reliability. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to $\Delta I_{LOAD(ESR)}$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem. The COMP pin external components and output capacitor shown in Typical Application Circuit will provide adequate compensation for most applications.

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as :

Efficiency = 100% – (L1+ L2+ L3+ ...) where L1, L2, etc. are the individual losses as a percentage of input power. Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses: V_{DD} quiescent current and I^2R losses.

The V_{DD} quiescent current loss dominates the efficiency loss at very low load currents whereas the I^2R loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is of no consequence.

1. The V_{DD} quiescent current is due to two components : the DC bias current as given in the electrical characteristics and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge ΔQ moves from V_{DD} to ground. The resulting $\Delta Q/\Delta t$ is the current out of V_{DD} that is typically larger than the DC bias current. In continuous mode, $I_{GATECHG} = f(QT+QB)$ where QT and QB are the gate charges of the internal top and bottom switches.

Both the DC bias and gate charge losses are proportional to V_{DD} and thus their effects will be more pronounced at higher supply voltages.

2. I^2R losses are calculated from the resistances of the internal switches, RSW and external inductor RL. In continuous mode, the average output current flowing through inductor L is "chopped" between the main switch and the synchronous switch. Thus, the series resistance looking into the LX pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (D) as follows :

$R_{SW} = R_{DS(ON)}TOP \times D + R_{DS(ON)}BOT \times (1"D)$ The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain I^2R losses, simply add RSW to RL and multiply the result by the square of the average output current. Other losses including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses generally account for less than 2% of the total loss.

Current Limit

RT8015B has cycle by cycle current limiting control. The current limit circuit employs a "peak" current sensing algorithm. If the magnitude of the current sense signal is above the current limit threshold, the controller will turn off high side MOSFET and turn on low side MOSFET.

Under Voltage Protection (UVP)

The output voltage can be continuously monitored for under voltage protection. When the output voltage is less than 25% of its set voltage threshold, the under voltage protection circuit will be triggered to terminate switching operation and the controller will be latched unless VDD POR is detected again. During soft-start, the UVP will be blanked until soft-start finish.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications of the RT8015B, the maximum junction temperature is 125°C and T_A is the ambient temperature. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For SOP-8 (Exposed Pad) packages, the thermal resistance, θ_{JA}, is 75°C/W on a standard JEDEC 51-7 four-layer thermal test board. For WDFN-10L 3x3 packages, the thermal resistance, θ_{JA}, is 70°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formulas :

$P_{D(MAX)}$ = (125°C – 25°C) / (75°C/W) = 1.333W for SOP-8 (Exposed Pad) package

$P_{D(MAX)}$ = (125°C – 25°C) / (70°C/W) = 1.429W for WDFN-10L 3x3 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. For the RT8015B packages, the derating curves in Figure 4 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

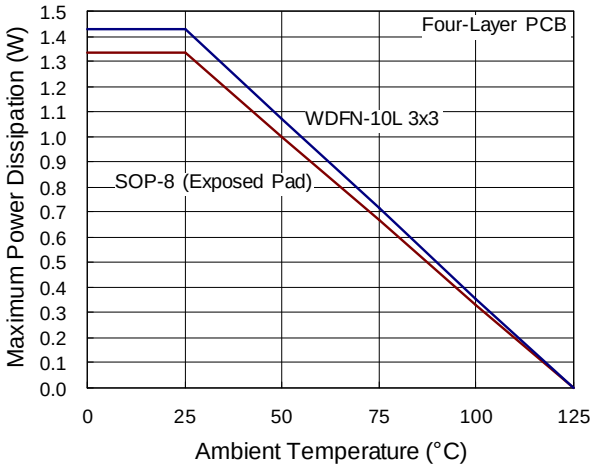


Figure 4. Derating Curves for RT8015B Package

Layout Considerations

Follow the PCB layout guidelines for optimal performance of RT8015B.

- A ground plane is recommended. If a ground plane layer is not used, the signal and power grounds should be segregated with all small-signal components returning to the GND pin at one point that is then connected to the PGND pin close to the IC. The exposed pad should be connected to GND.
- Connect the terminal of the input capacitor(s), C_{IN}, as close as possible to the PVDD pin. This capacitor provides the AC current into the internal power MOSFETs.
- LX node is with high frequency voltage swing and should be kept within small area. Keep all sensitive small-signal nodes away from the LX node to prevent stray capacitive noise pick-up.
- Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of powercomponents. You can connect the copper areas to any DC net (PVDD, VDD, VOUT, PGND, GND, or any other DC rail in your system).

} Connect the FB pin directly to the feedback resistors. The resistor divider must be connected between V_{OUT} and GND.

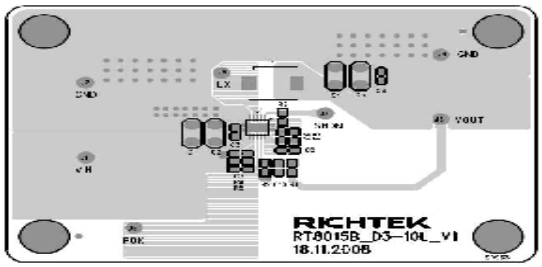


Figure 5

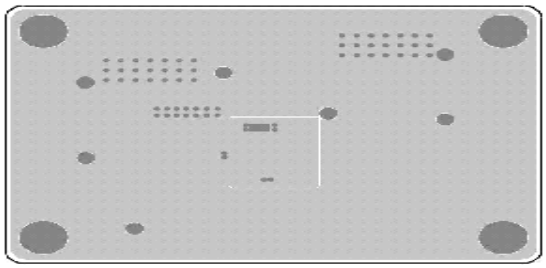


Figure 6

Recommended component selection for Typical Application

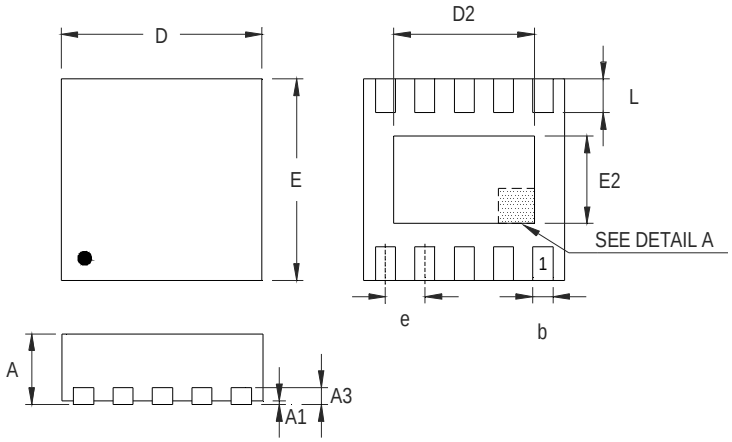
Table 1. Inductors

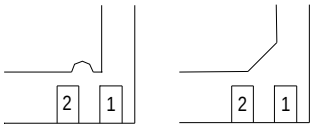
Component Supplier	Series	Inductance (μH)	DCR (mΩ)	Current Rating (mA)	Dimensions (mm)
TAIYO YUDEN	NR 8040	2	9	7800	8x8x4

Table 2. Capacitors for C_{IN} and C_{OUT}

Component Supplier	Part No.	Capacitance (μF)	Case Size
TDK	C3225X5R0J226M	22	1210
TDK	C2012X5R0J106M	10	0805
Panasonic	ECJ4YB0J226M	22	1210
Panasonic	ECJ4YB1A106M	10	1210
TAIYO YUDEN	LMK325BJ226ML	22	1210
TAIYO YUDEN	JMK316BJ226ML	22	1206
TAIYO YUDEN	JMK212BJ106ML	10	0805

Outline Dimension





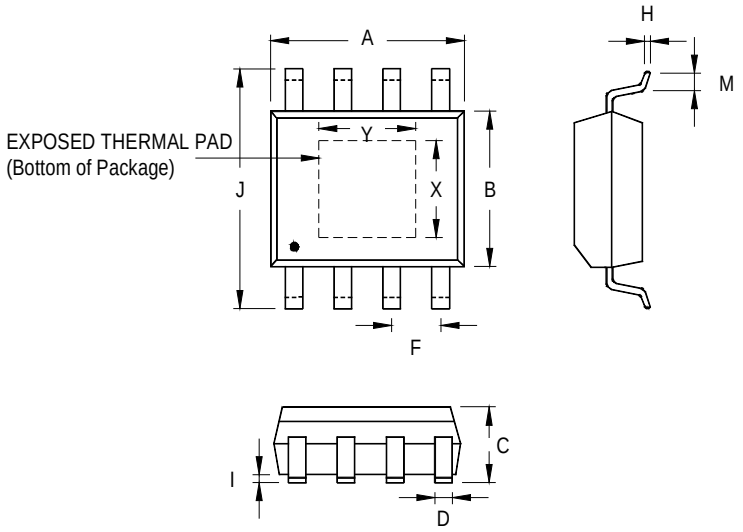
DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.500	1.750	0.059	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 10L DFN 3x3 Package



Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		4.801	5.004	0.189	0.197
B		3.810	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package

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