Power-Distribution Switches with Soft Start

Features

- **90mΩ High Side MOSFET**
- **2A Continuous Current**
- **Soft-Start Time Programmable by External Capacitor**
- **Wide Supply Voltage Range: 2.7V to 5.5V**
- **Current-Limit and Short-Circuit Protections**
- **Under-Voltage Lockout Protection**
- **Reverse Current Blocking when Switch Disabled**
- **Over-Temperature Protection**
- **Logic Level Enable Input**
  APL3512A: Active High
  APL3512B: Active Low
- **Lead Free and Green Devices Available (RoHS Compliant)**

Applications

- **TFT LCD Modules**
- **Notebook and Desktop Computers**
- **USB Ports**
- **High-Side Power Protection Switches**

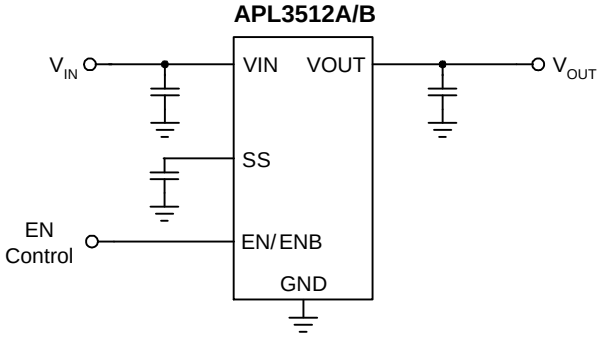
General Description

The APL3512A/B is a power-distribution switch with some protection functions that can deliver current up to 2A. The device incorporates a 90mΩ N-channel MOSFET power switch that is controlled by an enable logic pin and has a SS pin dedicated to soft-start ramp-up rate control that can be used in application where the inrush current is concerned.

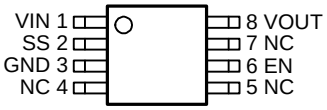
The device integrates some protection features, including current-limit protection, short-circuit protection, over-temperature protection, and UVLO. The current-limit and short-circuit protection can protect down-stream devices from catastrophic failure by limiting the output current at current-limit threshold during over-load or short-circuit events. When V_{OUT} drops below V_{IN}-1.5V the devices limit the current to a lower and safe level. The over-temperature protection function shuts down the N-channel MOSFET power switch when the junction temperature rises beyond 140°C and will automatically turns on the power switch when the temperature drops by 20°C. The UVLO function keeps the power switch in off state until there is a valid input voltage present.

The device is available in lead free SOT-23-5, TDFN2x2-6 and SOP-8 packages with enable active-high(EN) and active-low(ENB) versions.

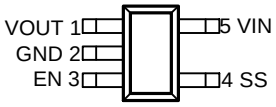
Simplified Application Circuit



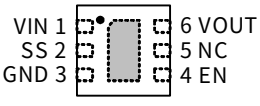
Pin Configuration



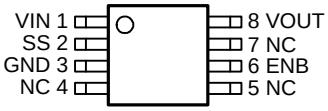
SOP-8
APL3512A



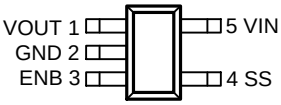
SOT-23-5
APL3512A



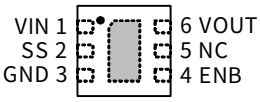
TDFN2x2-6
APL3512A



SOP-8
APL3512B



SOT-23-5
APL3512B



TDFN2x2-6
APL3512B

Exposed Pad, connect to large ground plane for heat dissipation

Ordering and Marking Information

APL3512 □□□-□□□ Assembly Material Handling Code Temperature Range Package Code EN Function	Package Code B : SOT-23-5 K : SOP-8 QB : TDFN2x2-6 Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel EN Function A : Active High B : Active Low Assembly Material G : Halogen and Lead Free Device

APL3512A B:	L2AX	X - Date Code
APL3512B B:	L2BX	X - Date Code
APL3512A K:	APL3512A XXXXX	XXXXX - Date Code
APL3512B K:	APL3512B XXXXX	XXXXX - Date Code
APL3512A QB:	L12A X	X - Date Code
APL3512B QB:	L12B X	X - Date Code

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant)and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{IN}	VIN to GND Voltage	-0.3 ~ 6	V
V_{OUT}	VOUT to GND Voltage	-0.3 ~ 6	V
V_{ENB}, V_{EN}	EN, ENB to GND Voltage	-0.3 ~ 6	V
V_{SS}	SS to GND Voltage	-0.3 ~ 6	V
I_{OUT}	Continuous Output Current	Internally Limited	A
T_J	Maximum Junction Temperature	-40 ~ 150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in Free Air (Note 2) SOT-23-5 SOP-8 TDFN2x2-6	 250 160 225	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{IN}	VIN Input Voltage	2.7 ~ 5.5	V
I_{OUT}	OUT Output Current	0 ~2	A
C_{SS}	SS Pin Soft-Start Capacitor (Note 4)	0.3 ~470	nF
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3: Refer to the typical application circuit.

Note 4: Attaching a capacitor on SS pin can adjust the V_{OUT} soft-start rate. If the C_{SS} is out of the recommended range, the soft-start rate could become internally controlled as if no C_{SS}.

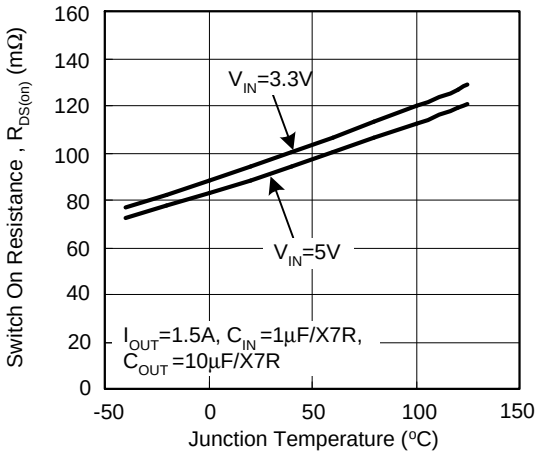
Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}=5V, V_{EN}=5V or V_{ENB}=0V and T_A=-40~85°C. Typical values are at T_A=25°C.

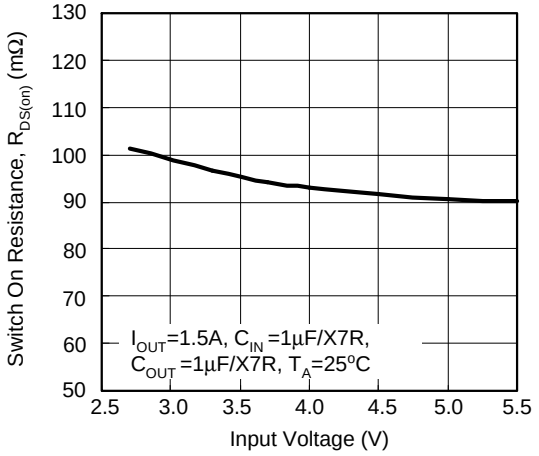
Symbol	Parameter	Test Conditions	APL3512A/B			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
	VIN Supply Current	No load, V_{EN}=0V or V_{ENB}=5V	-	-	1	μA
		No load, V_{EN}=5V or V_{ENB}=0V	-	60	100	μA
	Leakage Current	VOUT=GND, V_{EN}=0V or V_{ENB}=5V	-	-	1	μA
	Reverse Leakage Current	VIN=GND, V_{OUT}=5V, V_{EN}=0V or V_{ENB}=5V	-	-	1	μA
POWER SWITCH						
$R_{DS(ON)}$	Power Switch On Resistance	I_{OUT}=1.5A, T_A=25°C	-	90	110	mΩ
		I_{OUT}=1.5A, T_A=-40~85°C	-	90	140	mΩ
UNDER-VOLTAGE LOCKOUT						
	VIN UVLO Threshold Voltage	V_{IN} rising, T_A=-40~85°C	2.3	-	2.65	V
	VIN UVLO Hysteresis		-	0.2	-	V
CURRENT-LIMIT AND SHORT-CIRCUIT PROTECTIONS						
I_{LIM}	Current-Limit Threshold	V_{IN}=2.7V to 5.5V, T_A=-40~85°C	2.5	3.1	4.22	A
I_{SHORT}	Short-Circuit Output Current	V_{IN}=2.7V to 5.5V	-	0.8	-	A
SOFT-START CONTROL PIN						
	SS Current	V_{IN}=5V, T_A=-40~85°C	1	2	3	μA
t_{SS}	Soft-Start Time	V_{IN}=5V, No load, C_{OUT}=1μF, C_{SS}=10nF, T_A=-40~85°C	-	10	-	ms
		V_{IN}=3.3V, No load, C_{OUT}=1μF, C_{SS}=10nF, T_A=-40~85°C	-	6.6	-	ms
		V_{IN}=3.3V, No load, C_{OUT}=1μF, No C_{SS} or SS tied to V_{IN}, T_A=-40~85°C	1	2	3	ms
EN OR ENB INPUT PIN						
V_{IH}	Input Logic HIGH	V_{IN}=2.7V to 5V	2	-	-	V
V_{IL}	Input Logic LOW	V_{IN}=2.7V to 5V	-	-	0.8	V
	Input Current		-	-	1	μA
	VOUT Discharge Resistance	V_{EN}=0V or V_{ENB}=5V	-	150	-	Ω
OVER-TEMPERATURE PROTECTION (OTP)						
T_{OTP}	Over-Temperature Threshold	T_J rising	-	140	-	°C
	Over-Temperature Hysteresis		-	20	-	°C

Typical Operating Characteristics

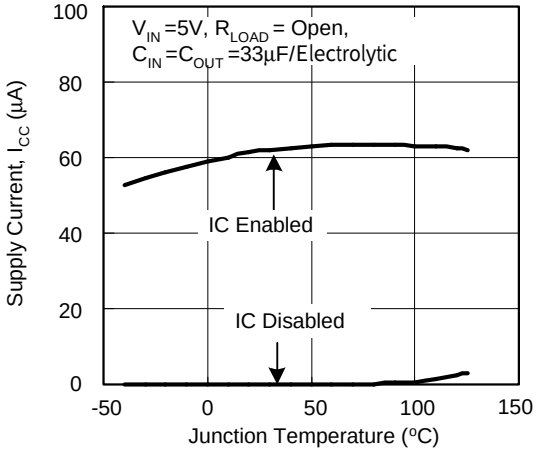
Switch On Resistance vs. Junction Temperature



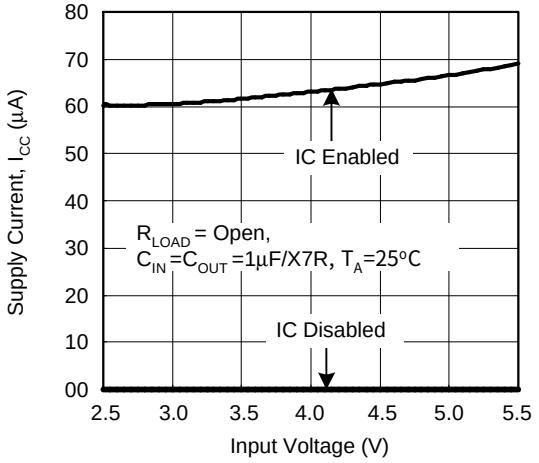
Switch On Resistance vs. Input Voltage



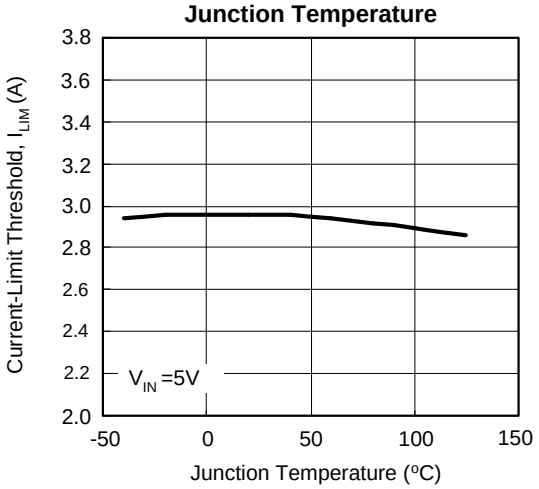
Supply Current vs. Junction Temperature



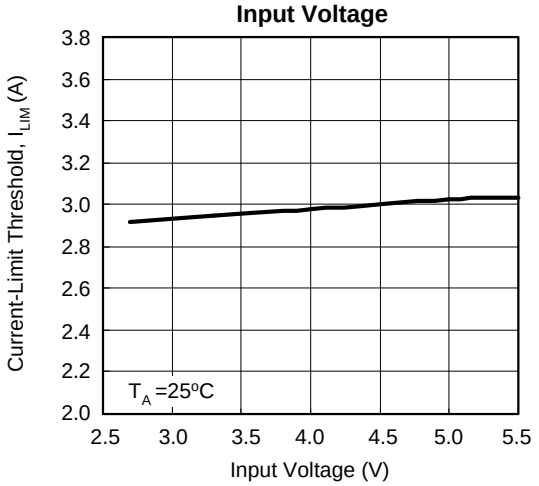
Supply Current vs. Input Voltage



Current-Limit Threshold vs. Junction Temperature

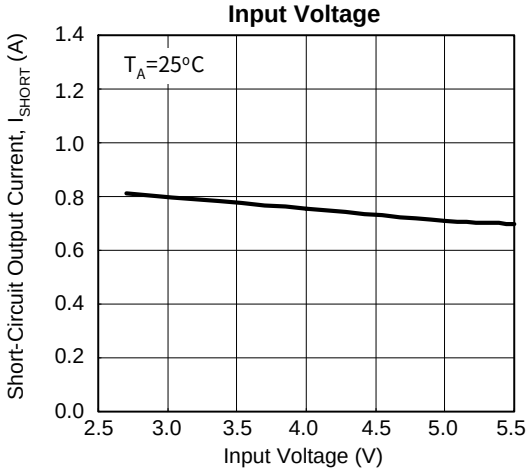


Current-Limit Threshold vs. Input Voltage

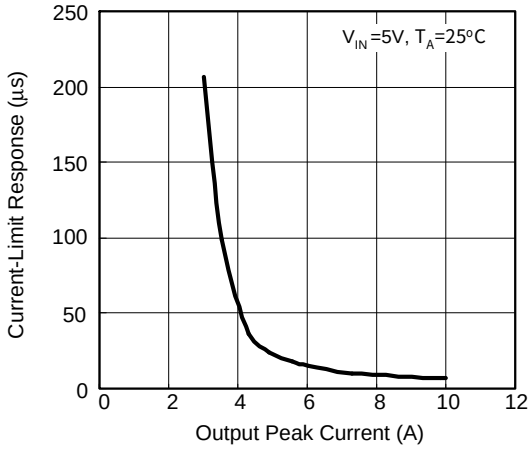


Typical Operating Characteristics (Cont.)

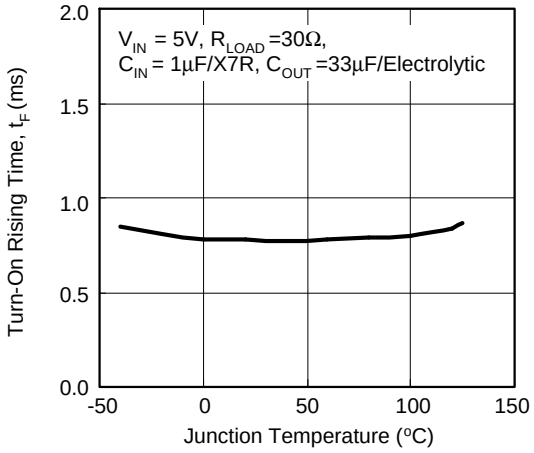
Short-Circuit Output Current vs. Input Voltage



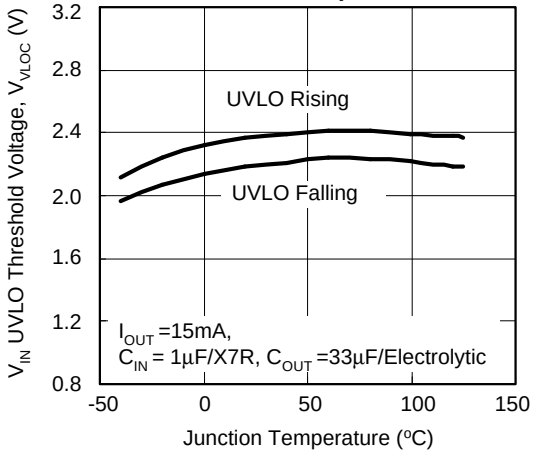
Current-Limit Response vs. Output Peak Current



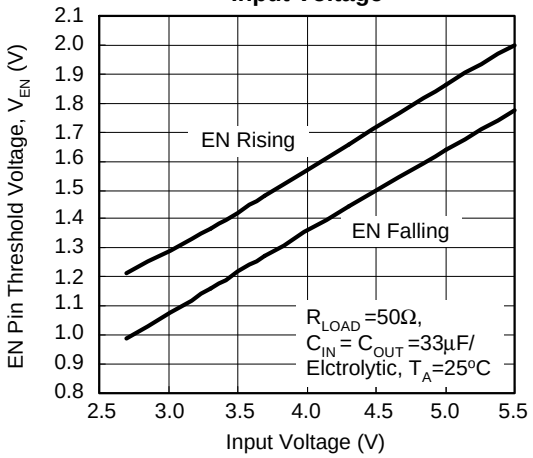
Turn-On Rising Time vs. Junction Temperature



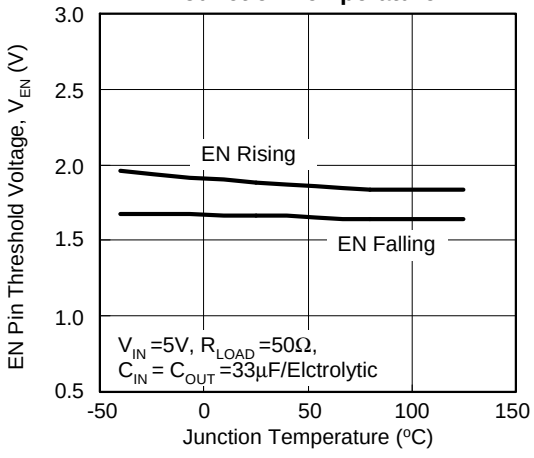
V_{IN} UVLO Threshold Voltage vs. Junction Temperature



EN Pin Threshold Voltage vs. Input Voltage

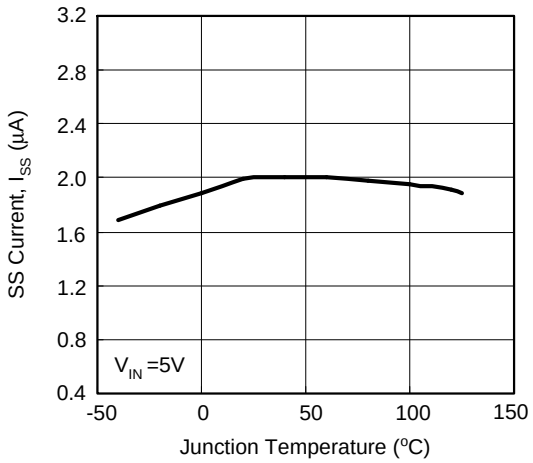


EN Pin Threshold Voltage vs. Junction Temperature

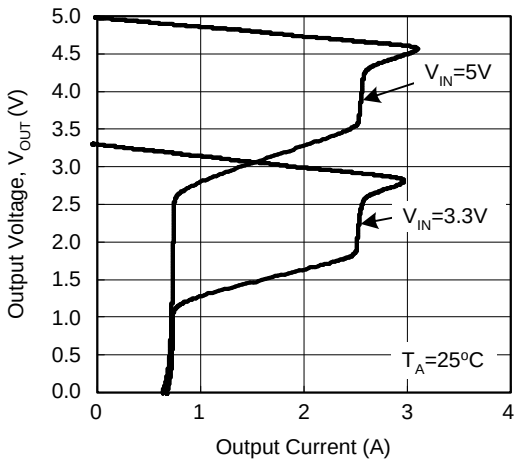


Typical Operating Characteristics (Cont.)

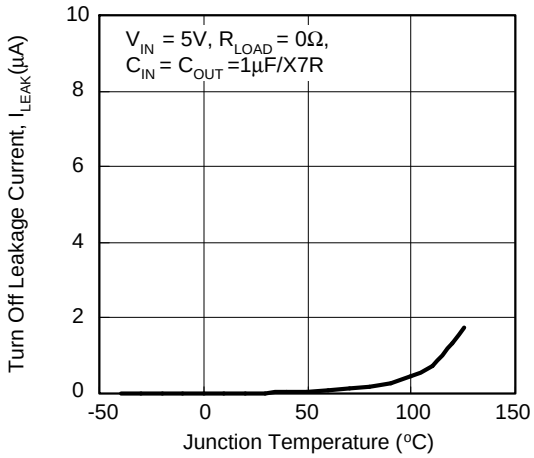
SS Current vs. Junction Temperature



Output Voltage vs. Output Current



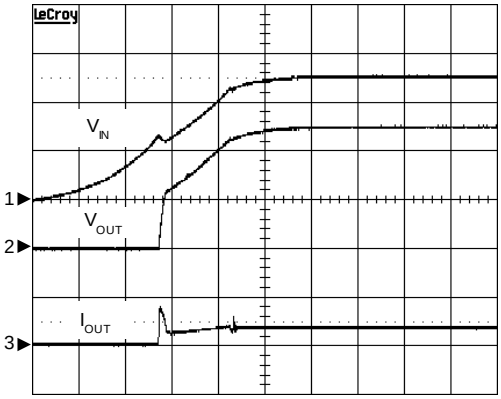
Turn Off Leakage Current vs. Junction Temperature



Operating Waveforms

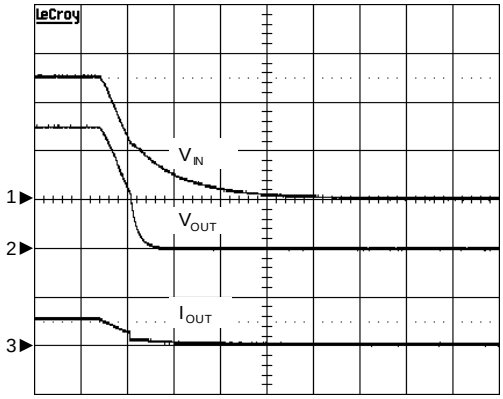
The test condition is V_{IN}=5V, T_A= 25°C unless otherwise specified.

Power On



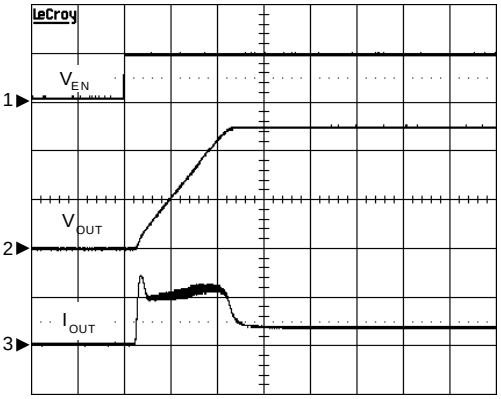
V_{IN} =5V, R_{LOAD} =30Ω, C_{IN} =1μF/MLCC,
C_{OUT} =100μF/Electrolytic, SS open
CH1: V_{IN}, 2V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: I_{OUT}, 0.5A/Div, DC
TIME:5ms/Div

Power Off



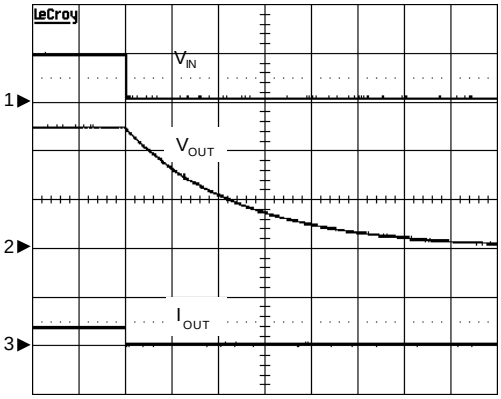
V_{IN} =5V, R_{LOAD} =30Ω, C_{IN} =1μF/MLCC,
C_{OUT} =100μF/Electrolytic, SS open
CH1: V_{IN}, 2V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: I_{OUT}, 0.5A/Div, DC
TIME:20ms/Div

Turn On Response



V_{IN} =5V, R_{LOAD} =30Ω, C_{IN} =1μF/MLCC,
C_{OUT} =100μF/Electrolytic, SS open
CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: I_{OUT}, 0.5A/Div, DC
TIME:0.5ms/Div

Turn Off Response

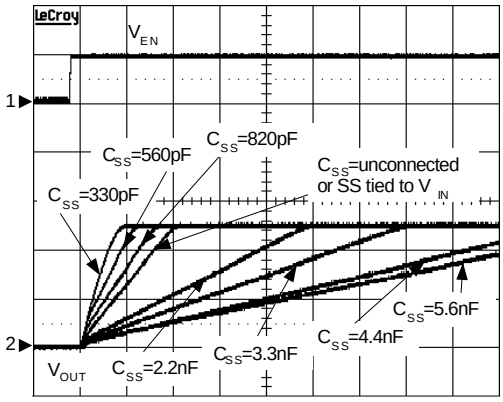


V_{IN} =5V, R_{LOAD} =30Ω, C_{IN} =1μF/MLCC,
C_{OUT} =100μF/Electrolytic, SS open
CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: I_{OUT}, 0.5A/Div, DC
TIME:1ms/Div

Operating Waveforms (Cont.)

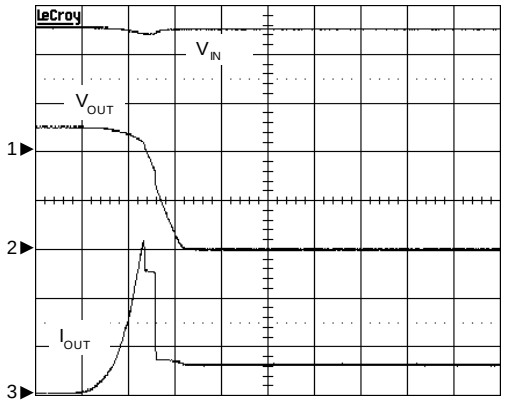
The test condition is V_{IN}=5V, T_A= 25°C unless otherwise specified.

Soft Start Ramp-up Control



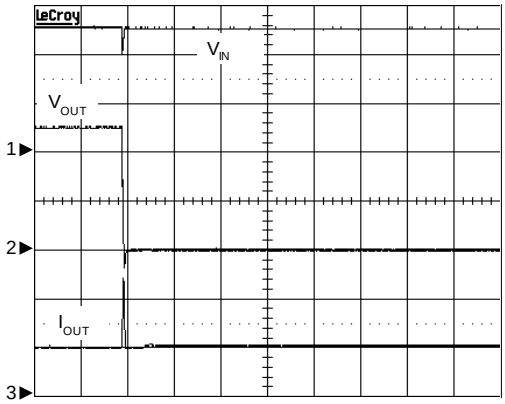
V_{IN} =5V, R_{LOAD} =30Ω, C_{IN} =1µF/MLCC,
C_{OUT}=33µF/Electrolytic
CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
TIME: 0.5ms/Div

Current Limit Response



V_{IN} =5V, C_{IN} =1µF/MLCC,
C_{OUT}=33µF/Electrolytic
CH1: V_{IN}, 2V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: I_{OUT}, 1A/Div, DC
TIME: 2ms/Div

Short Circuit Protection

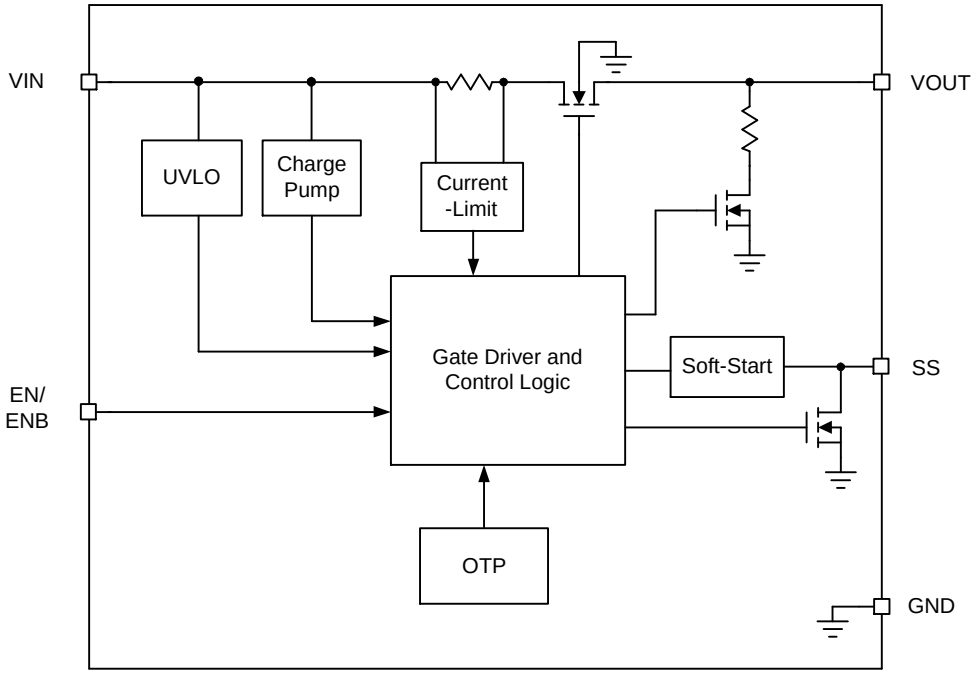


V_{IN} =5V, VOUT short to ground,
C_{IN} =1µF/MLCC, C_{OUT}=33µF/Electrolytic
CH1: V_{IN}, 2V/Div, DC
CH2: V_{OUT}, 2V/Div, DC
CH3: I_{OUT}, 20A/Div, DC
TIME: 100µs/Div

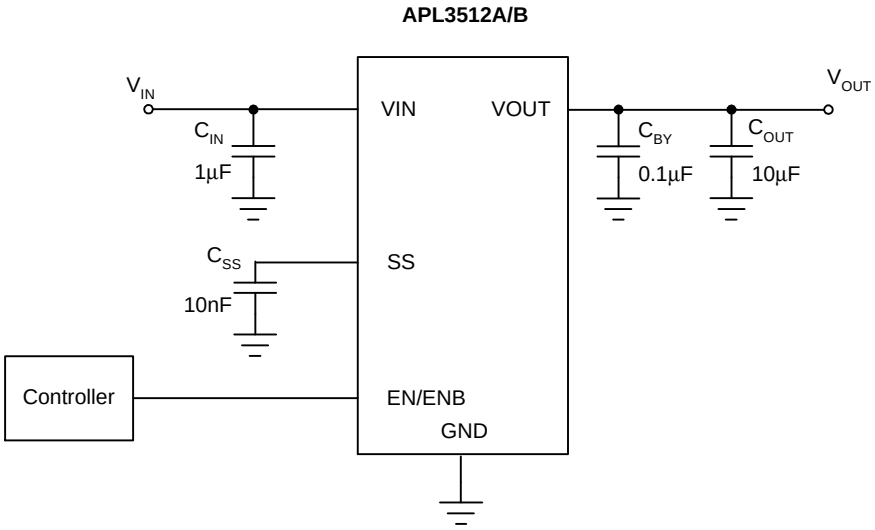
Pin Description

PIN			NAME	FUNCTION
NO.				
SOT-23-5	SOP-8	TDFN2x2-6		
1	8	6	VOUT	Output Voltage Pin. The output voltage follows the input voltage. When ENB is high or EN is low the output voltage is discharged by an internal resistor.
2	3	3	GND	Ground
3	6	4	EN (APL3512A)	Enable Input. Pull this pin to high to enable the device and pull this pin to low to disable device. The EN pin cannot be left floating.
			ENB (APL3512B)	Enable Input. Pull this pin to high to disable the device and pull this pin to low to enable device. The ENB pin cannot be left floating.
4	2	2	SS	Soft-Start Control Pin. Connect a capacitor to GND to control the soft-tart rate. If the SS pin is left floating or tied to V_{IN} the soft-tart time is 2ms when V_{IN}=5V.
5	1	1	VIN	Power Supply Input. Connect this pin to external DC supply.
-	4, 5, 7	5	NC	Internally not connected.

Block Diagram



Typical Application Circuit



Function Description

VIN Under-Voltage Lockout (UVLO)

The APL3512A/B power switch is built-in an under-voltage lockout circuit to keep the output shut off until internal circuitry is operating properly. The UVLO circuit has hysteresis and a de-glitch feature so that it will typically ignore undershoot transients on the input. When input voltage exceeds the UVLO threshold, the output voltage starts a soft-start to reduce the inrush current.

Power Switch

The power switch is an N-channel MOSFET with a low $R_{DS(ON)}$. The internal power MOSFET does not have the body diode. When IC is off, the MOSFET prevents a current flowing from the VOUT back to VIN and VIN to VOUT.

Current-Limit Protection

The APL3512A/B power switch provides the current-limit protection function. During current-limit, the devices limit output current at current-limit threshold. For reliable operation, the device should not be operated in current-limit for extended period.

Short-Circuit Protection

When the output voltage drops below V_{IN}-1.5V, which is caused by the over load or short-circuit, the devices limit the output current down to a safe level. The short circuit current-limit is used to reduce the power dissipation during short-circuit condition. If the junction temperature is over the thermal shutdown temperature, the device will enter the thermal shutdown.

Soft-Start

The APLA3512A/B provides an adjustable soft-start circuitry to control rise rate of the output voltage and limit the current surge during start-up. The soft-start ramp-up rate is controlled by a capacitor from SS pin to the ground. Under a specific V_{IN} being applied to the APL3512A/B, the soft start time can be calculated by the following equation:

$$t_{SS} = 0.2 \times C_{SS} \times V_{IN}$$

where,

t_{SS} is soft-start time of V_{OUT} rising from 0 to 100%, of which unit is second.

C_{SS} is the value of the capacitor connected from SS pin to GND, of which unit is micro-Farad.

V_{IN} is the amplitude of input voltage applied to this device, of which unit is volt.

If the C_{SS} is not connected or SS pin is tied to V_{IN}, the soft-start time is 2ms when V_{IN}=5V.

Enable/Disable

Pull the ENB above 2V, or EN below 0.8V to disable the device and pull ENB pin below 0.8V or EN above 2V to enable the device. When the IC is disabled, the supply current is reduced to less than 1μA. The enable input is compatible with both TTL and CMOS logic levels. The EN/ENB pins cannot be left floating.

Over-Temperature Protection

When the junction temperature exceeds 140°C, the internal thermal sense circuit turns off the power FET and allows the device to cool down. When the device's junction temperature cools by 20°C, the internal thermal sense circuit will enable the device, resulting in a pulsed output during continuous thermal protection. Thermal protection is designed to protect the IC in the event of over-temperature conditions. For normal operation, the junction temperature cannot exceed T_J=+125°C.

Application Information

Input Capacitor

A 1µF ceramic bypass capacitor from V_{IN} to GND, located near the APL3512, is strongly recommended to suppress the ringing during short-circuit fault event. Without the bypass capacitor, the output short may cause sufficient ringing on the input (from supply lead inductance) to damage internal control circuitry.

Output Capacitor

A low-ESR 10µF MLCC, aluminum electrolytic or tantalum between VOUT and GND is strongly recommended to reduce the voltage droop during hot-attachment of downstream peripheral. Higher-value output capacitor is better when the output load is heavy. Additionally, bypassing the output with a 0.1µF ceramic capacitor improves the immunity of the device to short-circuit transients.

During soft-start process, the output bulk capacitor draws inrush current from V_{IN}. If the inrush current reaches foldback current-limit threshold, namely 0.8A, the output current will be clamped in 0.8A level. It will take longer to complete the soft-start process since the soft-start rate is controlled neither by internal soft-start nor by external soft-start circuitry. When the C_{OUT} meets the following formula, the soft-start will be controlled by foldback current-limiting:

$$C_{OUT} > (0.8 x t_{SS})/V_{IN}$$

Where,

t_{SS} is 1ms when SS is open or tied to V_{IN}, or obtained by the tss equation, described in the paragraph of Soft-Start in Functional Description section when C_{SS} is used.

If the soft-start rate is controlled by the foldback current-limiting, the soft-start time can be got by the following equation:

$$t_{SS\_Foldback} = (C_{OUT} \times V_{IN})/0.8$$

Soft-Start Capacitor

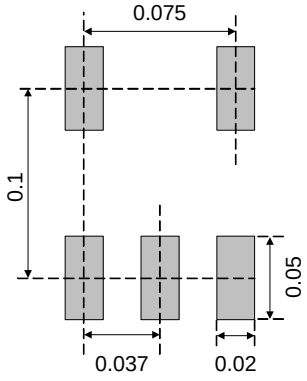
The APL3512 has a built-in adjustable soft-start control for user to set an optimum soft-start time for the application. The soft-start time can be calculated by the equation, described in the paragraph of Soft-Start in Functional Description section. Please note that there are minimum and maximum limitations of soft-start capacitor. If the value of soft-start capacitor is less than the minimum limitation or higher than the maximum limitation (please refer to the Recommended Operating Conditions), the soft-start time will become internally controlled as if there is no C_{SS}, t_{SS}=2ms when V_{IN}=5V, for example. If a soft-start capacitor is used, please make sure the C_{SS} is in the recommeded operating range.

Layout Consideration

The PCB layout should be carefully performed to maximize thermal dissipation and to minimize voltage drop, droop and EMI. The following guidelines must be considered:

1. Please place the input capacitors near the VIN pin as close as possible.
2. Output decoupling capacitors for load must be placed near the load as close as possible for decoupling high-frequency ripples.
3. Locate APL3512 and output capacitors near the load to reduce parasitic resistance and inductance for excellent load transient performance.
4. The negative pins of the input and output capacitors and the GND pin must be connected to the ground plane of the load.
5. Keep V_{IN} and V_{OUT} traces as wide and short as possible.

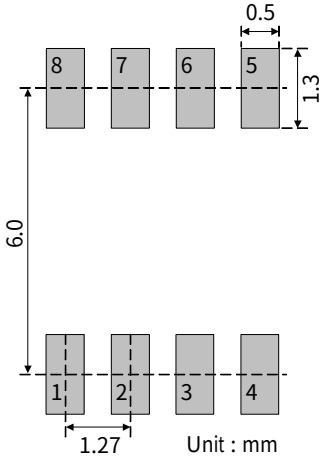
Recommended Minimum Footprint



Unit : Inch

SOT-23-5

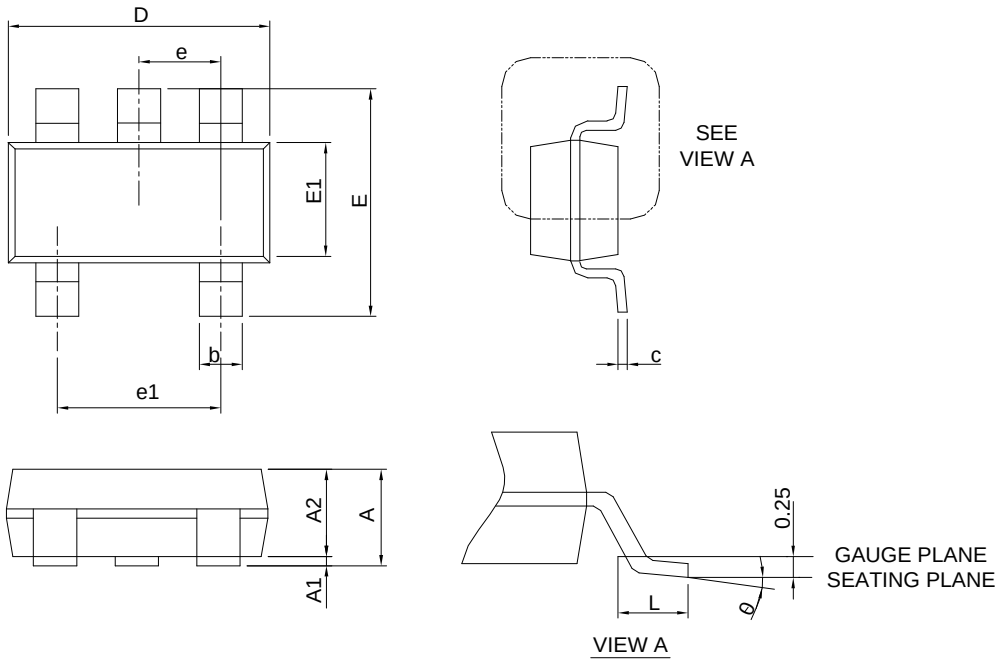
Recommended Minimum Footprint



SOP-8

Package Information

SOT-23-5

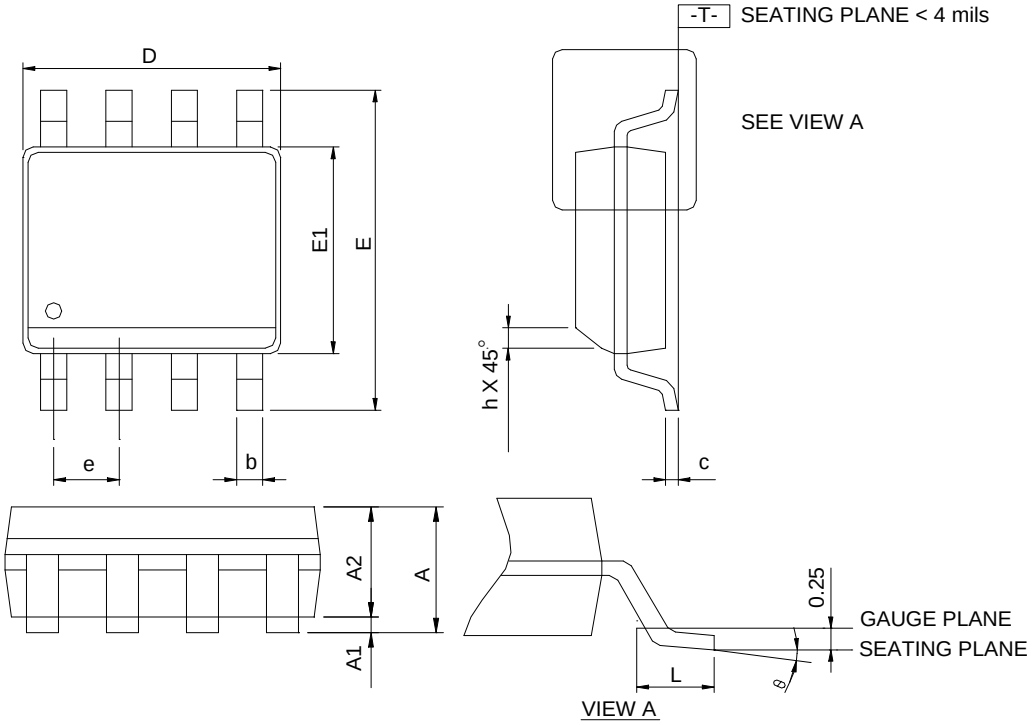


SYMBOL	SOT-23-5			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.45		0.057
A1	0.00	0.15	0.000	0.006
A2	0.90	1.30	0.035	0.051
b	0.30	0.50	0.012	0.020
c	0.08	0.22	0.003	0.009
D	2.70	3.10	0.106	0.122
E	2.60	3.00	0.102	0.118
E1	1.40	1.80	0.055	0.071
e	0.95 BSC		0.037 BSC	
e1	1.90 BSC		0.075 BSC	
L	0.30	0.60	0.012	0.024
θ	0°	8°	0°	8°

Note : 1. Follow JEDEC TO-178 AA.
2. Dimension D and E1 do not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 10 mil per side.

Package Information

SOP-8

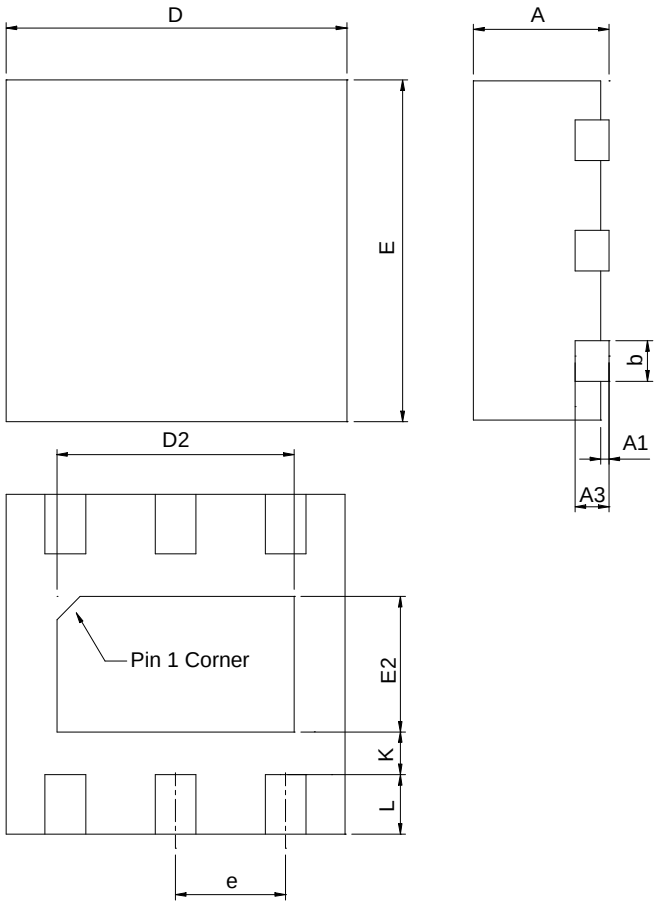


SYMBOL	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.10	0.25	0.004	0.010
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

Note: 1. Follow JEDEC MS-012 AA.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension “E” does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Package Information

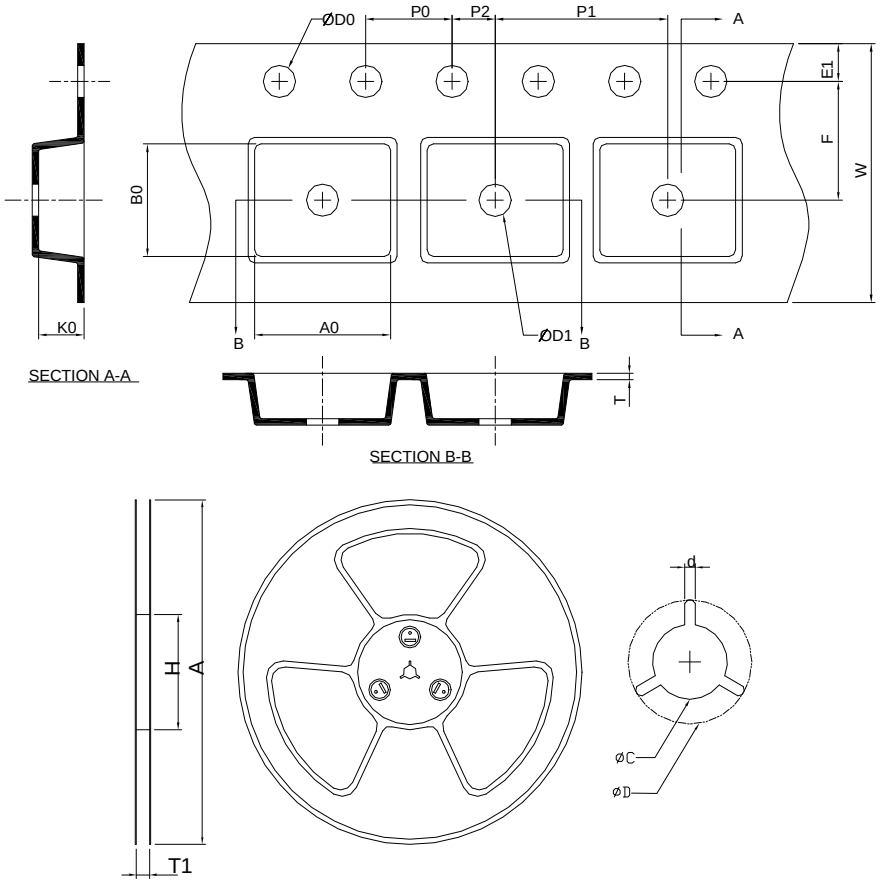
TDFN2x2-6



SYMBOL	TDFN2x2-6			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	1.90	2.10	0.075	0.083
D2	1.00	1.60	0.039	0.063
E	1.90	2.10	0.075	0.083
E2	0.60	1.00	0.024	0.039
e	0.65 BSC		0.026 BSC	
L	0.30	0.45	0.012	0.018
K	0.20		0.008	

Note : 1. Followed from JEDEC MO-229 WCCC.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
SOT-23-5	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.0 MIN.	0.6+0.00 -0.40	3.20±0.20	3.10±0.20	1.50±0.20
Application	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
SOP-8	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	5.20±0.20	2.10±0.20
Application	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
TDFN2x2-6	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	2.35±0.20	2.35±0.20	1.30±0.20

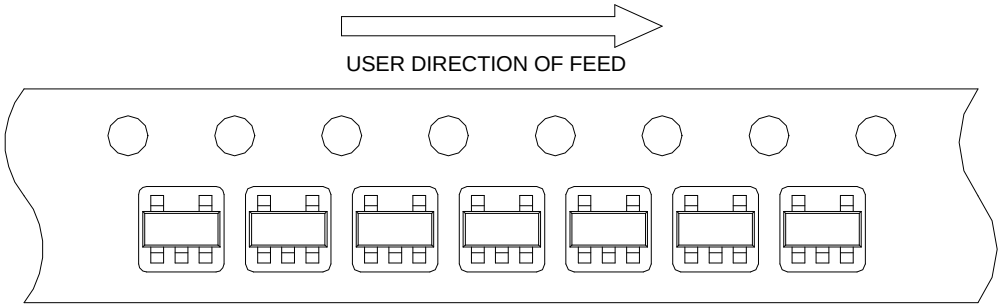
(mm)

Devices Per Unit

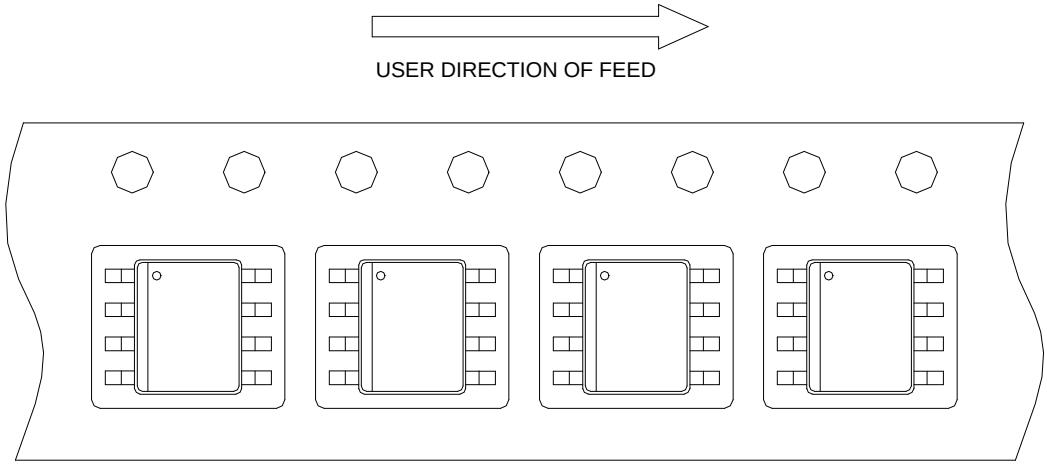
Package Type	Unit	Quantity
SOT-23-5	Tape & Reel	3000
SOP-8	Tape & Reel	2500
TQFN2x2-6	Tape & Reel	3000

Taping Direction Information

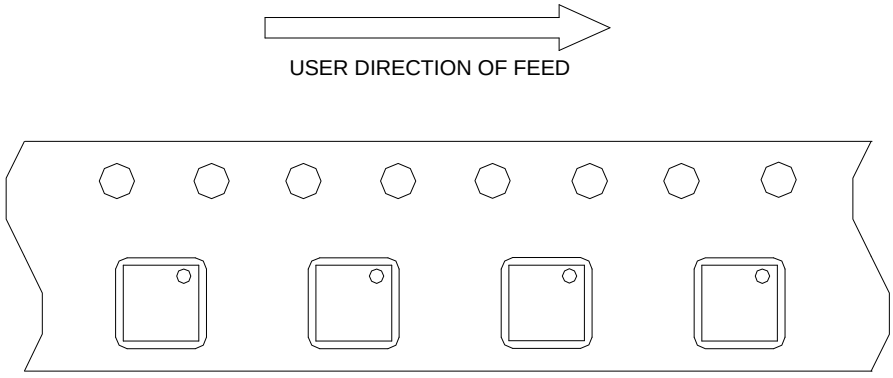
SOT-23-5



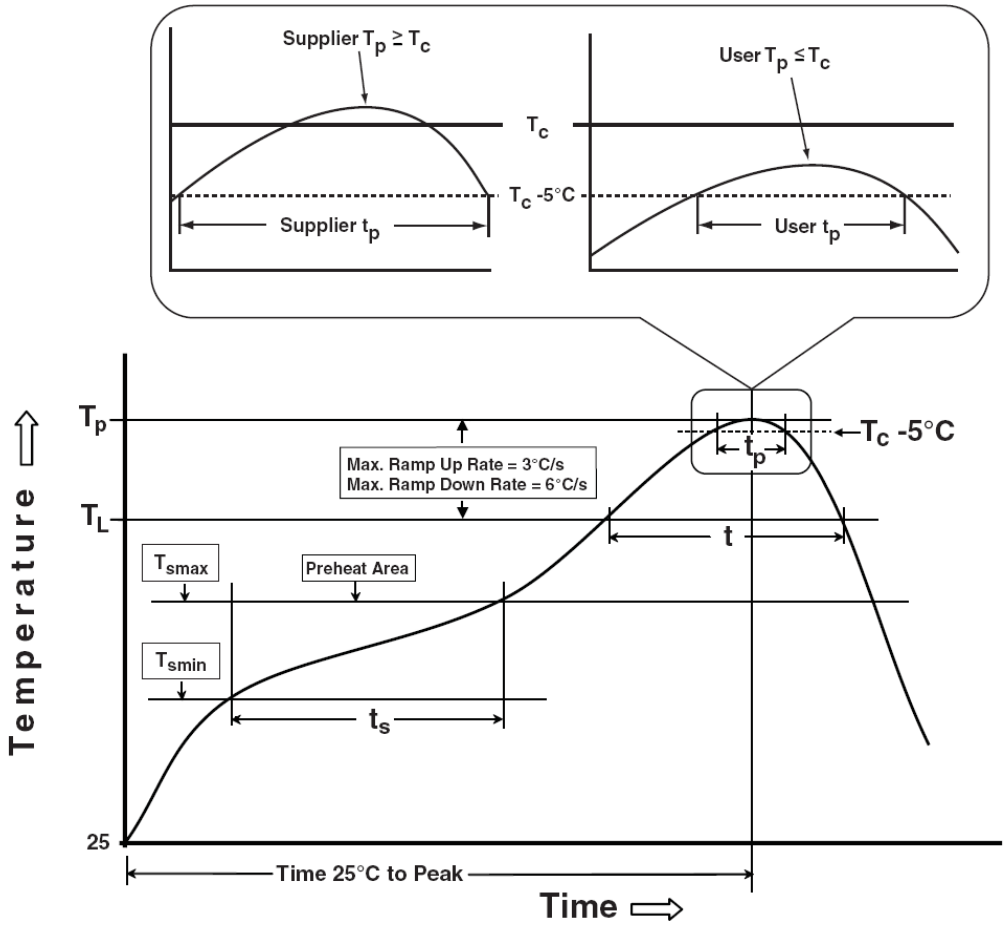
SOP-8



TDFN2x2-6



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Classification Reflow Profiles (Cont.)

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

Customer Service

Anpec Electronics Corp.
Head Office :
No.6, Dusing 1st Road, SBIP,
Hsin-Chu, Taiwan, R.O.C.
Tel : 886-3-5642000
Fax : 886-3-5642050

Taipei Branch :
2F, No. 11, Lane 218, Sec 2 Jhongsing Rd.,
Sindian City, Taipei County 23146, Taiwan
Tel : 886-2-2910-3838
Fax : 886-2-2917-3838