High-Performance Notebook PWM Controller

Features

- **Adjustable Output Voltage from +0.6V to +3.3V**
  - **0.6V Reference Voltage**
  - **±1% Accuracy Over Temperature**
- **Operates from an Input Battery Voltage Range of +3V to +25V**
- **Wide Output Load Range from 0A to 25A**
- **Power-On-Reset Monitoring on VCC Pin**
- **Excellent Line and Load Transient Response**
- **PFM Mode for Increased Light Load Efficiency**
- **Programmable PWM Frequency from 200kHz to 600kHz**
- **Integrated MOSFET Drivers and Bootstrap Diode**
- **Internal Integrated Soft-Start and Soft-Stop**
- **Selectable Forced PWM or Automatic PFM/PWM Mode (only for QFN4x4-16A and TQFN3x3-16 Packages)**
- **Power Good Monitoring**
- **Fault Identification by PGOOD Pull-Down Resistance**
- **70% Under-Voltage Protection (UVP)**
- **124% Over-Voltage Protection (OVP)**
- **Adjustable Over-Current Protection (OCP)**
  - **Sensing Low-Side MOSFET's Current**
- **Over-Temperature Protection (OTP)**
- **SSOP-16, Compact 4mmx4mm QFN-16 (QFN4x4-16A), and TQFN3x3-16 Packages**
- **Lead Free and Green Devices Available (RoHS Compliant)**

Applications

- **PCI Express Graphical Processing Unit**
- **Notebook Adapter**
- **Auxiliary Power Rail**
- **VRM**

General Description

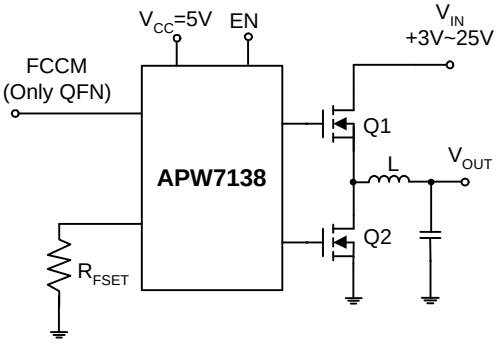
The APW7138 is a single-phase, constant-on-time, and synchronous PWM controller which drives N-channel MOSFETs. The APW7138 steps down high voltage of a battery to generate low-voltage chipset or RAM supplies in notebook computers.

The APW7138 provides excellent transient response and accurate DC voltage output in either PFM or PWM Mode. In Pulse Frequency Modulation (PFM) Mode, the APW7138 provides very high efficiency over light load with loading-modulated switching frequencies. When the inductor current is continuous, the operation automatically enters PWM mode with relatively constant switching frequency. For QFN4x4-16A and TQFN3x3-16 packages, the Forced-PWM Mode works nearly at constant frequency for low-noise requirements.

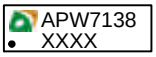
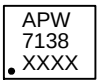
The APW7138 is equipped with accurate over-current, output under-voltage, and over-voltage protections perfect for NB application. A Power-On-Reset function monitors the voltage on VCC pin to prevent errorneous operation during power-on. The APW7138 has a digital soft-start and soft-stop. The internal integrated soft-start ramps up the output voltage with controlled slew rate to reduce the start-up current. The digital soft-stop function actively discharges the output capacitors with controlled reverse inductor current.

The APW7138 is available in SSOP-16, QFN4x4-16A, and TQFN3x3-16 packages.

Simpilfied Application Circuit

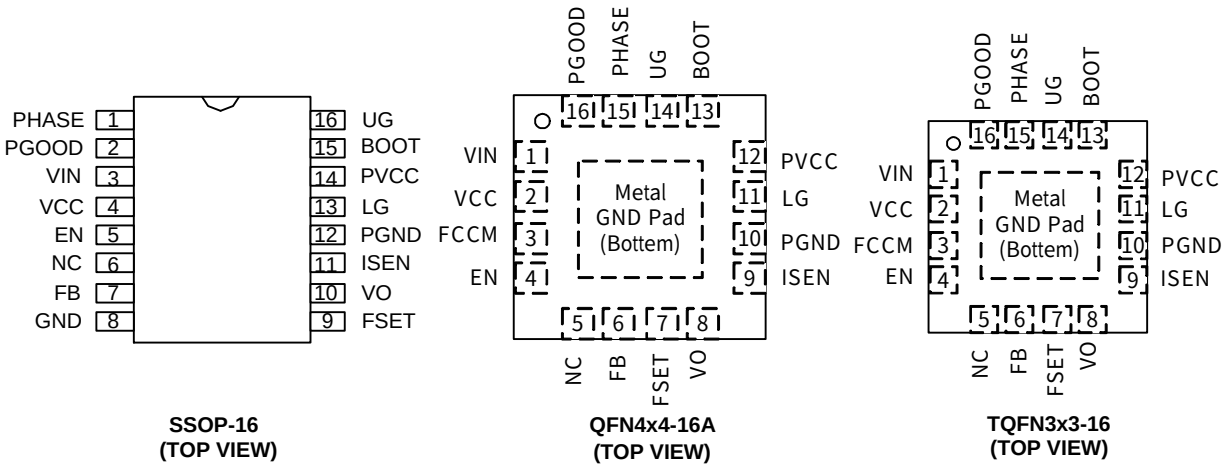


Ordering and Marking Information

APW7138 □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code N : SSOP-16 QA: QFN4x4-16A QB: TQFN3x3-16 Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APW7138 N : 	XXXXX - Date Code
APW7138 QA : 	XXXXX - Date Code
APW7138 QB : 	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Pin Configuration



SSOP-16 (TOP VIEW)

QFN4x4-16A (TOP VIEW)

TQFN3x3-16 (TOP VIEW)

= Thermal Pad (connected to GND plane for better heat dissipation)

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{CC}	VCC Supply Voltage (VCC to GND)	-0.3 ~ 7	V
V_{PVCC}	PVCC Supply Voltage (PVCC to GND)	-0.3 ~ 7	V
V_{IN}	Input Power Voltage (VIN to GND)	-0.3 ~28	V
V_{BOOT}	BOOT Supply Voltage (BOOT to PHASE)	-0.3 ~ 7	V
$V_{BOOT-GND}$	BOOT Supply Voltage (BOOT to GND)	-0.3 ~ 35	V
$V_{UG-PHASE}$	UG Voltage (UG to PHASE) <400ns pulse width >400ns pulse width	 -5 ~ V_{BOOT}+0.3 -0.3 ~ V_{BOOT}+0.3	V
$V_{LG-PGND}$	LG Voltage (LG to PGND) <400ns pulse width >400ns pulse width	 -5 ~ V_{CC}+0.3 -0.3 ~ V_{CC}+0.3	V
V_{PHASE}	PHASE Voltage (PHASE to GND) <400ns pulse width >400ns pulse width	 -5 ~ 35 -2 ~ 28	V
V_{PGND}	PGND to GND Voltage	-0.3 ~ 0.3	V
V_{ISEN}	ISEN Supply Voltage (ISEN to GND)	-0.3 ~ 28	V
V_{PGOOD}	PGOOD Supply Voltage (PGOOD to GND)	-0.3 ~ 7	V
$V_{I/O}$	All Other Pins (VO, FB, EN, FCCM and FSET to GND)	-0.3 ~ V_{CC}+0.3	V
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics (Note 2)

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Thermal Resistance -Junction to Ambient SSOP-16 QFN4x4-16A TQFN3x3-16	 105 40 55	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of package is soldered directly on the PCB.

Recommended Operating Conditions

Symbol	Parameter	Range	Unit
V_{CC},V_{PVCC}	VCC, PVCC Supply Voltage	4.5 ~ 5.5	V
V_{OUT}	Converter Output Voltage	0.6 ~ 3.3	V
V_{IN}	Converter Input Voltage	3 ~ 25	V
I_{OUT}	Converter Output Current	0 ~ 25	A
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Electrical Characteristics

Refer to the typical application circuits. These specifications apply over V_{CC}=5V, V_{IN}=7~25V and T_A= -40 ~ 85 °C, unless otherwise specified. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW7138			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
I_{VCC}	VCC Input Bias Current	V_{EN}=5V, V_{FB}=0.65V, V_{IN}=7V to 25V	-	1.7	2.5	mA
	VCC Shutdown Current	V_{EN}=GND, V_{CC}=5V	-	0.1	1.0	µA
	PVCC Shutdown Current	V_{EN}=GND, V_{PVCC}=5V	-	0.1	1.0	µA
I_{VIN}	VIN Input Bias Current	V_{EN}=5V, V_{IN}=7V	-	6.5	10	µA
		V_{EN}=5V, V_{IN}=25V	-	25	35	µA
	VIN Shutdown Current	V_{EN}=GND, V_{IN}=25V	-	0.1	1.0	µA
POWER-ON-RESET (POR)						
V_{VCC_THR}	Rising VCC POR Threshold Voltage		4.1	4.2	4.3	V
	VCC POR Hysteresis		-	0.2	-	V
VOLTAGE REGULATION						
V_{REF}	Reference Voltage		-	0.6	-	V
	Regulation Accuracy	Over Temperature	-1	-	+1	%
SWITCHING FREQUENCY						
F_{SW}	Frequency Range	DC Output Current	200	-	600	kHz
	Frequency-Set-Accuracy	R_{FSET}=44.5kΩ	270	300	330	kHz
PWM CONVERTERS						
	UG Minimum-Off Time	Over temperature and V_{CC}	-	550	-	ns
	VO Pin Input Impedance	V_{OUT} = 3.3V	-	134	-	kΩ
I_{FB}	FB Input Bias Current	V_{FB}=0.6V	-0.5	-	+0.5	µA
T_{SS}	Soft-Start Time	V_{EN} High to V_{OUT} Regulation (Note3)	-	1.5	-	ms
	Zero-Crossing Voltage Threshold		-5	0	+5	mV
	On-Time Ratio of PFM to PWM		-	1.5	-	-
POWER GOOD						
R_{PG_SS}	PGOOD Pull-Down Impedance	I_{PGOOD}=5mA Sink (Soft-Start)	75	95	125	Ω
R_{PG_UV}		I_{PGOOD}=5mA Sink (Under-Voltage)	75	95	125	Ω
R_{PG_OV}		I_{PGOOD}=5mA Sink (Over-Voltage)	50	63	85	Ω
R_{PG_OC}		I_{PGOOD}=5mA Sink (Over-Current)	25	32	45	Ω
I_{PGOOD}	PGOOD Leakage Current	V_{PGOOD}=5V	-	0.1	1.0	µA
	PGOOD Maximum Sink Current		-	5.0	-	mA
	PGOOD Soft-Start Delay	V_{EN} High to V_{PGOOD} High	2.20	2.75	3.30	ms
MOSFET GATE DRIVERS						
	UG Pull-Up Resistance	V_{BOOT}=5V, I_{UG}=0.1A	-	1	2	Ω
	UG Source Current	V_{BOOT}=5V, V_{UG}-V_{PHASE}=2.5V	-	2	-	A
	UG Sink Resistance	V_{BOOT}=5V, I_{UG}=0.1A	-	1	2	Ω
	UG Sink Current	V_{BOOT}=5V, V_{UG}-V_{PHASE}=2.5V	-	2	-	A

Electrical Characteristics (Cont.)

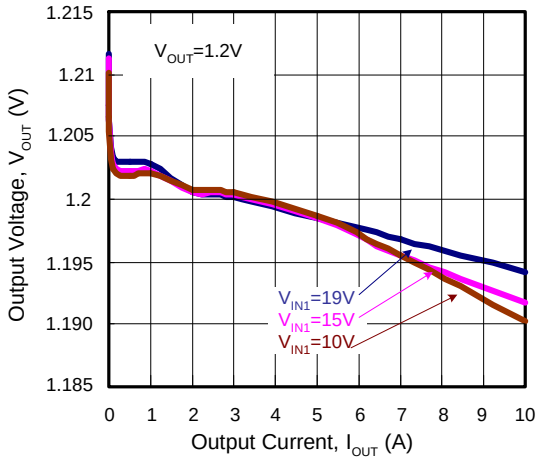
Refer to the typical application circuits. These specifications apply over V_{CC}=5V, V_{IN}=7~25V and T_A= -40 ~ 85 °C, unless otherwise specified. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW7138			Unit
			Min.	Typ.	Max.	
MOSFET GATE DRIVERS (CONT.)						
	LG Pull-Up Resistance	V_{PVCC}=5V, I_{LG}=0.1A	-	1	2	Ω
	LG Source Current	V_{PVCC}=5V, V_{LG}-V_{PGND}=2.5V	-	2	-	A
	LG Sink Resistance	V_{PVCC}=5V, I_{LG}=0.1A	-	0.6	1.2	Ω
	LG Sink Current	V_{PVCC}=5V, V_{LG}-V_{PGND}=2.5V	-	3	-	A
T_D	Dead Time		-	20	-	ns
BOOTSTRAP DIODE						
V_F	Forward Voltage	V_{PVCC}-$V_{BOOT-GND}$=5V, I_F=2mA	-	0.8	-	V
I_R	Reverse Leakage	V_R=25V	-	0.2	-	µA
CONTROL INPUTS						
$V_{FCCMTHR}$	FCCM High Threshold	Only for QFN4x4-16A and TQFN3x3-16 packages	2.0	-	-	V
$V_{FCCMTHF}$	FCCM Low Threshold		-	-	0.8	V
V_{ENR}	EN High Threshold		2.0	-	-	V
V_{ENF}	EN Low Threshold		-	-	0.8	V
	EN Leakage	V_{EN}=5V	-	0.1	1.0	µA
PROTECTION						
I_{OC}	ISEN OCP Threshold	I_{SEN} Sourcing	20	26	30	µA
I_{SC}	ISEN Short-Circuit Threshold	I_{SEN} Sourcing	-	50	-	µA
V_{UV}	UVP Threshold		65	70	75	%
	UVP Debounce Interval		-	2	-	µs
V_{OVR}	OVP Rising Threshold		119	124	129	%
V_{OVF}	OVP Falling Threshold		99	104	109	%
	OVP Debounce Interval		-	2	-	µs
T_{OTR}	OTP Rising Threshold (Note 3)		-	150	-	°C
	OTP Hysteresis (Note 3)		-	25	-	°C

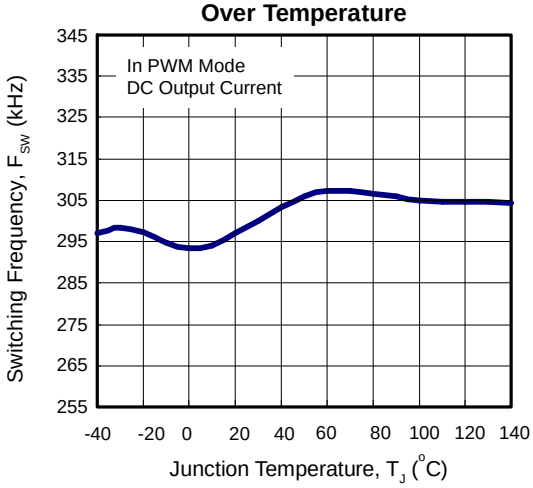
Note 3: Guaranteed by design.

Typical Operating Characteristics

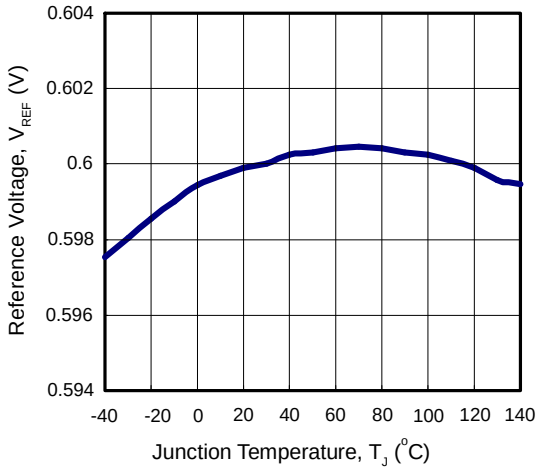
Output Voltage vs. Output Current



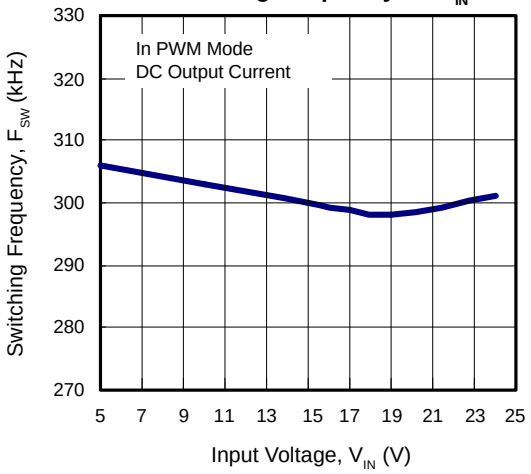
Switching Frequency (300kHz) Over Temperature



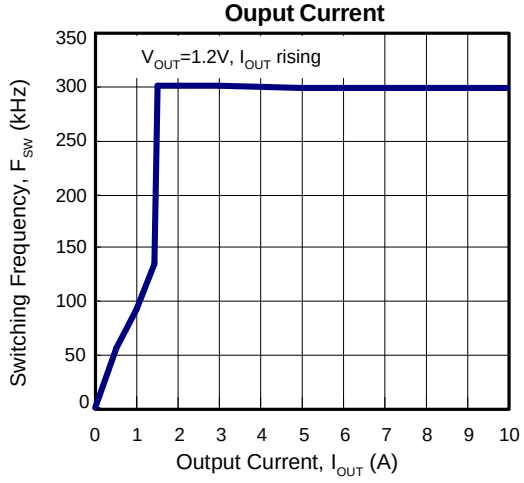
Reference Voltage Accuracy Over Temperature



Switching Frequency vs. V_{IN}

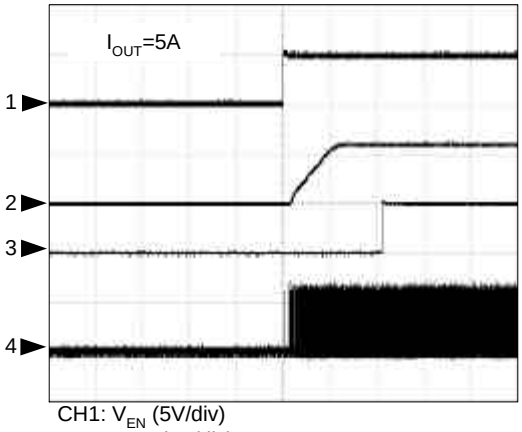


Switching Frequency vs. Ouput Current



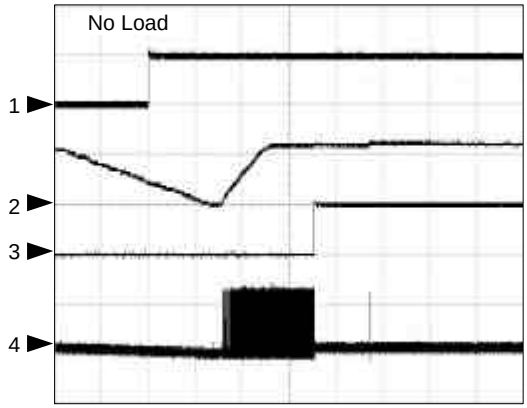
Operating Waveforms

Enable at Zero Initial Voltage of V_{OUT}



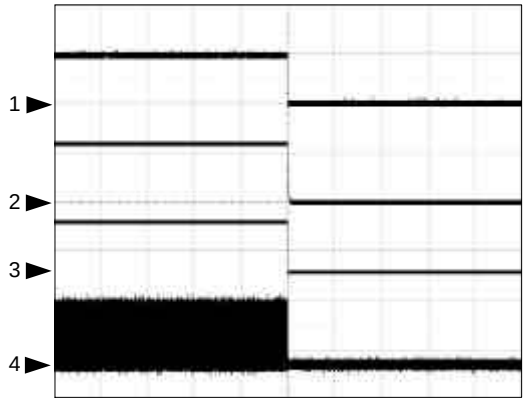
CH1: V_{EN} (5V/div)
CH2: V_{OUT} (1V/div)
CH3: V_{PGOOD} (5V/div)
CH4: V_{PHASE} (10V/div)
Time: 2ms/div

Enable Before End of Soft-Stop



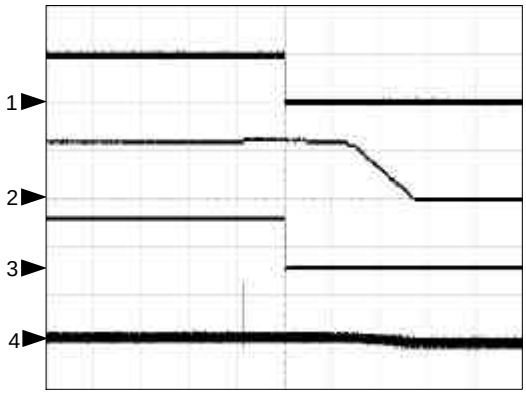
CH1: V_{EN} (5V/div)
CH2: V_{OUT} (1V/div)
CH3: V_{PGOOD} (5V/div)
CH4: V_{PHASE} (10V/div)
Time: 2ms/div

Shutdown at I_{OUT}=5A



CH1: V_{EN} (5V/div)
CH2: V_{OUT} (1V/div)
CH3: V_{PGOOD} (5V/div)
CH4: V_{PHASE} (10V/div)
Time: 5ms/div

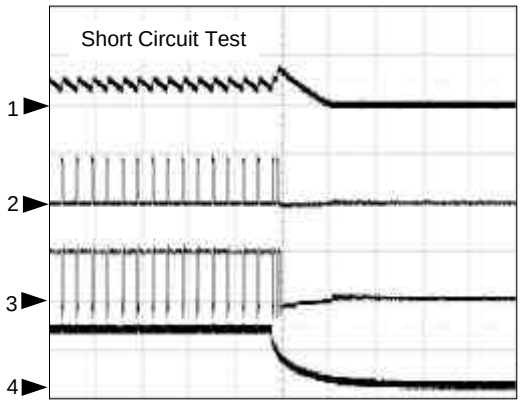
Shutdown with Soft-Stop at No Load



CH1: V_{EN} (5V/div)
CH2: V_{OUT} (1V/div)
CH3: V_{PGOOD} (5V/div)
CH4: V_{PHASE} (10V/div)
Time: 5ms/div

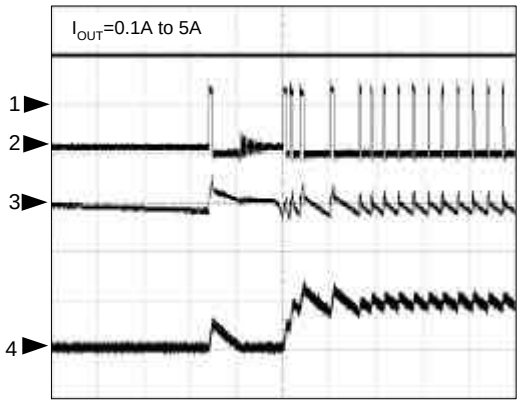
Operating Waveforms (Cont.)

Under-Voltage Protection



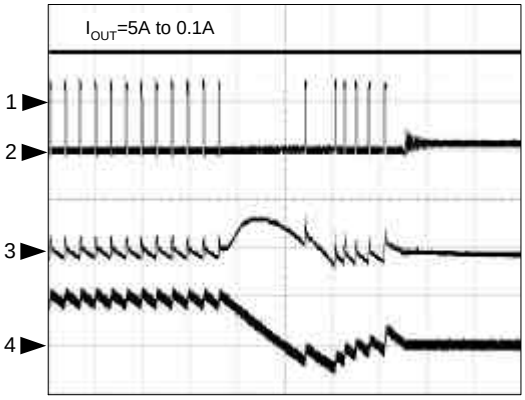
CH1: I_L (5A/div)
CH2: V_{UG} (20V/div)
CH3: V_{LG} (5V/div)
CH4: V_{OUT} (1V/div)
Time: 10µs/div

Mode Transient From PFM to PWM



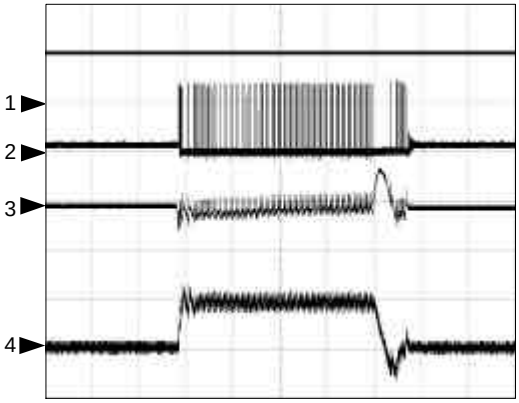
CH1: V_{PGOOD} (5V/div)
CH2: V_{PHASE} (10V/div)
CH3: V_{OUT} (AC, 100mV/div)
CH4: I_L (5A/div)
Time: 10µs/div

Mode Transient From PWM to PFM



CH1: V_{PGOOD} (5V/div)
CH2: V_{PHASE} (10V/div)
CH3: V_{OUT} (AC, 100mV/div)
CH4: I_L (5A/div)
Time: 10µs/div

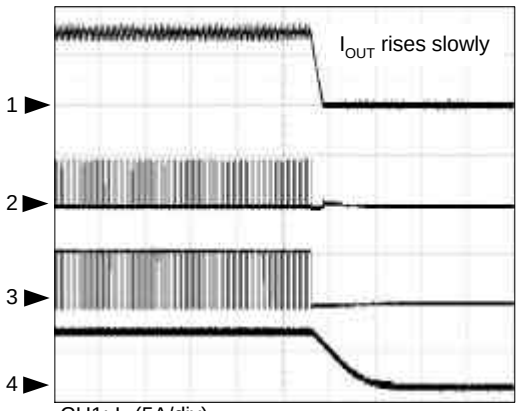
Load Transient
0A->5A->0A



CH1: V_{PGOOD} (5V/div)
CH2: V_{PHASE} (10V/div)
CH3: V_{OUT} (AC, 100mV/div)
CH4: I_L (5A/div)
Time: 50µs/div

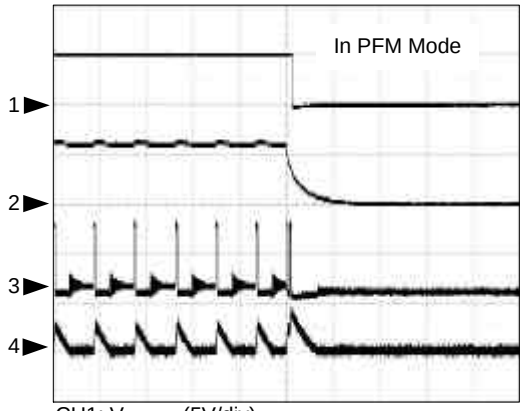
Operating Waveforms (Cont.)

Over-Current Protection



CH1: I_L (5A/div)
CH2: V_{UG} (20V/div)
CH3: V_{LG} (5V/div)
CH4: V_{OUT} (1V/div)
Time: 50µs/div

Short Circuit Test

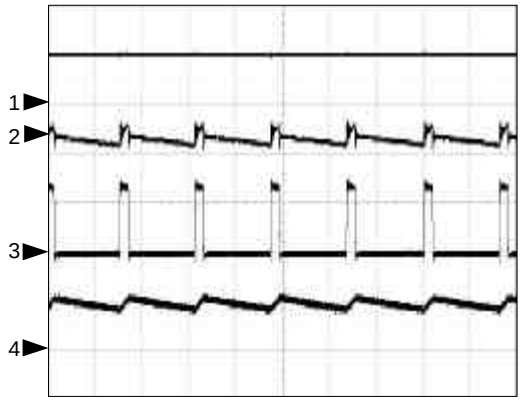


CH1: V_{PGOOD} (5V/div)
CH2: V_{OUT} (1V/div)
CH3: V_{PHASE} (10V/div)
CH4: I_L (5A/div)
Time: 20µs/div

Operating at Light Load of 100mA

CH1: V_{PGOOD} (5V/div)
CH2: V_{OUT1} (AC, 100mV/div)
CH3: V_{PHASE} (10V/div)
CH4: I_L (2A/div)
Time: 20us/div

Operating at Heavy Load of 5A

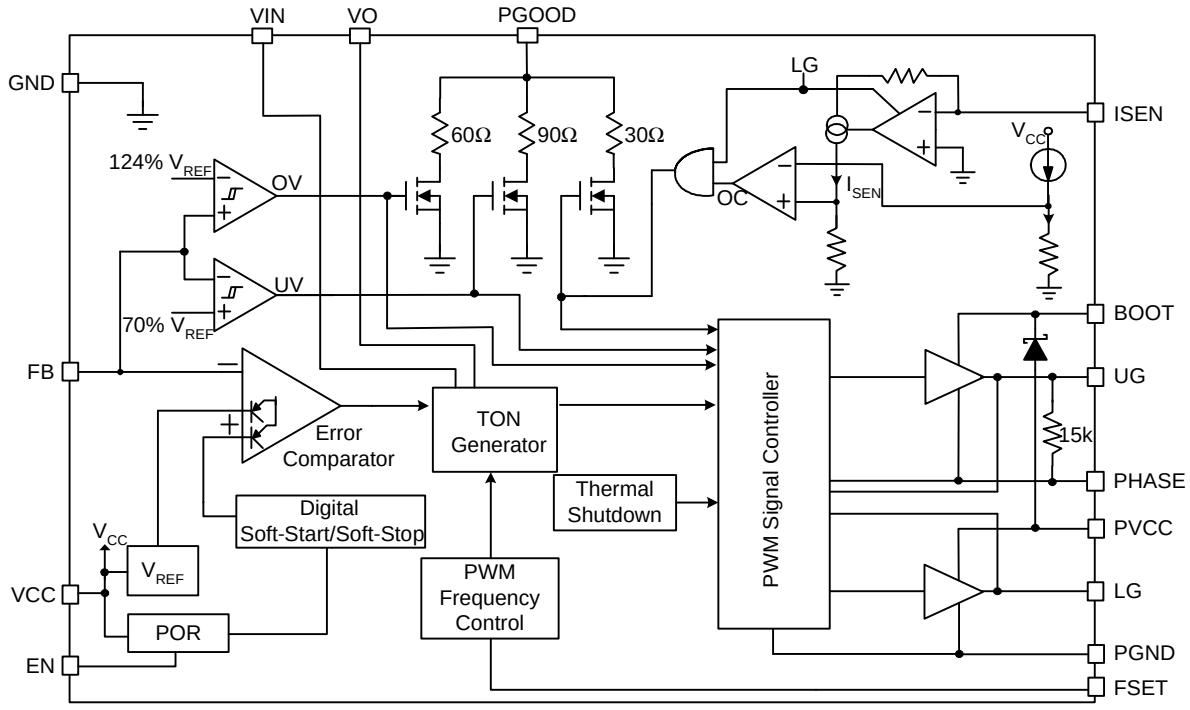


CH1: V_{PGOOD} (5V/div)
CH2: V_{OUT1} (AC, 100mV/div)
CH3: V_{PHASE} (10V/div)
CH4: I_L (5A/div)
Time: 2µs/div

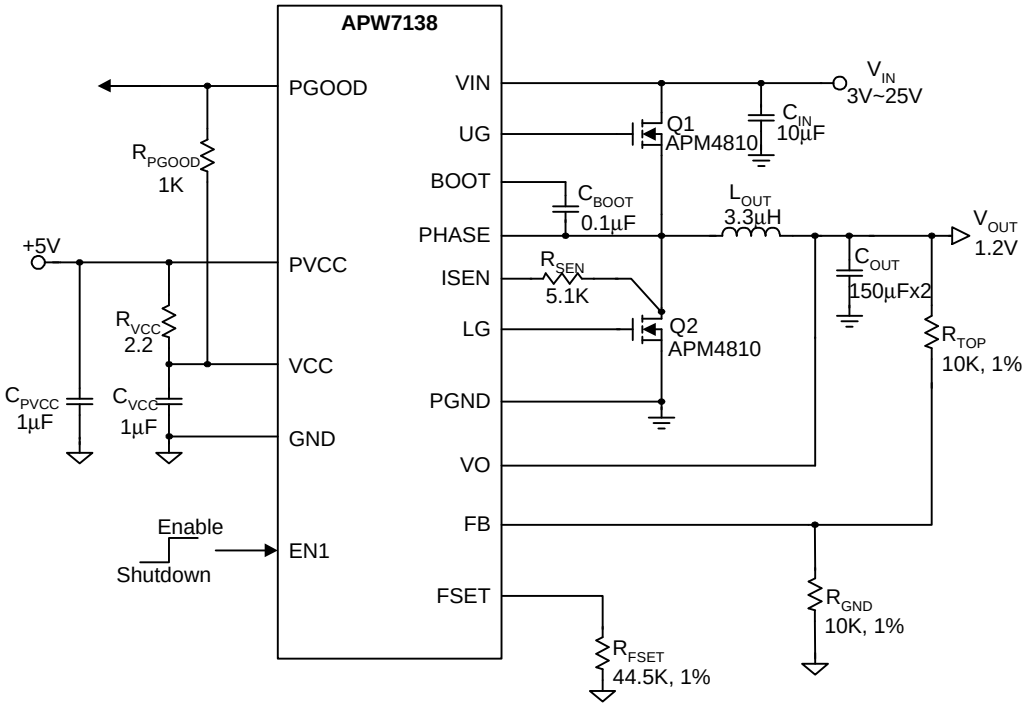
Pin Description

PIN			NAME	FUNCTION
NO.				
SSOP-16	QFN4x4-16A	TQFN3x3-16		
1	15	15	PHASE	Junction point of the high-side MOSFET Source, output filter inductor and the low-side MOSFET Drain. Connect this pin to the Source of the high-side MOSFET. PHASE serves as the lower supply rail for the UG high-side gate driver.
2	16	16	PGOOD	The PGOOD pin is an open-drain output that indicates when the converter is able to supply regulated voltage. Connect the PGOOD pin to +5V through a pull-up resistor. The PGOOD pin has three distinct pull-down impedances that correspond to an OVP (63Ω), OCP (32Ω), UVP (95Ω), and soft-start (95Ω).
3	1	1	VIN	Battery voltage input pin. Connect this pin to the drain of the high-side MOSFET.
4	2	2	VCC	Supply voltage input pin for control circuitry. Connect +5V from the VCC pin to the GND pin. Decoupling at least 1μF of a MLCC capacitor from the VCC pin to the GND pin.
-	3	3	FCCM	Selection pin for PWM controller to operate in either forced PWM or automatic PWM/PFM mode. Force PWM mode is enable when FCCM pin is pulled above the rising threshold voltage $V_{FCCMTHR}$, and force PWM is disabled when the FCCM pin is pulled below the falling threshold voltage $V_{FCCMTHF}$.
5	4	4	EN	Enable pin of the PWM controller. The PWM is enabled when EN=1. When the EN=0, the PWM is shutdown and only low leakage current is taken from V_{CC} and V_{IN}.
6	5	5	NC	No Connection.
7	6	6	FB	Output voltage feedback pin. This pin is connected to the resistive divider that set the desired output voltage. The UVP and OVP circuits detect this signal to report output voltage status.
8	Thermal Pad	Thermal Pad	GND	Signal ground for the IC.
9	7	7	FSET	This pin is allowed to adjust the switching frequency. Connect a resistor R_{FSET} from the FSET pin to the GND pin.
10	8	8	VO	The VO pin makes a direct measurement of the converter output voltage. The VO pin should be connected to the top feedback resistor at the converter output.
11	9	9	ISEN	Current sense pin. This pin is used to monitor the voltage drop across the Drain and Source of the low-side MOSFET for over-current protection. For precise current detection this input can be connected to the optional current sense resistor placed in series with the Source of the low-side MOSFET.
12	10	10	PGND	Power ground of the LG low-side MOSFET driver. Connect the pin to the Source of the low-side MOSFET.
13	11	11	LG	Output of the low-side MOSFET driver. Connect this pin to Gate of the low-side MOSFET. Swings from PGND to VCC.
14	12	12	PVCC	Supply voltage input pin for the LG low-side MOSFET gate driver. Connect +5V from the PVCC pin to the PGND pin. Decoupling at least 1μF of a MLCC capacitor from the PVCC pin to the PGND pin.
15	13	13	BOOT	Supply Input for the UG Gate Driver and an internal level-shift circuit. Connect to an external capacitor and diode to create a boosted voltage suitable to drive a logic-level N-channel MOSFET.
16	14	14	UG	Output of the high-side MOSFET driver. Connect this pin to Gate of the high-side MOSFET.

Block Diagram



Typical Application Circuit



Function Description

Constant-On-Time PWM Controller with Input Feed-Forward

The constant-on-time control architecture is a pseudo-fixed frequency with input voltage feed-forward. This architecture relies on the output filter capacitor's effective series resistance (ESR) to act as a current-sense resistor, so the output ripple voltage provides the PWM ramp signal. In PFM operation, the high-side switch on-time controlled by the on-time generator is determined solely by a one-shot whose pulse width is inversely proportional to input voltage and directly proportional to output voltage. In PWM operation, the high-side switch on-time is determined by a switching frequency control circuit in the on-time generator block. The switching frequency control circuit senses the switching frequency of the high-side switch and keeps regulating it at a constant frequency in PWM mode. This design improves the frequency variation to is more outstanding than a conventional constant-on-time controller which has large switching frequency variation over input voltage, output current, and temperature. Both in PFM and PWM, the on-time generator, which senses input voltage on VIN pin, provides very fast on-time response to input line transients.

Another one-shot sets a minimum off-time (typical: 550ns). The on-time one-shot is triggered if the error comparator is high, the low-side switch current is below the over-current threshold, and the minimum off-time one-shot has timed out.

Pulse-Frequency Modulation (PFM) Mode

In PFM mode, an automatic switchover to pulse-frequency modulation (PFM) takes place at light loads. This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current zero crossing. This mechanism causes the threshold between PFM and PWM operations to coincide with the boundary between continuous and discontinuous inductor-current operation (also known as the critical conduction point). The on-time of PFM mode is designed as 1.5 time of the nominal on-time of PWM mode. The on-time of PFM is given by:

$$T_{ON-PFM} = \frac{1.5}{F_{SW}} \times \frac{V_{OUT}}{V_{IN}}$$

Where F_{SW} is the nominal switching frequency of the converter in PWM mode.

This design provides a hysteresis of converter output current to prevent wrong or repeatedly PFM/PWM handoff with constant output current. The load current at handoff from PFM to PWM mode is given by:

$$I_{LOAD(PFM\ to\ PWM)} = \frac{1}{2} \times \frac{V_{IN} - V_{OUT}}{L} \times T_{ON-PFM} = \frac{V_{IN} - V_{OUT}}{2L} \times \frac{1.5}{F_{SW}} \times \frac{V_{OUT}}{V_{IN}}$$

The load current at handoff from PWM to PFM mode is given by:

$$I_{LOAD(PWM\ to\ PFM)} = \frac{1}{2} \times \frac{V_{IN} - V_{OUT}}{L} \times T_{ON-PWM} = \frac{V_{IN} - V_{OUT}}{2L} \times \frac{1}{F_{SW}} \times \frac{V_{OUT}}{V_{IN}}$$

Therefore, the $I_{LOAD(PFM\ to\ PWM)}$ is 1.5 time of the $I_{LOAD(PWM\ to\ PFM)}$.

Forced-PWM Mode (Only for QFN4x4-16A and TQFN3x3-16 Packages)

The Forced-PWM mode disables the zero-crossing comparator which truncates the low-side switch on-time at the inductor current zero crossing. This causes the low-side gate-drive waveform to become the complement of the high-side gate-drive waveform. This in turn causes the inductor current to reverse at light loads while UG maintains a duty factor of V_{OUT}/V_{IN}. The benefit of Forced-PWM mode is to keep the switching frequency fairly constant. The Forced-PWM mode is the most useful for reducing audio frequency noise, improving load-transient response, and providing sink-current capability for dynamic output voltage adjustment.

Power-On-Reset

A Power-On-Reset (POR) function is designed to prevent wrong logic controls when the V_{CC} voltage is low. The POR function continually monitors the bias supply voltage on the VCC pin if at least one of the enable pins is set high. When the rising V_{CC} voltage reaches the rising POR voltage threshold (4.2V typical), the POR signal goes high and the chip initiates soft-start operations. When this voltage drop lower than 4V (typical), the POR disables the chip.

Function Description (Cont.)

Enable Control

When the EN pin is high (EN=1), the PWM is enabled and the soft-start is initiated. When EN is low (EN=0), the chip is in the shutdown mode and only low leakage current is taken from V_{CC} and V_{IN}. In shutdown mode, LG will be pulled high.

Soft-Start and Soft-Stop

The APW7138 integrates digital soft-start/soft-stop circuits to ramp up/down the output voltage of the converter to the programmed regulation setpoint at a predictable slew rate. The slew rate of output voltage is internally controlled to limit the inrush current through the output capacitors during soft-start process. The figure 1 shows soft-start sequence. When the EN pin is pulled above the rising EN threshold voltage, the device initiates a soft-start process to ramp up the output voltage. The soft-start interval is 1.5ms (typical) and independent of the UG switching frequency.

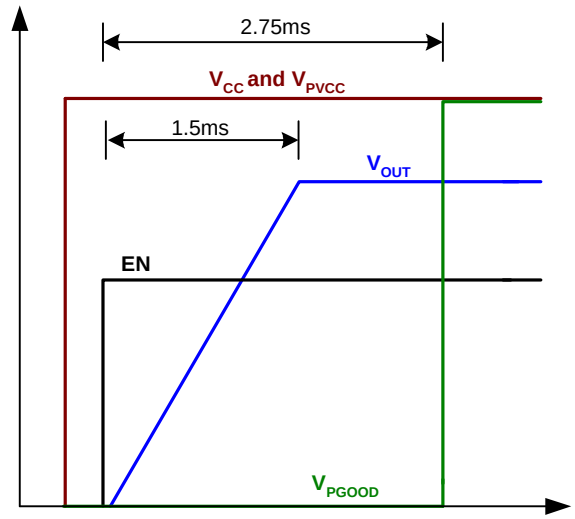


Figure 1. Soft-Start Sequence

During soft-start stage before the PGOOD pin is ready, the under-voltage protection is prohibited. The over-voltage and over-current protection functions are enabled. If the output capacitor has residue voltage before start-up, both low-side and high-side MOSFETs are in off-state until the internal digital soft start voltage equal the V_{FB} voltage, which ensures the output voltage starts from its existing voltage level.

In the event of under-voltage or EN shutdown, the chip enables the soft-stop function. At light load, the soft-stop gradually ramps down the output voltage, following the internal falling soft-stop voltage, by controlling the low-side MOSFET working as a sinking linear regulator. At heavy load, the soft-stop will not regulate the output voltage if the output voltage is below the falling soft-stop regulation voltage level. The soft-stop process, which takes about 3 times of the time from V_{EN} high to V_{PGOOD} high, is completed when the internal counter finishes counting. At this moment, the LG goes high level with latch. Cycling the EN signal or VCC power-on-reset signal can reset the latch.

Under-Voltage Protection (UVP)

In the process of operation, if a short-circuit occurs, the output voltage will drop quickly. The under-voltage continually monitors the V_{FB} voltage after soft-start process is completed. If a load step is strong enough to pull the output voltage lower than the under-voltage threshold, PGOOD pin will pull down to 95Ω immediately and start a soft-stop process to shut down the output. The under-voltage threshold is 70% of the normal output voltage. The under-voltage comparator has a built-in 2μs noise filter to prevent the chip from wrong UVP shutdown caused by noise. Toggling EN pin to low, or recycling VCC, will clear the latch and bring the chip back to operation.

Over-Voltage Protection (OVP)

The over-voltage function monitors the output voltage by FB pin. When the V_{FB} voltage increase over 124% of the reference voltage due to the high-side MOSFET failure or for other reasons, the over-voltage protection comparator is designed with a 2μs noise filter will force the low-side MOSFET gate driver to be high. This action actively pulls down the output voltage. When the OVP occurs, the PGOOD pin will pull down to 63Ω and latch-off the converter. This OVP scheme only clamps the voltage overshoot and doesn't invert the output voltage when otherwise activated with a continuously high output from low-side MOSFET driver. It's a common problem for OVP schemes with a latch. The OVP fault will remain latched until cycling the EN signal or VCC power-on-reset signal.

Function Description (Cont.)

Power Good Indicator

The APW7138 features an open-drain PGOOD output pin to indicate one of the IC's working statuses including soft-start, under-voltage fault, over-current fault, and over-voltage faule. The unique fault-identification capability can drastically reduce trouble-shooting time and effort.
The pull-down resistance of the PGOOD pin corresponds to the fault status of the controller. During soft-start or if an under voltage fault occurs, the PGOOD pull-down resistance is 95Ω, or 32Ω for an over current fault, or 63Ω for an over voltage fault. The pull-low resistance is undefined if V_{CC} is below the rising/falling POR threshold.

Over-Temperature Protection (OTP)

When the junction temperature increases above the rising threshold temperature TOTR, the IC will enter the over-temperature protection (OTP) state that suspends the PWM, which forces the LG and UG gate drivers to output low voltages. The status of the PGOOD pin does not change, nor does the converter latch-off. The thermal sensor allows the converters to start a start-up process and regulate the output voltage again after the junction temperature cools by 25°C. The OTP is designed with a 25°C hysteresis to lower the average T_J during continuous thermal overload conditions, which increases lifetime of the APW7138.

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

The over-current protection (OCP) is designed to resist the slow slew rate load current; on the other hand, the short-circuit protection (SCP) is used to take care of rapid shorted output. The setpoint for OCP and SCP is programmed with resistor R_{SEN} that is connected across the ISEN pin and drain of the low-side MOSFET. The SCP setpoint is internally set to twice the OCP setpoint.
The inductor current develops a negative voltage across the $R_{DS(ON)}$ of the low-side MOSFET that is sampled and held shortly before LG gate-driver output goes low. The OCP fault occurs if I_{SEN} rises above the OCP threshold current I_{OC} (typical :26μA) while attempting to null the negative voltage across the PHASE and GND pins. When the I_{SEN} exceeds I_{OC}, the OCP counter starts to work.

Meanwhile, pulses on all the PWM (I_{SEN} > I_{OC}) remains for 20μs, the OCP will be triggered. When I_{SEN} falls below I_{OC} on a PWM pulses before 20μs has elapsed, the counter will be reset. The SCP fault will occur within 10μs when I_{SEN} exceeds twice I_{OC}. The relationship between the sampled current and MOSFET current is given by:

$$I_{SEN} \times R_{SEN} = R_{DS(ON)} \times I_L$$

Which means the current sensing pin will source current to make the voltage drop on the MOSFET and is equal to the voltage generated on the sensing resistor along the ISEN pin current flowing path.
In the formula, the value of R_{SEN} is then written as:

$$R_{SEN} = \frac{R_{DS(ON)} \times I_{OUT(OC)}}{I_{OC}}$$

where:
- R_{SEN} is the resistor used to program the over-current setpoint.
- $I_{OUT(OC)}$ is the desired overcurrent setpoint, the setting value is close to the continuous DC load current I_{OUT}.
- I_{OC} is the I_{SEN} threshold current sourced from the ISEN pin that will activate the OCP circuit. The typical value is 26μA.

When the OCP or SCP fault is detected, the PGOOD pin will pull down to 32Ω and latch off the converter. The fault will remain latched until the EN pin has been pulled below the falling EN threshold voltage or if V_{CC} has decayed below the falling POR threshold voltage.

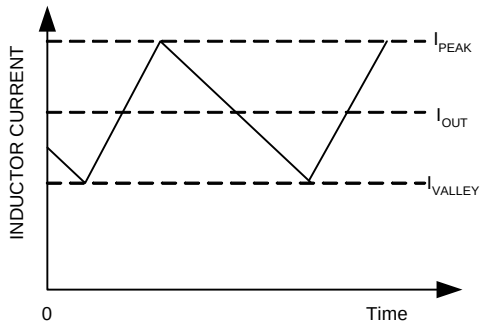


Figure 2. Over-Current Algorithm

Programming the PWM Switching Frequency

The APW7138 does not use a clock signal to produce PWM. The resistor R_{FSET} that is connected from the FSET pin to the GND pin programs the PWM switching frequency

Function Description (Cont.)

Programming the PWM Switching Frequency (Cont.)

F_{SW}. The approximate PWM switching frequency is written as:

$$F_{SW} = \frac{1}{K \times R_{FSET}}$$

Where:

- F_{SW} is the PWM switching frequency
- R_{FSET} is the F_{SW} programming resistor
- $K = 75 \times 10^{-12}$

Application Information

Output Voltage Setting

The output voltage is adjustable from 0.6V to 3.3V with a resistor-divider connected with FB, GND, and converter's output. Using 1% or better resistors for the resistor-divider is recommended. The output voltage is determined by:

$$V_{OUT} = 0.6 \times \left(1 + \frac{R_{TOP}}{R_{GND}}\right)$$

Where 0.6 is the reference voltage, R_{TOP} is the resistor connected from converter's output to FB, and R_{GND} is the resistor connected from FB to GND. Suggested R_{GND} is in the range from 1K to 20kΩ. To prevent stray pickup, locate resistors R_{TOP} and R_{GND} close to APW7138.

Output Inductor Selection

The duty cycle (D) of a buck converter is the function of the input voltage and output voltage. Once an output voltage is fixed, it can be written as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

The inductor value (L) determines the inductor ripple current, I_{RIPPLE}, and affects the load transient reponse. Higher inductor value reduces the inductor's ripple current and induces lower output ripple voltage. The ripple current and ripple voltage can be approximated by:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{F_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}}$$

Where F_{SW} is the switching frequency of the regulator. Although the inductor value and frequency are increased and the ripple current and voltage are reduced, there is a tradeoff exists between the inductor's ripple current and the regulator load transient response time.

A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current. Increasing the switching frequency (F_{SW}) also reduces the ripple current and voltage, but it will increase the switching loss of the MOSFETs and the power dissipation of the converter. The maximum ripple current occurs at the maximum input voltage. A good starting point is to choose the ripple current to be approximately 30% of the maximum output current. Once the inductance value has been chosen, selecting an inductor that is capable of carrying the required peak current without going into saturation. In some types of inductors, especially core that is made of ferrite, the ripple current will increase abruptly when it saturates. This results in a larger output ripple voltage.

Output Capacitor Selection

Output voltage ripple and the transient voltage deviation are factors that have to be taken into consideration when selecting an output capacitor. Higher capacitor value and lower ESR reduce the output ripple and the load transient drop. Therefore, selecting high performance low ESR capacitors is recommended for switching regulator applications. In addition to high frequency noise related to MOSFET turn-on and turn-off, the output voltage ripple includes the capacitance voltage drop ΔV_{COUT} and ESR voltage drop ΔV_{ESR} caused by the AC peak-to-peak inductor's current. These two voltages can be represented by:

$$\Delta V_{COUT} = \frac{I_{RIPPLE}}{8 C_{OUT} F_{SW}}$$

$$\Delta V_{ESR} = I_{RIPPLE} \times R_{ESR}$$

These two components constitute a large portion of the total output voltage ripple. In some applications, multiple capacitors have to be parallelled to achieve the desired ESR value. If the output of the converter has to support another load with high pulsating current, more capacitors are needed in order to reduce the equivalent ESR and suppress the voltage ripple to a tolerable level. A small decoupling capacitor in parallel for bypassing the noise is also recommended, and the voltage rating of the output capacitors are also must be considered. To support a load transient that is faster than the switching frequency, more capacitors are needed for reducing the voltage excursion during load step change. Another aspect of the capacitor selection is that the total AC current going through the capacitors has to be less than the rated RMS current specified on the capacitors in order to prevent the capacitor from overheating.

Application Information (Cont.)

Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, selecting the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage. The maximum RMS current rating requirement is approximately $I_{OUT}/2$, where I_{OUT} is the load current.

During power up, the input capacitors have to handle great amount of surge current. For low-duty notebook appliactions, ceramic capacitor is recommended. The capacitors must be connected between the drain of high-side MOSFET and the source of low-side MOSFET with very low-impeadance PCB layout.

MOSFET Selection

The application for a notebook battery with a maximum voltage of 24V, at least a minimum 30V MOSFETs should be used. The design has to trade off the gate charge with the $R_{DS(ON)}$ of the MOSFET:

· For the low-side MOSFET, before it is turned on, the body diode has been conducting. The low-side MOSFET driver will not charge the miller capacitor of this MOSFET.

· In the turning off process of the low-side MOSFET, the load current will shift to the body diode first. The high dv/dt of the phase node voltage will charge the miller capacitor through the low-side MOSFET driver sinking current path. This results in much less switching loss of the low-side MOSFETs. The duty cycle is often very small in high battery voltage applications, and the low-side MOSFET will conduct most of the switching cycle; therefore, when using smaller $R_{DS(ON)}$ of the low-side MOSFET, the converter can reduce power loss. The gate charge for this MOSFET is usually of secondary consideration. The high-side MOSFET does not have this zero voltage switching condition; in addition, because it conducts for less time compared to the low-side MOSFET, the switching loss tends to be dominant. Priority should be given to the MOSFETs with less gate charge, so that both the gate driver loss, and switching loss, will be minimized.

The selection of the N-channel power MOSFETs are determined by the $R_{DS(ON)}$, reversing transfer capacitance (C_{RSS}) and maximum output current requirement. The losses in the MOSFETs have two components: conduction loss and transition loss. For the high-side and low-side MOSFETs, the losses are approximately given by the following equations:

$$P_{high\text{-}side} = I_{OUT}^{2}(1+TC)(R_{DS(ON)})D + (0.5)(I_{OUT})(V_{IN})(t_{SW})F_{SW}$$

$$P_{low\text{-}side} = I_{OUT}^{2}(1+TC)(R_{DS(ON)})(1-D)$$

Where

I_{OUT} is the load current

TC is the temperature dependency of $R_{DS(ON)}$

F_{SW} is the switching frequency

t_{SW} is the switching interval

D is the duty cycle

Note that both MOSFETs have conduction losses while the high-side MOSFET includes an additional transition loss. The switching interval, t_{SW}, is the function of the reverse transfer capacitance C_{RSS}. The (1+TC) term is a factor in the temperature dependency of the $R_{DS(ON)}$ and can be extracted from the "$R_{DS(ON)}$ vs. Temperature" curve of the power MOSFET.

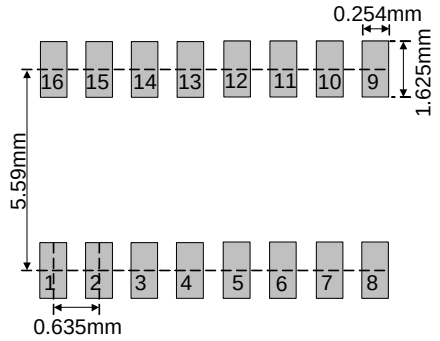
Layout Consideration

In any high switching frequency converter, a correct layout is important to ensure proper operation of the regulator. With power devices switching at higher frequency, the resulting current transient will cause voltage spike across the interconnecting impedance and parasitic circuit elements. As an example, consider the turn-off transition of the PWM MOSFET. Before turn-off condition, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is freewheeling by the low side MOSFET and parasitic diode. Any parasitic inductance of the circuit generates a large voltage spike during the switching interval. In general, using short and wide printed circuit traces should minimize interconnecting impedances and the magnitude of voltage spike. Besides, signal and power grounds are to be kept separate and finally combined using ground plane construction or single point grounding. The best tie-point between the signal ground and the power ground is at the negative side of the output capacitor on each channel, where there is less noise. Noisy traces beneath the IC are not recommended. Below is a checklist for your layout:

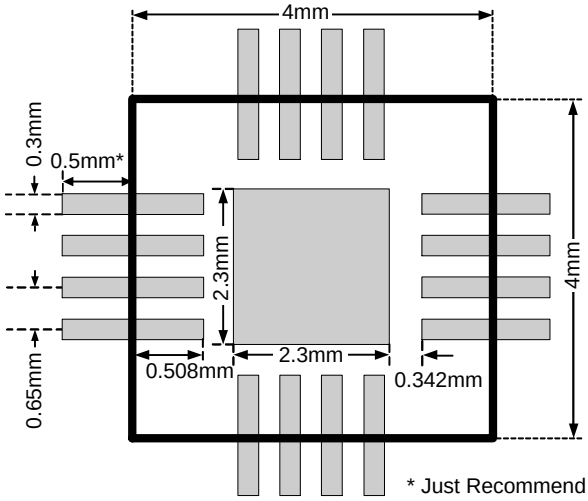
Application Information (Cont.)

Layout Consideration (Cont.)

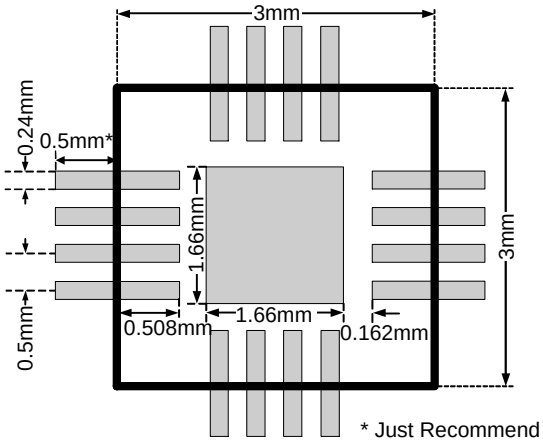
- Keep the switching nodes (UG, LG, BOOT, PHASE, and ISEN) away from sensitive small signal nodes since these nodes are fast moving signals.Therefore, keep traces to these nodes as short as possible and there should be no other weak signal traces in parallel with theses traces on any layer.
- The signals going through theses traces have both high dv/dt and high di/dt with high peak charging and discharging current. The traces from the gate drivers to the MOSFETs (UG, LG) should be short and wide.
- Place the source of the high-side MOSFET and the drain of the low-side MOSFET as close as possible. Minimizing the impedance with wide layout plane between the two pads reduces the voltage bounce of the node. In addition, the large layout plane between the drain of the MOSFETs (V_{IN} and PHASE nodes) can get better heat sinking.
- For accurate current sensing, the ISEN trace should be a separate trace and independently go to the drain terminal of the low side MOSFET. The PGND is the current sensing circuit reference ground and also the power ground of the LG low-side MOSFET. On the hand, the PGND trace should be a separate trace and independently go to the source of the low-side MOSFET. Besides, the current sense resistor should be close to ISEN pin to avoid parasitic capacitor effect and noise coupling.
- Decoupling capacitors, the resistor-divider, and boot capacitor should be close to their pins. (For example, place the decoupling ceramic capacitor close to the drain of the high-side MOSFET as close as possible).
- The input bulk capacitors should be close to the drain of the high-side MOSFET, and the output bulk capacitors should be close to the loads. The input capacitor's ground should be close to the grounds of the output capacitors and low-side MOSFET.
- Locate the resistor-divider close to the FB pin to minimize the high impedance trace. In addition, FB pin traces can't be close to the switching signal traces (UG, LG, BOOT, PHASE, and ISEN).



SSOP-16



QFN4x4-16A

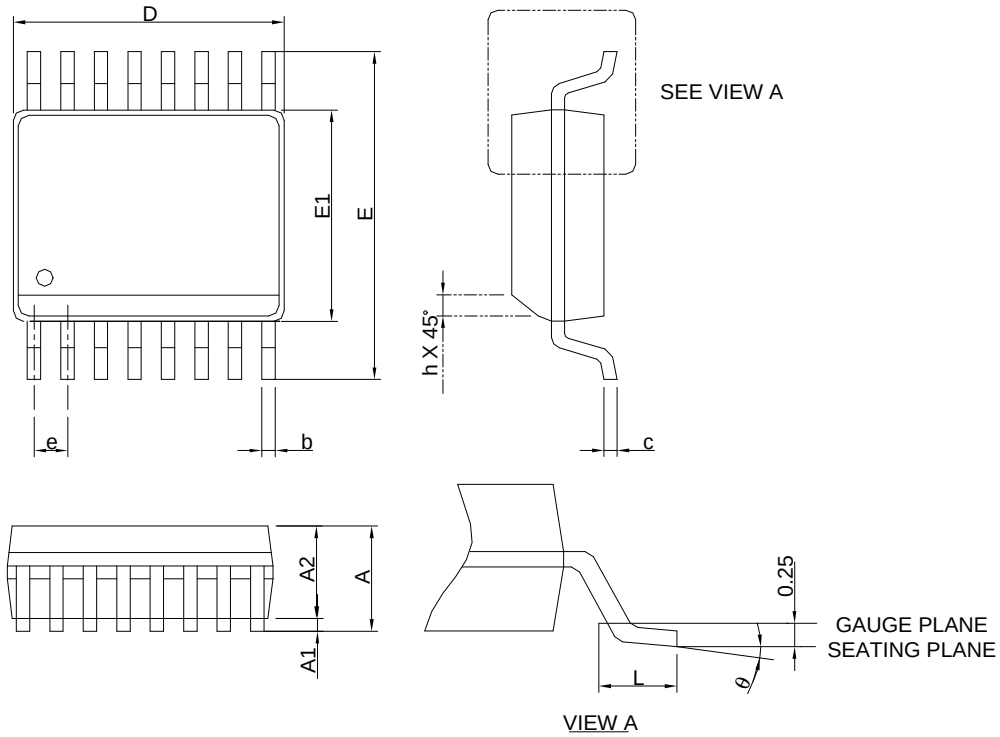


TQFN3x3-16

Figure 3. Recommended Minimum Footprint

Package Information

SSOP-16

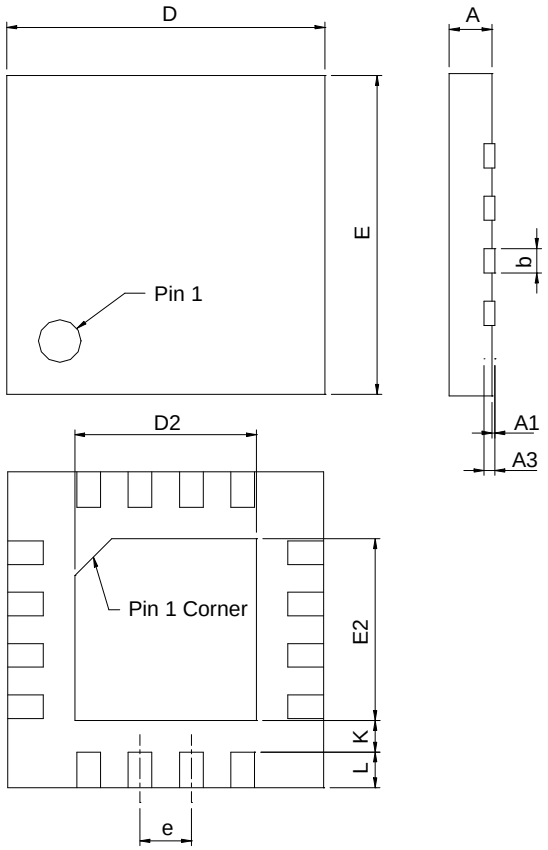


SYMBOL	SSOP-16			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.10	0.25	0.004	0.010
A2	1.24		0.049	
b	0.20	0.30	0.008	0.012
c	0.15	0.25	0.006	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	0.635 BSC		0.025 BSC	
L	0.40	1.27	0.016	0.050
h	0.25	0.50	0.010	0.020
θ	0°	8°	0°	8°

Note: 1. Follow JEDEC MO-137 AB.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Package Information

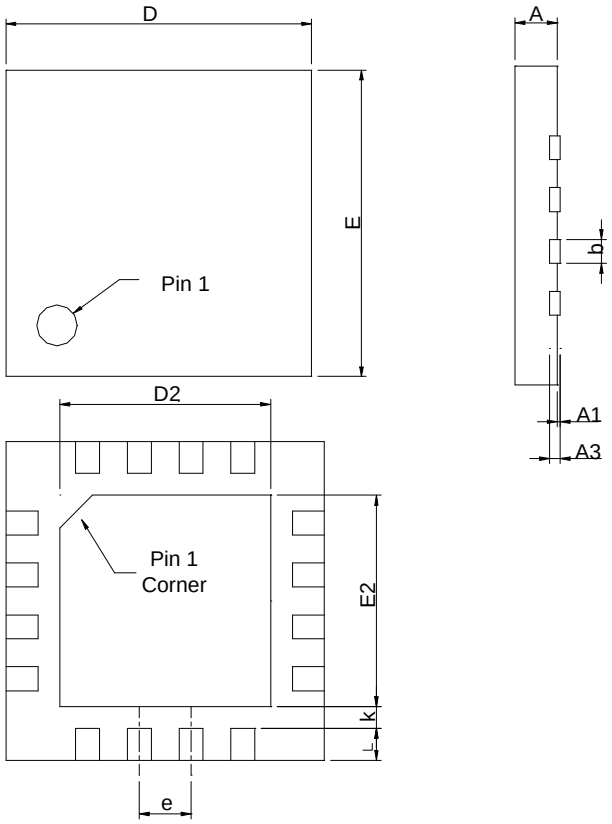
QFN4x4-16A



SYMBOL	QFN4x4-16A			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.25	0.35	0.010	0.014
D	3.90	4.10	0.154	0.161
D2	2.10	2.50	0.083	0.098
E	3.90	4.10	0.154	0.161
E2	2.10	2.50	0.083	0.098
e	0.65 BSC		0.026 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	

Package Information

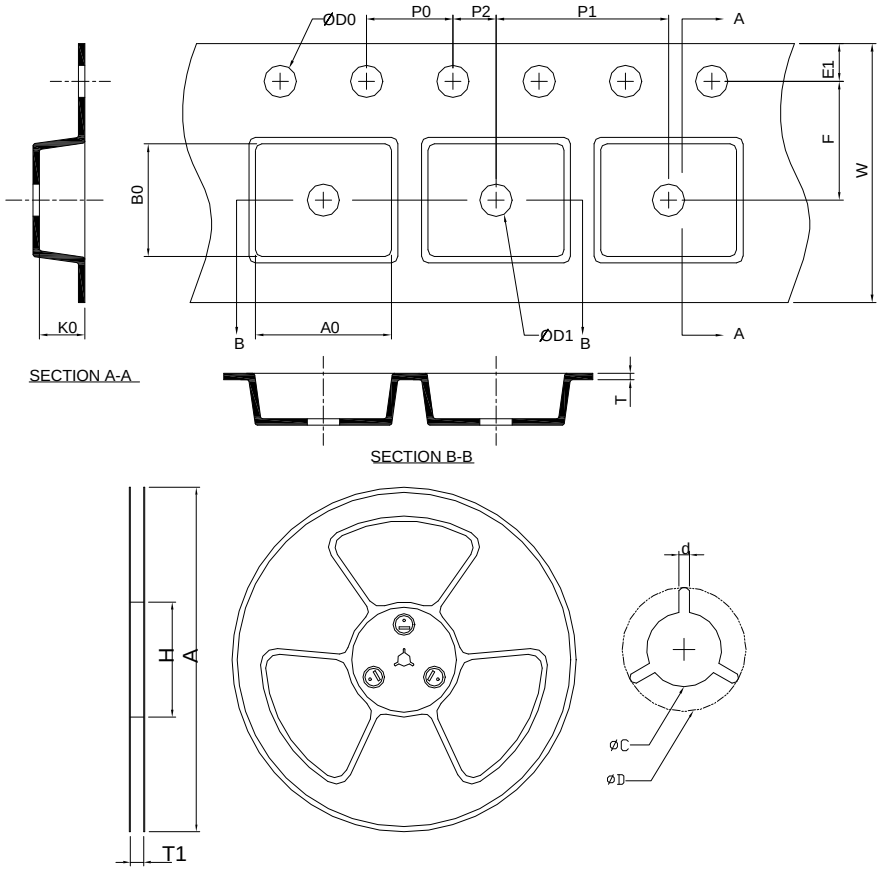
TQFN3x3-16



SYMBOL	TQFN3x3-16			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	2.90	3.10	0.114	0.122
D2	1.50	1.80	0.059	0.071
E	2.90	3.10	0.114	0.122
E2	1.50	1.80	0.059	0.071
e	0.50 BSC		0.020 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	

Note : Follow JEDEC MO-220 WEED-4.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
SSOP-16	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.50±0.10
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.00±0.10	8.00±0.10	2.00±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	5.20±0.20	2.10±0.20
Application	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
QFN4x4-16A	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	4.30±0.20	4.30±0.20	1.30±0.20
Application	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
TQFN3x3-16	330±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30±0.20	3.30±0.20	1.30±0.20

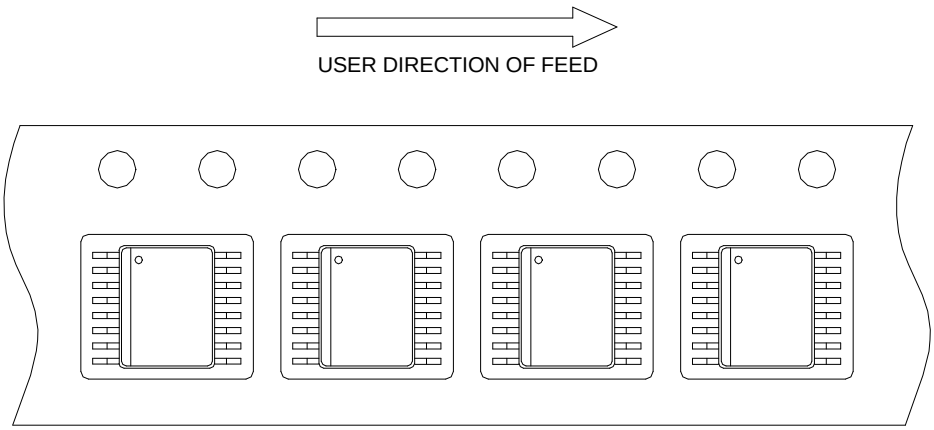
(mm)

Devices Per Unit

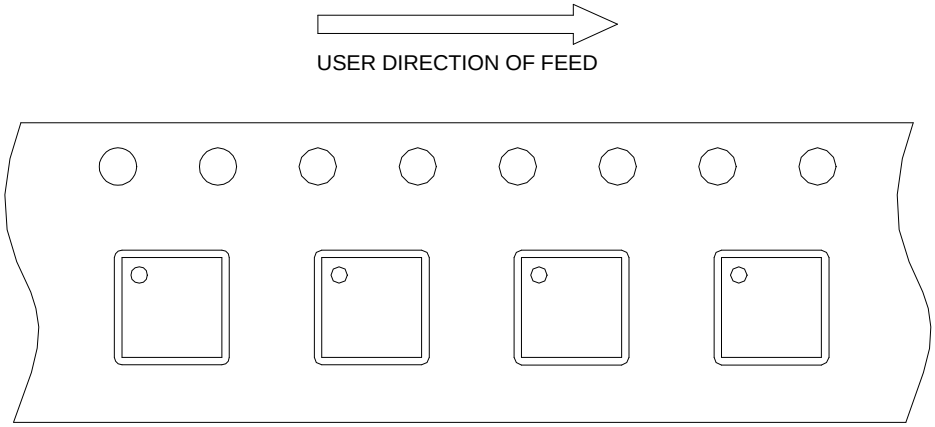
Package Type	Unit	Quantity
SSOP-16	Tape & Reel	2500
QFN4x4-16A	Tape & Reel	3000
TQFN3x3-16	Tape & Reel	3000

Taping Direction Information

SSOP-16

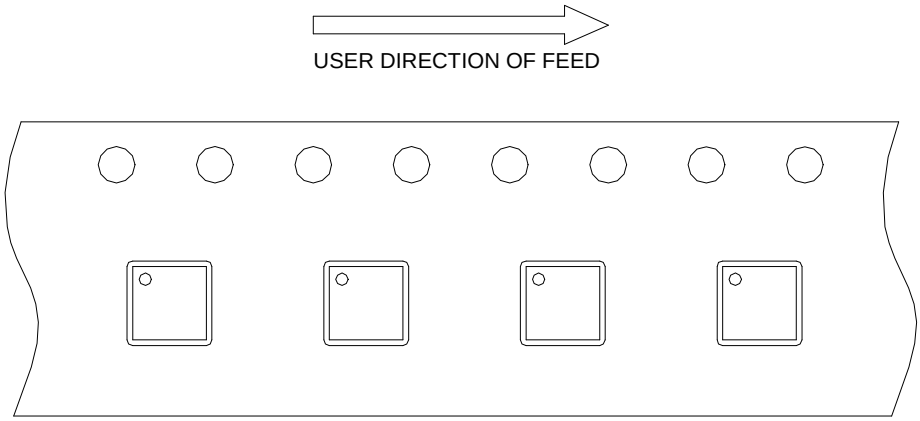


QFN4x4-16A

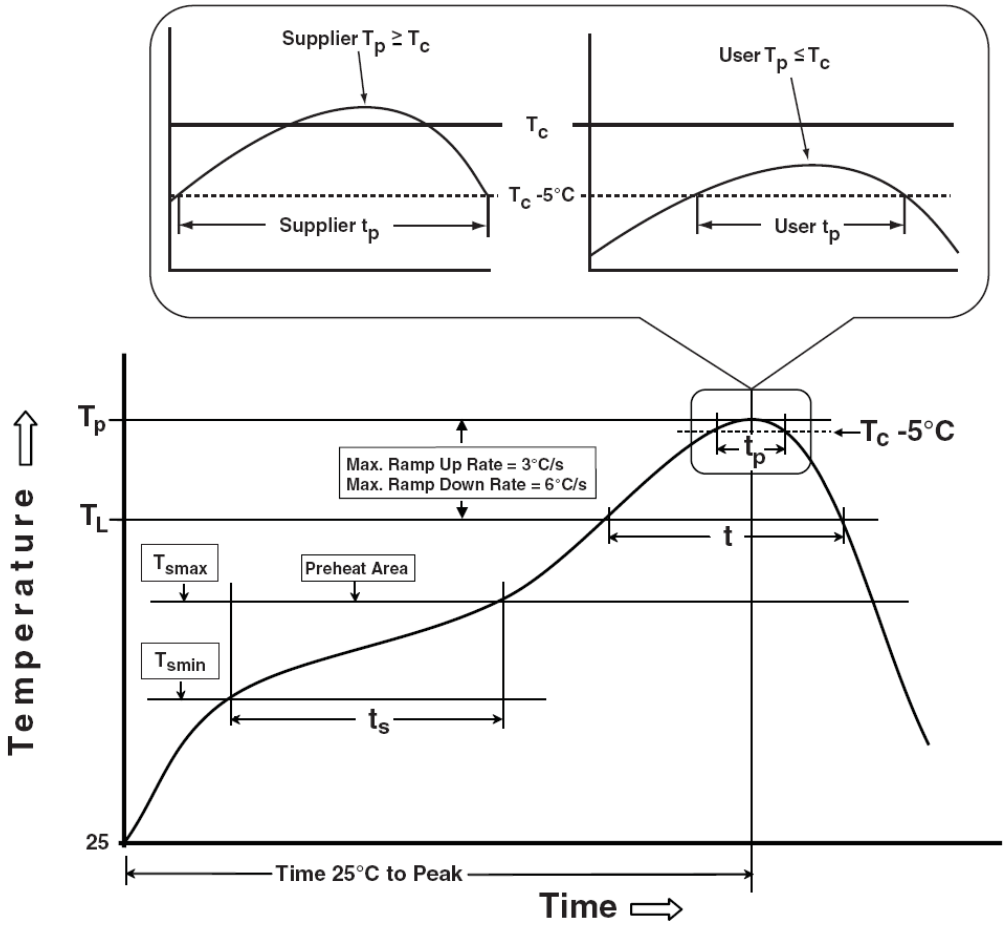


Taping Direction Information (Cont.)

TQFN3x3-16



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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