DDR TOTAL POWER SOLUTION
SYNCHRONOUS BUCK CONTROLLER WITH 1.5A LDO

Features

Buck Controller (VDDQ)

- **High Input Voltages Range from 3V to 28V Input Power**
- **Provide 1.8V (DDR2), 1.5V (DDR3) or Adjustable Output Voltage from 0.5V to 2V**
  - ±1% Accuracy Over-Temperature
- **Build in VREF Voltage 1.8V ±1% Accuracy over Temperature**
- **Integrated MOSFET Drivers**
- **Integrated Bootstrap Forward P-CH MOSFET**
- **Excellent Line and Load Transient Responses**
- **PFM Mode for Increased Light Load Efficiency**
- **Selectable 300kHz/400kHz/500kHz Switching Frequebcies**
- **Integrated MOSFET Drivers and Bootstrap Diode**
- **S3 and S5 Pins Control The Device in S0, S3, or S4/S5 State**
- **Power Good Monitoring**
- **50% Under-Voltage Protection (UVP)**
- **125% Over-Voltage Protection (OVP)**
- **Adjustable Current-Limit Protection**
  - Using Sense Low-Side MOSFET $R_{DS(ON)}$
- **QFN-20 3mmx3mm Package (QFN-20) and QFN-16 3mmx3mm Thin Package (TQFN-16)**
- **Lead Free Available (RoHS Compliant)**

±1.5A LDO Section (VTT)

- **Souring or Sinking Current up to 1.5A**
- **Fast Transient Response for Output Voltage**
- **Output Ceramic Capacitors Support at Least 10㎌F MLCC**
- **VTT and VTTREF Track at Half the VDDQSNS by Internal Divider**
- **±20mV Accuracy for VTT and VTTREF**
- **Independent Over-Current-Limit (OCL)**
- **Thermal Shutdown Protection**

General Description

The APW8819 integrates a synchronous buck PWM controller to generate VDDQ, a sourcing and sinking LDO linear regulator to generate VTT. It provides a complete power supply for DDR2 and DDR3 memory system. It offers the lowest total solution cost in system where space is at a premium.

The APW8819 provides excellent transient response and accurate DC voltage output in PFM Mode. In Pulse Frequency Mode (PFM), the APW8819 provides very high efficiency over light to heavy loads with loading-modulated switching frequencies.

The APW8819 is equipped with accurate current-limit, output under-voltage, and output over-voltage protections. A Power-On- Reset function monitors the voltage on VCC prevents wrong operation during power on.

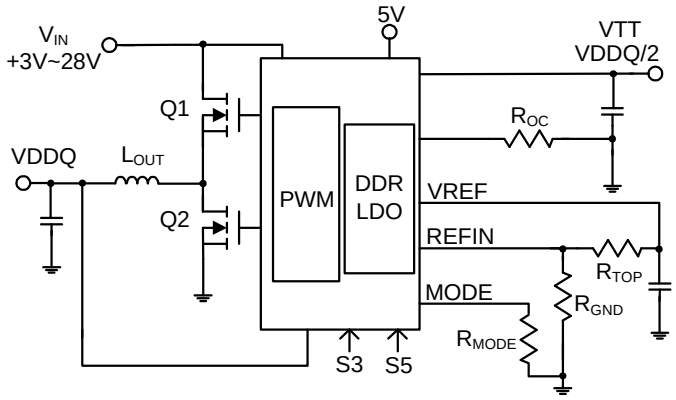
The LDO is designed to provide a regulated voltage with bi-directional output current for DDR-SDRAM termination. The device integrates two power transistors to source or sink current up to 1.5A. It also incorporates current-limit and thermal shutdown protection.

An internal resistor divider is used to provide a half voltage of VDDQSNS for VTTREF and VTT Voltage. The VTT output voltage is only requiring 20µF of ceramic output capacitance for stability and fast transient response. The S3 and S5 pins provide the sleep state for VTT (S3 state) and suspend state (S4/S5 state) for device, when S5 and S3 are both pulled low the device provides the soft-off for VTT and VTTREF.The APW8819 is available in 3mmx3mm 20-pin QFN and 3mmx3mm 16-pin TQFN packages.

Applications

- **DDR2, and DDR3 Memory Power Supplies**
- **SSTL-2 SSTL-18 and HSTL Termination**

Simplified Application Circuit

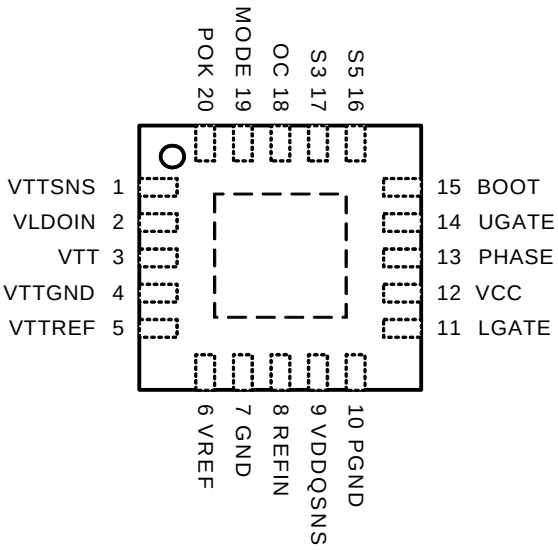


Ordering and Marking Information

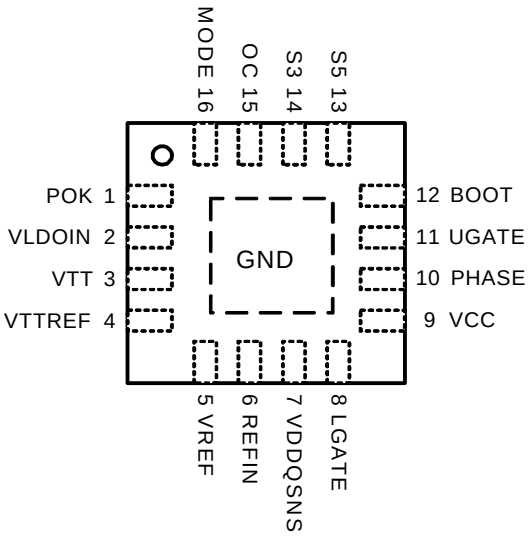
APW8819 □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code QA : QFN-20 QB : TQFN-16 Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel TY : Tray Assembly Material G : Halogen and Lead Free Device
APW8819 QA : APW 8819 XXXXX	XXXXX - Date Code
APW8819 QB : APW 8819 XXXXX	XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Pin Configuration



QFN 3x3-20
(Top View)



TQFN 3x3-16
(Top View)

= Thermal Pad (connected to GND plane for better heat dissipation)

Absolute Maximum Ratings (Note 1, 2)

Symbol	Parameter	Rating	Unit
V_{CC}	VCC Supply Voltage (VCC to GND)	-0.3 ~ 7	V
V_{BOOT}	BOOT Supply Voltage (BOOT to PHASE)	-0.3 ~ 7	V
$V_{BOOT-GND}$	BOOT Supply Voltage (BOOT to GND) <20ns Pulse Width >20ns Pulse Width	 -5 ~ 42 -0.3 ~ 35	V
	UGATE Voltage (UGATE to PHASE) <20ns Pulse Width >20ns Pulse Width	 -5 ~ V_{BOOT}+0.3 -0.3 ~ V_{BOOT}+0.3	V
	LGATE Voltage (LGATE to GND) <20ns Pulse Width >20ns Pulse Width	 -5 ~ VCC+0.3 -0.3 ~ VCC+0.3	V
	PHASE Voltage (PHASE to GND) <20ns Pulse Width >20ns Pulse Width	 -5 ~ 35 -0.3 ~ 28	V
	PGND and VTTGND to GND Voltage	-0.3 ~ 0.3	V
	All Other Pins (OC, MODE, S3, S5, VDDQSNS, VTTSNS, VLDOIN, VREF, POK, VTT, VTTREF and REFIN to GND Voltage)	-0.3 ~ 7	V
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Soldering Temperature, 10 Seconds	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Note 2: The device is ESD sensitive. Handling precautions are recommended.

Thermal Characteristics (Note 3)

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Thermal Resistance - Junction to Ambient QFN3x3-20 TQFN3x3-16	 95 95	°C/W

Note 3: θ_{JA} is measured with the component mounted on a high effective the thermal conductivity test board in free air. The exposed pad of package is soldered directly on the PCB.

Recommended Operating Conditions (Note 4)

Symbol	Parameter	Range	Unit
V_{CC}	VCC Supply Voltage	4.5 ~ 5.5	V
V_{IN}	Converter Input Voltage	3 ~ 28	V
V_{VDDQ}	Converter Output Voltage	0.5 ~2V/ DDR2 (1.8V)/ DDR3 (1.5V)	V
V_{VTT}	LDO Output Voltage	0.25~ 1	V
I_{OUT}	Converter Output Current	0 ~ 20	A
I_{VTT}	LDO Output Current	-1.5 ~ +1.5	A
C_{VCC}	VCC Capacitance	1~	µF
C_{VTT}	VTT Output Capacitance	10~	µF
C_{VTTREF}	VTTREF Output Capacitance	0.22 ~ 2.2	µF
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Electrical Characteristics

Refer to the typical application circuits. These specifications apply over V_{VCC}=V_{BOOT}=5V, V_{IN}=12V and T_A= -40 ~ 85 °C, unless otherwise specified. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW8819			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
I_{VCC}	VCC Supply Current	T_A = 25°C, V_{S3} = V_{S5} = 5V, no load	-	1.2	1.5	mA
I_{VCCSTB}	VCC Standby Current	T_A = 25°C, V_{S3} = 0V, V_{S5} = 5V, no load	-	740	850	µA
I_{VCCSDN}	VCC Shutdown Current	T_A =25°C, V_{S3} = V_{S5} = 0V, no load	-	0.1	1	µA
I_{LDOIN}	LDOIN Supply Current	T_A = 25°C, V_{S3} = V_{S5} = 5V, no load	0.3	0.6	1	mA
$I_{LDOINSTB}$	LDOIN Standby Current	T_A = 25°C, V_{S3} = 0V, V_{S5} = 5V, no load	-	0.1	10	µA
$I_{LDOINSDN}$	LDOIN Shutdown Current	T_A = 25°C, V_{S3} = V_{S5} = 0V, no load	-	0.1	1	
POWER-ON-RESET						
	VCC POR Threshold	VCC Rising	4.15	4.3	4.45	V
	VCC POR Hysteresis		-	100	-	mV
VTT OUTPUT						
V_{VREF}	VREF Output Voltage	I_{VREF}=30µA, T_A=25°C	-	1.8	-	V
		0uA≤I_{VREF}≤300uA, TA= -40°C~85°C	1.782	-	1.8144	V

Electrical Characteristics (Cont.)

Refer to the typical application circuits. These specifications apply over V_{VCC}=V_{BOOT}=5V, V_{IN}=12V and T_A= -40 ~ 85 °C, unless otherwise specified. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW8819			Unit
			Min.	Typ.	Max.	
VTT OUTPUT						
V_{VTT}	VTT Output Voltage	V_{LDOIN} = $V_{VDDQSNS}$ = 1.8V	-	0.9	-	V
		V_{LDOIN} = $V_{VDDQSNS}$ = 1.5V	-	0.75	-	
V_{VTT}	VTT Output Tolerance	V_{LDOIN} = $V_{VDDQSNS}$ = 1.8V, $V_{VDDQSNS}$/2 - V_{VTT}, I_{VTT} = 0A	-20	-	20	mV
		V_{LDOIN} = $V_{VDDQSNS}$ = 1.8V, $V_{VDDQSNS}$/2 - V_{VTT}, I_{VTT} = 1.5A	-30	-	30	
		V_{LDOIN} = $V_{VDDQSNS}$ = 1.5V, $V_{VDDQSNS}$/2 - V_{VTT}, I_{VTT} = 0A	-20	-	20	
		V_{LDOIN} = $V_{VDDQSNS}$ = 1.5V, $V_{VDDQSNS}$/2 - V_{VTT}, I_{VTT} = 1.5A	-30	-	30	
I_{LIM}	Current-Limit	Sourcing Current (V_{LDOIN} = 1.8V)	2	2.2	3	A
		Sinking Current (V_{LDOIN} = 1.8V)	-2	-2.2	-3	
		Sourcing Current (V_{LDOIN} = 1.5V)	2	2.2	3	A
		Sinking Current (V_{LDOIN} = 1.5V)	-2	-2.2	-3	
I_{VTTLK}	VTT Leakage Current	V_{VTT} = 1.25V, V_{S3} = 0V, V_{S5} = 5V, T_A = 25°C	-1.0	-	1.0	µA
$I_{VTTSNSLK}$	VTTSNS Leakage Current	V_{VTT} = 1.25V, T_A = 25°C	-1.00	0.01	1.00	µA
I_{VTTDIS}	VTT Discharge Current	V_{VTT} = 0.5V, V_{S3} = V_{S5} = 0V, T_A = 25°C, V_{VREF} = 0V	-	7.8	-	mA
VTTREF OUTPUT						
V_{VTTREF}	VTTREF Output Voltage	V_{LDOIN} = $V_{VDDQSNS}$ = 1.8V, $V_{VDDQSNS}$/2	-	0.9	-	V
		V_{LDOIN} = $V_{VDDQSNS}$ = 1.5V, $V_{VDDQSNS}$/2	-	0.75	-	
	VTTREF Tolerance	-10mA < I_{VTTREF} < 10mA, $V_{VDDQSNS}$/2 - V_{VTTREF} V_{LDOIN} = V_{VTTREF} =1.8V	-18	-	+18	mV
		-10mA < I_{VTTREF} < 10mA, $V_{VDDQSNS}$/2 - V_{VTTREF} V_{LDOIN} = $V_{VDDQSNS}$ = 1.5V	-15	-	+15	
I_{VTTREF}	VTTREF Source Current	V_{VTTREF} = 0V	-10	-25	-40	mA
I_{VTTREF}	VTTREF Sink Current	V_{VTTREF} = $V_{VDDQSNS}$	10	25	40	mA
$I_{VTTREFDIS}$	VTTREF Discharge Current	T_A = 25°C , S3=S5=0V, V_{VTTREF} = 0.5V	-	2.6	-	mA
VDDQ OUTPUT						
V_{VDDQ}	VDDQ Output Voltage	V_{REFIN} = 1.8V	-	1.8	-	V
	VDDQSNS Regulation Voltage Tolerance to REFIN	T_A = 25°C, V_{REFIN} = 1.8V, No Load	-15	-	15	mV
$I_{VDDQSNS}$	VDDQSNS Input Current	$V_{VDDQSNS}$=1.8V	-	12	-	µA
I_{REFIN}	REFIN Input Current	V_{REFIN}=1.8V	-0.1	-	0.1	µA
	VDDQ Discharge Current	V_{S3} = V_{S5} = 0V, $V_{VDDQSNS}$ = 0.5V, MODE Pin Pulled Down to GND Through 47kΩ (Non-Tracking)	-	12	-	mA
	LDOIN Discharge Current	V_{S3} = V_{S5} = 0V, $V_{VDDQSNS}$ = 0.5V, MODE Pin Pulled Down to GND Through 100kΩ (Tracking)	-	1000	-	mA

Electrical Characteristics (Cont.)

Refer to the typical application circuits. These specifications apply over V_{VCC}=V_{BOOT}=5V, V_{IN}=12V and T_A= -40 ~ 85 °C, unless otherwise specified. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW8819			Unit
			Min.	Typ.	Max.	
PWM CONTROLLERS						
F_{SW}	Operating Frequency	V_{IN}=12V, $V_{VDDQSNS}$=1.8V, R_{MODE}=100 kΩ	270	300	330	kHz
		V_{IN}=12V, $V_{VDDQSNS}$=1.8V, R_{MODE}=200 kΩ	360	400	440	kHz
T_{SS}	Internal Soft Start Time	S5 is High to V_{OUT} Regulation	0.9	1.2	1.5	ms
$T_{OFF(MIN)}$	Minimum off Time		350	450	550	ns
$T_{ON(MIN)}$	Minimum on Time		80	110	140	ns
	Zero-Crossing Threshold		-9.5	0.5	10.5	mV
VDDQ PROTECTIONS						
	OC Pin Source Current	T_A = 25°C	9	10	11	µA
		Temperature Coefficient, On The Basis of 25 °C	-	4500	-	ppm/°C
	OCP Comparator Offset	(V_{OC} – V_{PGND}) – (V_{PGND} – V_{PHASE}), V_{OC} – V_{PGND} = 60mV	-10	0	+10	mV
	VDDQ Current Limit Setting Range	V_{OC}-V_{PGND}	0.2	-	3	V
	VDDQ OVP Trip Threshold	V_{VDDQ} Rising	120	125	130	%
	VDDQ OVP Debounce Delay	V_{VDDQ} Rising, DV=10mV	-	2	-	µs
	VDDQ UVP Trip Threshold	V_{VDDQ} Falling	40	50	60	%
	VDDQ UVP Trip Hysteresis		-	3	-	%
	VDDQ UVP Debounce		-	16	-	µs
	VDDQ UVP Enable Delay		2	2.4	2.8	ms
POK						
V_{POK}	POK Threshold	POK in from Lower (POK Goes High)	87	90	93	%
		POK Out from Normal (POK Goes Low)	120	125	130	%
I_{POK}	POK Leakage Current	V_{POK}=5V	-	0.1	1.0	µA
	POK Sink Current	V_{POK}=0.5V	2.5	7.5	-	mA
	POK Enable Delay Time	S5 High to POK High	2	2.4	2.8	ms
	POK Delay Time	Delay for POK In	-	63	-	µs
GATE DRIVERS						
	UGATE Pull-Up Resistance	BOOT-UGATE=0.5V	-	1.5	3	Ω
	UGATE Sink Resistance	UGATE-PHASE=0.5V	-	0.7	1.8	Ω
	LGATE Pull-Up Resistance	VCC-LGATE=0.5V	-	1	2.2	Ω
	LGATE Sink Resistance	LGATE-PGND=0.5V	-	0.5	1.2	Ω
	UGATE to LGATE Dead time	UGATE falling to LGATE rising, no load	-	20	-	ns
	LGATE to UGATE Dead time	LGATE falling to UGATE rising, no load	-	20	-	ns

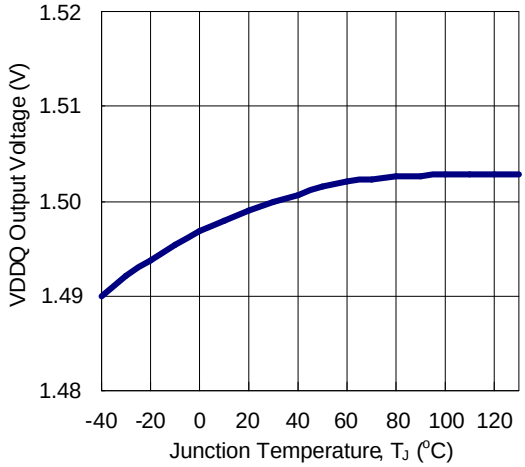
Electrical Characteristics (Cont.)

Refer to the typical application circuits. These specifications apply over V_{VCC}=V_{BOOT}=5V, V_{IN}=12V and T_A= -40 ~ 85 °C, unless otherwise specified. Typical values are at T_A=25°C.

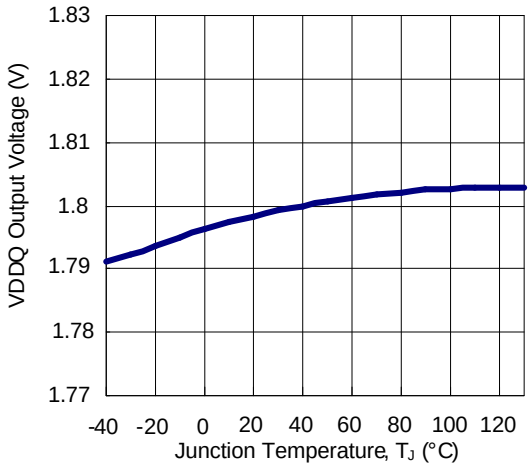
Symbol	Parameter	Test Conditions	APW8819			Unit
			Min.	Typ.	Max.	
BOOTSTRAP SWITCH						
V_F	R_{ON}	V_{VCC} - V_{BOOT}, I_F = 10mA, T_A = 25°C	-	0.5	0.8	V
I_F	Reverse Leakage	V_{BOOT} = 30V, V_{PHASE} = 25V, V_{VCC} = 5V, T_A = 25°C	-	-	0.5	µA
LOGIC THRESHOLD						
V_{IH}	S3, S5 High Threshold Voltage	S3, S5 Rising	1.6	-	-	V
V_{IL}	S3, S5 Low Threshold Voltage	S3, S5 Falling	-	-	0.9	V
I_{ILEAK}	Logic Input Leakage Current	V_{S3} = V_{S5} = 5V, T_A =25°C	-1	-	1	µA
I_{MODE}	MODE Source Current		14	15	16	µA
V_{THMODE}	MODE Threshold Voltage	MODE = 0	-	-	0.829	V
		MODE = 1	0.879	-	1.202	
		MODE = 2	1.262	-	1.76	
		MODE = 3	1.84	-	1.95	
		MODE = 4	VCC-1	-	-	
THERMAL SHUTDOWN						
T_{SD}	Thermal Shutdown Temperature	T_J Rising	-	160	-	°C
	Thermal Shutdown Hysteresis		-	25	-	°C

Typical Operating Characteristics

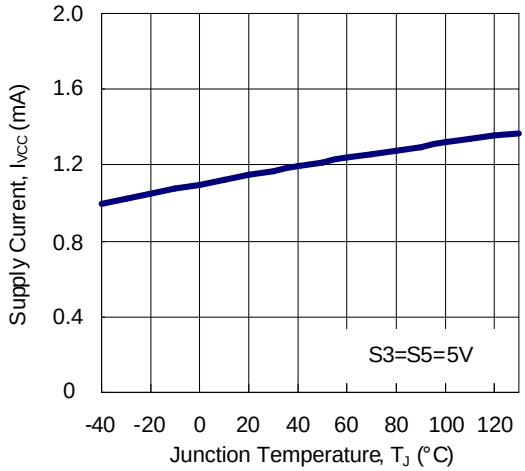
V_{REFIN}=1.5V, VDDQ=1.5V



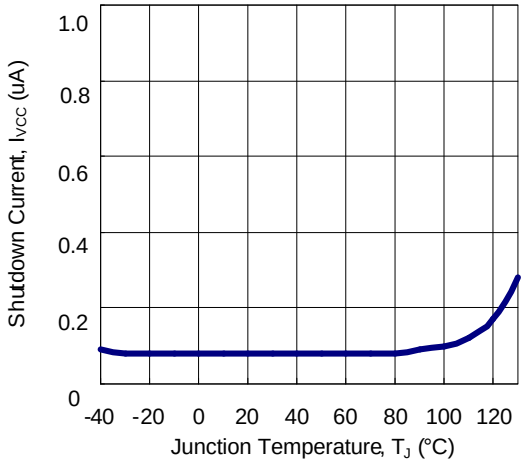
V_{REFIN}=1.8V, VDDQ=1.8V



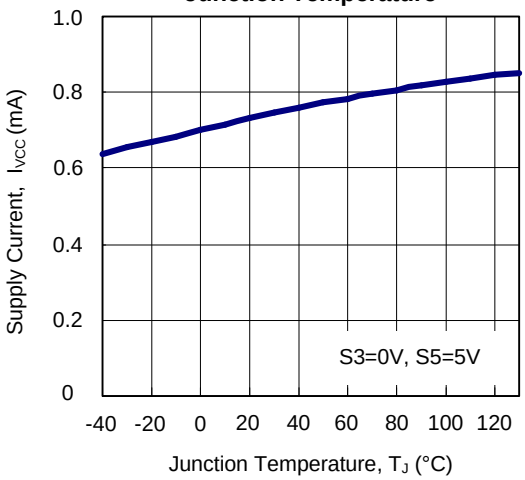
Supply Current in S 0 State vs. Junction Temperature



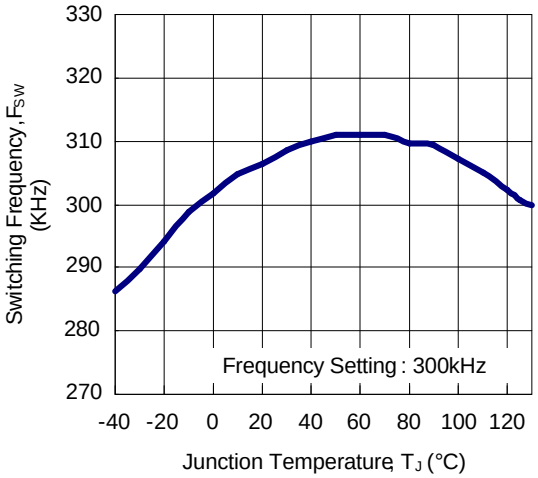
Shutdown Current vs. Junction Temperature



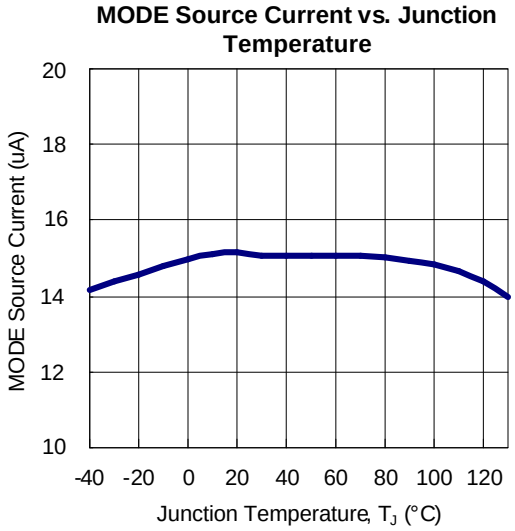
Supply Current in S3 State vs. Junction Temperature

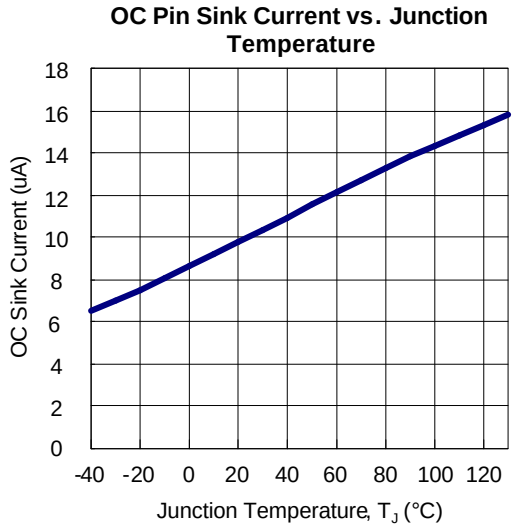


Frequency vs. Junction Temperature



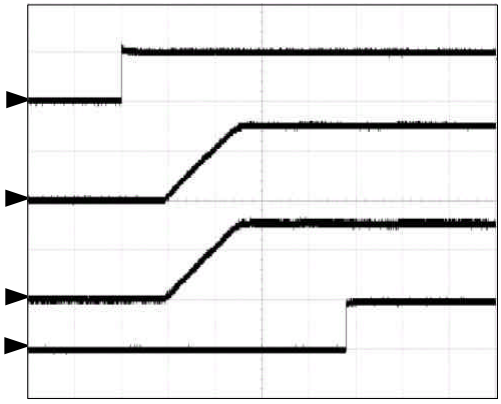
Typical Operating Characteristics





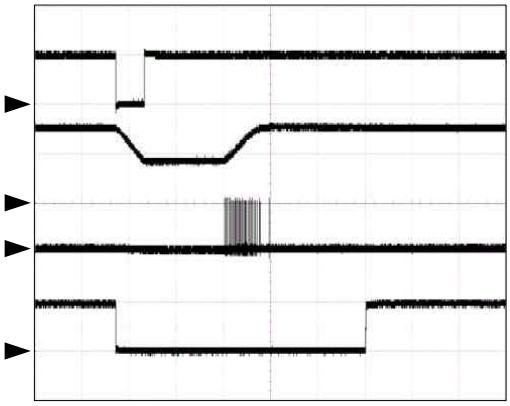
Operating Waveforms

S5 Enable, No Load



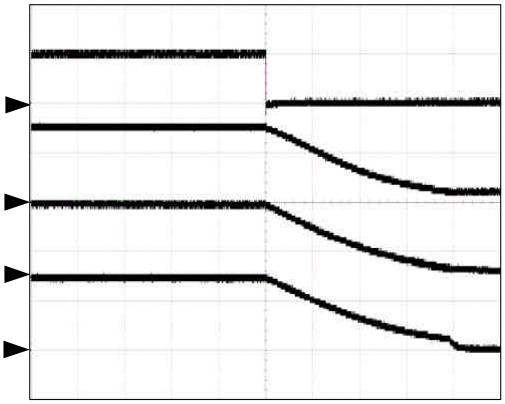
CH1: V_{S5} (5V/div)
CH2: V_{VDDQ} (1V/div)
CH3: V_{VTT} (500mV/div)
CH4: V_{POK} (5V/div)
Time: 500µs/div

Non-Zero VDDQ S5 Enable



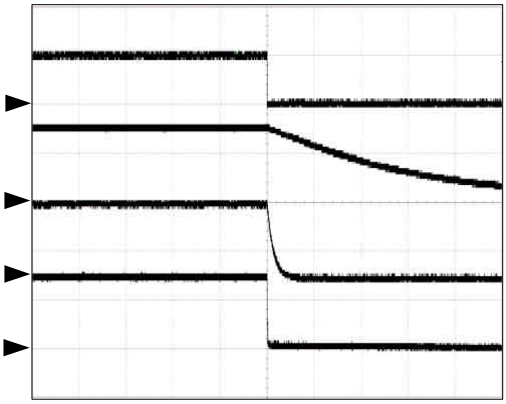
CH1: V_{S5} (5V/div)
CH2: V_{VDDQ} (1V/div)
CH3: V_{UGATE} (20V/div)
CH4: V_{POK} (5V/div)
Time: 500µs/div

S5 Shutdown - Tracking Discharge



CH1: V_{S5} (5V/div)
CH2: V_{VDDQ} (1V/div)
CH3: V_{VTT} (500mV/div)
CH4: V_{VTTREF} (500mV/div)
Time: 200µs/div

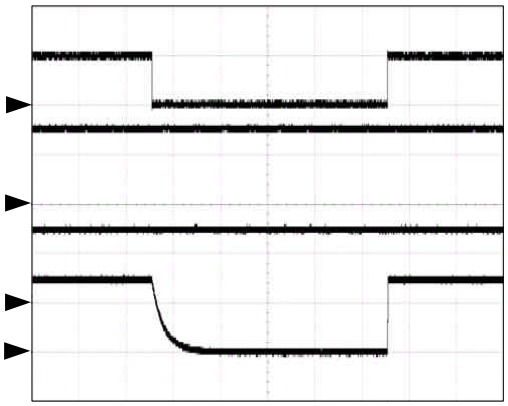
S5 Shutdown - Non-Tracking Discharge



CH1: V_{S5} (5V/div)
CH2: V_{VDDQ} (1V/div)
CH3: V_{VTT} (500mV/div)
CH4: V_{VTTREF} (500mV/div)
Time: 5ms/div

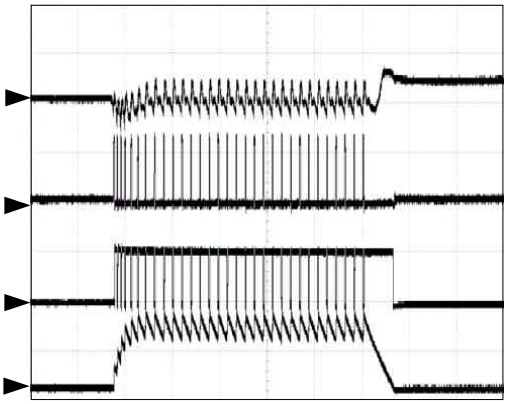
Operating Waveforms

S3 Enable-Shutdown



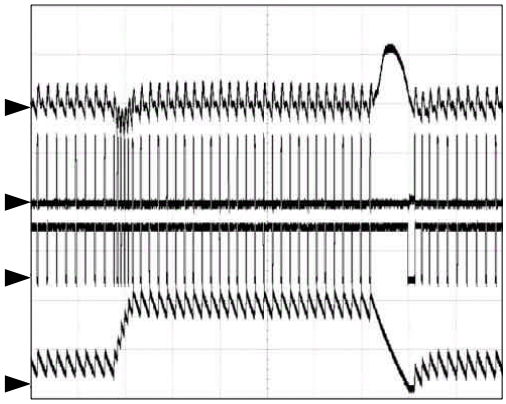
CH1: V_{S3} (5V/div)
CH2: V_{VDDQ} (1V/div)
CH3: V_{VTTREF} (500mV/div)
CH4: V_{VTT} (500mV/div)
Time: 10ms/div

Load Transient, I_{VDDQ}= 0A->12A->0A



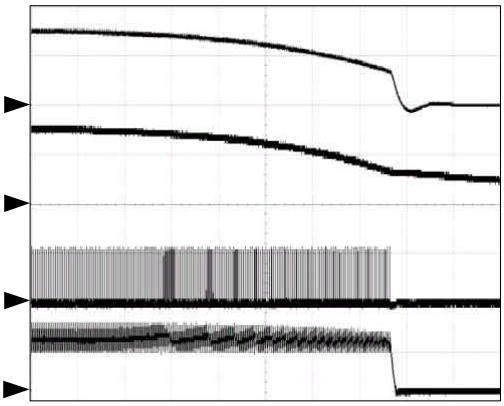
CH1: V_{VDDQ} (100mV/div)
CH2: V_{UGATE} (20V/div)
CH3: V_{LGATE} (5V/div)
CH4: I_L (10A/div)
Time: 20µs/div

Load Transient, I_{VDDQ}= 5A->17A->5A



CH1: V_{VDDQ} (100mV/div)
CH2: V_{UGATE} (20V/div)
CH3: V_{LGATE} (5V/div)
CH4: I_L (10A/div)
Time: 20µs/div

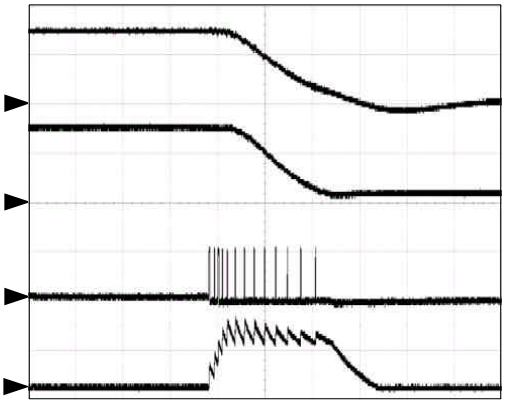
Current Limit then Occur UVP



CH1: V_{VDDQ} (1V/div)
CH2: V_{VTT} (500mV/div)
CH3: V_{PHASE} (20V/div)
CH4: I_L (10A/div)
Time: 100µs/div

Operating Waveforms

Short Circuit Test : VDDQ Short to GND

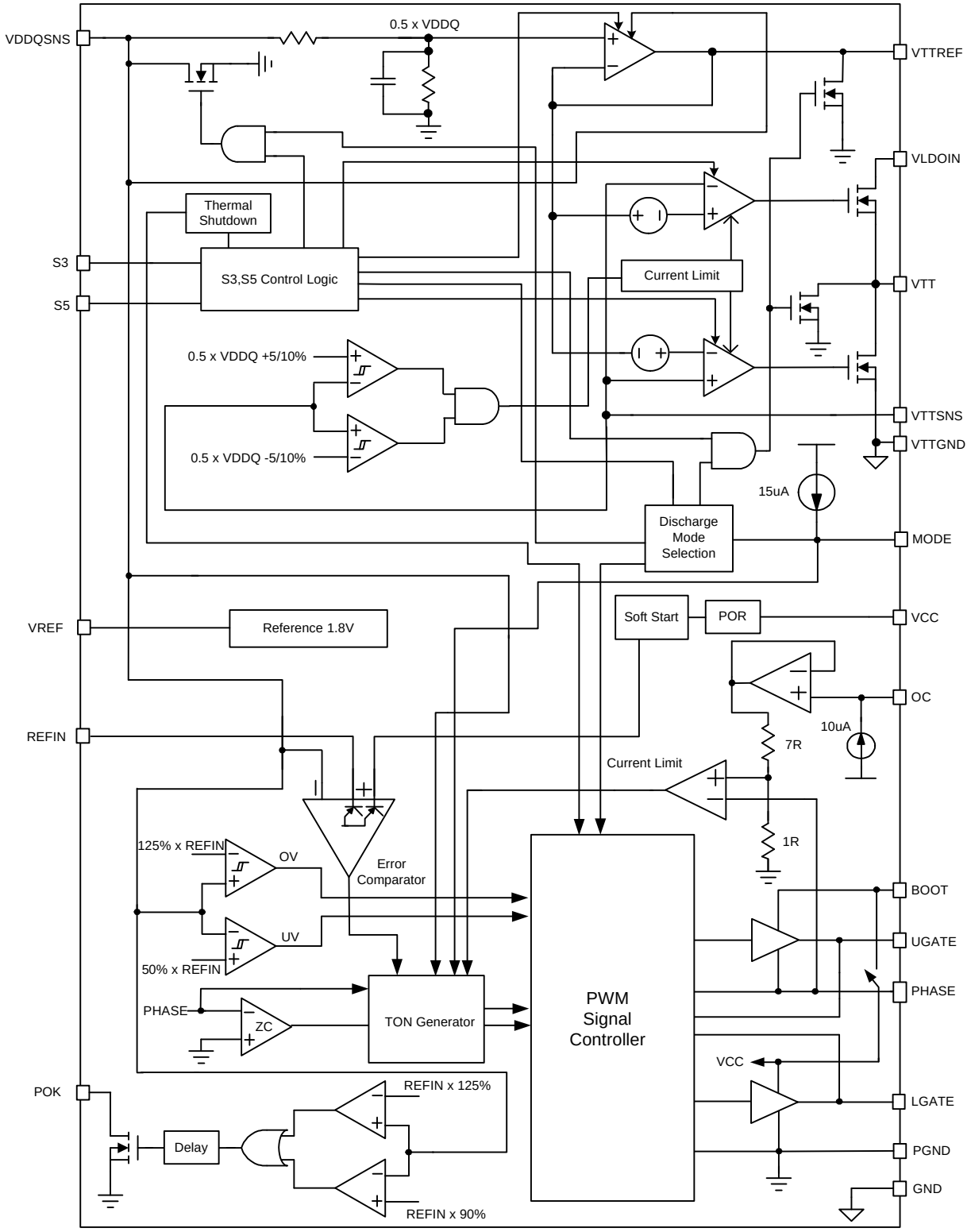


CH1: V_{VDDQ} (1V/div)
CH2: V_{VTT} (500mV/div)
CH3: V_{PHASE} (20V/div)
CH4: I_L (10A/div)
Time: 20µs/div

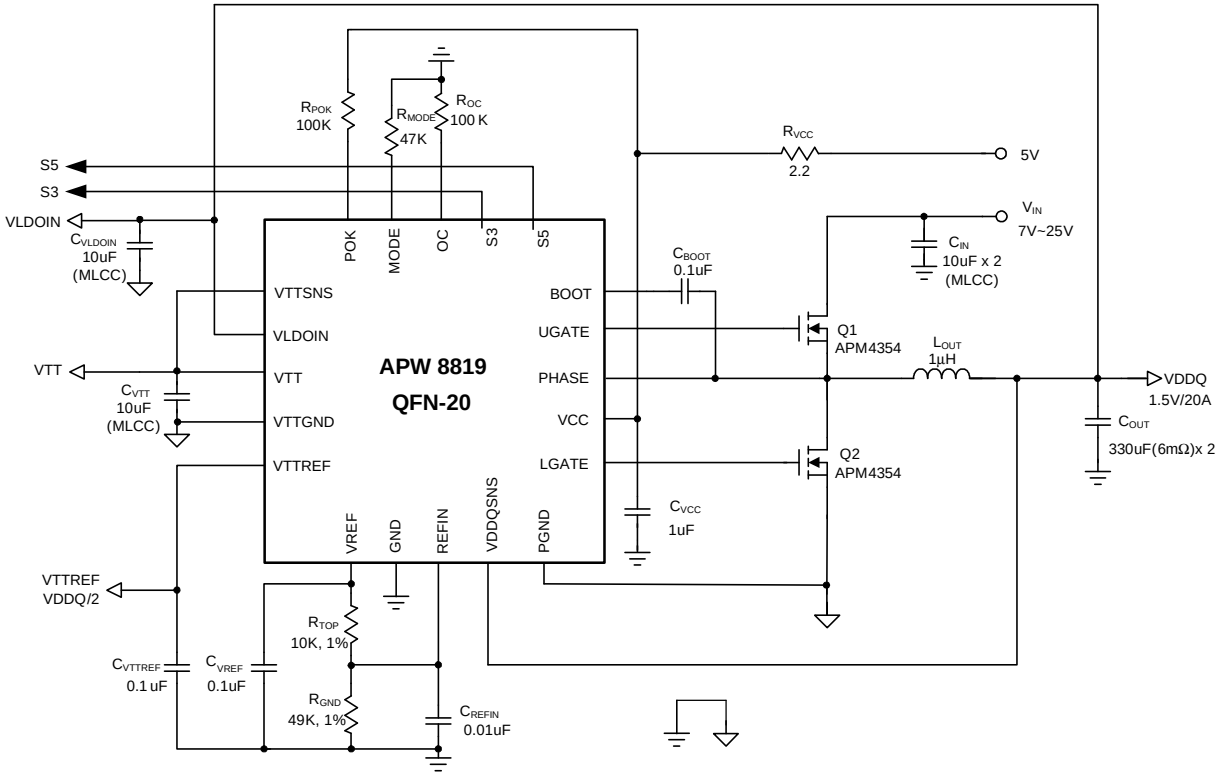
Pin Description

NO.		NAME	FUNCTION
QFN-20	TQFN-16		
1	-	VTTSNS	Voltage sense input for the VTT LDO. Connect to plus terminal of the VTT LDO output capacitor.
2	2	VLDOIN	Supply voltage input for the VTT LDO.
3	3	VTT	Power output for the VTT LDO.
4	-	VTTGND	Power ground output for the VTT LDO.
5	4	VTTREF	VTTREF buffered reference output.
6	5	VREF	1.8V Reference Output. A recommended capacitor with a value of 0.1uF should be attached to the VREF terminal.
7	Thermal Pad	GND	Signal ground for the PWM controller and VTT LDO. Connect to minus terminal of the VTT LDO output capacitor.
8	6	REFIN	Reference input for VDDQ. Programmed by the resistor-divider connected between VREF and GND.
9	7	VDDQSNS	VDDQ reference input for VTT and VTTREF. Power supply for the VTTREF. Discharge current sinking terminal for VDDQ non-tracking discharge. Output voltage feedback input for VDDQ output if VDDQSET pin is connected to VCC or GND.
10	-	PGND	Power ground of the LGATE low-side MOSFET driver. Connect the pin to the Source of the low-side MOSFET. Also it is current sense comparator positive input terminal and the ground of power good circuit.
11	8	LGATE	Output of the low-side MOSFET driver for PWM. Connect this pin to Gate of the low-side MOSFET. Swings from PGND to VCC.
12	9	VCC	Filtered 5V power supply input for internal control circuitry.
13	10	PHASE	Junction point of the high-side MOSFET Source, output filter inductor and the low-side MOSFET Drain. Connect this pin to the Source of the high-side MOSFET. PHASE serves as the lower supply rail for the UGATE high-side gate driver.
14	11	UGATE	Output of the high-side MOSFET driver for PWM. Connect this pin to Gate of the high-side MOSFET.
15	12	BOOT	Supply Input for the UGATE Gate Driver and an internal level-shift circuit. Connect to an external capacitor and diode to create a boosted voltage suitable to drive a logic-level N-channel MOSFET.
16	13	S5	S5 signal input.
17	14	S3	S3 signal input.
18	15	OC	Over-current trip voltage setting input for $R_{DS(ON)}$ current sense scheme. Connect resistor to GND to set over-current threshold at $V_{OC}/8$.
19	16	MODE	Discharge mode and switching frequency setting pin.
20	1	POK	Power-okay output pin. POK is an open drain output used to Indicate the status of the output voltage. When VDDQ output voltage is within the target range, it is in high state.

Block Diagram



Typical Application Circuit



DDR3, 400kHz Application Circuit

Function Description

The APW8819 integrates a synchronous buck PWM controller to generate VDDQ, a sourcing and sinking LDO linear regulator to generate VTT. It provides a complete power supply for DDR2 and DDR3 memory system in 20-pin QFN and 16-pin TQFN packages. User defined output voltage is also possible and can be adjustable from 0.5V to 2V. Input voltage range of the PWM converter is 3V to 28V. The converter runs an adaptive on-time PWM operation at high-load condition and automatically reduces frequency to keep excellent efficiency down to several mA.

The VTT LDO can source and sink up to 1.5A peak current with only 10µF ceramic output capacitor. VTTREF tracks VDDQ/2 within 1% of VDDQ. VTT output tracks VTTREF within 20 mV at no load condition while 40 mV at full load. The LDO input can be separated from VDDQ and optionally connected to a lower voltage by using VLDOIN pin. This helps reducing power dissipation in sourcing phase. The APW8819 is fully compatible to JEDEC DDR2/DDR3 specifications at S3/S5 sleep state (see Table 1). When both VTT and VDDQ are disabled, the part has two options of output discharge function. The tracking discharge mode discharges VDDQ and VTT outputs through the internal LDO transistors and then VTT output tracks half of VDDQ voltage during discharge. The non-tracking discharge mode discharges outputs using internal discharge MOSFETs that are connected to VDDQSNS and VTT. The current capability of these discharge MOSFETs are limited and discharge occurs more slowly than the tracking discharge. Selecting non-discharge mode can disable these discharge functions.

Constant-On-Time PWM Controller with Input Feed-Forward

The constant on-time control architecture is a pseudo-fixed frequency with input voltage feed-forward. This architecture relies on the output filter capacitor's effective series resistance (ESR) to act as a current-sense resistor, so the output ripple voltage provides the PWM ramp signal. In PFM operation, the high-side switch on-time controlled by the on-time generator is determined solely by a one-shot whose pulse width is inversely proportional to input voltage and directly proportional to output voltage.

In PWM operation, the high-side switch on-time is determined by a switching frequency control circuit in the on-time generator block. The switching frequency control circuit senses the switching frequency of the high-side switch and keeps regulating it at a constant frequency in PWM mode. The design improves the frequency variation and be more outstanding than a conventional constant on-time controller which has large switching frequency variation over input voltage, output current and temperature. Both in PFM and PWM, the on-time generator, which senses input voltage on PHASE pin, provides very fast on-time response to input line transients.

Another one-shot sets a minimum off-time (typical: 450ns). The on-time one-shot is triggered if the error comparator is high, the low-side switch current is below the current-limit threshold, and the minimum off-time one-shot has timed out.

Power-On-Reset

A Power-On-Reset (POR) function is designed to prevent wrong logic controls when the VCC voltage is low. The POR function continually monitors the bias supply voltage on the VCC pin if at least one of the enable pins is set high. When the rising VCC voltage reaches the rising POR voltage threshold (4.3V typical), the POR signal goes high and the chip initiates soft-start operations. There is almost no hysteresis to POR voltage threshold (about 100mV typical). When VCC voltage drop lower than 4.2V (typical), the POR disables the chip.

Soft-Start

The APW8819 integrates digital soft-start circuits to ramp up the output voltage of the converter to the programmed regulation set point at a predictable slew rate. The slew rate of output voltage is internally controlled to limit the inrush current through the output capacitors during soft-start process. The figure 1 shows VDDQ soft-start sequence. When the S5 pin is pulled above the rising S5 threshold voltage, the switch regulator wait for 400µs and Mode status is read in this period. And then, the device initiates a soft-start process to ramp up the output voltage. The total soft-start interval is 1.2ms (typical) from S5 goes high to VDDQ ramps up to regulation and independent of the UGATE switching frequency.

Function Description (Cont.)

Soft-Start (Cont.)

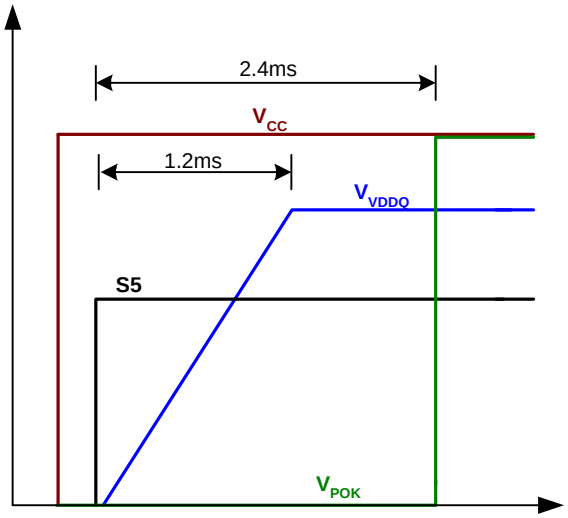


Figure 1. Soft-Start Sequence

During soft-start stage before the POK pin is ready, the under voltage protection is prohibited. The over voltage and current limit protection functions are enabled. If the output capacitor has residue voltage before startup, both low-side and high-side MOSFETs are in off-state until the internal digital soft start voltage equal the VVDDQ voltage. This will ensure the output voltage starts from its existing voltage level.

The VTT LDO part monitors the output current, both sourcing and sinking current, and limits the maximum output current to prevent damages during current overload or short circuit (shorted from VTT to GND or VLDOIN) conditions.

The VTT LDO provides a soft-start function, using the constant current to charge the output capacitor that gives a rapid and linear output voltage rise. If the load current is above the current limit start-up, the VTT cannot start successfully.

APW8819 has an independent counter for each output, but the POK signal indicates only the status of VDDQ and does not indicate VTT power good externally.

Power-Good Output (POK)

POK is an open-drain output and the POK comparator continuously monitors the output voltage. POK is actively held low in shutdown, and standby.

When PWM converter's output voltage is greater than 90% of its target value, the internal open-drain device will be pulled low. After 63µs debounce time, the POK goes high. When the output voltage VDDQ outruns 125% of the target voltage, POK signal will be pulled low immediately.

Under Voltage Protection

In the process of operation, if a short-circuit occurs, the output voltage will drop quickly. When load current is bigger than current limit threshold value, the output voltage will fall out of the required regulation range. The undervoltage continually monitors the setting output voltage after 2.4ms of PWM operations to ensure startup. If a load step is strong enough to pull the output voltage lower than the under voltage threshold (50% of normal output voltage), the internal UVP delay counter begins counting. After 16µs debounce time, the device turns off both high-side and low-side MOSEFET with latched and starts a soft-stop process to shut down the output gradually. Toggling VCC power-on-reset signal can only reset it and bring the chip back to operation.

Over-Voltage Protection (OVP)

The feedback voltage should increase over 125% of the reference voltage due to the high-side MOSFET failure or for other reasons, and the over voltage protection comparator designed with a 1.5µs noise filter will force the low-side MOSFET gate driver to be high. This action actively pulls down the output voltage.

When the OVP occurs, the POK pin will pull down and latch-off the converter. This OVP scheme only clamps the voltage overshoot, and does not invert the output voltage when otherwise activated with a continuously high output from low-side MOSFET driver. It's a common problem for OVP schemes with a latch. Once an over-voltage fault condition is set, toggling VCC power-on-reset signal can only reset it.

Function Description (Cont.)

PWM Converter Current-Limit

The current-limit circuit employs a "valley" current-sensing algorithm (See Figure 2). The APW8819 uses the low-side MOSFET's $R_{DS(ON)}$ of the synchronous rectifier as a current-sensing element. If the magnitude of the current-sense signal at PHASE pin is above the current limit threshold, the PWM is not allowed to initiate a new cycle. The actual peak current is greater than the current limit threshold by an amount equals to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are the functions of the sense resistance, inductor value, and input voltage.

The PWM controller uses the low-side MOSFET's on-resistance $R_{DS(ON)}$ to monitor the current for protection against shortened outputs. The MOSFET's $R_{DS(ON)}$ is varied by temperature and gate to source voltage, the user should determine the maximum $R_{DS(ON)}$ in manufacture's datasheet.

The OC pin can source 10μA through an external resistor for adjusting current-limit threshold. The voltage at OC pin is equal to 10μA x R_{OC}. The relationship between the sampled voltage V_{OC} and the current-limit threshold I_{LIMIT} is given by:

$$\frac{1}{8} \times 10uA \times R_{OC} = I_{LIMIT} \times R_{DS(ON)}$$

Where R_{OC} is the resistor of current-limit setting threshold. $R_{DS(ON)}$ is the low side MOSFETs conducive resistance. ILIMIT is the setting current-limit threshold. I_{LIMIT} can be expressed as I_{OUT} minus half of peak-to-peak inductor current.

The PCB layout guidelines should ensure that noise and DC errors do not corrupt the current-sense signals at PHASE. Place the hottest power MOSEFTs as close to the IC as possible for best thermal coupling. When combined with the under-voltage protection circuit, this current-limit method is effective in almost every circumstance.

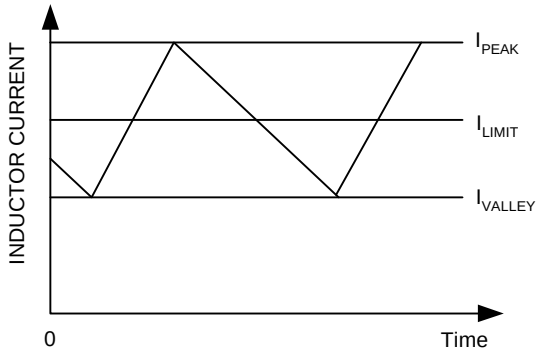


Figure 2. Current-Limit Algorithm

VTT Sink/Source Regulator

The output voltage at VTT pin tracks the reference voltage applied at VTTREF pin. Two internal N-channel MOSFETs controlled by separate high bandwidth error amplifiers regulate the output voltage by sourcing current from VLDOIN pin or sinking current to GND pin. To prevent two pass transistors from shoot-through, a small voltage offset is created between the positive inputs of the two error amplifiers. The VTT with fast response feedback loop keeps tracking to the VTTREF within ±40mV at all conditions including fast load transient.

S3, S5 Control

In the DDR2/DDR3 memory applications, it is important to keep VDDQ always higher than VTT/VTTREF including both start-up and shutdown.

The S3 and S5 signals control the VDDQ, VTT, VTTREF states and these pins should be connected to SLP_S3 and SLP_S5 signals respectively. The table1 shows the truth table of the S3 and S5 pins. When both S3 and S5 are above the logic threshold voltage, the VDDQ, VTT and VTTREF are turned on at S0 state. When S3 is low and S5 is high, the VDDQ and VTTREF are kept on while the VTT voltage is disabled and left high impedance in S3 state. When both S3 and S5 are low, the VDDQ, VTT and VTTREF are turned off and discharged to the ground according to the discharge mode selected by MODE pin during S4/S5 state.

Function Description (Cont.)

S3, S5 Control (Cont.)

Table1: The Truth Table of S3 and S5 Pins.

STATE	S3	S5	VDDQ	VTTREF	VTT
S0	H	H	1	1	1
S3	L	H	1	1	0 (high-Z)
S4/5	L	L	0 (discharge)	0 (discharge)	0 (discharge)

VDDQ and VTT Discharge Control

APW8819 discharges VDDQ, VTTREF and VTT outputs during S3 and S5 are both low. There are two different discharge modes. A 15μA current is sourced from MODE pin across R_{MODE} resistor connected between MODE pin to GND. Table 2 shows R_{MODE} values, corresponding switching frequency and discharge mode configuration.

Table 2. MODE Selection.

MODE	R_{MODE}(kΩ)	F_{SW}(kHz)	DISCHARGE MODE
0	47	400	Non-Tracking
1	68	300	
2	100	300	Tracking
3	200	400	
4	Open	500	Tracking

When in tracking-discharge mode, APW8819 discharges outputs through the internal VTT regulator transistors and VTT output tracks half of VDDQ voltage during this discharge. Note that VDDQ discharge current flows via VLDOIN to VTTGND thus VLDOIN must be connected to VDDQ output in this mode. The internal LDO can handle up to 1.5A and discharge quickly. After VDDQ is discharged down to 0.2V, the internal LDO is turned off and the operation mode is changed to the non-tracking discharge mode.

When in non-tracking-discharge mode, APW8819 discharges outputs using internal MOSFETs that are connected to VDDQSNS and VTT. The current capability of these MOSFETs is limited to discharge slowly.

Note that VDDQ discharge current flows from VDDQSNS to PGND in this mode. In case of no discharge mode, APW8819 does not discharge output charge at all.

Thermal Shutdown

A thermal shutdown circuit limits the junction temperature of APW8819. When the junction temperature exceeds +160°C, PWM converter, VTTLDO and VTTREF are shut off, allowing the device to cool down. The regulator regulates the output again through initiation of a new soft-start cycle after the junction temperature cools by 25°C, resulting in a pulsed output during continuous thermal overload conditions. The thermal shutdown designed with a 25°C hysteresis lowers the average junction temperature during continuous thermal overload conditions, extending life time of the device.

For normal operation, device power dissipation should be externally limited so that junction temperatures will not exceed +125°C.

Application Information

Output Voltage Selection

The Output VDDQSNS Voltage is defined by REFIN voltage. The APW8819 provides a 1.8V voltage reference from VREF. In normal application circuit, the VREF output voltage drive the REFIN input voltage through a voltage divider circuit. The VDDQ output range is between 0.75 V and 1.8V, programmed by the resister-divider connected between VREF and GND. For stability operation, connecting a few nano farads of capacitance from REFIN to GND is necessary.

Output Inductor Selection

The duty cycle of a buck converter is the function of the input voltage and output voltage. Once an output voltage is fixed, it can be written as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

The inductor value determines the inductor ripple current and affects the load transient reponse. Higher inductor value reduces the inductor's ripple current and induces lower output ripple voltage. The ripple current and ripple voltage can be approxminated by:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{F_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}}$$

Where F_{SW} is the switching frequency of the regulator. Although increase the inductor value and frequency reduce the ripple current and voltage, there is a tradeoff between the inductor's ripple current and the regulator load transient response time.

A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current. Increasing the switching frequency (F_{SW}) also reduces the ripple current and voltage, but it will increase the switching loss of the MOSFETs and the power dissipation of the converter. The maximum ripple current occurs at the maximum input voltage. A good starting point is to choose the ripple current to be approximately 30% of the maximum output current. Once the inductance value has been chosen, selecting an inductor is capable of carrying the required peak current without going into saturation.

In some types of inductors, especially core that is made of ferrite, the ripple current will increase abruptly when it saturates. This will be result in a larger output ripple voltage.

Output Capacitor Selection

Output voltage ripple and the transient voltage deviation are factors that have to be taken into consideration when selecting an output capacitor. Higher capacitor value and lower ESR reduce the output ripple and the load transient drop. Therefore, selecting high performance low ESR capacitors is intended for switching regulator applications. In addition to high frequency noise related MOSFET turn-on and turn-off, the output voltage ripple includes the capacitance voltage drop and ESR voltage drop caused by the AC peak-to-peak current. These two voltages can be represented by:

$$\Delta V_{COUT} = \frac{I_{RIPPLE}}{8 C_{OUT} F_{SW}}$$

$$\Delta V_{ESR} = I_{RIPPLE} \times R_{ESR}$$

These two components constitute a large portion of the total output voltage ripple. In some applications, multiple capacitors have to be paralleled to achieve the desired ESR value. If the output of the converter has to support another load with high pulsating current, more capacitors are needed in order to reduce the equivalent ESR and suppress the voltage ripple to a tolerable level. A small decoupling capacitor in parallel for bypassing the noise is also recommended, and the voltage rating of the output capacitors must also be considered.

To support a load transient that is faster than the switching frequency, more capacitors have to be used to reduce the voltage excursion during load step change. Another aspect of the capacitor selection is that the total AC current going through the capacitors has to be less than the rated RMS current specified on the capacitors to prevent the capacitor from over-heating.

Application Information (Cont.)

Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, select the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage. The maximum RMS current rating requirement is approximately $I_{OUT}/2$, where I_{OUT} is the load current. During power up, the input capacitors have to handle large amount of surge current. In low-duty notebook appliactions, ceramic capacitors are remmended. The capacitors must be connected between the drain of high-side MOSFET and the source of low-side MOSFET with very low-impeadance PCB layout.

MOSFET Selection

The application for a notebook battery with a maximum voltage of 24V, at least a minimum 30V MOSFETs should be used. The design has to trade off the gate charge with the $R_{DS(ON)}$ of the MOSFET:

- For the low-side MOSFET, before it is turned on, the body diode has been conducted. The low-side MOSFET driver will not charge the miller capacitor of this MOSFET.
- In the turning off process of the low-side MOSFET, the load current will shift to the body diode first. The high dv/dt of the phase node voltage will charge the miller capacitor through the low-side MOSFET driver sinking current path. This results in much less switching loss of the low-side MOSFETs. The duty cycle is often very small in high battery voltage applications, and the low-side MOSFET will conduct most of the switching cycle; therefore, the $R_{DS(ON)}$ of the low-side MOSFET, the less the power loss. The gate charge for this MOSFET is usually a secondary consideration. The high-side MOSFET does not have this zero voltage switching condition, and because it conducts for less time compared to the low-side MOSFET, the switching loss tends to be dominant. Priority should be given to the MOSFETs with less gate charge, so that both the gate driver loss and switching loss will be minimized.

The selection of the N-channel power MOSFETs are determined by the $R_{DS(ON)}$, reversing transfer capacitance (C_{RSS}) and maximum output current requirement. The losses in the MOSFETs have two components: conduction loss and transition loss. For the high-side and low-side MOSFETs, the losses are approximately given by the following equations :

$$P_{high\text{-}side} = I_{OUT}^{2}(1+TC)(R_{DS(ON)})D + (0.5)(I_{OUT})(V_{IN})(t_{SW})F_{SW}$$

$$P_{low\text{-}side} = I_{OUT}^{2}(1+TC)(R_{DS(ON)})(1-D)$$

Where

I_{OUT} is the load current
TC is the temperature dependency of $R_{DS(ON)}$
F_{SW} is the switching frequency
t_{SW} is the switching interval
D is the duty cycle

Note that both MOSFETs have conduction losses while the high-side MOSFET includes an additional transition loss. The switching internal, t_{SW}, is the function of the reverse transfer capacitance C_{RSS}. The (1+TC) term is to factor in the temperature dependency of the $R_{DS(ON)}$ and can be extracted from the "$R_{DS(ON)}$ vs Temperature" curve of the power MOSFET..

Layout Consideration

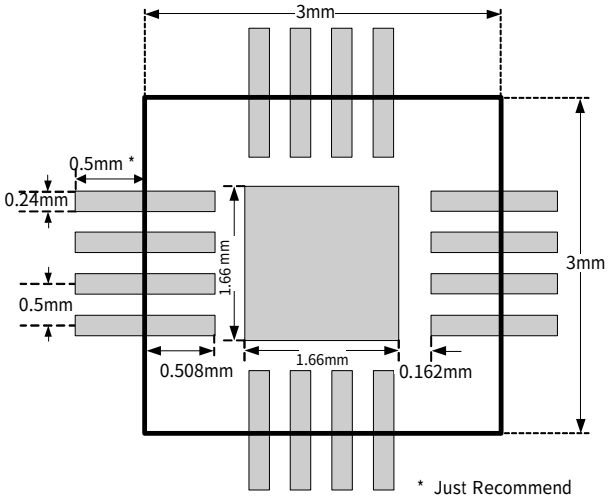
In any high switching frequency converter, a correct layout is important to ensure proper operation of the regulator. With power devices switching at higher frequency, the resulting current transient will cause voltage spike across the interconnecting impedance and parasitic circuit elements. As an example, consider the turn-off transition of the PWM MOSFET. Before turn-off condition, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is freewheeling by the lower MOSFET and parasitic diode. Any parasitic inductance of the circuit generates a large voltage spike during the switching interval. In general, using short and wide printed circuit traces should minimize interconnecting impedances and the magnitude of voltage spike. And signal and power grounds are to be kept separating and finally combined to use the ground plane construction or single point grounding. The best tie-point between the signal ground and the power ground is at the negative side of the output capacitor on each channel, where there is less noise. Noisy traces beneath the IC are not recommended. Below is a checklist for your layout:

Application Information (Cont.)

Layout Consideration (Cont.)

- Keep the switching nodes (UGATE, LGATE, BOOT, and PHASE) away from sensitive small signal nodes (VREF, REFIN, VTTREF, OC, and MODE) since these nodes are fast mov ing signals. Therefore, keep traces to these nodes as short as possible and there should be no other weak signal traces in parallel with theses traces on any layer.
- The signals going through theses traces have both high dv/dt and high di/dt, with high peak charging and discharging current. The traces from the gate drivers to the MOSFETs (UGATE and LGATE) should be short and wide.
- Place the source of the high-side MOSFET and the drain of the low-side MOSFET as close as possible. Minimizing the impedance with wide layout plane between the two pads reduces the voltage bounce of the node.
- Decoupling capacitor, the resistor dividers, boot capacitors, and current limit stetting resistor should be close their pins. (For example, place the decoupling ceramic capacitor near the drain of the high-side MOSFET as close as possible. The bulk capacitors are also placednear the drain). And need to noted, connecting capacitor with OC pin is forbidden.
- The input capacitor should be near the drain of the up per MOSFET; the high quality ceramic decoupling capacitor can be put close to the VCC and GND pins; the VTTREF decoupling capacitor should be close to the VTTREF pin and GND; A capacitor with a value of 0.1µF or larger should be close to the VREF terminal; the REFIN decoupling capacitor should be close to the REFIN pin and GND; the VDDQ and VTT output capacitors should be located right across their output pin as clase as possible to the part to minimize parasitics. The input capacitor GND should be close to the output capacitor GND and the lower MOSFET GND.
- The drain of the MOSFETs (PHASE node) should be a large plane for heat sinking. And PHASE pin traces are also the return path for UGATE. Connect this pin to the converter's upper MOSFET source.
- The PGND trace should be a separate trace, and inde pendently go to the source of the low-side MOSFETs for current limit accuracy.

TQFN3X3-16



QFN3x3-20

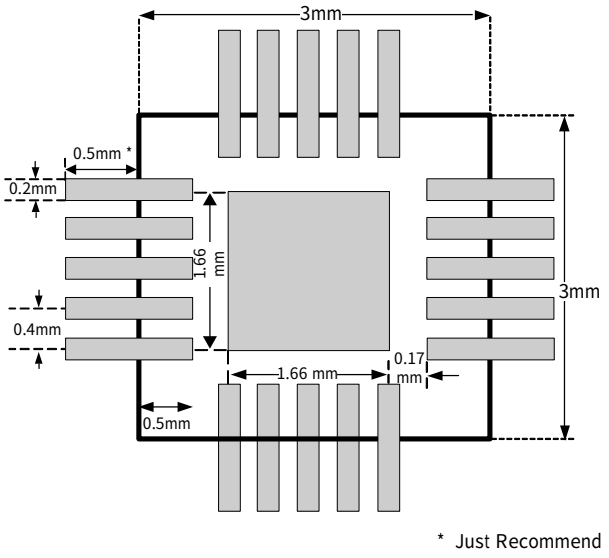
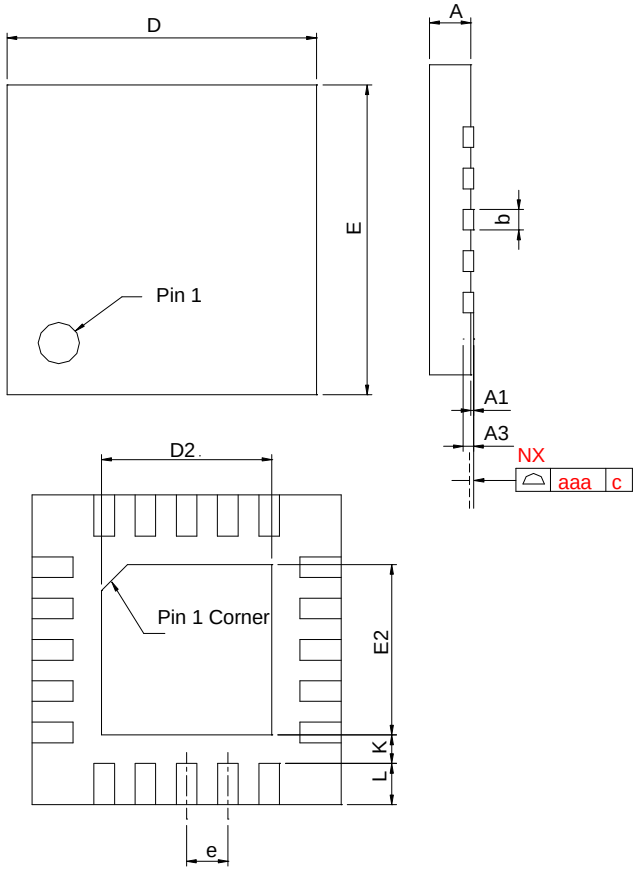


Figure3. Recommended Minimum Footprint

Package Information

QFN3x3-20

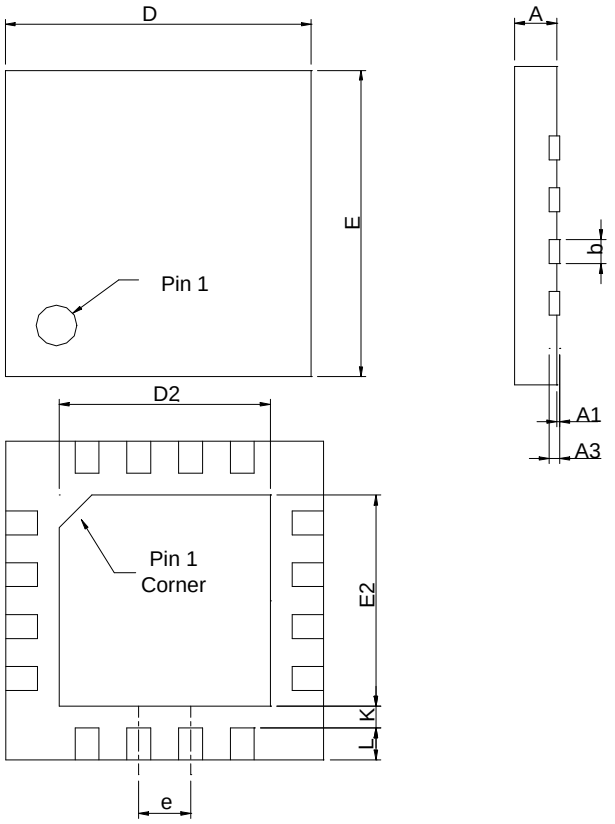


SYMBOL	QFN3x3-20			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.15	0.25	0.006	0.010
D	2.90	3.10	0.114	0.122
D2	1.50	1.80	0.059	0.071
E	2.90	3.10	0.114	0.122
E2	1.50	1.80	0.059	0.071
e	0.40 BSC		0.016 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	
aaa	0.08		0.003	

Note : 1. Followed from JEDEC MO-220 WEEE

Package Information

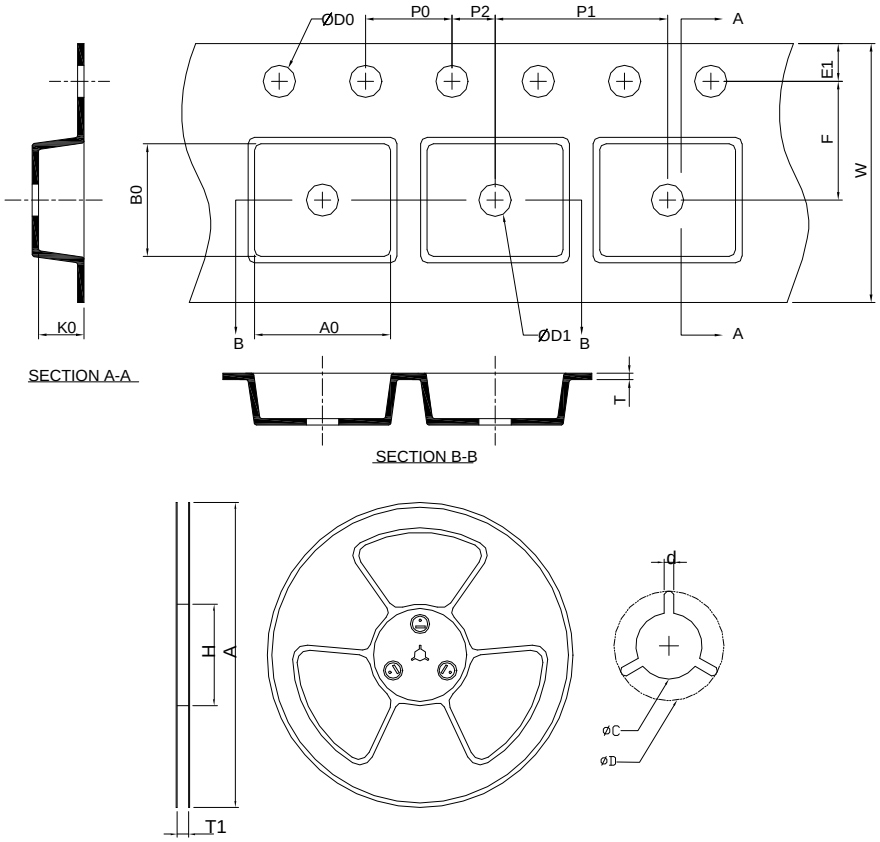
TQFN3x3-16



SYMBOL	TQFN3x3-16			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	2.90	3.10	0.114	0.122
D2	1.50	1.80	0.059	0.071
E	2.90	3.10	0.114	0.122
E2	1.50	1.80	0.059	0.071
e	0.50 BSC		0.020 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	

Note : Follow JEDEC MO-220 WEED-4.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
QFN3X3-20	330±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30±0.20	3.30±0.20	1.30±0.20
TQFN3x3-16	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
	330±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30±0.20	3.30±0.20	1.30±0.20

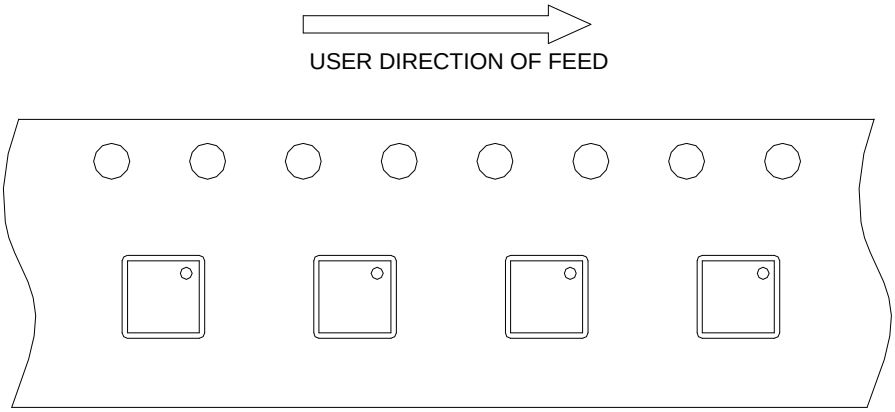
(mm)

Devices Per Unit

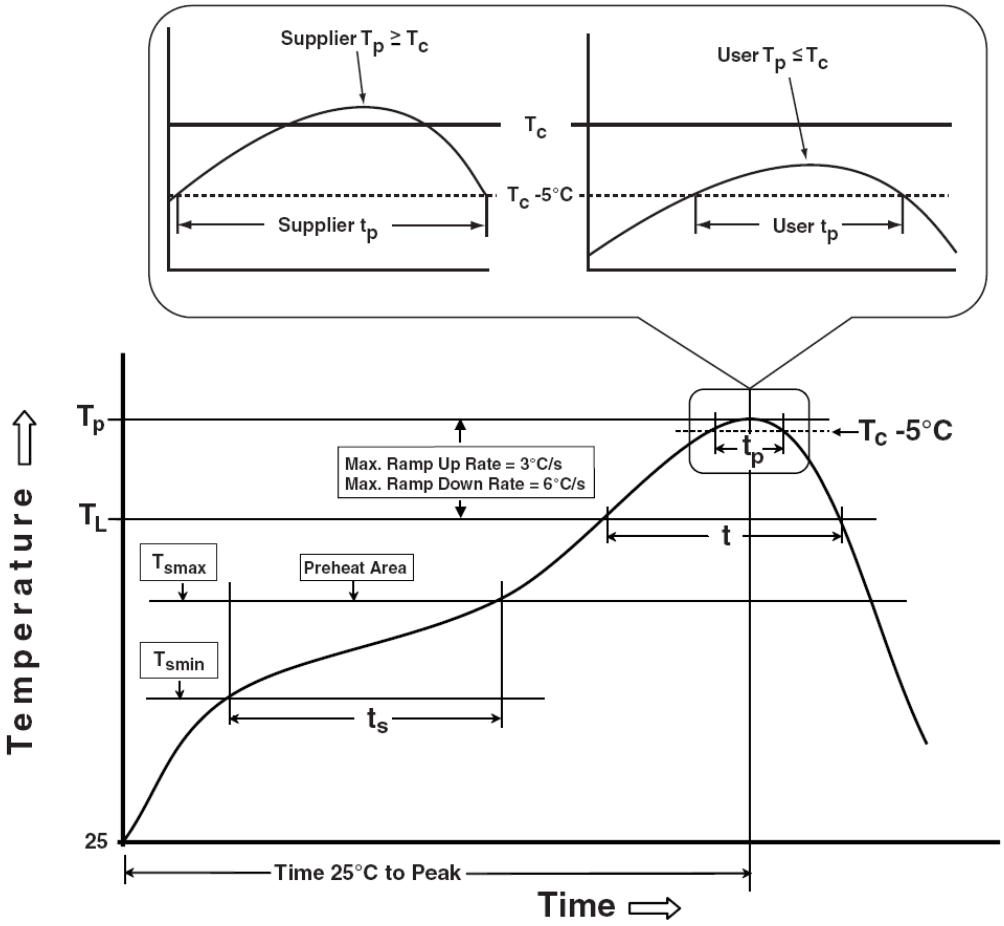
Package Type	Unit	Quantity
QFN3x3-20	Tape & Reel	3000
TQFN3x3-16	Tape & Reel	3000

Taping Direction Information

QFN3x3-20 & TQFN3x3-16



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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