High-Speed 2:4 Differential Multiplexer / Demultiplexer

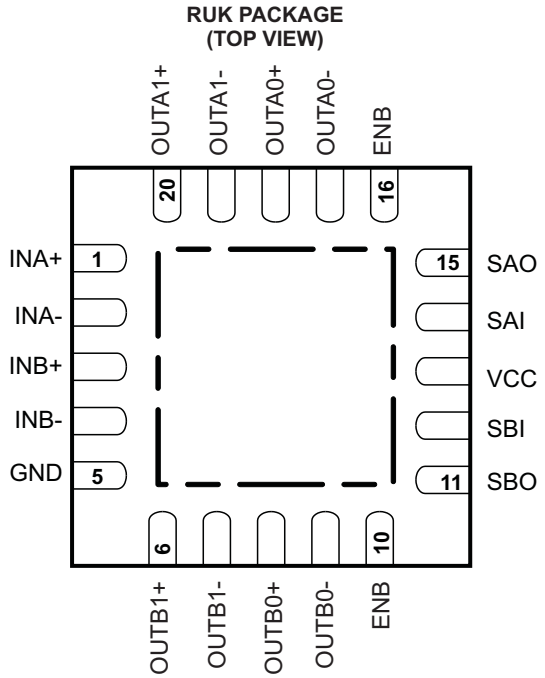
Check for Samples: TS3DS10224

FEATURES

- **2:4 Differential Multiplexer/Demultiplexer**
- **Bidirectional Operation**
- **Can be used in**
  - **Single 1:4 Configuration**
  - **Dual 1:2 Configuration**
  - **Fan out 1:2 Configuration**
- **High BW (1.2 GHz Typ)**
- **Low R_{ON} and C_{ON}:**
  - **13 Ω R_{ON} Typ**
  - **9 pF C_{ON} Typ**
- **ESD Performance (I/O Pins)**
  - **±8-kV Contact Discharge (IEC61000-4-2)**
  - **2-kV Human Body Model per JESD22-A114E (to GND)**
- **ESD Performance (All Pins)**
  - **2-kV Human Body Model per JESD22-A114E**
- **Small QFN package (3 x 3 mm, 0.4-mm pitch)**

APPLICATIONS

- **Desktop/Notebooks Computers**
- **DisplayPort Auxiliary Channel Multiplexing**
- **USB 2.0 Multiplexing**
- **Netbooks/eBooks/Tablets**



DESCRIPTION

The TS3DS10224 is a 2:4 bidirectional multiplexer for high-speed differential and single ended signal applications (up to 720 Mbps). The TS3DS10224 can be used in a 1:4 or dual 1:2 multiplexer/demultiplexer configuration. The TS3DS10224 offers a high BW of 1.2 GHz with channel R_{ON} of 13 Ω (Typ).

The TS3DS10224 can also be used to fan out a differential or single ended signal pair to two ports simultaneously (fan-out configuration). The BW performance is lower in this configuration.

The TS3DS10224 operates with a 3 to 3.6V power supply. It features ESD protection of up to ±8-kV contact discharge and 2-kV Human Body Model on its I/O pins.

The TS3DS10224 provides fail-safe protection by isolating the I/O pins with high impedance when the power supply (V_{CC}) is not present.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	PACKAGE(1)(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN	Tape and Reel	TS3DS10224RUKR	ZTB

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

PIN FUNCTIONS

PIN NAME	PIN TYPE	DESCRIPTION
SAI	Input	Control input
SAO	Input	Control input
SBI	Input	Control input
SBO	Input	Control input
ENA	Input	Enable
INA+	I/O	Input A
INA–	I/O	Input A
ENB	Input	Enable
INB+	I/O	Input B
INB-	I/O	Input B
OUTB0–	I/O	Output B0
OUTB0+	I/O	Output B0
OUTB1–	I/O	Output B1
OUTB1+	I/O	Output B1
GND	Ground	Ground
VCC	Power	Power supply
OUTA0–	I/O	Output A0
OUTA0+	I/O	Output A0
OUTA1–	I/O	Output A1
OUTA1+	I/O	Output A1

LOGIC DIAGRAM

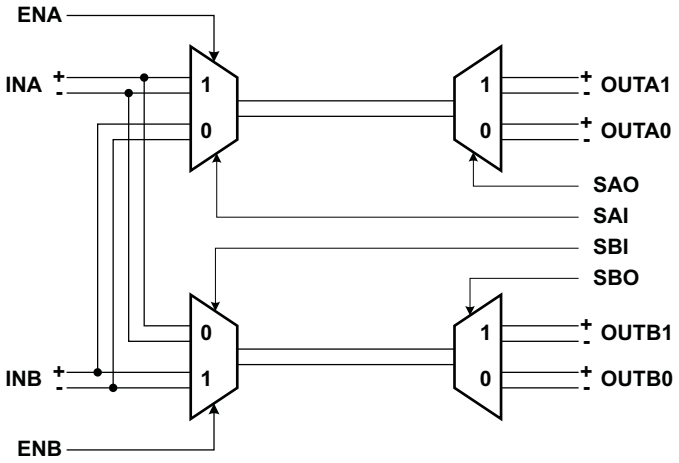


Table 1. FUNCTION TABLE

ENA, ENB	OUTA0	OUTA1	OUTB0	OUTB1
00	Hi-Z	Hi-Z	Hi-Z	Hi-Z
01	Hi-Z	Hi-Z	–	–
10	–	–	Hi-Z	Hi-Z
11	–	–	–	–

SAI, SAO, SBI, SBO	OUTA0	OUTA1	OUTB0	OUTB1
0000	INB	–	INA	–
0001	INB	–	–	INA
0010	INB	–	INB	–
0011	INB	–	–	INB
0100	–	INB	INA	–
0101	–	INB	–	INA
0110	–	INB	INB	
0111	–	INB	–	INB
1000	INA	–	INA	–
1001	INA	–	–	INA
1010	INA	–	INB	–
1011	INA	–	–	INB
1100	–	INA	INA	–
1101	–	INA	–	INA
1110	–	INA	INB	–
1111	–	INA	–	INB

CONFIGURATIONS

1. Single 1:4 Configuration

   In this configuration either INA or INB is not connected and the other input can be multiplexed/demultiplexed to either of the four outputs.

2. Dual 1:2 Configuration

   In this configuration SAI and SBI are both connected to V_{CC}. SAO and SBO are used to control two separate 1:2 multiplexers/demultiplexers.

3. Fan out 1:2 Configuration

   In this configuration either INA or INB can be multiplexed to both OUTAx and OUTBx simultaneously. There is an impact on the device characteristics.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.3	4.0	V
$V_{I/O}$	Analog I/O voltage range(2)(3)(4)		–0.3	V_{CC} + 0.3	V
$I_{I/O}$	ON-state switch current(5)			±100	mA
I_{CC}	Continuous current through VCC or GND			±100	
V_{IN}	Control input voltage range(2)(3)		–0.3	V_{CC} + 0.3	V
θ_{JA}	Package thermal impedance(6)	RUK package		82.7	°C/W
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses above these ratings may cause permanent damage. These are stress ratings only, and functional operation of the device at these or any other conditions beyond the recommended operating conditions is not implied. Exposure to absolute maximum conditions for extended periods may degrade device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) VI and VO are used to denote specific conditions for VI/O.
(5) II and IO are used to denote specific conditions for II/O
(6) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS(1)(2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	3	3.6	V
V_{IH}	High-level control input voltage	0.75 x V_{CC}	V_{CC}	V
V_{IL}	Low-level control input voltage	0	0.6	V
$V_{I/O}$	Input/Output voltage	0	V_{CC}	V
T_A	Operating free-air temperature	–40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.
(2) It is recommended to pull down to ground unused I/O pins through a 1-kΩ resistor.

ELECTRICAL CHARACTERISTICS(1)

For Single 1:4 or Dual 1:2 configurations. T_A = –40°C to 85°C, Typical values are at V_{CC} = 3.3V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
V_{IK}	Digital input clamp voltage	V_{CC} = 3.6 V, I_I = –18 mA	–1.2	-0.9		V
I_{IN}	Digital input leakage current	V_{CC} = 3.6 V, V_{IN} = 0 to 3.6 V			±2	µA
I_{OZ}(3)		V_{CC} = 3.6 V, V_O = 0 V to 3.6 V, V_I = 0 V, Switch OFF			±2	µA
I_{OFF}	Power off leakage current	V_{CC} = 0 V, V_{IN} = V_{CC} or GND,$V_{I/O}$ = 0 V to 3.6 V			±5	µA
I_{CC}	Supply current	V_{CC} = 3.6 V, $I_{I/O}$ = 0, Switch ON or OFF		50	100	µA
C_{IN}	Digital input capacitance	V_{CC} = 3.3 V, V_{IN} = V_{CC} or GND		3	5	pF
$C_{I/O(OFF)}$	OFF capacitance	V_{CC} = 3.3 V, $V_{I/O}$ = 3.3 V or 0, f = 10 MHz, Switch OFF		6	7	pF
$C_{I/O(ON)}$	ON capacitance	V_{CC} = 3.3 V, $V_{I/O}$ = 3.3 V or 0, f = 10 MHz, Switch ON		9	10	pF
r_{on}	ON state resistance	V_{CC} = 3.6 V, V_I = V_{CC}, I_O = –30 mA		13	19	Ω
		V_{CC} = 3.3 V, V_I = 0.5V, I_O = –30 mA		10		Ω
Δr_{on}	ON state resistance match between channels	V_{CC} = 3 V, V_I = 0 to V_{CC}, I_O = –30 mA		2	2.5	Ω
$r_{on(flat)}$	ON state resistance flatness	V_{CC} = 3 V, V_I = 1.5 V and V_{CC}, I_O = –30 mA		4	6	Ω

(1) V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.
(2) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.

DYNAMIC CHARACTERISTICS

For Single 1:4 or Dual 1:2 configurations. T_A = –40°C to 85°C, Typical values are at V_{CC} = 3.3 V ± 10% and T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	UNIT
BW	Bandwidth	R_L = 50 Ω, Switch ON	1.2	GHz
O_{ISO}	OFF Isolation	R_L = 50 Ω , f = 250 MHz	–30	dB
X_{TALK}	Crosstalk	R_L = 50 Ω , f = 250 MHz	–30	dB

SWITCHING CHARACTERISTICS

For Single 1:4 or Dual 1:2 configurations. Over operating range, T_A = –40°C to 85°C, V_{CC} = 3.3 V ±10%, GND = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd} (1)		R_L = 50 Ω, C_L = 2 pF		50		ps
t_{ON}	SAI/SAO/SBI/SBO to OUTAx/OUTBx	R_L = 50 Ω, C_L = 2 pF		40	100	ns
t_{OFF}	SAI/SAO/SBI/SBO to OUTAx/OUTBx	R_L = 50 Ω, C_L = 2 pF		20	30	ns
$t_{sk(o)}$ (2)		R_L = 50 Ω, C_L = 2 pF		40		ps
$t_{sk(p)}$(3)		R_L = 50 Ω, C_L = 2 pF		40		ps

(1) The propagation delay is the calculated RC time constant of the typical ON-State resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).
(2) Output skew between center channel and any other channel.
(3) Skew between opposite transitions of the same output ($|t_{PHL} – t_{PLH}|$).

ELECTRICAL CHARACTERISTICS(1)

For fan-out 1:2 configurations. T_A = –40°C to 85°C, Typical values are at V_{CC} = 3.3V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
V_{IK}	Digital input clamp voltage	V_{CC} = 3.6 V, I_I = –18 mA	-1.2	-0.9		V
I_{IN}	Digital input leakage current	V_{CC} = 3.6 V, V_{IN} = 0 to 3.6 V			±2	µA
I_{OZ}(3)		V_{CC} = 3.6 V, V_O = 0 V to 3.6 V, V_I = 0 V, Switch OFF			±2	µA
I_{OFF}	Power off leakage current	V_{CC} = 0 V, V_{IN} = V_{CC} or GND, $V_{I/O}$ = 0 V to 3.6 V			±5	µA
I_{CC}	Supply current	V_{CC} = 3.6 V, $I_{I/O}$ = 0, Switch ON or OFF		50	100	µA
C_{IN}	Digital input capacitance	V_{CC} = 3.3 V, V_{IN} = V_{CC} or GND		3	5	pF
$C_{I/O(OFF)}$	OFF capacitance	V_{CC} = 3.3 V, $V_{I/O}$ = 3.3 V or 0, f = 10 MHz, Switch OFF		6	7	pF
$C_{I/O(ON)}$	ON capacitance	V_{CC} = 3.3 V, $V_{I/O}$ = 3.3 V or 0, f = 10 MHz, Switch ON		12	13	pF
r_{on}	ON state resistance	V_{CC} = 3.6 V, V_I = V_{CC}, I_O = –30 mA		13	19	Ω
Δr_{on}	ON state resistance match between channels	V_{CC} = 3 V, V_I = 0 to V_{CC}, I_O = –30 mA		2	2.5	Ω
$r_{on(flat)}$	ON state resistance flatness	V_{CC} = 3 V, V_I = 1.5 V and V_{CC}, I_O = –30 mA		4	6	Ω

(1) V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.
(2) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.

DYNAMIC CHARACTERISTICS

For fan-out 1:2 configurations. T_A = –40°C to 85°C, Typical values are at V_{CC} = 3.3 V ± 10% and T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	UNIT
BW	Bandwidth	R_L = 50 Ω, Switch ON	500	MHz
O_{ISO}	OFF Isolation	R_L = 50 Ω , f = 250 MHz	–30	dB
X_{TALK}	Crosstalk	R_L = 50 Ω , f = 250 MHz	–30	dB

SWITCHING CHARACTERISTICS

For fan-0ut 1:2 configurations. Over operating range, T_A = –40°C to 85°C, V_{CC} = 3.3 V ±10%, GND = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd} (1)		R_L = 50 Ω, C_L = 2 pF		140		ps
t_{ON}	SAI/SAO/SBI/SBO to OUTAx/OUTBx	R = 50 Ω, C_L = 2 pF		40	100	ns
t_{OFF}	SAI/SAO/SBI/SBO to OUTAx/OUTBx	R_{LL} = 50 Ω, C_L = 2 pF		20	30	ns
$t_{sk(o)}$ (2)		R_L = 50 Ω, C_L = 2 pF		60		ps
$t_{sk(p)}$ (3)		R_L = 50 Ω, C_L = 2 pF		60		ps

(1) The propagation delay is the calculated RC time constant of the typical ON-State resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).
(2) Output skew between center channel and any other channel.
(3) Skew between opposite transitions of the same output ($|t_{PHL} – t_{PLH}|$).

TYPICAL CHARACTERISTICS (Single 1:4 or Dual 1:2 configurations)

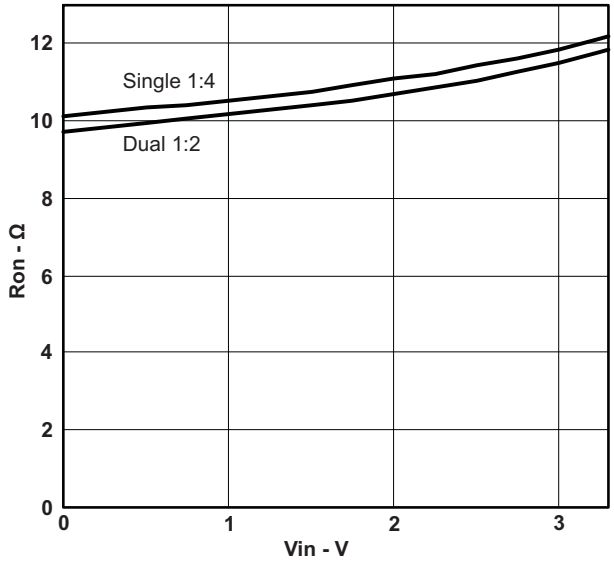


Figure 1. ON-Resistance vs. Vout

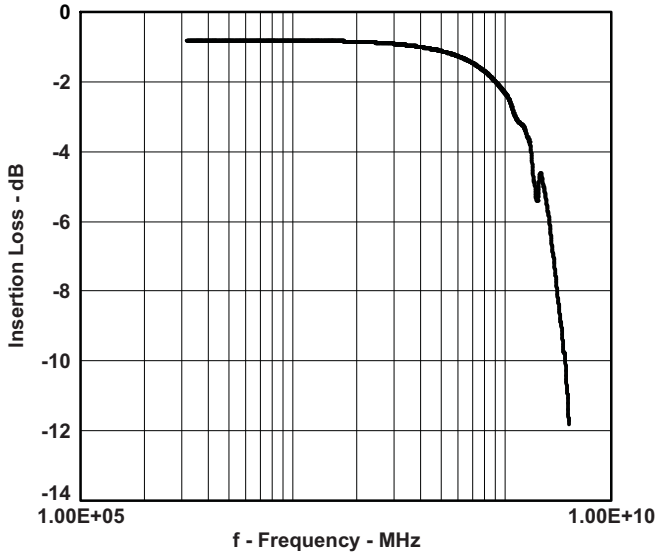


Figure 2. Insertion loss vs. Frequency

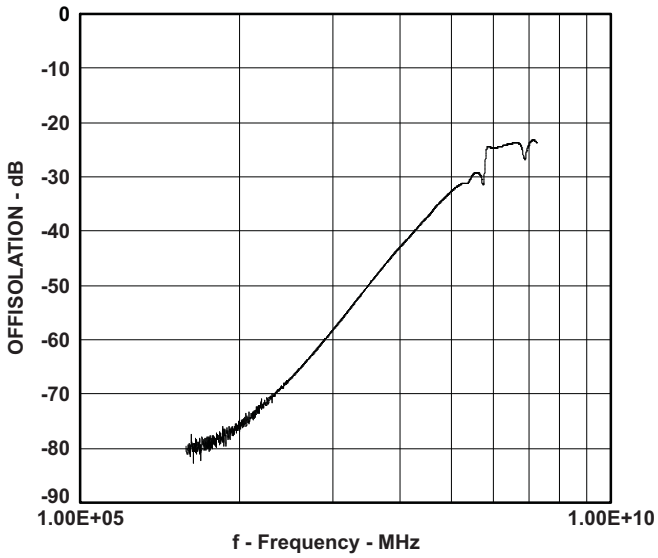


Figure 3. Off Isolation vs. Frequency

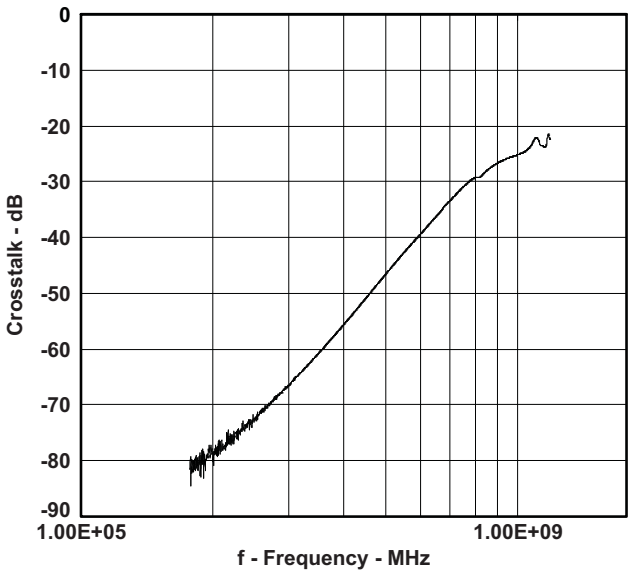


Figure 4. Crosstalk vs. Frequency

TYPICAL CHARACTERISTICS (Fan out 1:2 configurations)

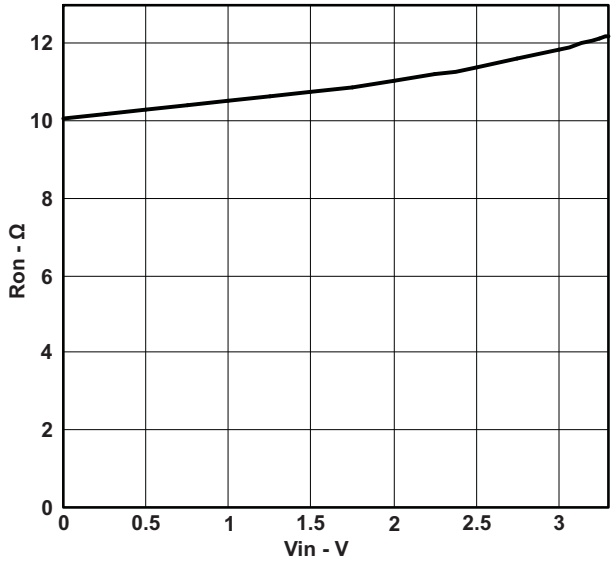


Figure 5. ON-Resistance vs. Vout

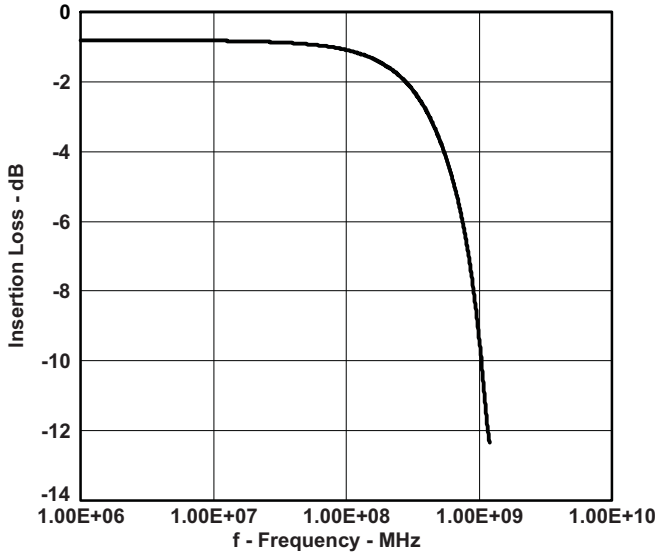


Figure 6. Insertion loss vs. Frequency

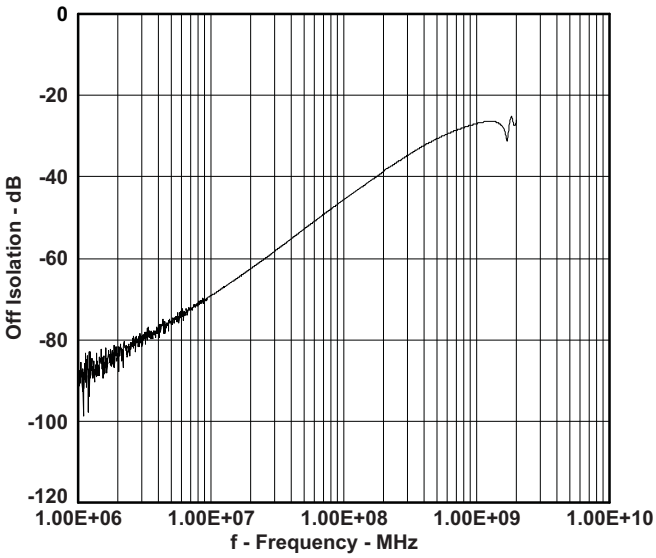


Figure 7. Off Isolation vs. Frequency

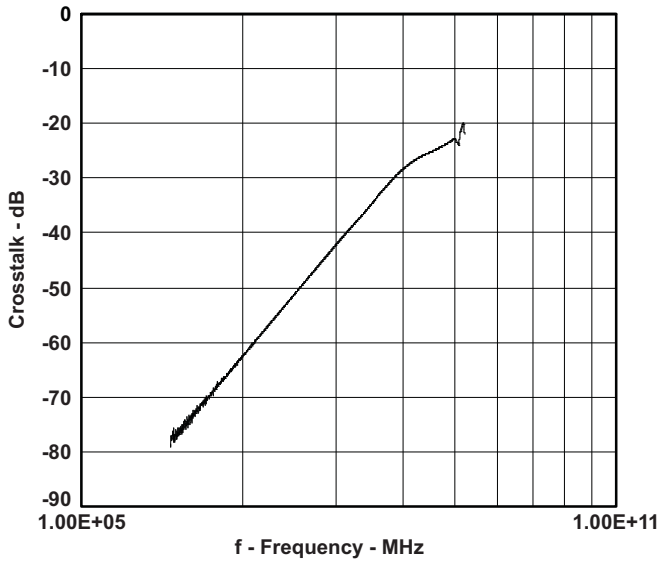
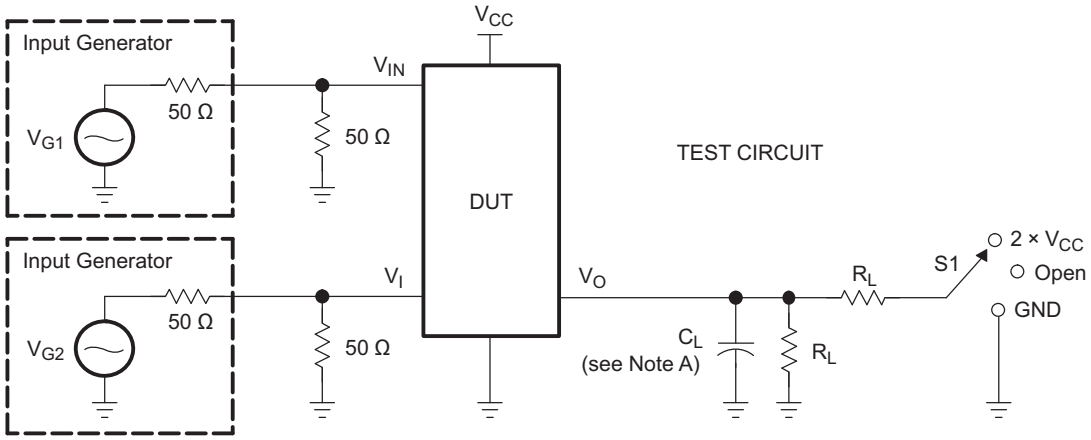
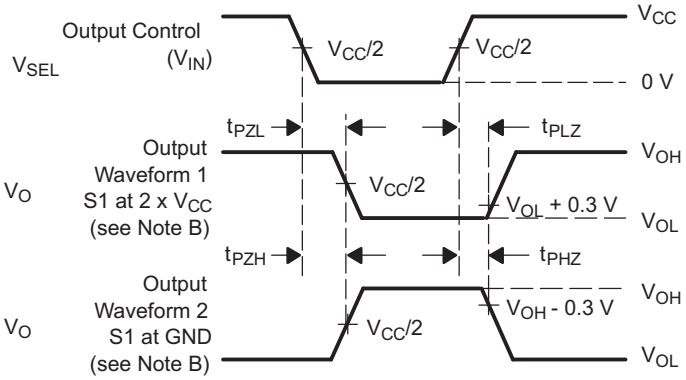


Figure 8. Crosstalk vs. Frequency

PARAMETER MEASUREMENT INFORMATION



TEST	V_{CC}	S1	R_L	V_{in}	C_L	V_Δ
t_{PLZ}/t_{PZL}	3.3 V ± 0.3 V	2 × V_{CC}	50 Ω	GND	2 pF	0.3 V
t_{PHZ}/t_{PZH}	3.3 V ± 0.3 V	GND	50 Ω	V_{CC}	2 pF	0.3 V

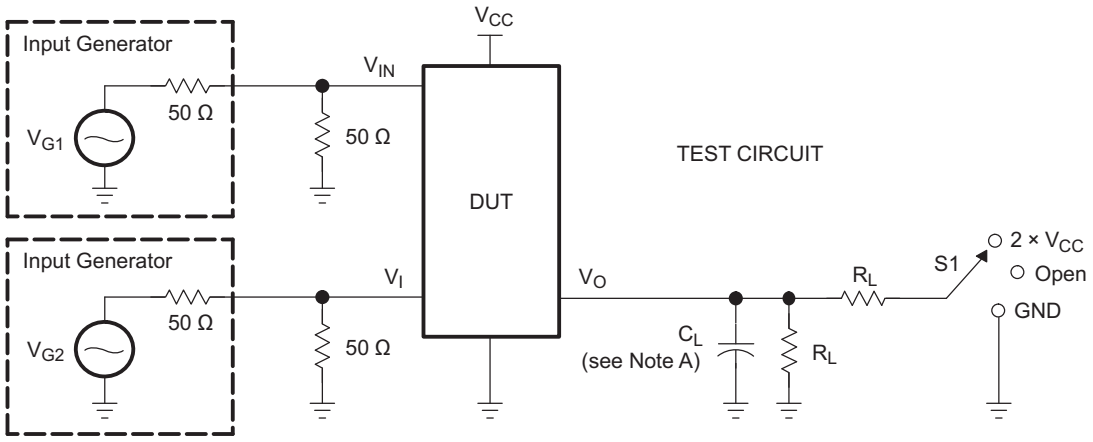


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

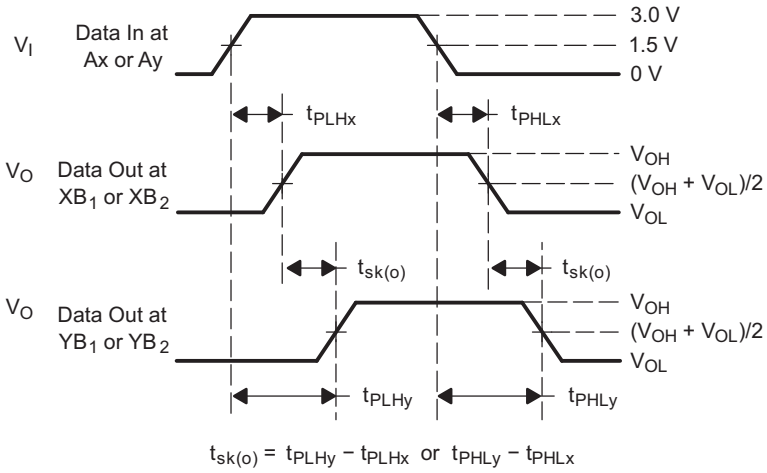
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics:PRR ≤10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{OFF}.
F. t_{PZL} and t_{PZH} are the same as t_{ON}.

Figure 9. Test Circuit and Voltage Waveforms

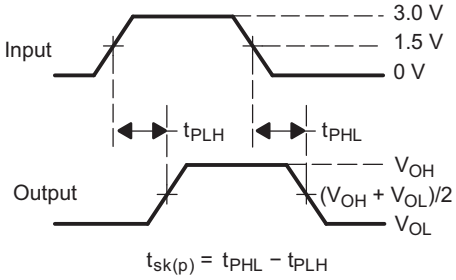
PARAMETER MEASUREMENT INFORMATION (continued)



TEST	V_{CC}	S1	R_L	V_{in}	C_L
$t_{sk(o)}$	3.3 V ± 0.3 V	Open	50 Ω	V_{CC} or GND	2 pF
$t_{sk(p)}$	3.3 V ± 0.3V	Open	50 Ω	V_{CC} or GND	2 pF



VOLTAGE WAVEFORMS
OUTPUT SKEW ($t_{sk(o)}$)



VOLTAGE WAVEFORMS
PULSE SKEW [$t_{sk(p)}$]

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.

Figure 10. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

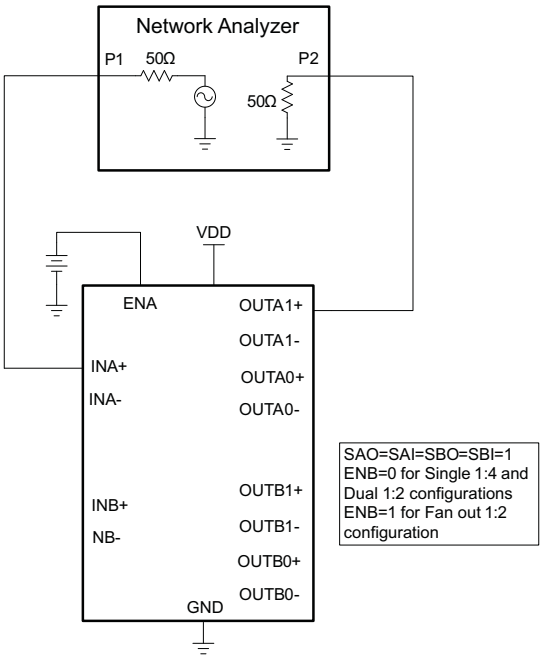


Figure 11. Frequency Response (BW)

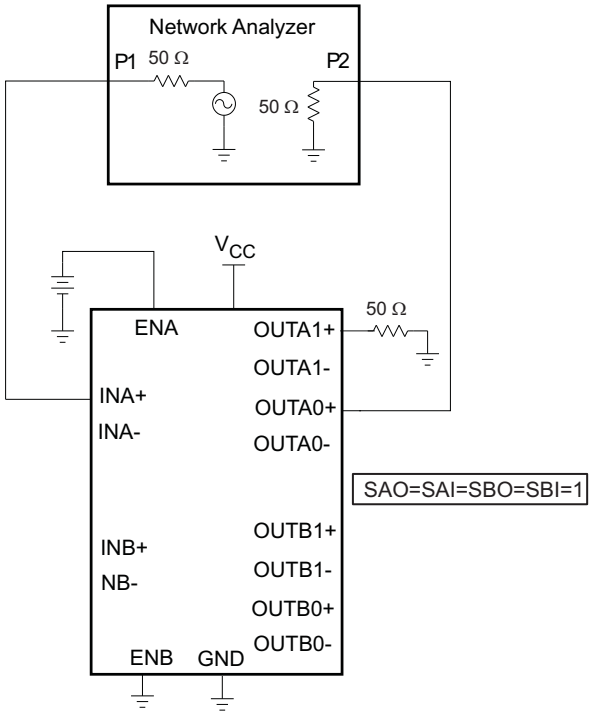


Figure 12. Off Isolation (O_{ISO})

PARAMETER MEASUREMENT INFORMATION (continued)

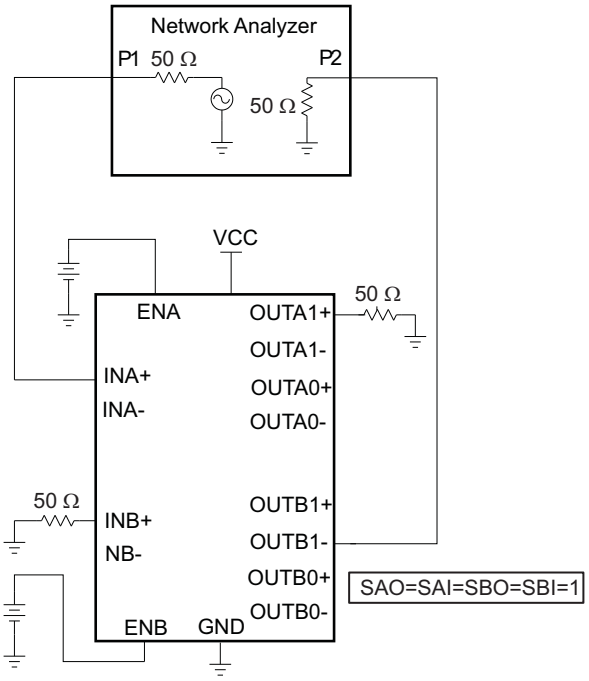


Figure 13. Crosstalk (X_{TALK})

PACKAGING INFORMATION

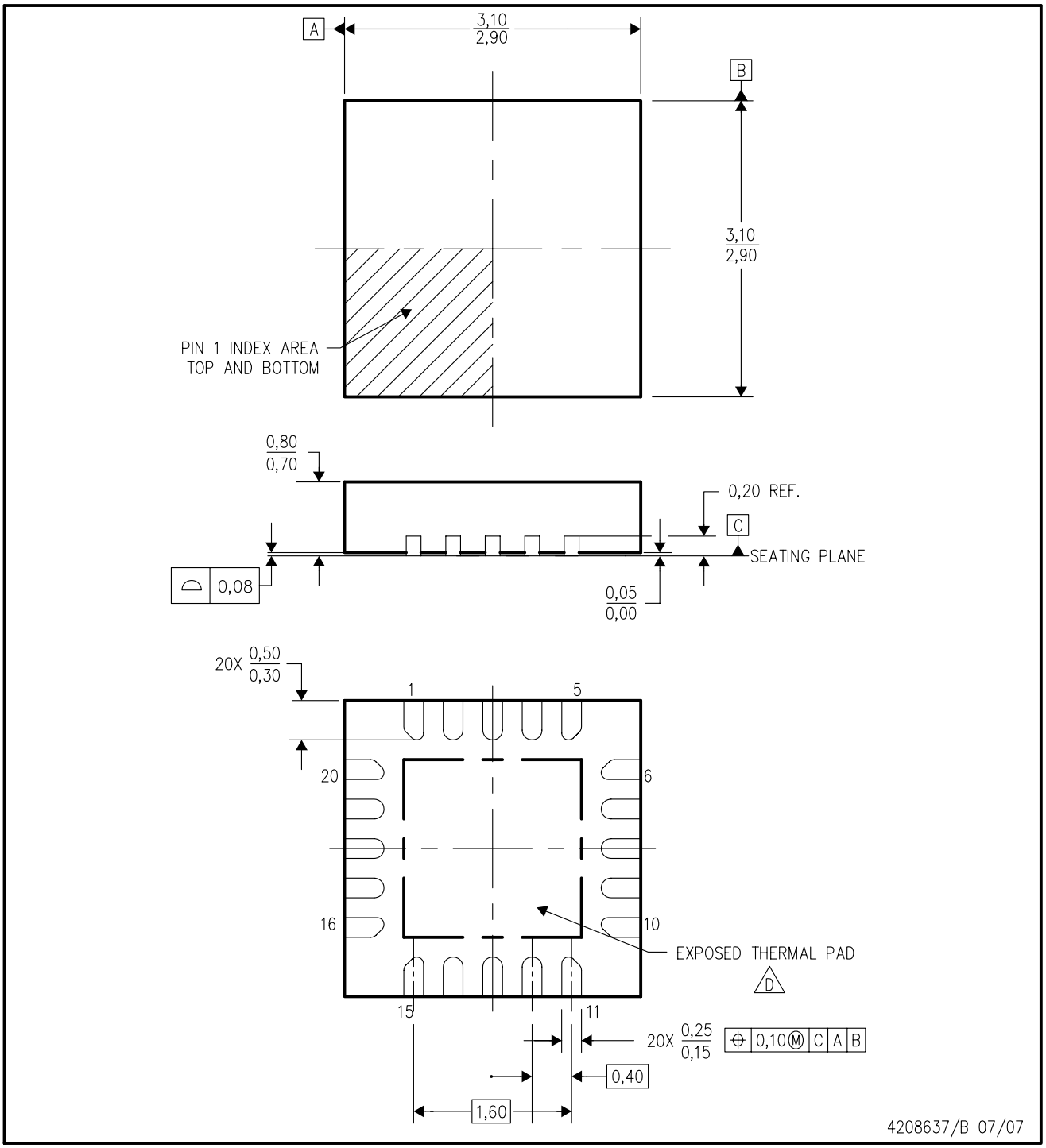
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TS3DS10224RUKR	PREVIEW	QFN	RUK	20	3000	TBD	Call TI	Call TI	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

RUK (S–PQFP–N20) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

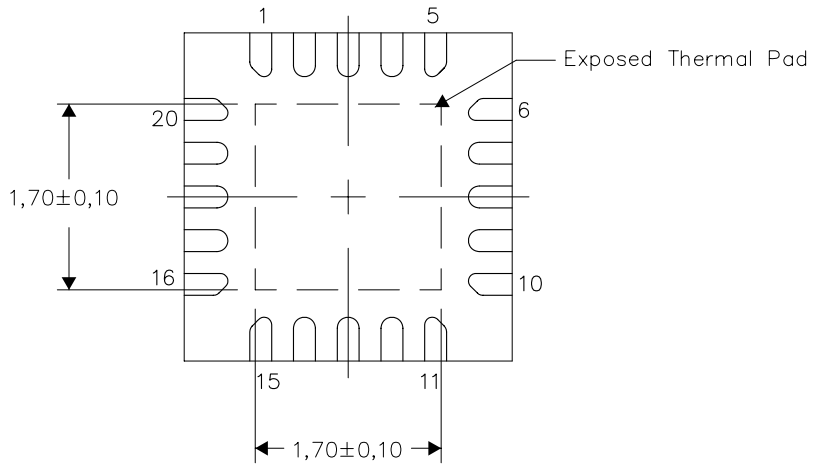
RUK (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

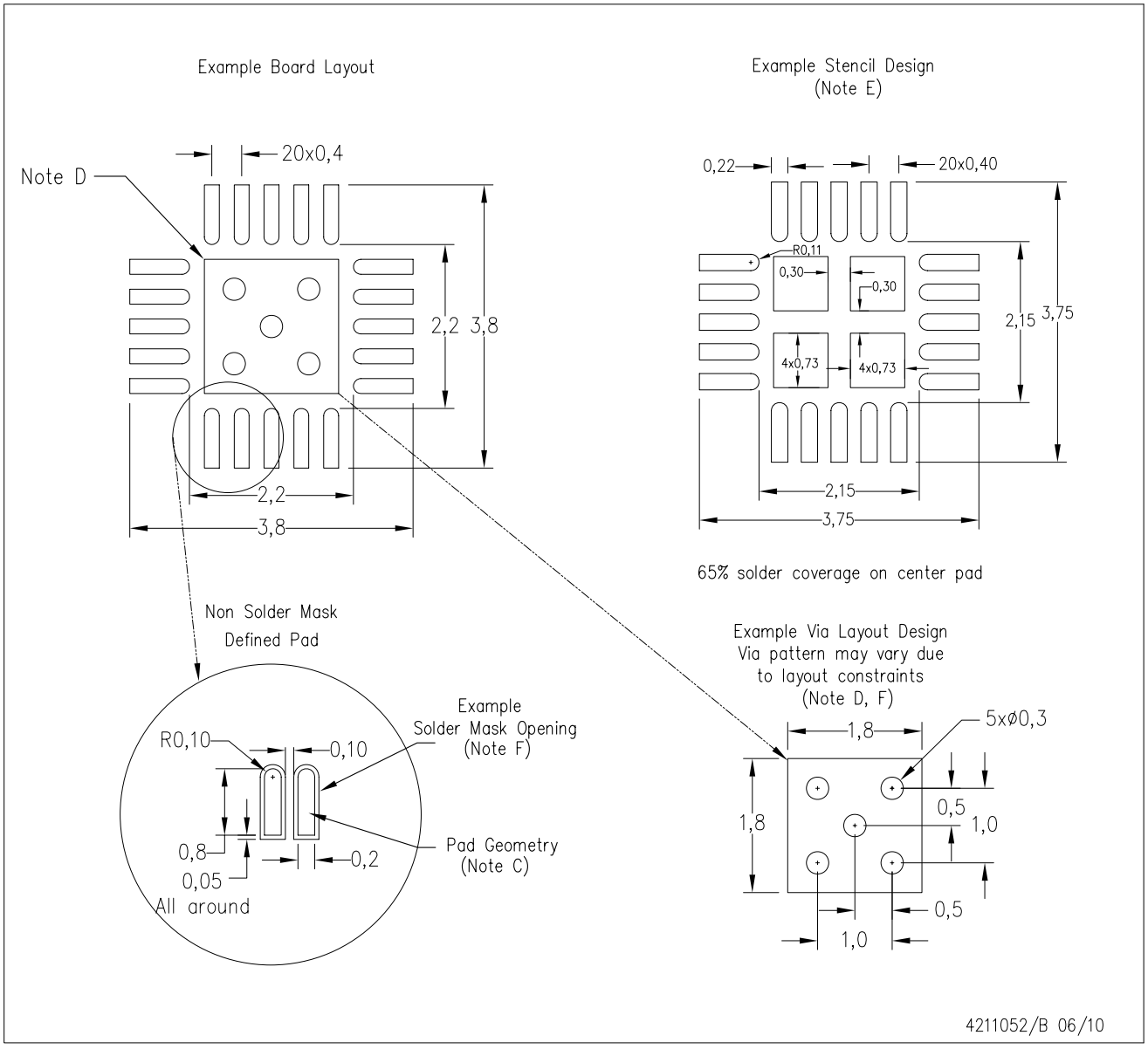


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RUK (S–PWQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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