3A 5V 1MHz Synchronous Buck Converter

Features

- **High Efficiency up to 95%**
  - Automatic Skip/PWM Mode Operation
- **Adjustable Output Voltage from 0.6V to VIN**
- **Integrated 110mΩ High side 80mΩ Low Side MOSFET**
- **Low Dropout Operation : 100% Duty cycle**
- **Stable with Low ESR Ceramic Capacitors**
- **Power-On-Reset Detection on VIN**
- **Integrate Soft Start and Soft-Stop**
- **Over-Temperature Protection**
- **Over Voltage Protection**
- **Under Voltage Protection**
- **High/ Low Side Current Limit**
- **Power Good Indication**
- **Enable/Shutdown Function**
- **Small SOT-23-6 and TDFN2x2-8 packages**
- **Lead Free and Green Devices Available (RoHS compliant)**

General Description

APW8825 is a 3A synchronous buck converter with integrated 110mΩ high side and 80mΩ low side power MOSFETs. The APW8825 design with a current-mode control scheme, can convert wide input voltage of 2.6V to 5.5V to the output voltage adjustable from 0.6V to 5.5V to provide excellent output voltage regulation.

The APW8825 is equipped with an automatic Skip/PWM mode operation. At light load, the IC operates in the Skip mode to reduce the switching losses. At heavy load, the IC works in PWM mode. At PWM mode, the switching frequency is set by the external resistor.

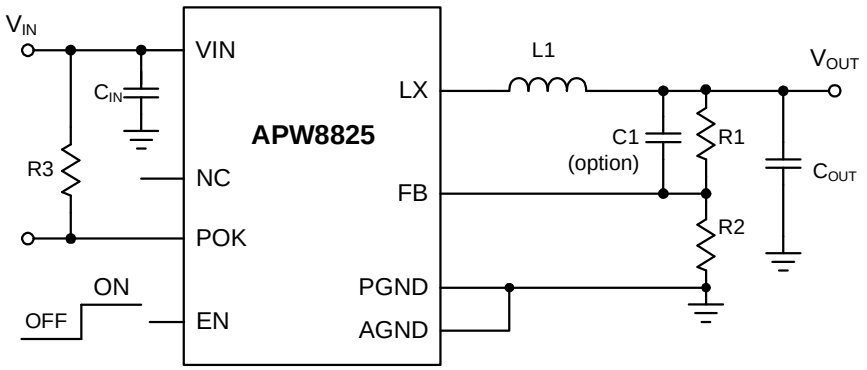
The APW8825 is also equipped with Power-on-reset, soft start, soft-stop, and whole protections (under-voltage, over-voltage, over-temperature and current-limit) into a single package.

This device, available TDFN2X2-8 and SOT-23-6 provide a very compact system solution external components and PCB area.

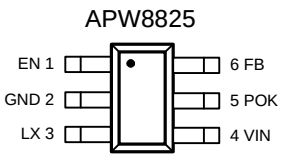
Applications

- **Notebook Computer & UMPC**
- **LCD Minitor/TV**
- **Set-Top Box**
- **DSL, Switch HUB**
- **Portable Instrument**

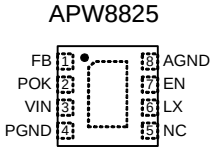
Simplified Application Circuit



Pin Configurations



SOT23-6
(Top View)



TDFN2x2-8
(Top View)

Ordering and Marking Information

APW8825 □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code QB : TDFN-2x2-8 C: SOT23-6 Operating Ambient Temperature Range I : -40 to 85°C Handling Code TR : Tape & Reel Assembly Material G: Halogen and Lead Free Device
APW8825QB : W25 X • X - Date Code	APW8825C : W25X • X - Date Code

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant)and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter		Rating	Unit
V_{IN}	Input Supply Voltage to PGND		-0.3 ~ 6.5	V
V_{LX}	LX to GND Voltage	< 30ns pulse width	-3 ~ 8	V
		> 30ns pulse width	-1 ~V_{IN}+0.3	V
	POK, FB, EN to PGND Voltage		-0.3 ~ 6.5	V
	AGND to PGND Voltage		-0.3 ~ 0.3	V
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature		-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature(10 Seconds)		260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter		Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2)	TDFN2x2-8	75	°C/W
		TSOT23-6	250	

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{IN}	Control and Driver Supply Voltage	2.6 ~ 5.5	V
V_{OUT}	Converter Output Voltage	0.6 ~ V_{IN}	V
L	Inductance	1 ~ 2.2	µH
I_{OUT}	Converter Output Current	0 ~ 3	A
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3 : Refer to the typical application circuit

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}=3.7V and T_A= -40 to 85 °C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW8825			Unit
			Min	Typ	Max	
Supply Current						
I_{DD}	VIN Supply Current	V_{FB}=0.66V	-	65	-	µA
I_{SHDN}	VIN Shutdown Supply Current	EN=GND	-	-	1	µA
Power-On-Reset (POR)						
	VIN POR Voltage Threshold	V_{IN} Rising	2.3	2.4	2.5	V
	VIN POR Hysteresis		0.1	0.2	0.3	V
Reference Voltage						
V_{REF}	Reference Voltage		-	0.6	-	V
		T_A=25°C	-1	-	+1	%
	Output Accuracy	I_{OUT}=10mA~3A, V_{IN}=2.6~5.5V	-1.5	-	+1.5	%
Oscillator						
F_{OSC}	Oscillator Frequency		0.85	1	1.15	MHz
	Minimum on Time		-	70	-	ns

Electrical Characteristics

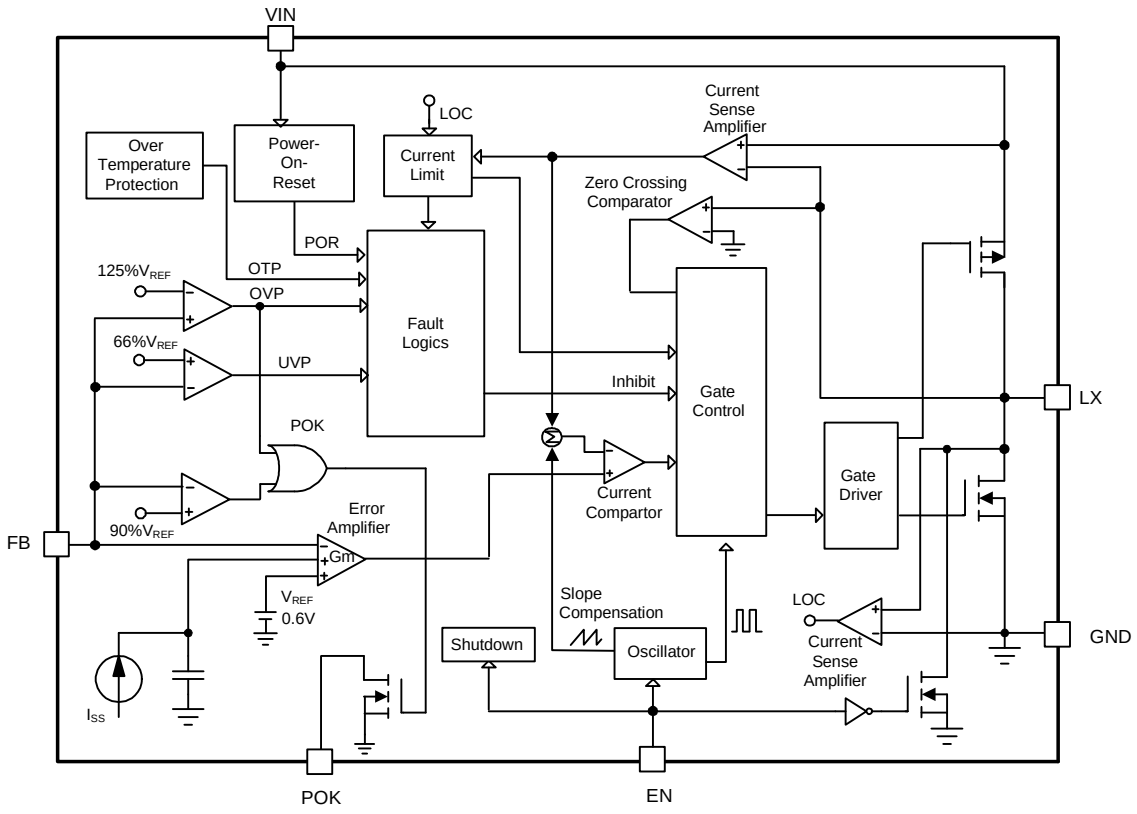
Unless otherwise specified, these specifications apply over V_{IN}=3.7V and T_A= -40 to 85 °C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APW8825			Unit
			Min	Typ	Max	
Power MOSFET						
	High Side P-MOSFET Resistance	V_{IN}=5V, I_{LX}=0.5A, T_A=25°C	-	110	-	mΩ
	Low Side N-MOSFET Resistance	V_{IN}=5V, I_{LX}=0.5A, T_A=25°C	-	80	-	mΩ
	High/Low Side MOSFET Leakage Current		-	-	10	μA
Protections						
I_{LIM}	High Side MOSFET current-limit	Peak Current, V_{IN}=2.6~5.5V T_A= -40 ~125 °C	4	5	6	A
T_{OTP}	Over-temperature Trip Point (Resoft start after OTP)		-	160	-	°C
	Over-temperature Hysteresis		-	50	-	°C
	Over- Voltage Protection threshold	V_{OUT} Rising	120	125	130	%V_{REF}
	Under-Voltage Protection threshold		57	66	75	%V_{REF}
	Over-Voltage Protection debounce time		20	25	30	μs
	Low Side Switch Current-Limit	From Drain to Source	-	-1	-	A
Soft-Start, Enable and POK						
	Soft Start time		-	0.8	-	ms
	EN Enable threshold		-	-	1.4	V
	EN shutdown threshold		0.5	-	-	V
	EN Pull Low Current		-	0.5	2	μA
	POK threshold	POK in from Lower (POK Goes High)	82.5	87.5	92.5	%V_{OUT}
		POK Low Hysteresis (POK Goes Low)	-	5	-	%V_{OUT}
		POK in from Higher (POK Goes High)	120	125	130	%V_{OUT}
		POK High Hysteresis (POK Goes Low)	-	5	-	%V_{OUT}
	Power Good pull low resistance		-	100	-	Ω
	Power Good Debounce	High to low	-	20	-	us

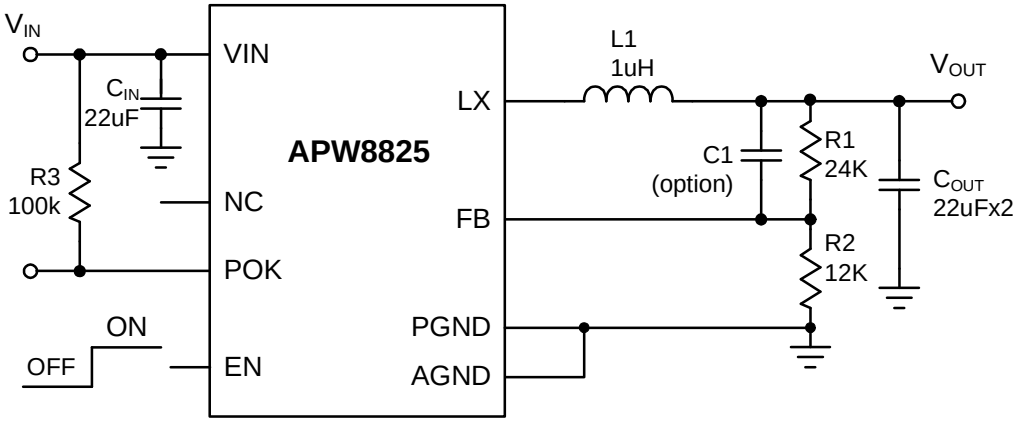
Pin Description

PIN			Function
TDFN2x2-8	TSOP23-6	Name	
1	6	FB	Output Feedback Input. The APW8825 senses the feedback voltage via FB and regulates the voltage at 0.6V. Connecting FB with a resistor-divider from the converter's output sets the output voltage.
2	5	POK	Power Good Output. This pin is open-drain logic output that is pulled to ground when the output voltage is not within 10% of regulation point.
3	4	VIN	The control circuitry and converter supply input. Connecting a ceramic bypass capacitor from VIN to GND to eliminate switching noise and voltage ripple on the input to the IC.
4, Exposed pad	-	PGND	Power ground. Connect this pin to AGND.
5	-	NC	No internal connection.
6	3	LX	Power Switching Output. LX is the Junction of the high-side and low-side Power MOSFETs to supply power to the output LC filter.
7	1	EN	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator, drive it low to turn it off.
8	-	AGND	Analog ground. Connect this pin to PGND.
-	2	GND	Power and signal ground.

Block Diagram



Typical Application Circuit



Function Description

VCC and VIN Power-On-Reset (POR)

TThe APW8825 keeps monitoring the voltage on VIN pin to prevent wrong logic operations which may occur when VIN voltage is not high enough for internal control circuitry to operate. The VIN POR rising threshold is 2.4V with 0.2V hysteresis.

During startup, the VIN voltage must exceed the POR threshold. Then the IC starts a starts-up process and ramps up the output voltage to the voltage target.

Output Under-Voltage Protection (UVP)

In the operational process, if a short-circuit occurs, the output voltage will drop quickly. Before the current-limit circuit responds, the output voltage will fall out of the required regulation range. The under-voltage continually monitors the FB voltage after soft-start is completed. If a load step is strong enough to pull the output voltage lower than the under-voltage threshold, the IC shuts down converter's output.

The under-voltage threshold is 66% of the nominal output voltage. The APW8825 will be latched after under-voltage protection.

Over-Voltage Protection (OVP)

The over-voltage function monitors the output voltage by FB pin. When the FB voltage increases over 125% of the reference voltage due to the high-side MOSFET failure or for other reasons, the over-voltage protection comparator will trigger soft-stop function and shutdown the converter output.

Over-Temperature Protection (OTP)

The over-temperature circuit limits the junction temperature of the APW8825. When the junction temperature exceeds T_J =160°C, a thermal sensor turns off the both power MOSFETs, allowing the devices to cool.

The thermal sensor allows the converters to start a start-up process and to regulate the output voltage again after the junction temperature cools by 50°C. The OTP is designed with a 50°C hysteresis to lower the average T_J during continuous thermal overload conditions, increasing lifetime of the APW8825.

Current-Limit Protection

The APW8825 monitors the output current, flows through the high-side and low-side power MOSFETs, and limits the current peak at current-limit level to prevent the IC from damaging during overload, short-circuit and over-voltage conditions. Typical high side power MOSFET current limit is 5A, and low side MOSFET current limit is 1A.

Soft-Start

The APW8825 has a built-in soft-start to control the rise rate of the output voltage and limit the input current surge during start-up. During soft-start, an internal voltage ramp connected to one of the positive inputs of the error amplifier, rises up to replace the reference voltage until the voltage ramp reaches the reference voltage. During soft-start without output over-voltage, the APW8825 converter's sinking capability is disabled until the output voltage reaches the voltage target.

Soft-Stop

At the moment of shutdown controlled by EN signal, under-voltage event or over-voltage event, the APW8825 initiates a soft-stop process to discharge the output voltage in the output capacitors. Certainly, the load current also discharges the output voltage. During soft-stop, the internal voltage ramp (V_{RAMP}) falls down to replace the reference voltage. The low side MOSFET turns on each cycle to discharge the output voltage. Therefore, the output voltage falls down slowly at the light load. After the soft-stop interval elapses, the soft-stop process ends and the IC turns off.

Enable and Shutdown

Driving EN to ground places the APW8825 in shutdown. In shutdown mode, the internal power MOSFETs turns off, all internal circuitry shuts down and the quiescent supply current reduces to less than 1μA.

Function Description (Cont.)

Power Good Indicator

POK is actively held low in shutdown and soft-start status. In the soft-start process, the POK is an open-drain. When the soft-start is finished, the POK is high. In normal operation, the POK window is from 85% to 125% of the converter reference voltage. When the output voltage stays within this window, POK signal will become high after 0.5ms internal delay. When the output voltage outruns 80% or 120% of the target voltage, POK signal will be pulled low immediately. In order to prevent false POK drop, capacitors need to parallel at the output to confine the voltage deviation with severe load step transient. The POK pin, if used, needs an axternal pull high resistor, the recommended resistor should be in the range of 30KΩ to 100KΩ.

Application Information

Input Capacitor Selection

Because buck converters have a pulsating input current, a low ESR input capacitor is required. This results in the best input voltage filtering, minimizing the interference with other circuits caused by high input voltage spikes. Also, the input capacitor must be sufficiently large to stabilize the input voltage during heavy load transients. For good input voltage filtering, usually a 22µF input capacitor is sufficient. It can be increased without any limit for better input-voltage filtering. Ceramic capacitors show better performance because of the low ESR value, and they are less sensitive against voltage transients and spikes compared to tantalum capacitors. Place the input capacitor as close as possible to the input and GND pin of the device for better performance.

Inductor Selection

For high efficiencies, the inductor should have a low DC resistance to minimize conduction losses. Especially at high-switching frequencies, the core material has a higher impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. A reasonable starting point for setting ripple current, $\Delta I_{L,}$ is 40% of maximum output current. The recommended inductor value can be calculated as below:

$$L \geq \frac{V_{OUT}\left(1-\frac{V_{OUT}}{V_{IN}}\right)}{F_{SW}\cdot \Delta I_L}$$

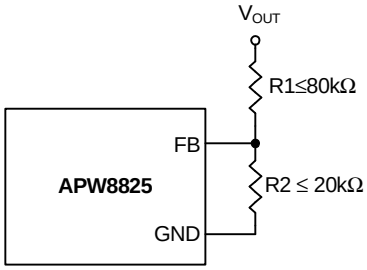
$$I_{L(MAX)} = I_{OUT(MAX)} + 1/2 \times \Delta I_L$$

To avoid the saturation of the inductor, the inductor should be rated at least for the maximum output current of the converter plus the inductor ripple current.

Output Voltage Setting

In the adjustable version, the output voltage is set by a resistive divider. The external resistive divider is connected to the output, allowing remote voltage sensing as shown in “Typical Application Circuits”. A suggestion of maximum value of R2 is 20kΩ to keep the minimum current that provides enough noise rejection ability through the resistor divider. The output voltage can be calculated as below:

$$V_{OUT} = V_{REF}\cdot\left(1+\frac{R1}{R2}\right) = 0.6\cdot\left(1+\frac{R1}{R2}\right)$$

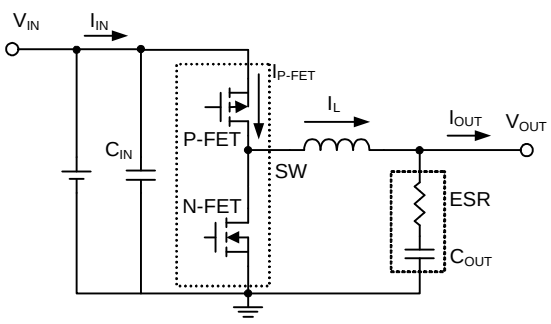


Output Capacitor Selection

The current-mode control scheme of the APW8825 allows the use of tiny ceramic capacitors. The higher capacitor value provides the good load transients response. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. If required, tantalum capacitors may be used as well. The output ripple is the sum of the voltages across the ESR and the ideal output capacitor.

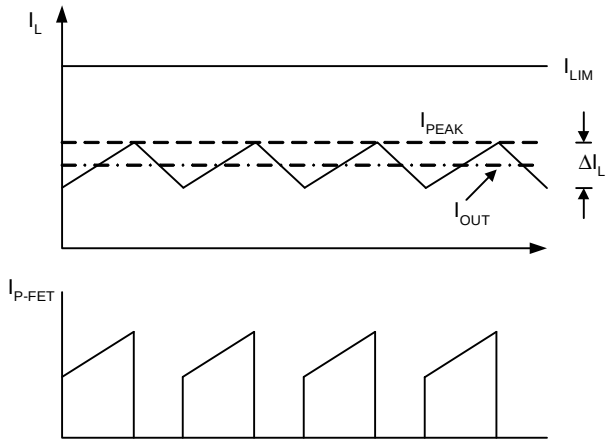
$$\Delta V_{OUT} \cong \frac{V_{OUT}\cdot\left(1-\frac{V_{OUT}}{V_{IN}}\right)}{F_{SW}\cdot L}\cdot\left(ESR+\frac{1}{8\cdot F_{SW}\cdot C_{OUT}}\right)$$

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.



Application Information (Cont.)

Output Capacitor Selection (Cont.)



Power Sequencing

At start-up, it is necessary to ensure that the VIN (the voltage supplied to MOSFET drain) and VEN are sequenced correctly to avoid erroneous latch-off. To avoid UVP latch-off happened at start-up due to sequencing issues, the key method is the VIN should be larger than the output under-voltage threshold plus the drop through the pass MOSFET when that output is enabled.
Figure 1 shows the VIN comes up before the VEN. Recommended power on sequence is shown in Figure1.

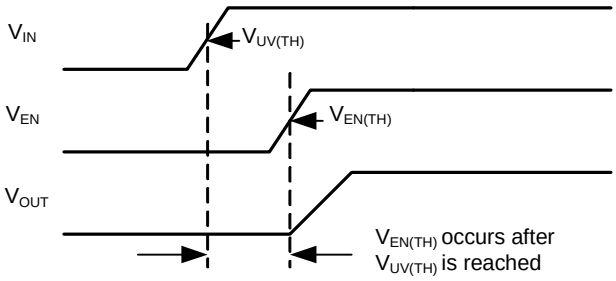
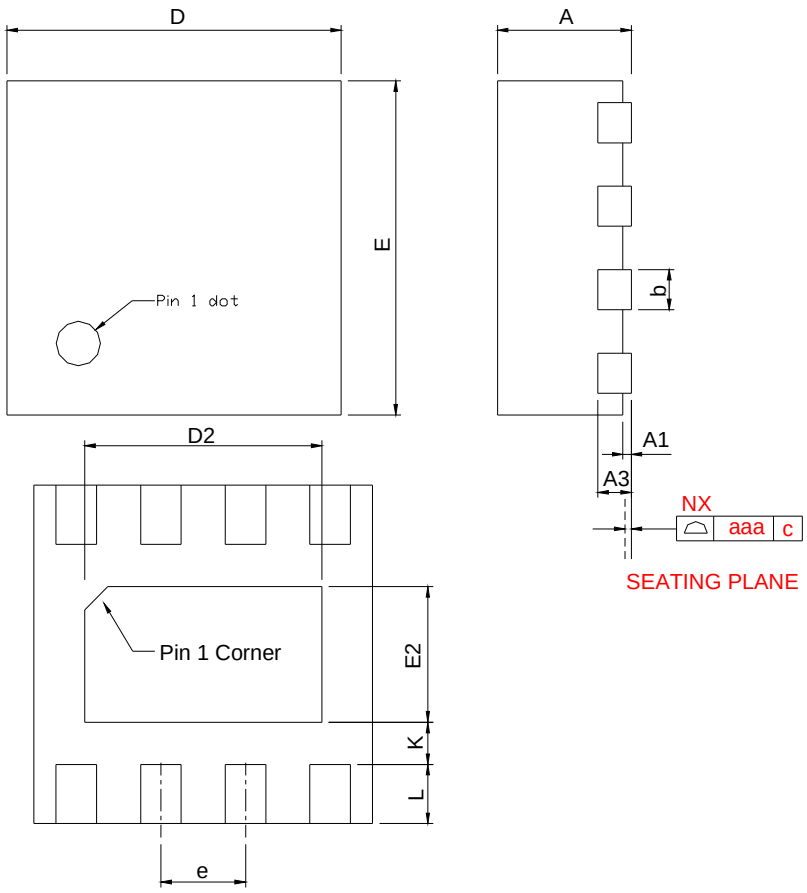


Figure 1. APW8825 power on sequence.

Package Information

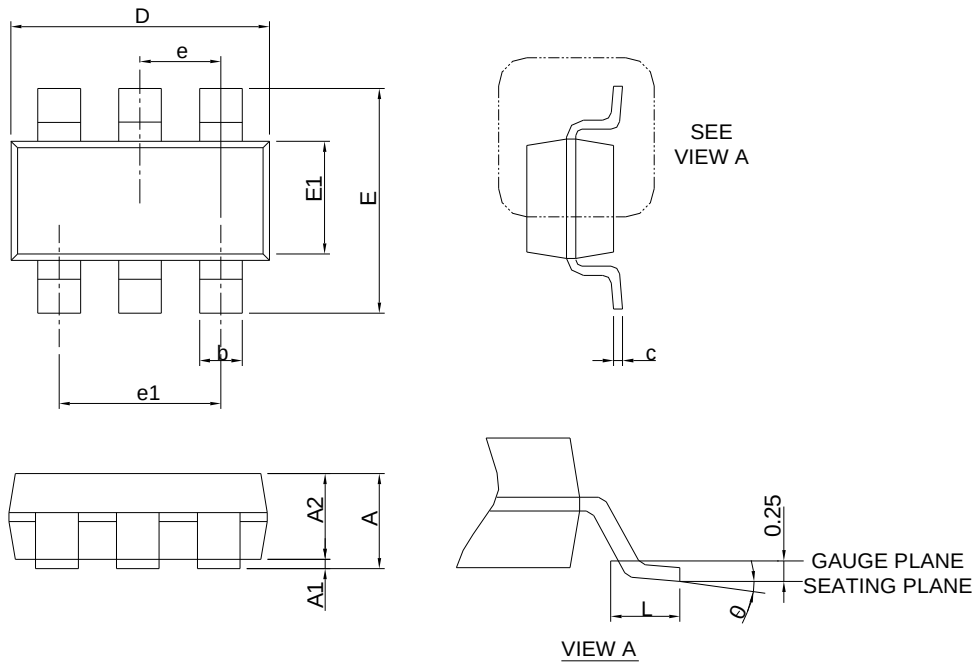
TDFN2x2-8



SYMBOL	TDFN2*2-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	1.90	2.10	0.075	0.083
D2	1.00	1.60	0.039	0.063
E	1.90	2.10	0.075	0.083
E2	0.60	1.00	0.024	0.039
e	0.50 BSC		0.020 BSC	
L	0.30	0.45	0.012	0.018
K	0.20	0.30	0.008	0.012
aaa	0.08		0.003	

Package Information

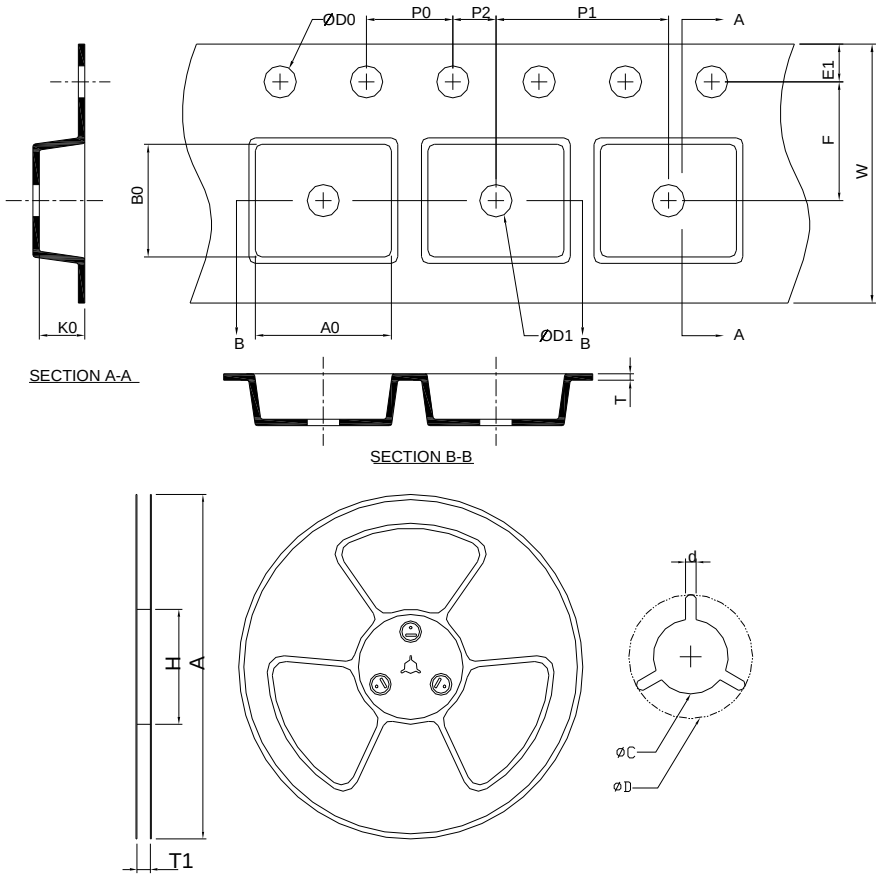
SOT-23-6



SYMBOL	SOT-23-6			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.45		0.057
A1	0.00	0.15	0.000	0.006
A2	0.90	1.30	0.035	0.051
b	0.30	0.50	0.012	0.020
c	0.08	0.22	0.003	0.009
D	2.70	3.10	0.106	0.122
E	2.60	3.00	0.102	0.118
E1	1.40	1.80	0.055	0.071
e	0.95 BSC		0.037 BSC	
e1	1.90 BSC		0.075 BSC	
L	0.30	0.60	0.012	0.024
θ	0°	8°	0°	8°

Note : 1. Follow JEDEC TO-178 AB.
2. Dimension D and E1 do not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 10 mil per side.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TDFN2x2-8	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.20	1.75±0.10	3.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	2.35±0.20	2.35±0.20	1.00±0.20
Application	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
SOT-23-6	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.0 MIN.	0.6+0.00 -0.40	3.20±0.20	3.10±0.20	1.50±0.20

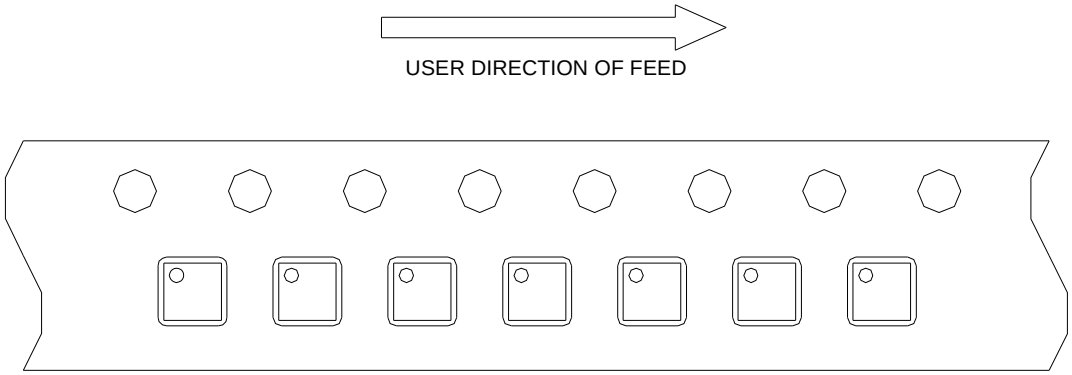
(mm)

Devices Per Unit

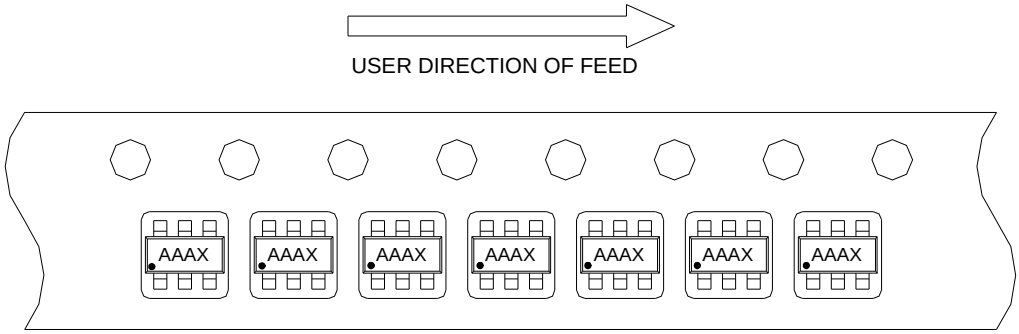
Package Type	Unit	Quantity
SOT-23-6	Tape & Reel	3000
TDFN2x2-8	Tape & Reel	3000

Taping Direction Information

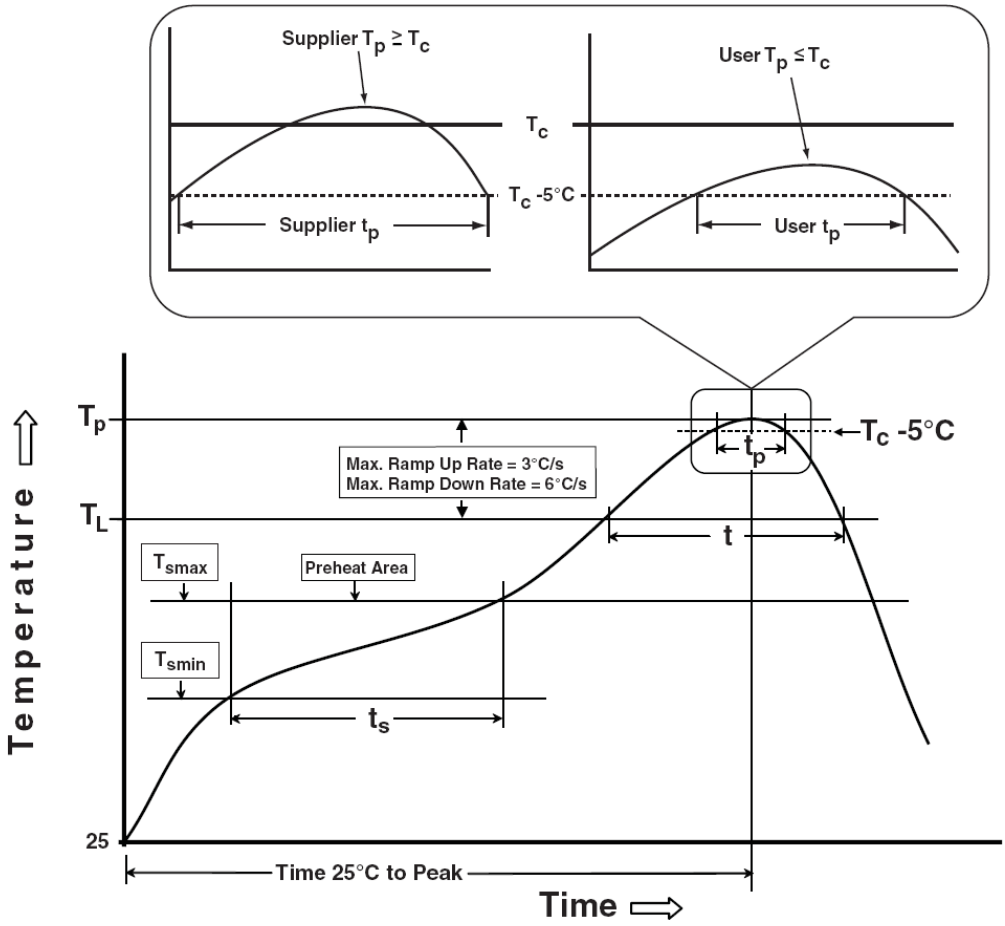
TDFN2x2-8



SOT-23-6



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ Tj=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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