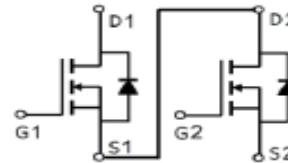
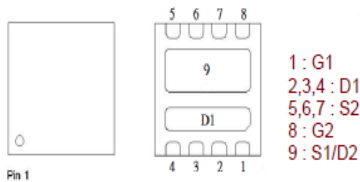


# PE642DT

## Dual N-Channel Enhancement Mode MOSFET

### PRODUCT SUMMARY

	$V_{(BR)DSS}$	$R_{DS(ON)}$	$I_D$
Q2	30V	9mΩ @ $V_{GS} = 10V$	34A
Q1	30V	10.5mΩ @ $V_{GS} = 10V$	31A



### PDFN 3X3S

### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25\text{ °C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	Q2	Q1	UNITS	
Drain-Source Voltage	$V_{DS}$	30	30	V	
Gate-Source Voltage	$V_{GS}$	±20	±20		
Continuous Drain Current <sup>3</sup>	$T_C = 25\text{ °C}$	34	31	A	
	$T_C = 100\text{ °C}$	22	20		
Pulsed Drain Current <sup>1</sup>	$I_{DM}$	48	46		
Continuous Drain Current <sup>3</sup>	$T_A = 25\text{ °C}$	11	9.7		
	$T_A = 70\text{ °C}$	8.8	7.7		
Avalanche Current	$I_{AS}$	21	18.3		
Avalanche Energy	$L = 0.1\text{mH}$	$E_{AS}$	22	16.7	mJ
Power Dissipation	$T_C = 25\text{ °C}$	$P_D$	20	19	W
	$T_C = 100\text{ °C}$	$P_D$	8	7.6	
Power Dissipation	$T_A = 25\text{ °C}$	$P_D$	2	1.7	
	$T_A = 70\text{ °C}$	$P_D$	1.2	1.1	
Operating Junction & Storage Temperature Range	$T_J, T_{stg}$	-55 to 150		°C	

### THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient <sup>2</sup>	$R_{\theta JA}$	Q2	62	°C / W
	$R_{\theta JA}$	Q1	70	
Junction-to-case	$R_{\theta JC}$	Q2	6.2	
	$R_{\theta JC}$	Q1	6.5	

<sup>1</sup>Pulse width limited by maximum junction temperature  $T_{J(MAX)}=150\text{ °C}$ .

<sup>2</sup>The value of  $R_{\theta JA}$  is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A = 25\text{ °C}$ . The value in any given application depends on the user's specific board design.

<sup>3</sup>Package limitation current is Q2=14A , Q1=9.5A.

# PE642DT

## Dual N-Channel Enhancement Mode MOSFET

### ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
<b>STATIC</b>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	Q2	30		V
			Q1	30		
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	Q2	1.3	1.75	2.3
			Q1	1.3	1.75	2.3
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±20V	Q2			±100
			Q1			±100
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 24V, V <sub>GS</sub> = 0V	Q2			1
			Q1			1
		V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0V , T <sub>J</sub> = 55 °C	Q2			10
			Q1			10
Drain-Source On-State Resistance <sup>1</sup>	R <sub>DS(ON)</sub>	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 10A	Q2		8	12
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 9A	Q1		13	15.5
		V <sub>GS</sub> = 10V, I <sub>D</sub> = 10A	Q2		6.3	9
		V <sub>GS</sub> = 10V, I <sub>D</sub> = 9.5A	Q1		8.6	10.5
Forward Transconductance <sup>1</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 5V, I <sub>D</sub> = 10A	Q2		43	S
		V <sub>DS</sub> = 5V, I <sub>D</sub> = 9.5A	Q1		45	
<b>DYNAMIC</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 15V, f = 1MHz	Q2		782	pF
			Q1		616	
Output Capacitance	C <sub>oss</sub>		Q2		139	
			Q1		120	
Reverse Transfer Capacitance	C <sub>rss</sub>		Q2		76	
			Q1		83	
Gate Resistance	R <sub>g</sub>	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V, f = 1MHz	Q2		2.3	3.5
		Q1		2.7	4	
Total Gate Charge <sup>2</sup>	Q <sub>g</sub>	Q2 V <sub>DS</sub> = 15V, V <sub>GS</sub> = 10V, I <sub>D</sub> = 10A Q1 V <sub>DS</sub> = 15V, V <sub>GS</sub> = 10V, I <sub>D</sub> = 9.5A	V <sub>GS</sub> = 10V	Q2		18
			V <sub>GS</sub> = 4.5V	Q1		14
				Q2		9.6
			Gate-Source Charge <sup>2</sup>	Q <sub>gs</sub>	Q1	
Q2					2.2	
Gate-Drain Charge <sup>2</sup>	Q <sub>gd</sub>		Q1		2.1	
			Q2		5.2	
				Q1		4

## PE642DT

### Dual N-Channel Enhancement Mode MOSFET

Turn-On Delay Time <sup>2</sup>	$t_{d(on)}$	Q2 $V_{DS} = 15V,$ $I_D \cong 10A, V_{GS} = 10V, R_{GEN} = 6\Omega$ Q1 $V_{DS} = 15V,$ $I_D \cong 9.5A, V_{GS} = 10V, R_{GEN} = 6\Omega$	Q2		27		nS
Rise Time <sup>2</sup>	$t_r$		Q1		18		
			Q2		24		
Turn-Off Delay Time <sup>2</sup>	$t_{d(off)}$		Q1		24		
			Q2		47		
Fall Time <sup>2</sup>	$t_f$		Q1		44		
			Q2		25		
			Q1		23		
<b>SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (<math>T_J = 25^\circ C</math>)</b>							
Continuous Current <sup>3</sup>	$I_S$		Q2		16		A
			Q1		17		
Forward Voltage <sup>1</sup>	$V_{SD}$	$I_F = 10A, V_{GS} = 0V$	Q2		1.2		V
		$I_F = 9.5A, V_{GS} = 0V$	Q1		1.1		
Reverse Recovery Time	$t_{rr}$	Q2 $I_F = 10A, di_F/dt = 100A/\mu S$ Q1 $I_F = 9.5A, di_F/dt = 100A/\mu S$	Q2		10.5		nS
			Q1		9.3		
Reverse Recovery Charge	$Q_{rr}$	Q2 $I_F = 10A, di_F/dt = 100A/\mu S$ Q1 $I_F = 9.5A, di_F/dt = 100A/\mu S$	Q2		2.8		nC
			Q1		2.2		

<sup>1</sup>Pulse test : Pulse Width  $\leq 300 \mu\text{sec}$ , Duty Cycle  $\leq 2\%$ .

<sup>2</sup>Independent of operating temperature.

<sup>3</sup>Package limitation current is Q2=14A , Q1=9.5A.

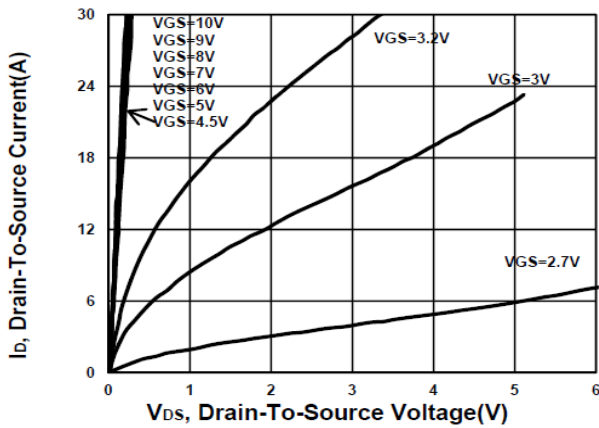
# PE642DT

## Dual N-Channel Enhancement Mode MOSFET

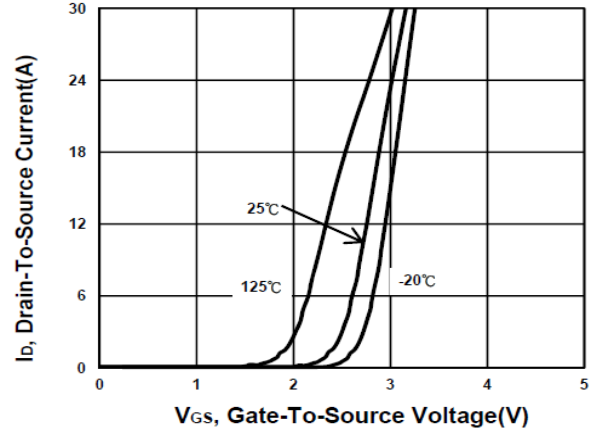
### TYPICAL PERFORMANCE CHARACTERISTICS

#### Q2

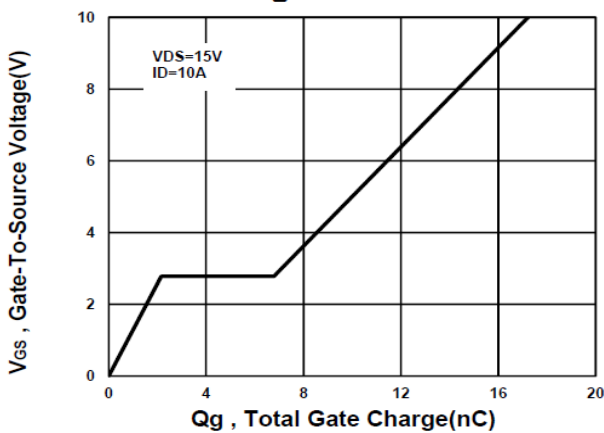
**Output Characteristics**



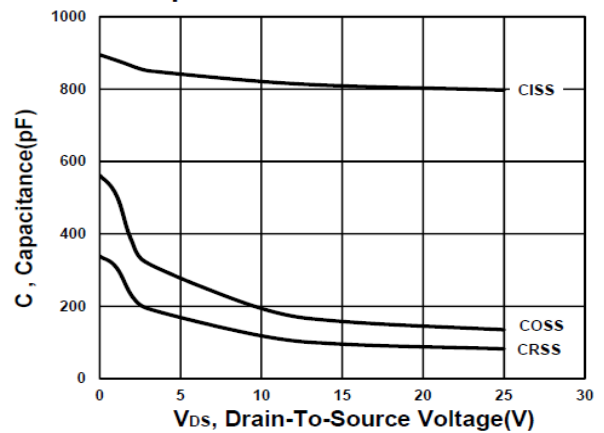
**Transfer Characteristics**



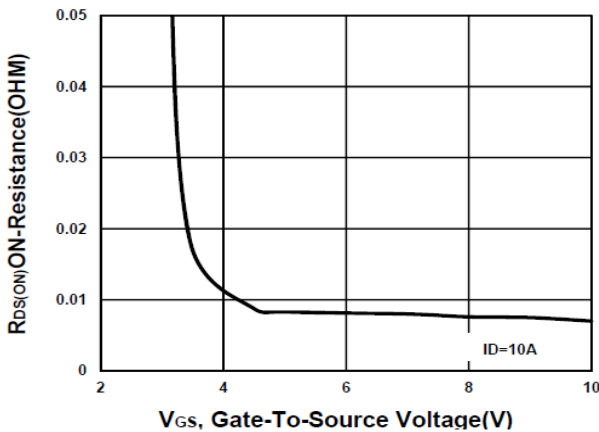
**Gate charge Characteristics**



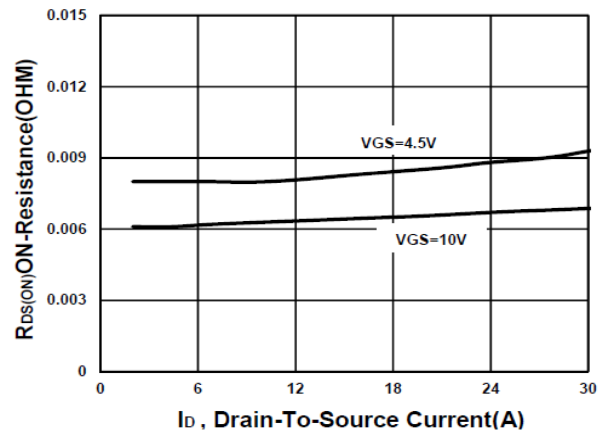
**Capacitance Characteristic**



**On-Resistance VS Gate-To-Source**



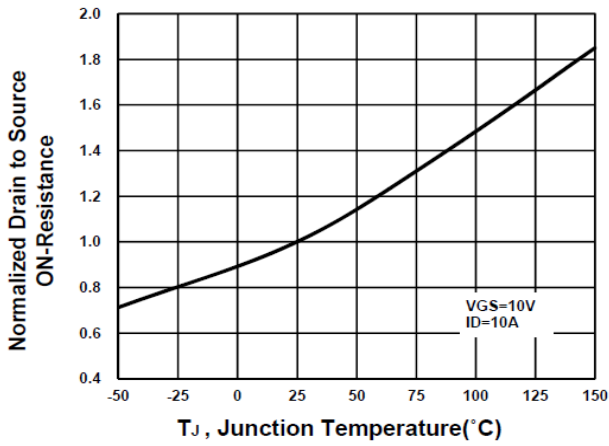
**On-Resistance VS Drain Current**



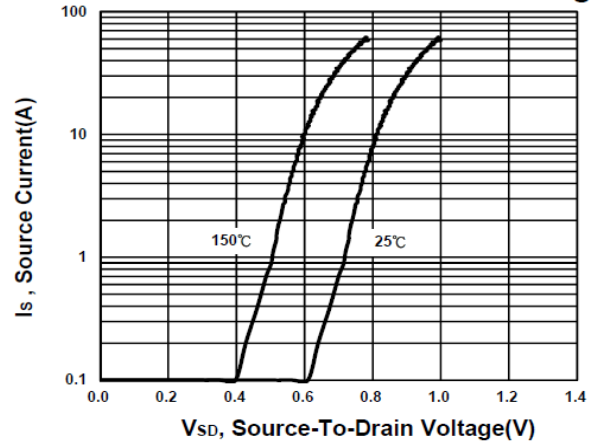
# PE642DT

## Dual N-Channel Enhancement Mode MOSFET

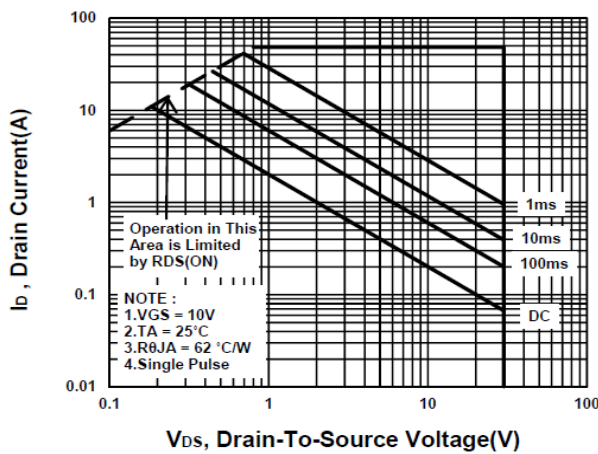
**On-Resistance VS Temperature**



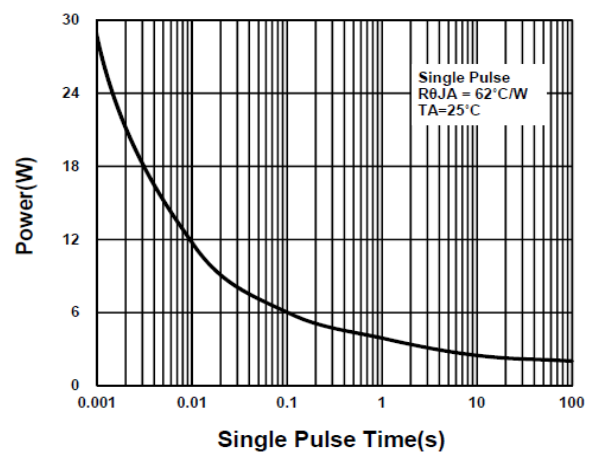
**Source-Drain Diode Forward Voltage**



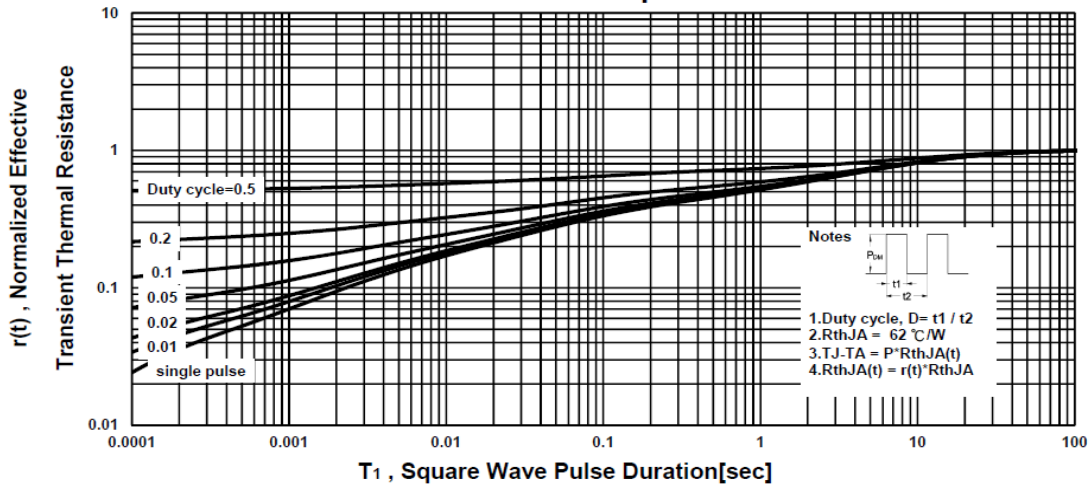
**Safe Operating Area**



**Single Pulse Maximum Power Dissipation**



**Transient Thermal Response Curve**

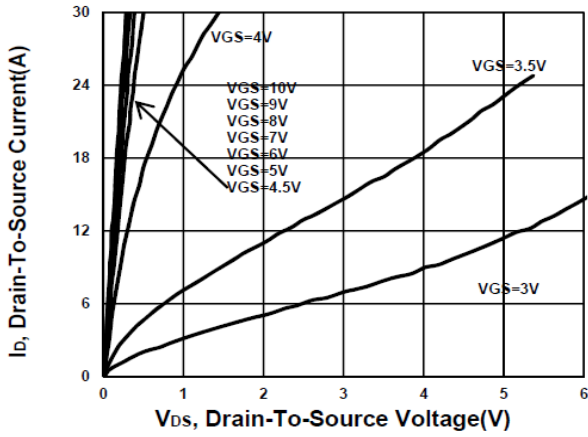


# PE642DT

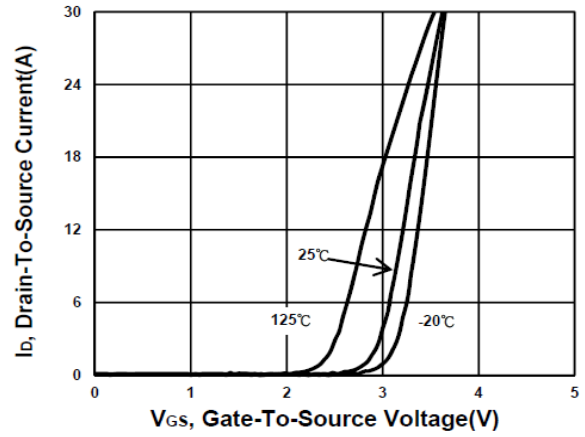
## Dual N-Channel Enhancement Mode MOSFET

**Q1**

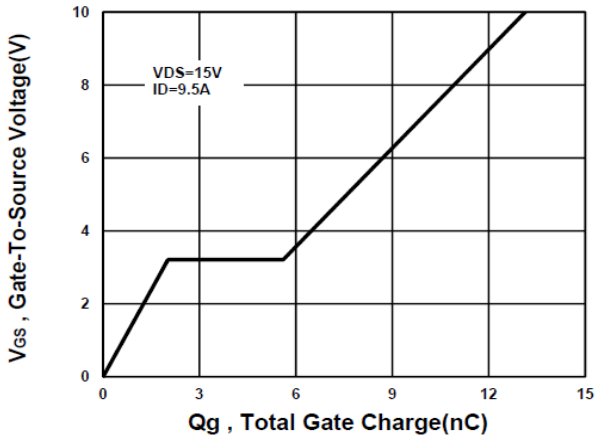
**Output Characteristics**



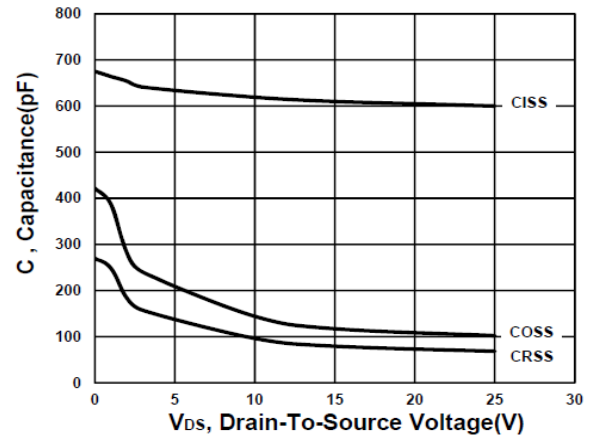
**Transfer Characteristics**



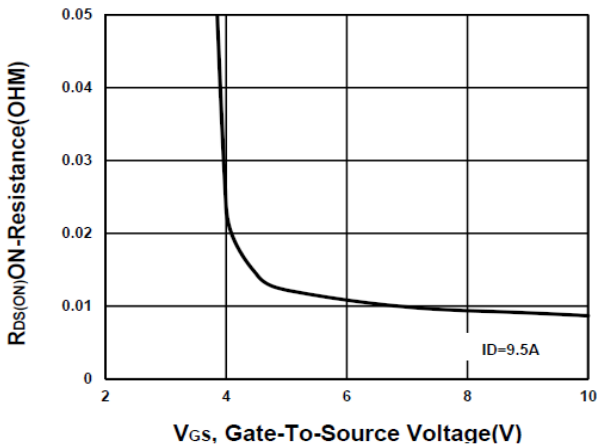
**Gate charge Characteristics**



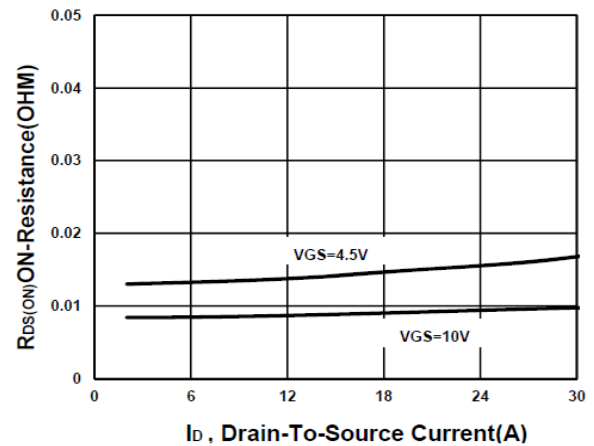
**Capacitance Characteristic**



**On-Resistance VS Gate-To-Source**



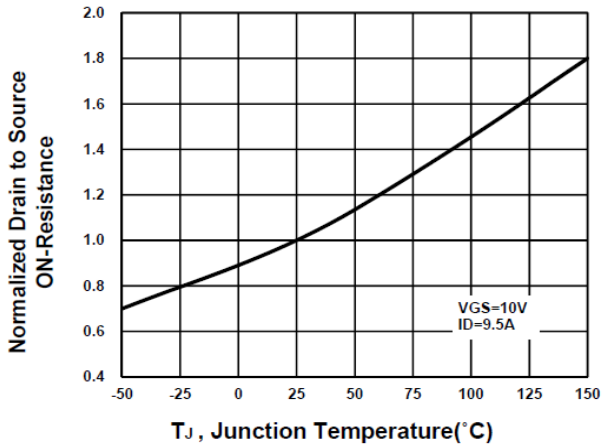
**On-Resistance VS Drain Current**



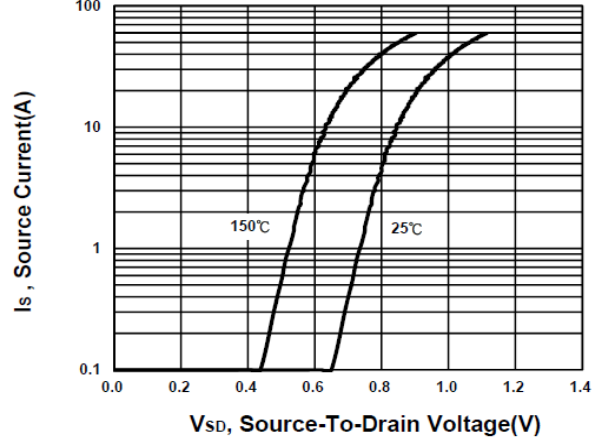
# PE642DT

## Dual N-Channel Enhancement Mode MOSFET

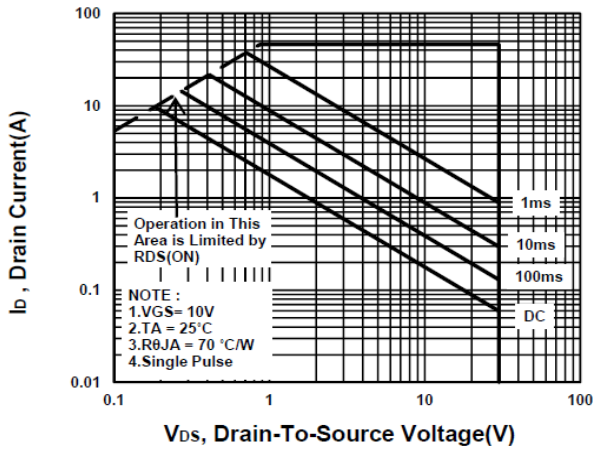
**On-Resistance VS Temperature**



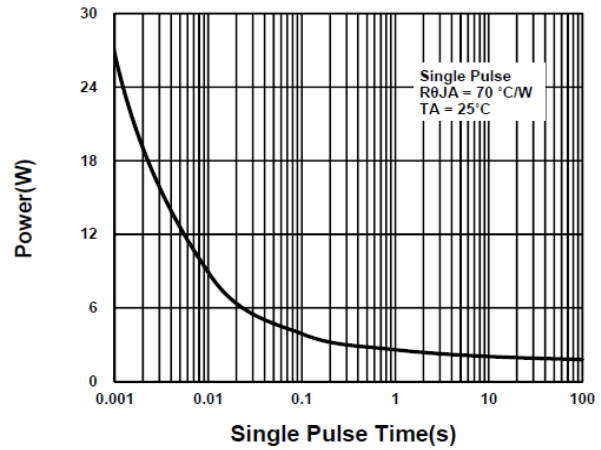
**Source-Drain Diode Forward Voltage**



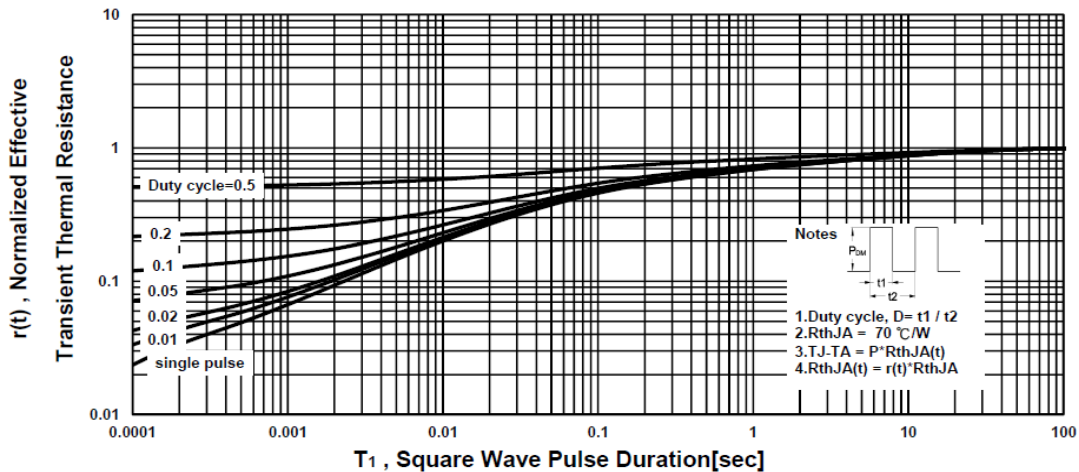
**Safe Operating Area**



**Single Pulse Maximum Power Dissipation**



**Transient Thermal Response Curve**



# PE642DT

## Dual N-Channel Enhancement Mode MOSFET

### Package Dimension

### PDFN 3x3S(上下 Dual) MECHANICAL DATA

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	2.9	3	3.1	I		0.25	
B	2.9	3	3.1	J	0.94	0.99	1.04
C	0.8	0.85	0.9	K	0.47	0.52	0.57
D	0.195	0.203	0.211	L	0.35	0.4	0.45
E	0		0.05				
F		0.65					
G	0.27	0.32	0.37				
H		1.86					

