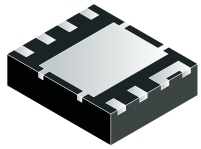


Synchronous Buck NexFET™ Power Block

FEATURES

- Half-Bridge Power Block
- 91% system Efficiency at 15A
- High Frequency Operation (Up To 1.5MHz)
- High Density – SON 5-mm × 6-mm Footprint
- Optimized for 5V Gate Drive
- Low Switching Losses
- Ultra Low Inductance Package
- RoHS Compliant
- Halogen Free
- Pb-Free Terminal Plating

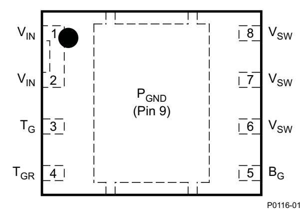
APPLICATIONS

- Synchronous Buck Converters
  - High Frequency Applications
  - High Current, Low Duty Cycle Applications
- Multiphase Synchronous Buck Converters
- POL DC-DC Converters
- IMVP, VRM, and VRD Applications

DESCRIPTION

The CSD87352Q5D NexFET™ power block is an optimized design for synchronous buck applications offering high current, high efficiency, and high frequency capability in a small 5-mm × 6-mm outline. Optimized for 5V gate drive applications, this product offers a flexible solution capable of offering a high density power supply when paired with any 5V gate drive from an external controller/driver.

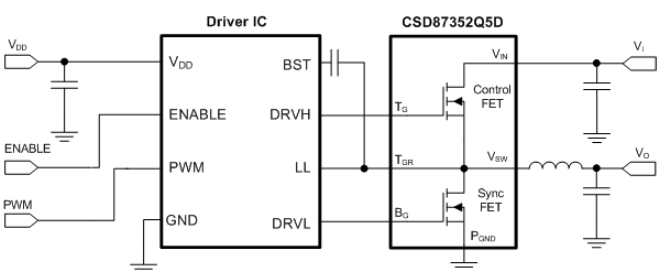
Top View



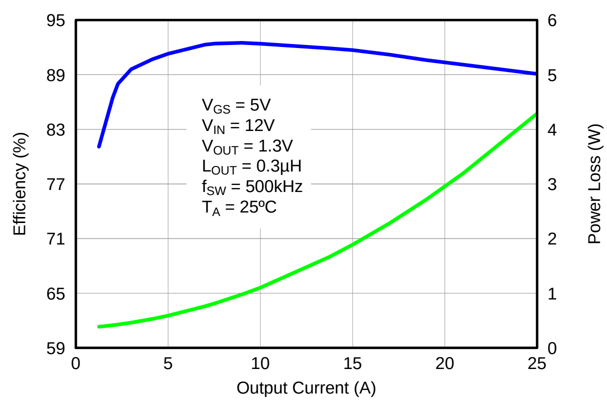
ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD87352Q5D	SON 5-mm × 6-mm Plastic Package	13-Inch Reel	2500	Tape and Reel

TYPICAL CIRCUIT



TYPICAL POWER BLOCK EFFICIENCY and POWER LOSS



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C (unless otherwise noted) (1)

Parameter	Conditions	VALUE	UNIT
Voltage Range	V_{IN} to P_{GND}	30	V
	V_{SW} to P_{GND}	30	V
	V_{SW} to P_{GND} (10ns)	32	V
	T_G to T_{GR}	-8 to 10	V
	B_G to P_{GND}	-8 to 10	V
Pulsed Current Rating, I_{DM}		60	A
Power Dissipation, P_D		8.5	W
Avalanche Energy E_{AS}	Sync FET, I_D = 65A, L = 0.1mH	211	mJ
	Control FET, I_D = 37A, L = 0.1mH	68	
Operating Junction and Storage Temperature Range, T_J, T_{STG}		-55 to 150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

T_A = 25° (unless otherwise noted)

Parameter	Conditions	MIN	MAX	UNIT
Gate Drive Voltage, V_{GS}		4.5	8	V
Input Supply Voltage, V_{IN}			27	V
Switching Frequency, f_{SW}	C_{BST} = 0.1µF (min)		1500	kHz
Operating Current			25	A
Operating Temperature, T_J			125	°C

POWER BLOCK PERFORMANCE

T_A = 25° (unless otherwise noted)

Parameter	Conditions	MIN	TYP	MAX	UNIT
Power Loss, P_{LOSS} (1)	V_{IN} = 12V, V_{GS} = 5V, V_{OUT} = 1.3V, I_{OUT} = 15A, f_{SW} = 500kHz, L_{OUT} = 0.3µH, T_J = 25ºC		1.8		W
V_{IN} Quiescent Current, I_{QVIN}	T_G to T_{GR} = 0V B_G to P_{GND} = 0V		10		µA

(1) Measurement made with six 10µF (TDK C3216X5R1C106KT or equivalent) ceramic capacitors placed across V_{IN} to P_{GND} pins and using a high current 5V driver IC.

THERMAL INFORMATION

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance (Min Cu) (1)(2)			150	°C/W
	Junction to ambient thermal resistance (Max Cu) (1)(2)			82	
$R_{\theta JC}$	Junction to case thermal resistance (Top of package) (2)			33	
	Junction to case thermal resistance (P_{GND} Pin) (2)			2.8	

(1) Device mounted on FR4 material with 1-inch^2 (6.45-cm^2) Cu.

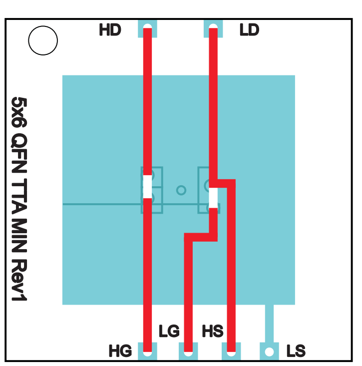
(2) $R_{\theta JC}$ is determined with the device mounted on a 1-inch^2 (6.45-cm^2), 2 oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 board. $R_{\theta JC}$ is specified by design while $R_{\theta JA}$ is determined by the user's board design.

ELECTRICAL CHARACTERISTICS

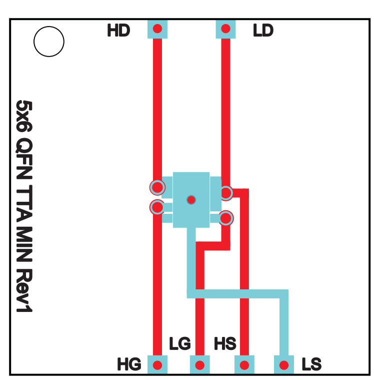
T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	Q1 Control FET			Q2 Sync FET			
			MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Static Characteristics									
BV_{DSS}	Drain to Source Voltage	V_{GS} = 0V, I_{DS} = 250μA	30			30			V
I_{DSS}	Drain to Source Leakage Current	V_{GS} = 0V, V_{DS} = 24V			1			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{DS} = 0V, V_{GS} = +10 / -8			100			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = 250μA	1		2.1	0.75		1.15	V
$Z_{DS(on)}$ (1)	Effective AC On-Impedance	V_{IN} = 12V, V_{GS} = 5V, V_{OUT} = 1.3V, I_{OUT} = 15A, f_{SW} = 500kHz, L_{OUT} = 0.3μH, T_J = 25ºC		9	10.8		2.8	3.6	mΩ
g_{fs}	Transconductance	V_{DS} = 15V, I_{DS} = 15A		51			87		S
Dynamic Characteristics									
C_{ISS}	Input Capacitance	V_{GS} = 0V, V_{DS} = 15V, f = 1MHz		740	890		1500	1800	pF
C_{OSS}	Output Capacitance			315	380		645	775	pF
C_{RSS}	Reverse Transfer Capacitance			12	14		38	46	pF
R_G	Series Gate Resistance			1.2	2.4		0.6	1.2	Ω
Q_g	Gate Charge Total (4.5V)	V_{DS} = 15V, I_{DS} = 15A		4.6	5.5		10.4	12.5	nC
Q_{gd}	Gate Charge - Gate to Drain			0.9			1.9		nC
Q_{gs}	Gate Charge - Gate to Source			1.5			2.2		nC
$Q_{g(th)}$	Gate Charge at Vth			0.9			1.2		nC
Q_{OSS}	Output Charge	V_{DS} = 9.8V, V_{GS} = 0V		6.6			13		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 15V, V_{GS} = 4.5V, I_{DS} = 15A, R_G = 2Ω		5.4			6.1		ns
t_r	Rise Time			11			7		ns
$t_{d(off)}$	Turn Off Delay Time			9.5			16		ns
t_f	Fall Time			2			2.7		ns
Diode Characteristics									
V_{SD}	Diode Forward Voltage	I_{DS} = 15A, V_{GS} = 0V		0.8			0.8		V
Q_{rr}	Reverse Recovery Charge	V_{dd} = 9.8V, I_F = 15A, di/dt = 300A/μs		11.3			16.3		nC
t_{rr}	Reverse Recovery Time			16			20		ns

(1) Equivalent System Performance based on application testing. See page 9 for details.



Max $R_{\theta JA}$ = 82°C/W when mounted on 1 inch^2 (6.45 cm^2) of 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 150°C/W when mounted on minimum pad area of 2-oz. (0.071-mm thick) Cu.

TYPICAL POWER BLOCK DEVICE CHARACTERISTICS

T_J = 125°C, unless stated otherwise.

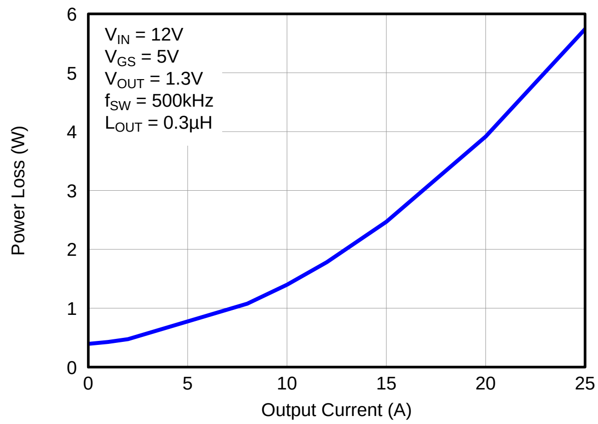


Figure 1. Power Loss vs Output Current

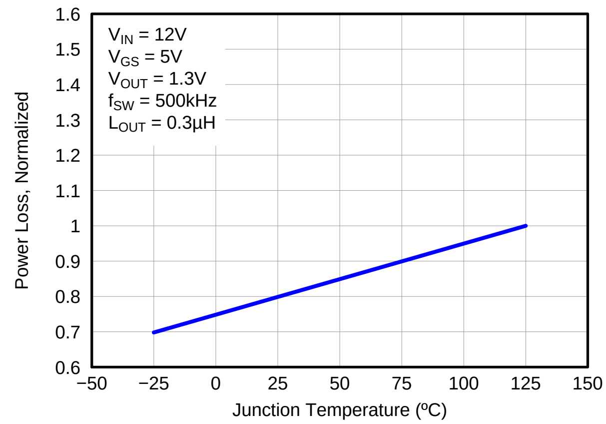


Figure 2. Normalized Power Loss vs Temperature

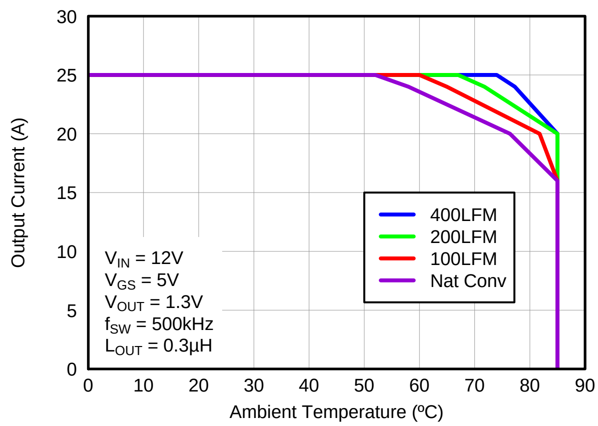


Figure 3. Safe Operating Area – PCB Vertical Mount(1)

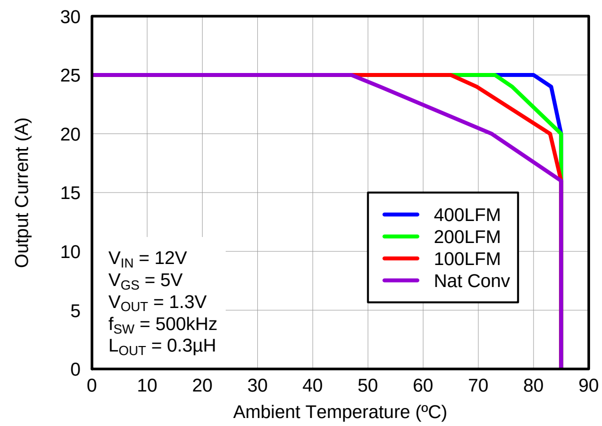


Figure 4. Safe Operating Area – PCB Horizontal Mount(1)

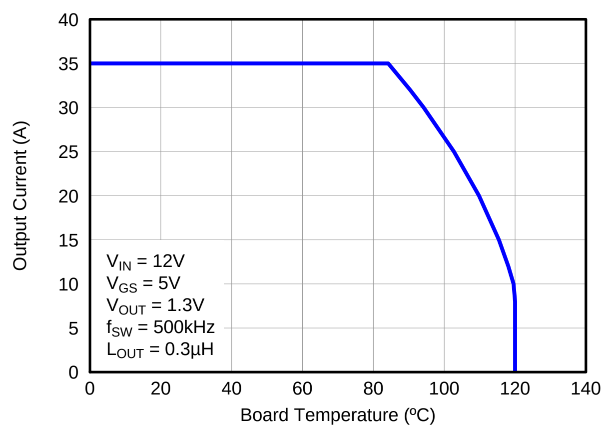


Figure 5. Typical Safe Operating Area(1)

(1) The Typical Power Block System Characteristic curves are based on measurements made on a PCB design with dimensions of 4.0" (W) × 3.5" (L) x 0.062" (H) and 6 copper layers of 1 oz. copper thickness. See Application Section for detailed explanation.

TYPICAL POWER BLOCK DEVICE CHARACTERISTICS (continued)

T_J = 125°C, unless stated otherwise.

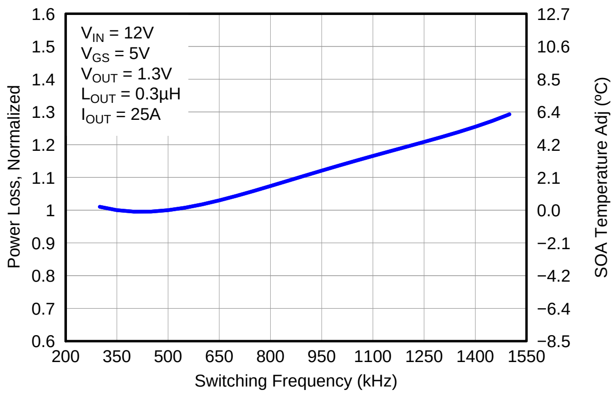


Figure 6. Normalized Power Loss vs Switching Frequency

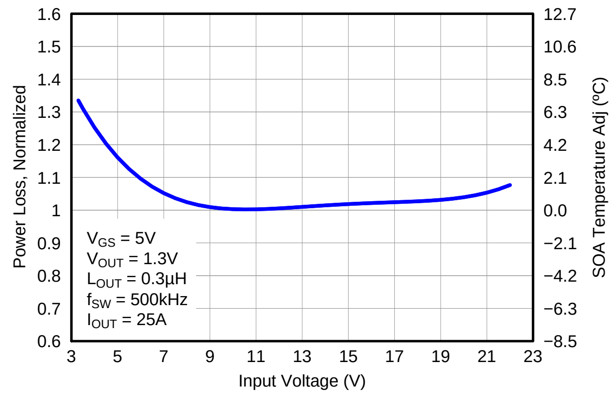


Figure 7. Normalized Power Loss vs Input Voltage

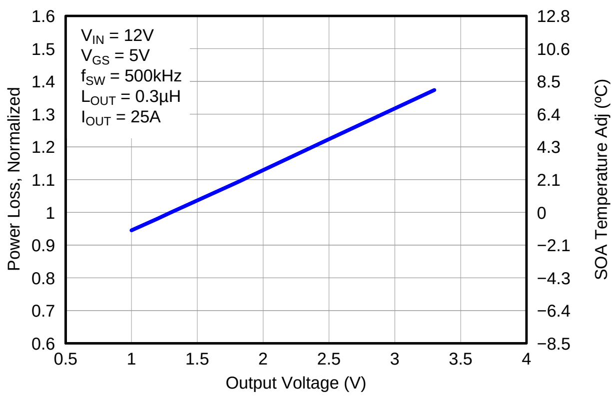


Figure 8. Normalized Power Loss vs. Output Voltage

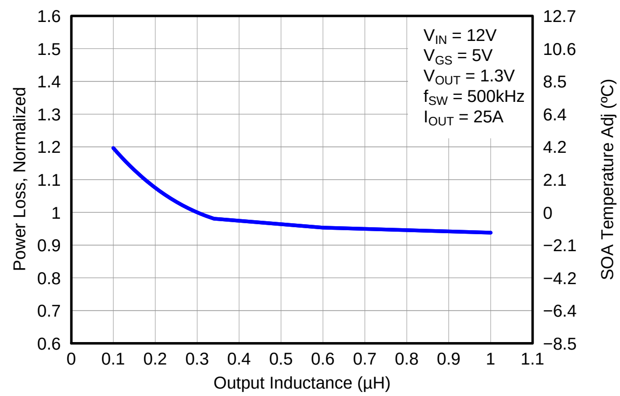


Figure 9. Normalized Power Loss vs. Output Inductance

TYPICAL POWER BLOCK MOSFET CHARACTERISTICS

T_A = 25°C, unless stated otherwise.

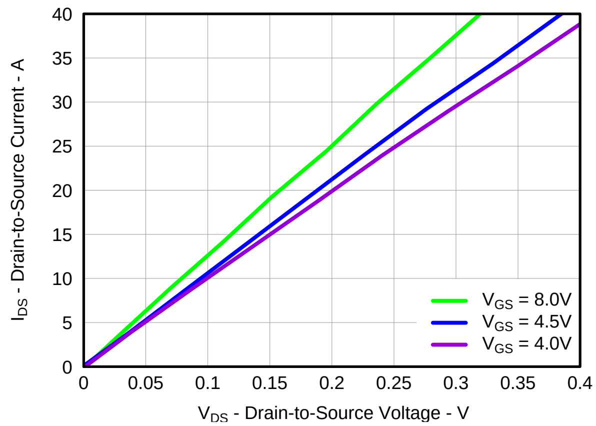


Figure 10. Control MOSFET Saturation

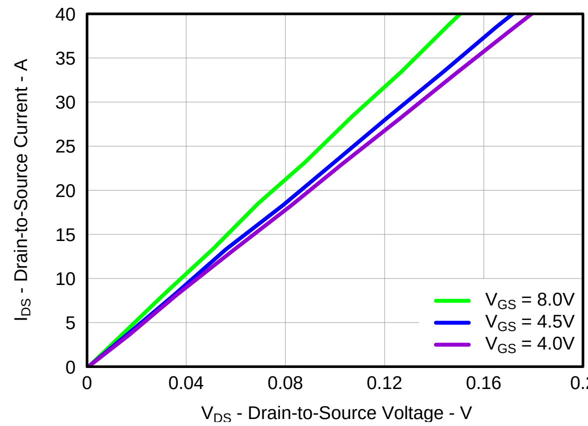


Figure 11. Sync MOSFET Saturation

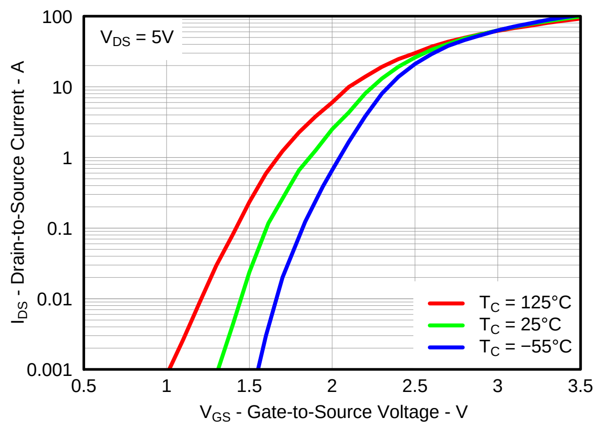


Figure 12. Control MOSFET Transfer

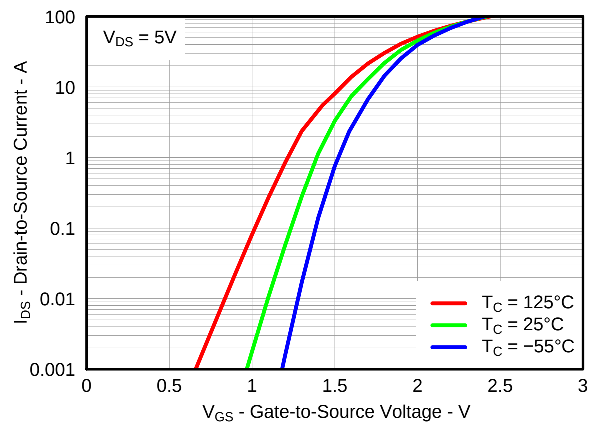


Figure 13. Sync MOSFET Transfer

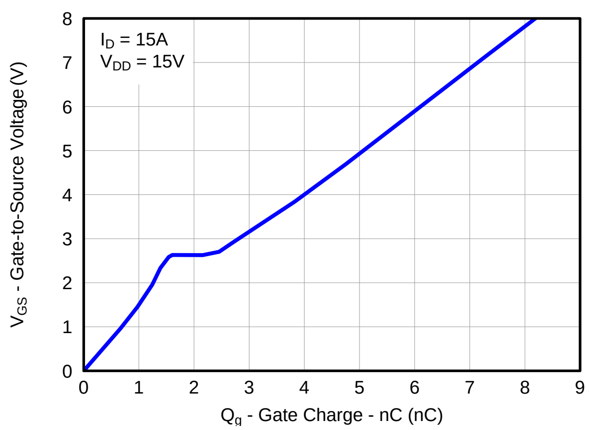


Figure 14. Control MOSFET Gate Charge

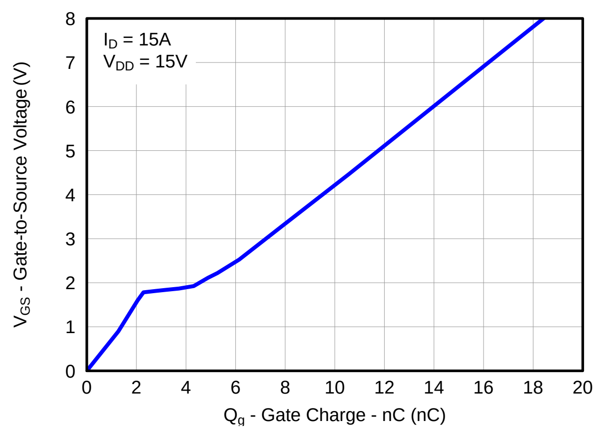


Figure 15. Sync MOSFET Gate Charge

TYPICAL POWER BLOCK MOSFET CHARACTERISTICS (continued)

T_A = 25°C, unless stated otherwise.

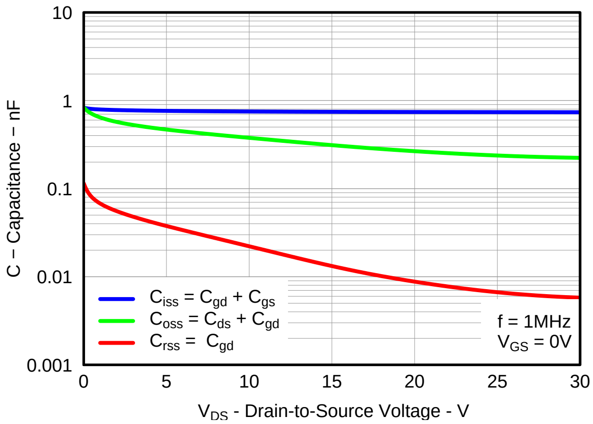


Figure 16. Control MOSFET Capacitance

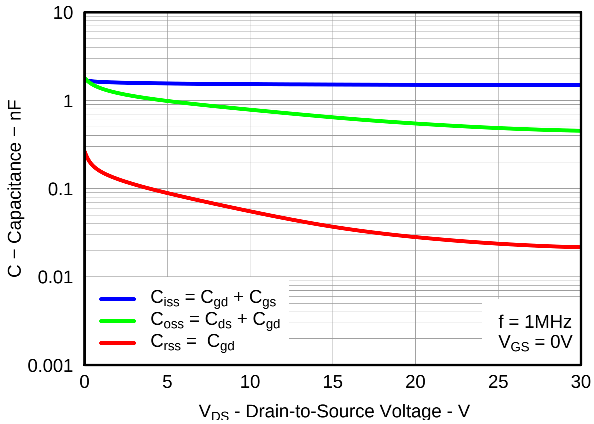


Figure 17. Sync MOSFET Capacitance

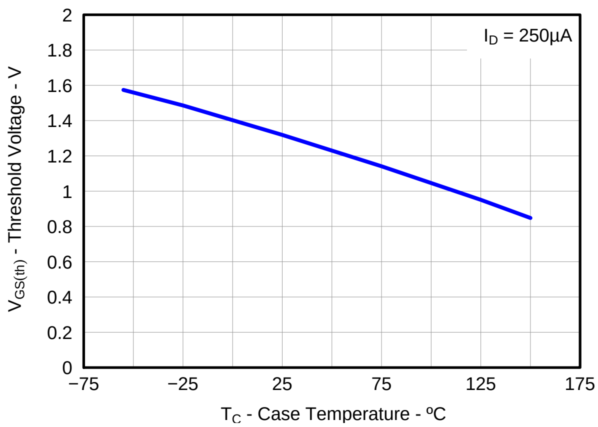


Figure 18. Control MOSFET $V_{GS(th)}$

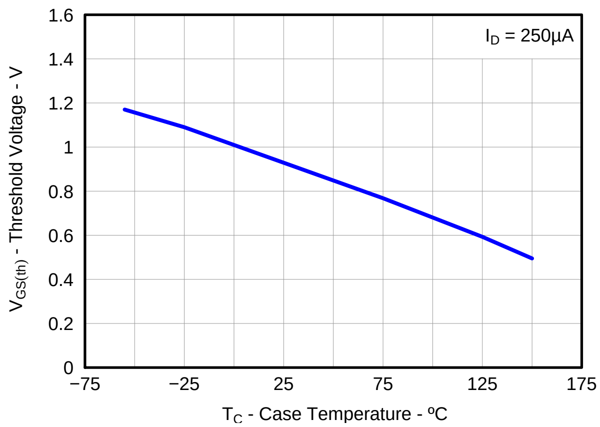


Figure 19. Sync MOSFET $V_{GS(th)}$

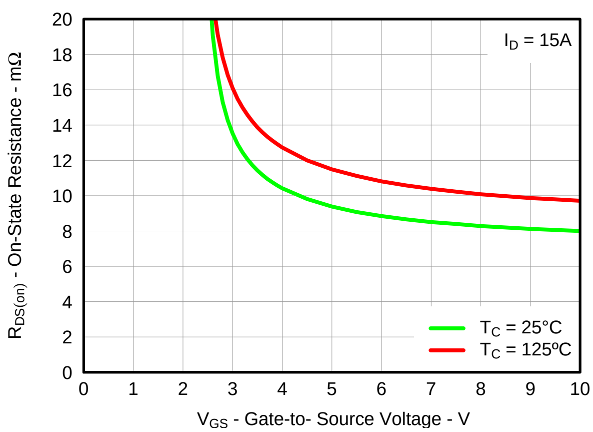


Figure 20. Control MOSFET $R_{DS(on)}$ vs V_{GS}

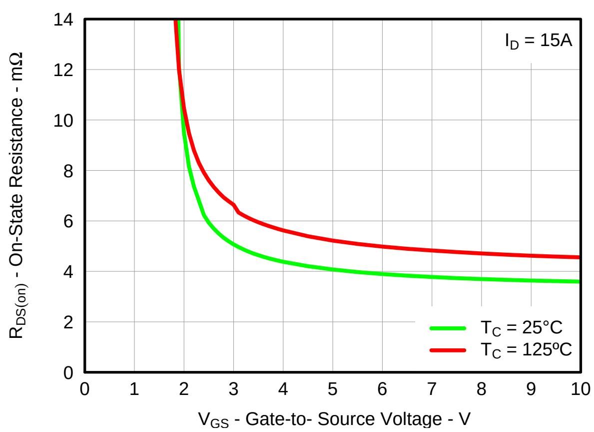


Figure 21. Sync MOSFET $R_{DS(on)}$ vs V_{GS}

TYPICAL POWER BLOCK MOSFET CHARACTERISTICS (continued)

T_A = 25°C, unless stated otherwise.

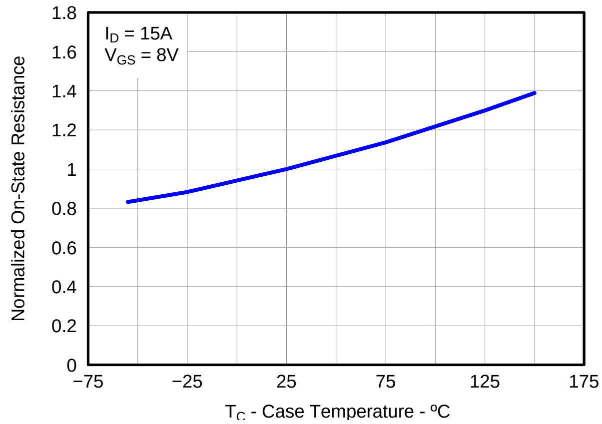


Figure 22. Control MOSFET Normalized $R_{DS(on)}$

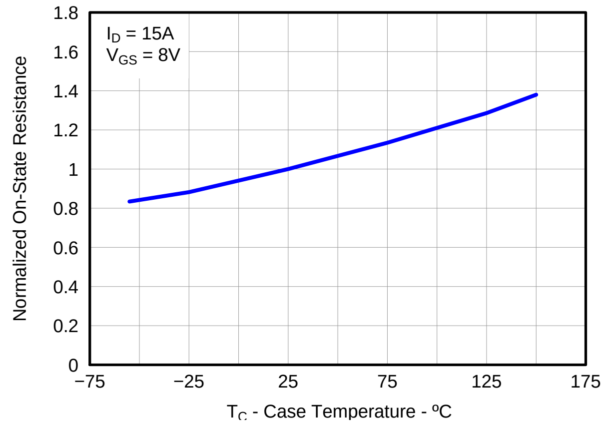


Figure 23. Sync MOSFET Normalized $R_{DS(on)}$

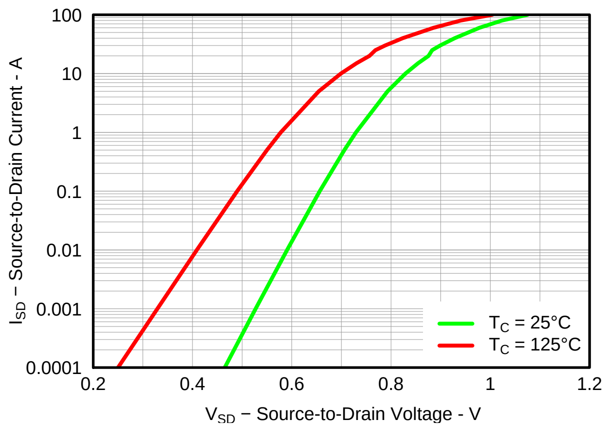


Figure 24. Control MOSFET Body Diode

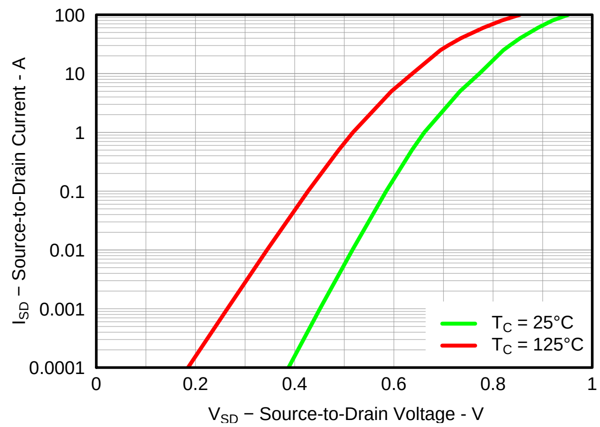


Figure 25. Sync MOSFET Body Diode

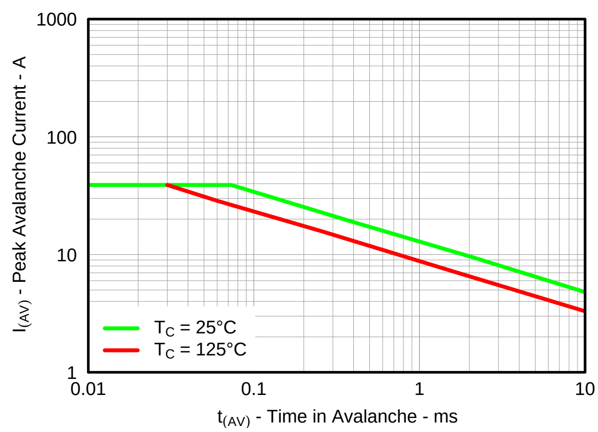


Figure 26. Control MOSFET Unclamped Inductive Switching

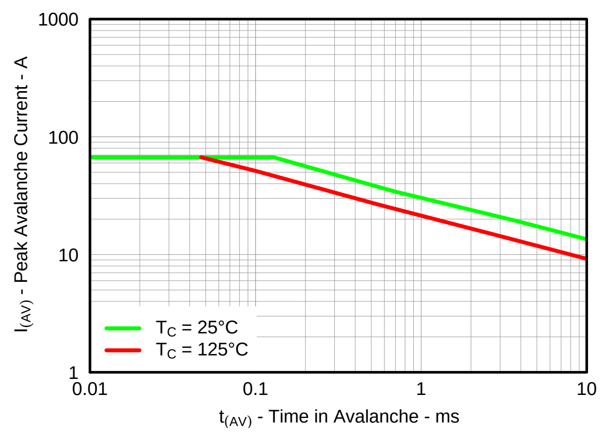


Figure 27. Sync MOSFET Unclamped Inductive Switching

APPLICATION INFORMATION

Equivalent System Performance

Many of today's high performance computing systems require low power consumption in an effort to reduce system operating temperatures and improve overall system efficiency. This has created a major emphasis on improving the conversion efficiency of today's Synchronous Buck Topology. In particular, there has been an emphasis in improving the performance of the critical Power Semiconductor in the Power Stage of this Application (see Figure 28). As such, optimization of the power semiconductors in these applications, needs to go beyond simply reducing $R_{DS(ON)}$.

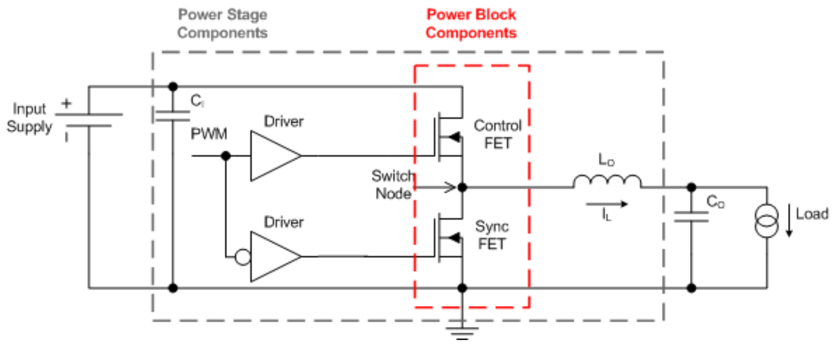


Figure 28.

The CSD87352Q5D is part of TI's Power Block product family which is a highly optimized product for use in a synchronous buck topology requiring high current, high efficiency, and high frequency. It incorporates TI's latest generation silicon which has been optimized for switching performance, as well as minimizing losses associated with Q_{GD}, Q_{GS}, and Q_{RR}. Furthermore, TI's patented packaging technology has minimized losses by nearly eliminating parasitic elements between the Control FET and Sync FET connections (see Figure 29). A key challenge solved by TI's patented packaging technology is the system level impact of Common Source Inductance (CSI). CSI greatly impedes the switching characteristics of any MOSFET which in turn increases switching losses and reduces system efficiency. As a result, the effects of CSI need to be considered during the MOSFET selection process. In addition, standard MOSFET switching loss equations used to predict system efficiency need to be modified in order to account for the effects of CSI. Further details behind the effects of CSI and modification of switching loss equations are outlined in TI's Application Note SLPA – 009.

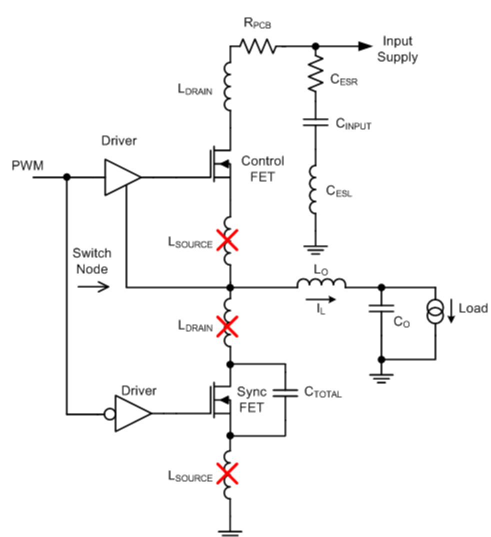


Figure 29.

The combination of TI's latest generation silicon and optimized packaging technology has created a benchmarking solution that outperforms industry standard MOSFET chipsets of similar $R_{DS(ON)}$ and MOSFET chipsets with lower $R_{DS(ON)}$. Figures 30 and 31 compare the efficiency and power loss performance of the CSD87352Q5D versus industry standard MOSFET chipsets commonly used in this type of application. This comparison purely focuses on the efficiency and generated loss of the power semiconductors only. The performance of CSD87352Q5D clearly highlights the importance of considering the Effective AC On-Impedance ($Z_{DS(ON)}$) during the MOSFET selection process of any new design. Simply normalizing to traditional MOSFET $R_{DS(ON)}$ specifications is not an indicator of the actual in-circuit performance when using TI's Power Block technology.

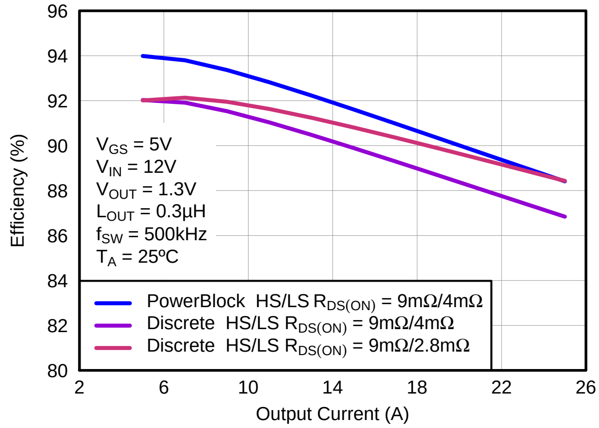


Figure 30.

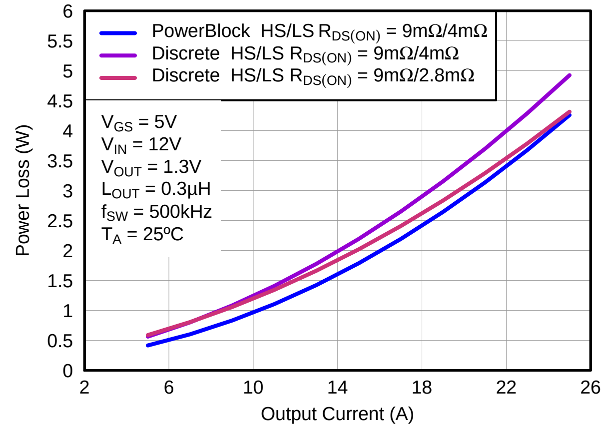


Figure 31.

The chart below compares the traditional DC measured $R_{DS(ON)}$ of CSD87352Q5D versus its $Z_{DS(ON)}$. This comparison takes into account the improved efficiency associated with TI's patented packaging technology. As such, when comparing TI's Power Block products to individually packaged discrete MOSFETs or dual MOSFETs in a standard package, the in-circuit switching performance of the solution must be considered. In this example, individually packaged discrete MOSFETs or dual MOSFETs in a standard package would need to have DC measured $R_{DS(ON)}$ values that are equivalent to CSD87352Q5D's $Z_{DS(ON)}$ value in order to have the same efficiency performance at full load. Mid to light-load efficiency will still be lower with individually packaged discrete MOSFETs or dual MOSFETs in a standard package.

Comparison of $R_{DS(ON)}$ vs. $Z_{DS(ON)}$

Parameter	HS		LS	
	Typ	Max	Typ	Max
Effective AC On-Impedance $Z_{DS(ON)}$ (V_{GS} = 5V)	9	10.8	2.8	3.6
DC Measured $R_{DS(ON)}$ (V_{GS} = 4.5V)	9	10.8	4	4.8

The CSD87352Q5D NexFET™ power block is an optimized design for synchronous buck applications using 5V gate drive. The Control FET and Sync FET silicon are parametrically tuned to yield the lowest power loss and highest system efficiency. As a result, a new rating method is needed which is tailored towards a more systems centric environment. System level performance curves such as Power Loss, Safe Operating Area, and normalized graphs allow engineers to predict the product performance in the actual application.

Power Loss Curves

MOSFET centric parameters such as $R_{DS(ON)}$ and Q_{gd} are needed to estimate the loss generated by the devices. In an effort to simplify the design process for engineers, Texas Instruments has provided measured power loss performance curves. Figure 1 plots the power loss of the CSD87352Q5D as a function of load current. This curve is measured by configuring and running the CSD87352Q5D as it would be in the final application (see Figure 32).The measured power loss is the CSD87352Q5D loss and consists of both input conversion loss and gate drive loss. Equation 1 is used to generate the power loss curve.

$$(V_{IN} \times I_{IN}) + (V_{DD} \times I_{DD}) - (V_{SW\_AVG} \times I_{OUT}) = \text{Power Loss} \quad (1)$$

The power loss curve in Figure 1 is measured at the maximum recommended junction temperatures of 125°C under isothermal test conditions.

Safe Operating Curves (SOA)

The SOA curves in the CSD87352Q5D data sheet provides guidance on the temperature boundaries within an operating system by incorporating the thermal resistance and system power loss. Figure 3 to Figure 5 outline the temperature and airflow conditions required for a given load current. The area under the curve dictates the safe operating area. All the curves are based on measurements made on a PCB design with dimensions of 4” (W) x 3.5” (L) x 0.062” (T) and 6 copper layers of 1 oz. copper thickness

Normalized Curves

The normalized curves in the CSD87352Q5D data sheet provides guidance on the Power Loss and SOA adjustments based on their application specific needs. These curves show how the power loss and SOA boundaries will adjust for a given set of systems conditions. The primary Y-axis is the normalized change in power loss and the secondary Y-axis is the change is system temperature required in order to comply with the SOA curve. The change in power loss is a multiplier for the Power Loss curve and the change in temperature is subtracted from the SOA curve.

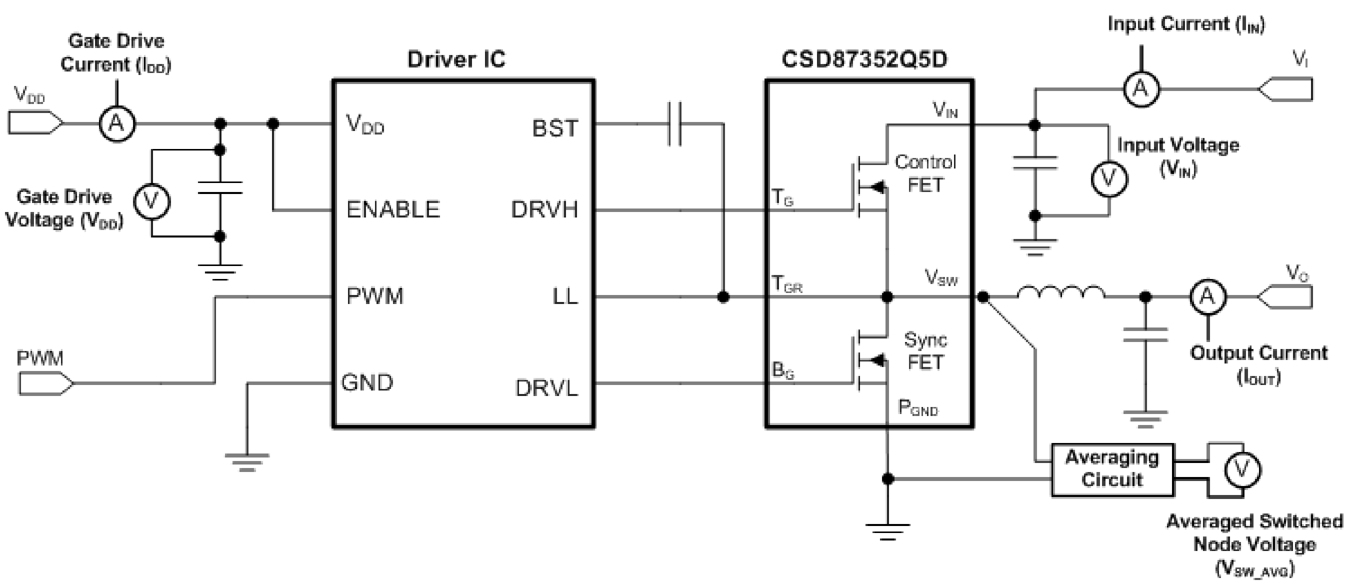


Figure 32. Typical Application

Calculating Power Loss and SOA

The user can estimate product loss and SOA boundaries by arithmetic means (see Design Example). Though the Power Loss and SOA curves in this data sheet are taken for a specific set of test conditions, the following procedure will outline the steps the user should take to predict product performance for any set of system conditions.

Design Example

Operating Conditions:

- Output Current = 15A
- Input Voltage = 7V
- Output Voltage = 1V
- Switching Frequency = 800kHz
- Inductor = 0.2µH

Calculating Power Loss

- Power Loss at 15A = 2.5W (Figure 1)
- Normalized Power Loss for input voltage ≈ 1.05 (Figure 7)
- Normalized Power Loss for output voltage ≈ 0.95 (Figure 8)
- Normalized Power Loss for switching frequency ≈ 1.08 (Figure 6)
- Normalized Power Loss for output inductor ≈ 1.07 (Figure 9)
- **Final calculated Power Loss = 2.5W x 1.05 x 0.95 x 1.08 x 1.07 ≈ 2.88W**

Calculating SOA Adjustments

- SOA adjustment for input voltage ≈ 1.05ºC (Figure 7)
- SOA adjustment for output voltage ≈ -1.05ºC (Figure 8)
- SOA adjustment for switching frequency ≈ 1.8ºC (Figure 6)
- SOA adjustment for output inductor ≈ 1.7ºC (Figure 9)
- **Final calculated SOA adjustment = 1.05 + (-1.05) + 1.8 + 1.7 ≈ 3.5ºC**

In the design example above, the estimated power loss of the CSD87352Q5D would increase to 2.88W. In addition, the maximum allowable board and/or ambient temperature would have to decrease by 3.5ºC. Figure 33 graphically shows how the SOA curve would be adjusted accordingly.

1. Start by drawing a horizontal line from the application current to the SOA curve.
2. Draw a vertical line from the SOA curve intercept down to the board/ambient temperature.
3. Adjust the SOA board/ambient temperature by subtracting the temperature adjustment value.

In the design example, the SOA temperature adjustment yields a reduction in allowable board/ambient temperature of 3.5ºC. In the event the adjustment value is a negative number, subtracting the negative number would yield an increase in allowable board/ambient temperature.

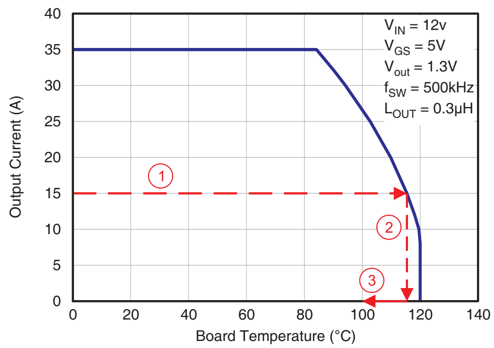


Figure 33. Power Block SOA

RECOMMENDED PCB DESIGN OVERVIEW

There are two key system-level parameters that can be addressed with a proper PCB design: Electrical and Thermal performance. Properly optimizing the PCB layout will yield maximum performance in both areas. A brief description on how to address each parameter is provided.

Electrical Performance

The Power Block has the ability to switch voltages at rates greater than 10kV/µs. Special care must be then taken with the PCB layout design and placement of the input capacitors, Driver IC, and output inductor.

- The placement of the input capacitors relative to the Power Block's VIN and PGND pins should have the highest priority during the component placement routine. It is critical to minimize these node lengths. As such, ceramic input capacitors need to be placed as close as possible to the VIN and PGND pins (see Figure 34). The example in Figure 34 uses 6x10µF ceramic capacitors (TDK Part # C3216X5R1C106KT or equivalent). Notice there are ceramic capacitors on both sides of the board with an appropriate amount of vias interconnecting both layers. In terms of priority of placement next to the Power Block, C5, C7, C19, and C8 should follow in order.
- The Driver IC should be placed relatively close to the Power Block Gate pins. T_G and B_G should connect to the outputs of the Driver IC. The T_{GR} pin serves as the return path of the high-side gate drive circuitry and should be connected to the Phase pin of the IC (sometimes called LX, LL, SW, PH, etc.). The bootstrap capacitor for the Driver IC will also connect to this pin.
- The switching node of the output inductor should be placed relatively close to the Power Block VSW pins. Minimizing the node length between these two components will reduce the PCB conduction losses and actually reduce the switching noise level.[(1)]

Thermal Performance

The Power Block has the ability to utilize the GND planes as the primary thermal path. As such, the use of thermal vias is an effective way to pull away heat from the device and into the system board. Concerns of solder voids and manufacturability problems can be addressed by the use of three basic tactics to minimize the amount of solder attach that will wick down the via barrel:

- Intentionally space out the vias from each other to avoid a cluster of holes in a given area.
- Use the smallest drill size allowed in your design. The example in Figure 34 uses vias with a 10 mil drill hole and a 16 mil capture pad.
- Tent the opposite side of the via with solder-mask.

In the end, the number and drill size of the thermal vias should align with the end user's PCB design rules and manufacturing capabilities.

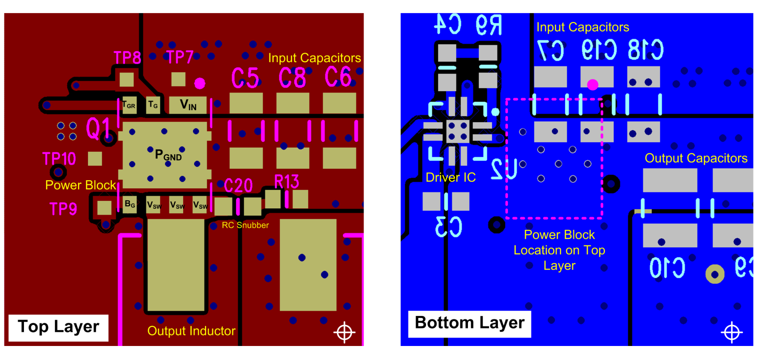
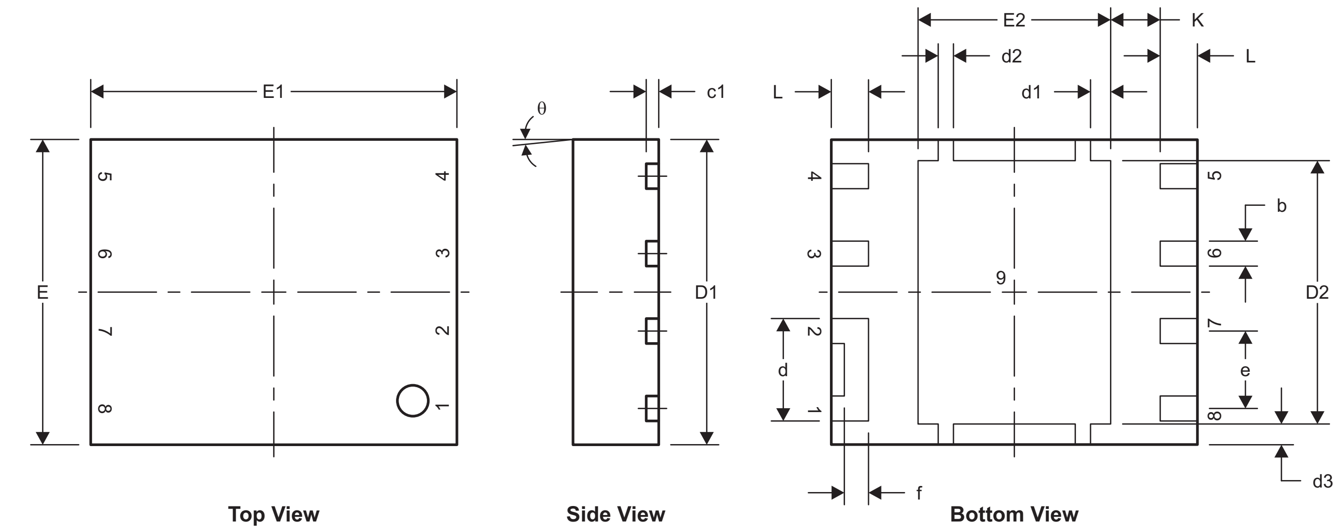


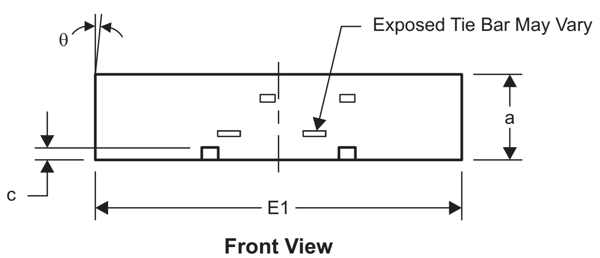
Figure 34. Recommended PCB Layout (Top Down View)

(1) Keong W. Kam, David Pommerenke, "EMI Analysis Methods for Synchronous Buck Converter EMI Root Cause Analysis", University of Missouri – Rolla

MECHANICAL DATA

Q5D Package Dimensions



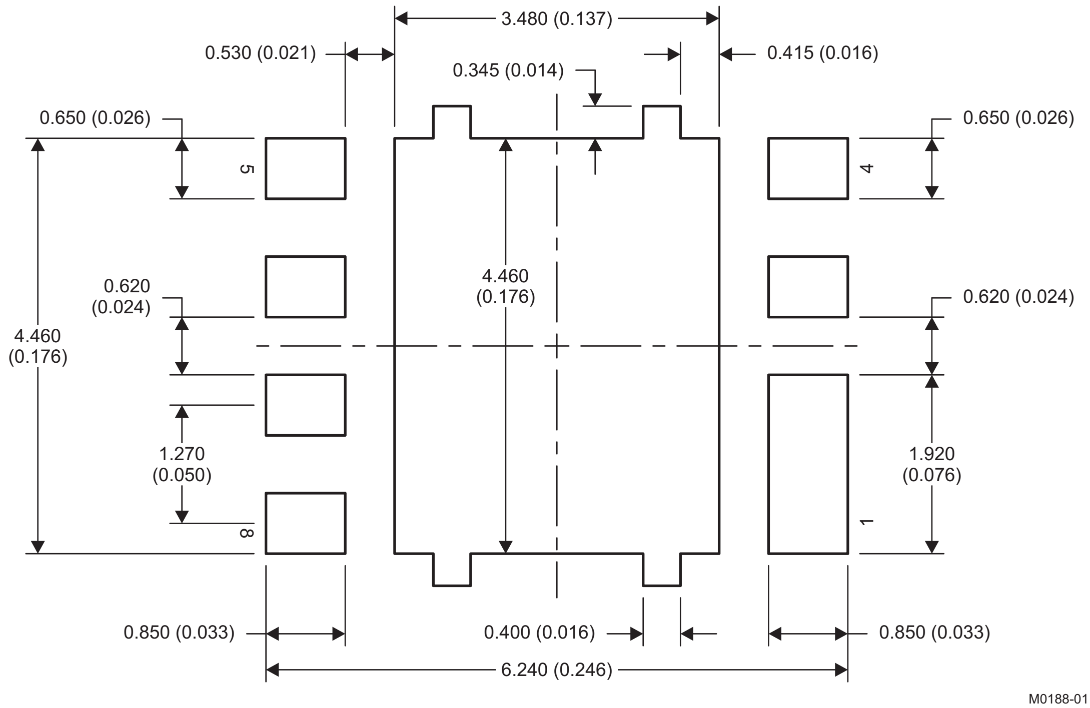


Pinout	
Position	Designation
Pin 1	V_{IN}
Pin 2	V_{IN}
Pin 3	T_G
Pin 4	T_{GR}
Pin 5	B_G
Pin 6	V_{SW}
Pin 7	V_{SW}
Pin 8	V_{SW}
Pin 9	P_{GND}

M0187-01

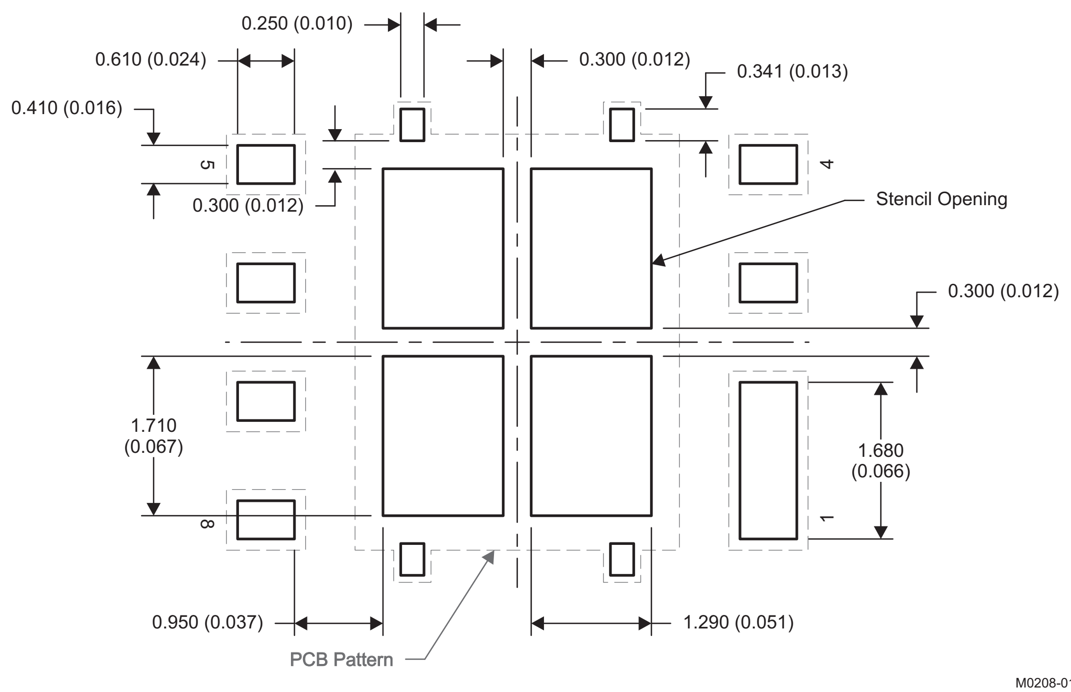
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
a	1.40	1.55	0.055	0.061
b	0.360	0.460	0.014	0.018
c	0.150	0.250	0.006	0.010
c1	0.150	0.250	0.006	0.010
d	1.630	1.730	0.064	0.068
d1	0.280	0.380	0.011	0.015
d2	0.200	0.300	0.008	0.012
d3	0.291	0.391	0.012	0.015
D1	4.900	5.100	0.193	0.201
D2	4.269	4.369	0.168	0.172
E	4.900	5.100	0.193	0.201
E1	5.900	6.100	0.232	0.240
E2	3.106	3.206	0.122	0.126
e	1.27 TYP		0.050	
f	0.396	0.496	0.016	0.020
L	0.510	0.710	0.020	0.028
θ	0.00	–	–	–
K	0.812		0.032	

Land Pattern Recommendation



NOTE: Dimensions are in mm (inches).

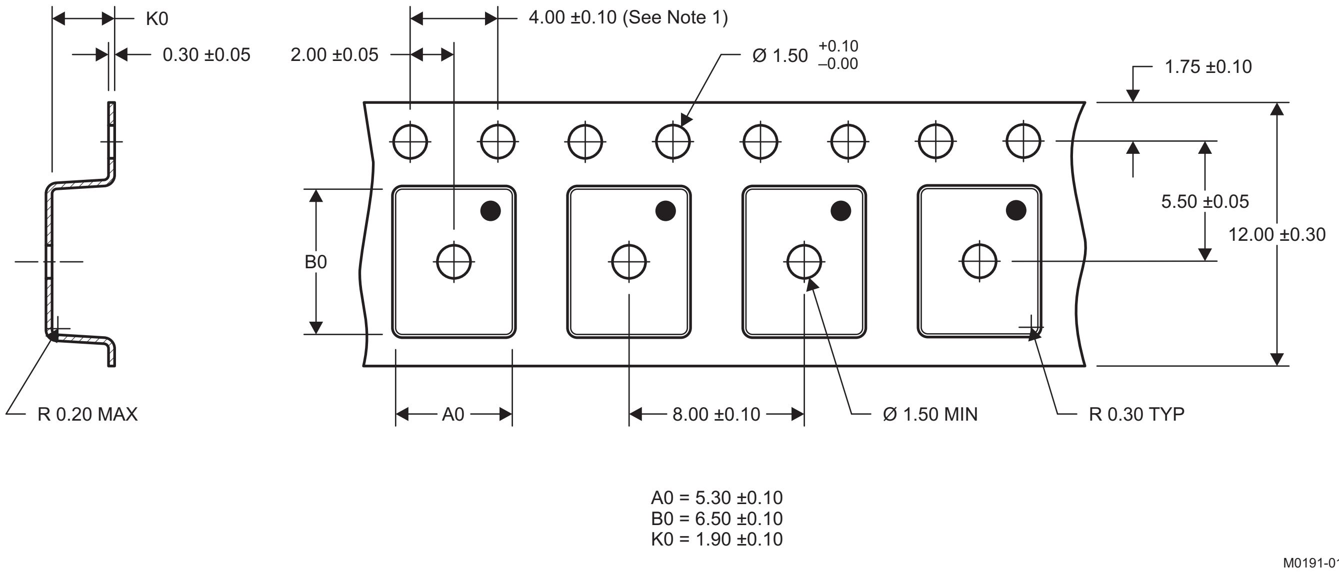
Stencil Recommendation



NOTE: Dimensions are in mm (inches).

For recommended circuit layout for PCB designs, see application note SLPA005 – *Reducing Ringing Through PCB Layout Techniques*.

Q5D Tape and Reel Information



NOTES:
1. 10-sprocket hole-pitch cumulative tolerance ±0.2
2. Camber not to exceed 1mm in 100mm, noncumulative over 250mm
3. Material: black static-dissipative polystyrene
4. All dimensions are in mm, unless otherwise specified.
5. Thickness: 0.30 ±0.05mm
6. MSL1 260°C (IR and convection) PbF reflow compatible

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
CSD87352Q5D	PREVIEW	SON	DQY	8	2500	TBD	Call TI	Call TI	

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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