MT6323 PMIC Technical Brief

Version: 0.1
Release date: 2013/1/10

Document Revision History

Revision	Date	Author	Description
0.1	2013/01/10	ShangYing Chung	Initial

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1 Overview

1.1 Features

- Handles all 2G/3G/smart phone baseband power management
- Input range: 3.4 ~ 4.5V
- 3 buck converters and 23 LDOs optimized for specific 2G/3G/smart phone subsystems
- Full-set high-quality audio feature: Supports uplink/downlink audio CODEC and high-power/quality audio amplifier
- 32K RTC crystal oscillator for system timing, 1.8 and 2.8V clock buffer output
- Multiple function GPIO
- Flexibility for various configurations of indicator LED current source: 4ISINK
- SPI interface
- Li-ion battery charging function
- Over-current and thermal overload protection
- Programmable under voltage lockout protection
- Watchdog timer
- Flexibility hardware PMIC reset function
- Power-on reset and start-up timer
- Precision voltage, temperature, and current measurement fuel gauge
- VFBGA - 145L package

1.2 Applications

Ideal for power management of 2G, 3G, smart phones and other portable systems.

1.3 General Descriptions

MT6323 is a power management system chip optimized for 2G/3G handsets and smart phones, especially based on the MediaTek MT6572 system solution. MT6323 contains 3 buck converters and 23 LDOs, which are optimized for specific 2G/3G/smart phone subsystems.

MT6323 provides mono 0.7W into 8Ω, high efficiency Class AB/D audio amplifiers and flexibility for various applications of indicator LED drivers. It supports up to 4 channel LEDs with independent controlled. Flexible control includes: register mode, PWM mode and breath mode.

Sophisticated controls are available for power-up, battery charging and the RTC alarm. MT6323 is optimized for maximum battery life. It allows the RTC circuit to stay alive without a battery for several hours. The battery charger in MT6323 supports lithium- ion (Li-ion) battery and provides pre-charge indication. The charger input voltage can be up to 10V and allows USB charging, too.

Some multi-purpose pins enable MT6323 to be configured in various applications.

MT6323 adopts SPI interface and SRCLKEN control pin to control buck converters, LDOs, Class AB/D, various drivers and charger. Besides, it provides enhanced safety control and protocol for handshaking with BB.

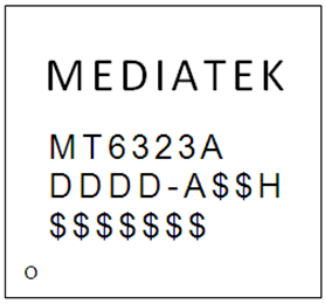
MT6323 is available in a VFBGA - 145L package. The operating temperature ranges from -25 to +85°C.

1.4 Ordering Information

Order #	Marking	Temp. range	Package
MT6323A/A		-25 ~ +85°C	VFBGA - 145L

1.5 Top Marking Definition

MT6323A/A



DDDD: Date Code
$$$$$$$: Random Code

1.6 Pin Assignments and Descriptions

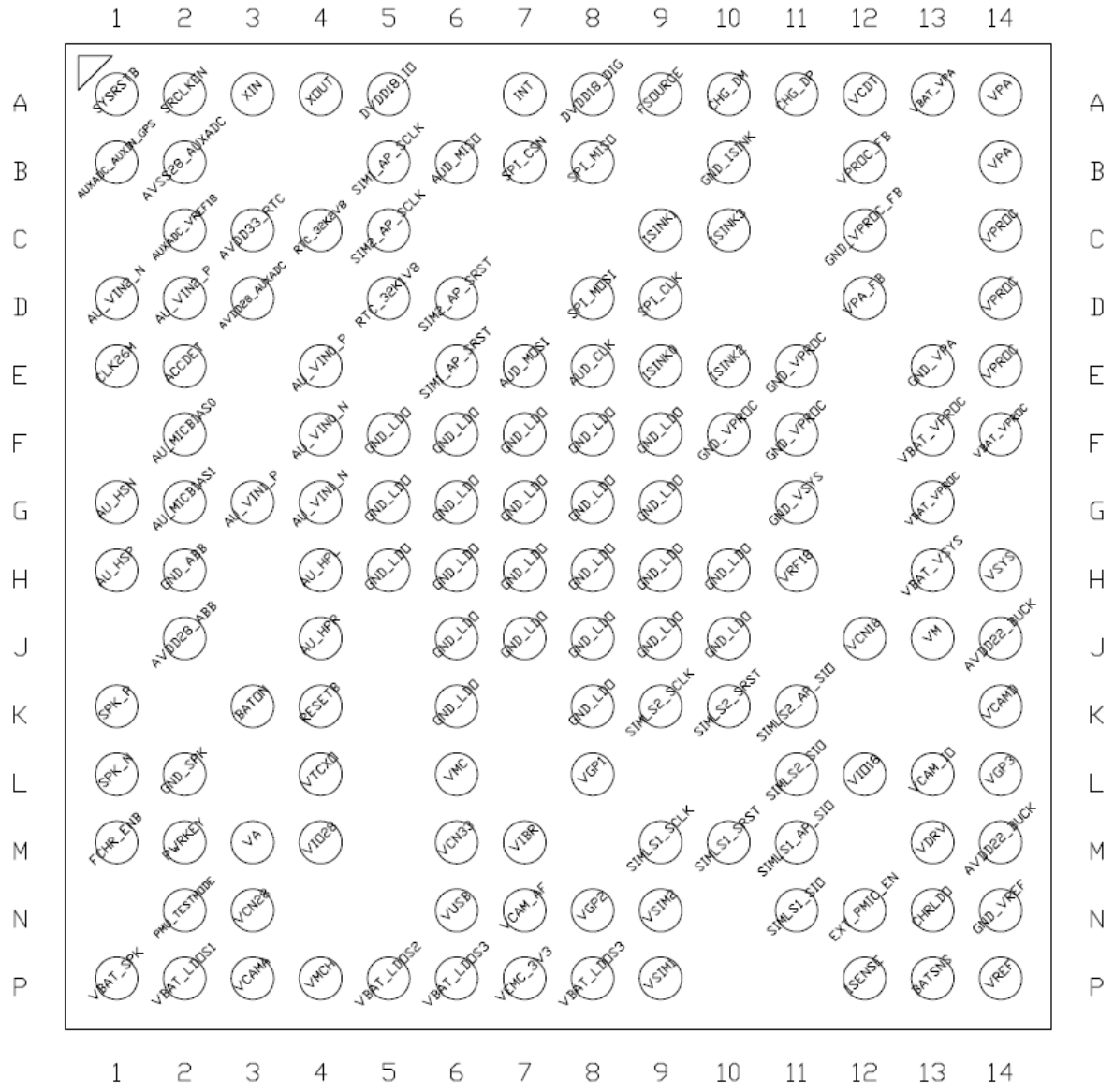


Figure 1-1. MT6323 VFBGA - 145L (5.8x5.8mm) pin assignment

Table 1-1. MT6323 pin descriptions

Ball	Symbol	I/O	Description
A1	SYSRSTB	I	Watchdog reset from AP
A10	CHG_DM	I	USB D- for BC1.1 standard
A11	CHG_DP	I	USB D+ for BC1.1 standard

Ball	Symbol	I/O	Description
A12	VCDT	I	Fractional charger input voltage for charger detection
A13	VBAT_VPA	PWR	Battery power supply input of VPA
A14	VPA	O	SW node of VPA
A2	SRCLKEN	I	26MHz CLK enable
A3	XIN	I	1. One of 32K crystal connection port while using crystal to generate 32kHz clock 2. Tie to ground with 32kHz crystal absence
A4	XOUT	I	1. One of 32K crystal connection port while using crystal to generate 32kHz clock 2. External 32kHz clock input with 32kHz crystal absence
A5	DVDD18_IO	PWR	Power of VIO18 IO/CORE
A7	INT	O	Default: Output 0 Interrupt to BB, high active
A8	DVDD18_DIG	PWR	Power of VDIG18
A9	FSOURCE	PWR	EFUSE power source
B1	AUXADC_AUXIN_GPS	I	AUXADC input
B10	GND_ISINK	GND	GND for ISINK
B12	VPROC_FB	I	Feedback of VPROC
B14	VPA	O	SW node of VPA
B2	AVSS28_AUXADC	GND	GND for AUXADC
B5	SIM1_AP_SCLK	I	AP/PMIC SIM1 clock
B6	AUD_MISO	O	Uplink AUDIO ADC serial data
B7	SPI_CSN	I	SPI interface's chip select signal to identify which device is selected
B8	SPI_MISO	IO	SPI interface's serial data signal. Default is output only.
C10	ISINK3	O	Current sink channel 3 output
C12	GND_VPROC_FB	I	Remote sense on ground of VPROC
C14	VPROC	O	SW node of VPROC
C2	AUXADC_VREF18	O	1.8V AUXADC reference output
C3	AVDD33_RTC	PWR	RTC LDO output. Supply of RTC macro where backup battery can be added.
C4	RTC_32K2V8	O	RTC domain 32kHz clock output
C5	SIM2_AP_SCLK	I	AP/PMIC SIM2 clock
C9	ISINK1	O	Current sink channel 1 output
D1	AU_VIN2_N	I	Analog input 3 negative
D12	VPA_FB	I	Feedback of VPA
D14	VPROC	O	SW node of VPROC
D2	AU_VIN2_P	I	Analog input 3 positive

Ball	Symbol	I/O	Description
D3	AVDD28_AUXADC	PWR	2.8V power input for AUXADC
D5	RTC_32K1V8	O	VIO18 domain 32kHz clock output
D6	SIM2_AP_SRST	I	AP/PMIC SIM2 SRST
D8	SPI_MOSI	IO	SPI interface's serial data signal. Default is input only.
D9	SPI_CLK	I	SPI interface's clock
E1	CLK26M	I	26MHz CLK
E10	ISINK2	O	Current sink channel 2 output
E11	GND_VPROC	GND	Ground of VPROC
E13	GND_VPA	GND	Ground of VPA
E14	VPROC	O	SW node of VPROC
E2	ACCDET	I	Accessory detection input
E4	AU_VIN0_P	I	Analog input 1 positive
E6	SIM1_AP_SRST	I	AP/PMIC SIM1 SRST
E7	AUD_MOSI	I	Downlink DAC serial data
E8	AUD_CLK	I	26M clock (can be hopping)
E9	ISINK0	O	Current sink channel 0 output
F10	GND_VPROC	GND	Ground of VPROC
F11	GND_VPROC	GND	Ground of VPROC
F13	VBAT_VPROC	PWR	Battery power supply input of VPROC
F14	VBAT_VPROC	PWR	Battery power supply input of VPROC
F2	AU_MICBIAS0	PWR	Microphone bias for main and 2nd microphone
F4	AU_VIN0_N	I	Analog input 1 negative
F5	GND_LDO	GND	Ground for LDO
F6	GND_LDO	GND	Ground for LDO
F7	GND_LDO	GND	Ground for LDO
F8	GND_LDO	GND	Ground for LDO
F9	GND_LDO	GND	Ground for LDO
G1	AU_HSN	O	Receiver output
G11	GND_VSYS	GND	Ground of VSYS BUCK
G13	VBAT_VPROC	PWR	Battery power supply input of VPROC
G2	AU_MICBIAS1	PWR	Microphone vias for earphone
G3	AU_VIN1_P	I	Analog input 2 positive
G4	AU_VIN1_N	I	Analog input 2 negative
G5	GND_LDO	GND	Ground for LDO
G6	GND_LDO	GND	Ground for LDO
G7	GND_LDO	GND	Ground for LDO
G8	GND_LDO	GND	Ground for LDO

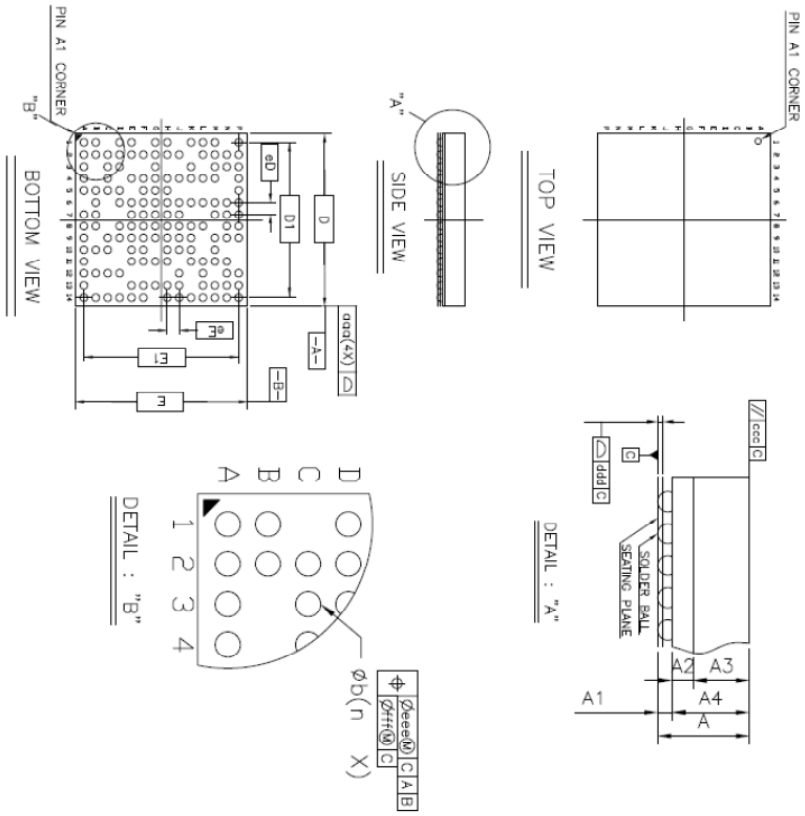
Ball	Symbol	I/O	Description
G9	GND_LDO	GND	Ground for LDO
H1	AU_HSP	O	Receiver output
H10	GND_LDO	GND	Ground for LDO
H11	VRF18	O	VRF18 output voltage
H13	VBAT_VSYS	PWR	Battery power supply input of VSYS BUCK
H14	VSYS	O	SW node of VSYS BUCK
H2	GND_ABB	GND	GND of ABB
H4	AU_HPL	O	Headphone L-ch output
H5	GND_LDO	GND	Ground for LDO
H6	GND_LDO	GND	Ground for LDO
H7	GND_LDO	GND	Ground for LDO
H8	GND_LDO	GND	Ground for LDO
H9	GND_LDO	GND	Ground for LDO
J10	GND_LDO	GND	Ground for LDO
J12	VCN18	O	VCN18 output voltage
J13	VM	O	VM output voltage
J14	AVDD22_BUCK	PWR	Power supply input of VSYSLDO
J2	AVDD28_ABB	PWR	2.8V power input for ABB
J4	AU_HPR	O	Headphone R-ch output
J6	GND_LDO	GND	Ground for LDO
J7	GND_LDO	GND	Ground for LDO
J8	GND_LDO	GND	Ground for LDO
J9	GND_LDO	GND	Ground for LDO
K1	SPK_P	O	Positive output for internal speaker amp
K10	SIMLS2_SRST	O	SIMLS2 SRST
K11	SIMLS2_AP_SIO	IO	SIM2_AP data signal
K14	VCAMD	O	VCAMD output voltage
K3	BATON	I	Battery NTC pin for battery and its temperature sensing
K4	RESETB	O	System reset release signal
K6	GND_LDO	GND	Ground for LDO
K8	GND_LDO	GND	Ground for LDO
K9	SIMLS2_SCLK	O	SIMLS2 SCLK
L1	SPK_N	O	Negative output for internal speaker amp
L11	SIMLS2_SIO	IO	SIMLS2 data signal
L12	VIO18	O	VIO18 output voltage
L13	VCAM_IO	O	VCAM_IO output voltage
L14	VGP3	O	VGP3 output voltage

Ball	Symbol	I/O	Description
L2	GND_SPK	GND	Ground for VBAT_SPK
L4	VTCXO	O	VTLDO output voltage
L6	VMC	O	VMC output voltage
L8	VGP1	O	VGP1 output voltage
M1	FCHR_ENB	I	Force charging ENB
M10	SIMLS1_SRST	O	SIMLS1 SRST
M11	SIMLS1_AP_SIO	IO	SIM1_AP data signal
M13	VDRV	O	Charger current drive output
M14	AVDD22_BUCK	PWR	Power supply input of VSYSLDO
M2	PWRKEY	I	Power key signal
M3	VA	O	VA output voltage
M4	VIO28	O	VIO28 output voltage
M6	VCN33	O	VCN33 output voltage
M7	VIBR	O	VIBR output voltage
M9	SIMLS1_SCLK	O	SIMLS1 SCLK
N11	SIMLS1_SIO	IO	SIMLS1 data signal
N12	EXT_PMIC_EN	O	External PMIC enable (vbat domain)
N13	CHRLDO	O	Charger LDO28 output
N14	GND_VREF	GND	Ground for bandgap
N2	PMU_TESTMODE	I	PMU testmode signal (tied to GND in normal operation)
N3	VCN28	O	VCN28 output voltage
N6	VUSB	O	VSUB output voltage
N7	VCAM_AF	O	VCAM_AF output voltage
N8	VGP2	O	VGP2 output voltage
N9	VSIM2	O	VSIM2 output voltage
P1	VBAT_SPK	PWR	Battery power supply input of SPK
P12	ISENSE	I	Positive terminal for battery's charging current sensing resistor
P13	BATSNS	I	Negative terminal for battery's charging current sensing resistor
P14	VREF	O	Bandgap reference voltage
P2	VBAT_LDOS1	PWR	LDO1 vbat power
P3	VCAMA	O	VCAMA output voltage
P4	VMCH	O	VMCH output voltage
P5	VBAT_LDOS2	PWR	LDO2 vbat power
P6	VBAT_LDOS3	PWR	LDO3 vbat power
P7	VEMC_3V3	O	VEMC_3V3 output voltage

Ball	Symbol	I/O	Description
P8	VBAT_LDOS3	PWR	LDO3 vbat power
P9	VSIM1	O	VSIM1 output voltage

2 MT6323 Packaging

2.1 Package Dimensions



Item		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package Type			VFBGA		
Body Size	X	D	5.70	5.80	5.90
	Y	E	5.70	5.80	5.90
Ball Pitch	X	eD		0.40	
	Y	eE		0.40	
Total Thickness		A	-	-	1.00
Mold Thickness		A3		0.65 Ref.	
Substrate Thickness		A2		0.11 Ref.	
Substrate+Mold Thickness		A4	0.69	0.76	0.83
Ball Diameter				0.25	
Stand Off		A1	0.12	0.16	0.20
Ball Width		b	0.20	0.25	0.30
Package Edge Tolerance		aaa		0.05	
Mold Flatness		ccc		0.10	
Coplanarity		ddd		0.08	
Ball Offset (Package)		eee		0.15	
Ball Offset (Ball)		fff		0.05	
Ball Count		n		145	
Edge Ball Center to Center	X	D1		5.20	
	Y	E1		5.20	

Appendix

N/A