TPS65094 PMIC for Intel™ Apollo Lake Platform

1 Device Overview

1.1 Features

- Wide V_{IN} range from 5.6 V to 21 V
- Three variable-output voltage synchronous Step-down controllers With D-CAP2™ Topology
  - 5 A for BUCK1 (VNN), 7 A for BUCK6 (VDDQ), and 21 A for BUCK2 (VCCGI) using external FETs for typical applications
  - I^2C Dynamic Voltage Scaling (DVS) control (0.5 V to 1.45 V in 10-mV Steps) for BUCK1 and BUCK2
  - OTP-Programmable default output voltage for BUCK6 (VDDQ)
- Three variable-output voltage synchronous Step-down converters with dcs-control topology and I^2C DVS capabilities
  - V_{IN} range from 4.5 V to 5.5 V
  - 3 A of output current for BUCK3 (VCCRAM)
  - 2 A of output current for BUCK4 (V1P8A) and BUCK5 (V1P24A) for typical applications
- Three LDO regulators with adjustable output voltage
  - LDOA1: I^2C-Selectable output voltage from 1.35 V to 3.3 V for up to 200 mA of output current
  - LDOA2 and LDOA3: I^2C-Selectable output voltage from 0.7 V to 1.5 V for up to 600 mA of Output Current
- VTT LDO for DDR memory termination
- Three load switches with slew rate control
  - Up to 400 mA of output current with voltage drop less than 1.5% of nominal input voltage
  - R_{DSON} < 96 mΩ at input voltage of 1.8 V
- I^2C Interface (device address 0x5E) supports:
  - Standard mode (100 kHz)
  - Fast mode (400 kHz)
  - Fast mode plus (1 MHz)

1.2 Applications

- 2-, 3-, or 4-Series cell li-ion battery-powered products (NVDC or Non-NVDC)
- Wall-powered designs, particularly from 12-V supply
- Tablets, Ultrabook™, and notebook computers
- Mobile PCs and mobile internet devices

1.3 Description

The TPS65094 device is a single-chip solution, power-management integrated chip (PMIC) designed specifically for the latest Intel™ processors targeted for tablets, ultrabooks, notebooks, industrial PCs, and Internet-of-Things (IOT) applications using 2S, 3S, or 4S Li-Ion battery packs (NVDC or non-NVDC power architectures), as well as wall-powered applications.

The TPS65094 device is used for essential systems with low-voltage rails merged for the smallest footprint and lowest-cost system-power solution. The TPS65094 device provides the complete power solution based on the Intel Reference Designs. Six highly efficient step-down voltage regulators (VRs), a sink or source LDO (VTT), and a load switch are controlled by power-up sequence logic to provide the proper power rails, sequencing, and protection—including DDR3 and DDR4 memory power. The two regulators (BUCK1 and BUCK2) support dynamic voltage scaling (DVS) for maximum efficiency—including support for Connected Standby. The high-frequency VRs use small inductors and capacitors to achieve a small solution size. An I^2C interface allows simple control by an embedded controller (EC) or by a system on chip (SoC).

The PMIC comes in an 8-mm × 8-mm single-row VQFN package with a thermal pad for good thermal dissipation and ease of board routing.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS65094	VQFN (64)	8.00 mm × 8.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

1.4 Functional Block Diagram

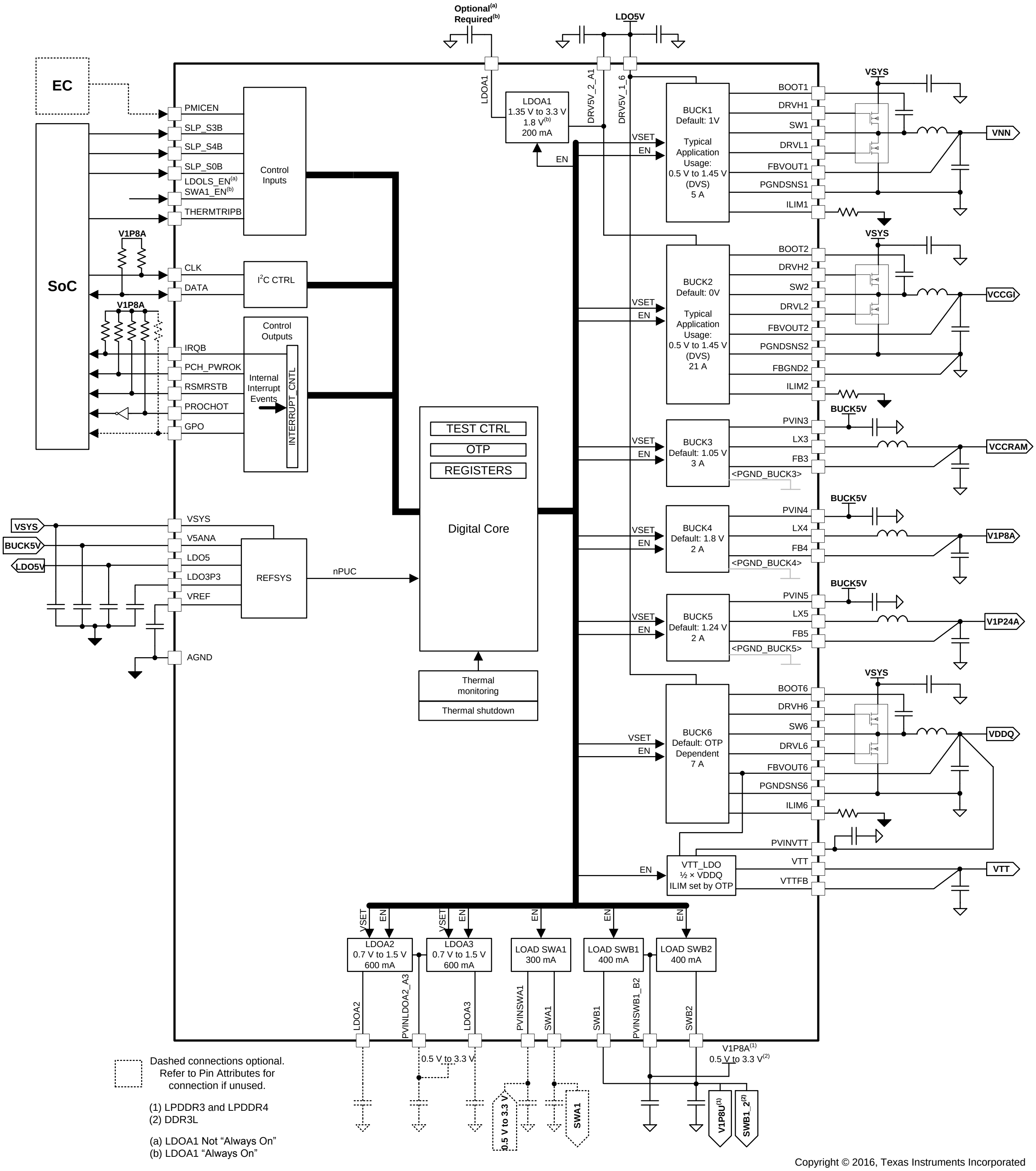


Figure 1-1. PMIC Functional Block Diagram

Table of Contents

2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (February 2017) to Revision C	Page
• Changed TPS65094x to TPS65094 in title	1
• Deleted variants from top of each page	1
• Added "BUCK3-5 Mode" row and "TPS650945" column to *Summary of TPS65094x OTP Differences* table	6
• Changed the description of the VTTFB pin in the *Pin Functions* table	9
• Changed VSYS to PVIN in the efficiency graphs for BUCK3, BUCK4, and BUCK5 in the *Typical Characteristics* section	28
• Added to the description of the deassertion condition that causes an emergency shutdown in the *Emergency Shutdown* section	48
• Added TPS650945 settings to Section 6.6	53
• Changed OCP event to power fault event in the OCP bit description in the *OFFONSRC Register Field Descriptions* table	55
• Changed second reference of TPS650940 to TPS650944 for the bit reset values in the *LDOA2VID Register Field Descriptions* and *LDOA3VID Register Field Descriptions* tables	62
• Changed the bit values of the LDOA3_SLPVID[0] and LDOA3_VID[0] bits in the *LDOA3VID Register* figure	62

Changes from Revision A (June 2016) to Revision B	Page
• Updated the PROCHOT pin description in the *Pin Functions* table	10
• Changed the values for LX3, LX4, LX5 from –1 V and 7 V to –2 V and 8 V in the *Absolute Maximum Ratings* table	11
• Changed the reset value of the LDOA2 VID register (LDOA2VID) to OTP dependent	62
• Added the *Receiving Notification of Documentation Updates* section	84
• Changed the *Electrostatic Discharge Caution* statement	84

Changes from September 11, 2015 to June 2, 2016 (from * Revision (September 2015) to A Revision)	Page
• Released full data sheet as SWCS133A version from SWCS130B version	1
• Changed device status to PROD_DATA	1
• Changed V_{IN} recommended minimum	1
• Changed Features to improve description of converters	1
• Changed Features to up to 400 mA of output current for load switches	1
• Changed functional block diagram to include TPS65094x family	3
• Changed the *Functional Block Diagram* to include an inverter on PROCHOT pin	3
• Changed PROCHOTB to PROCHOT throughout the document	7
• Changed minimum absolute-maximum-rating value for SW1, SW2, and SW6 in Section 5.1	11
• Changed VSYS in Section 5.3, *Recommended Operating Conditions*	12
• Deleted nominal value from PVINVTT in Section 5.3, *Recommended Operating Conditions*	12
• Deleted (nu = symbol for efficiency)	14
• Changed BUCK1 DC output voltage step size to show full range and be consistent in Section 5.7	14
• Changed typo to match correct default of 1 V for ΔV_{OUT_TR} in Section 5.7	14
• Changed BUCK2 DC output voltage to show full range and be consistent in Section 5.7	15
• Changed set condition for BUCK6 for V_{OUT} range in Section 5.7 to match BUCK1 and BUCK2	16
• Updated formatting and added new OTP information for BUCK6 in Section 5.7	16
• Updated formatting for BUCK3 DC output voltage in Section 5.8	18
• Changed DC output voltage formatting for BUCK4 in Section 5.8	19
• Changed maximum I_{OUT} value for BUCK4 in Section 5.8 to match device capabilities	19
• Changed I_{OUT} and $\Delta V_{OUT}/\Delta I_{OUT}$ for VTT LDO in Section 5.9 for new OTPs	24
• Changed test conditions for VTT LDO overcurrent protection in Section 5.9	24
• Changed Section 5.10 to show SWB1_2 R_{DSON} is specified per output	25
• Changed f_{SW} values in Section 5.15 to provide more values	27
• Changed current to 1.9 A to match SoC requirements in Table 6-1	29
• Changed BUCK6, LDOA2, LDOA3 typical output voltage range to: OTP Dependent in Table 6-1	29
• Changed table note to include additional DDR types in Table 6-1	29
• Changed *PMIC Functional Block Diagram* to match specifications table	31
• Changed PROCHOTB to PROCHOT in the *Apollo Lake Power Map*	31
• Changed current ratings in *Apollo Lake Power Map*	31
• Deleted SWBx PG from PG of PCH_PWROK in Table 6-2	32
• Changed BUCK1–2 to all BUCKs and LDOAs in Section 6.3.3.3	37
• Added Table 6-5 and Table 6-6 to Section 6.3.4.2	39
• Added more DDR values to the table note in Table 6-7	40
• Changed Section 6.3.5 to include LDOA1 and reset information	41
• Changed Section 6.6 to include multiple DDRs	41
• Changed Figure 6-7 and Figure 6-8 to include alternate SWB1_2 Timing	43
• Changed SWB1_2 from: V3P3A to: V1P8U in Table 6-10	43
• Changed VDDQ voltage to OTP Dependent and SWBx to SWB1_2 in Table 6-11	45
• Updated Figure 6-10 to include alternate SWB1_2 Timing	46
• Changed Section 6.3.5.5 to include alternate SWB1_2 Timing	47
• Changed Section 6.3.5.6 to include THERMTRIPB	48
• Added the TPS65094x family OTP values to Section 6.6	53
• Replaced VID values with link to full VID table in Table 6-18 and Table 6-19	56
• Updated naming of bits in the TEMPHOT register	71

3 Device Options

3.1 OTP Comparison

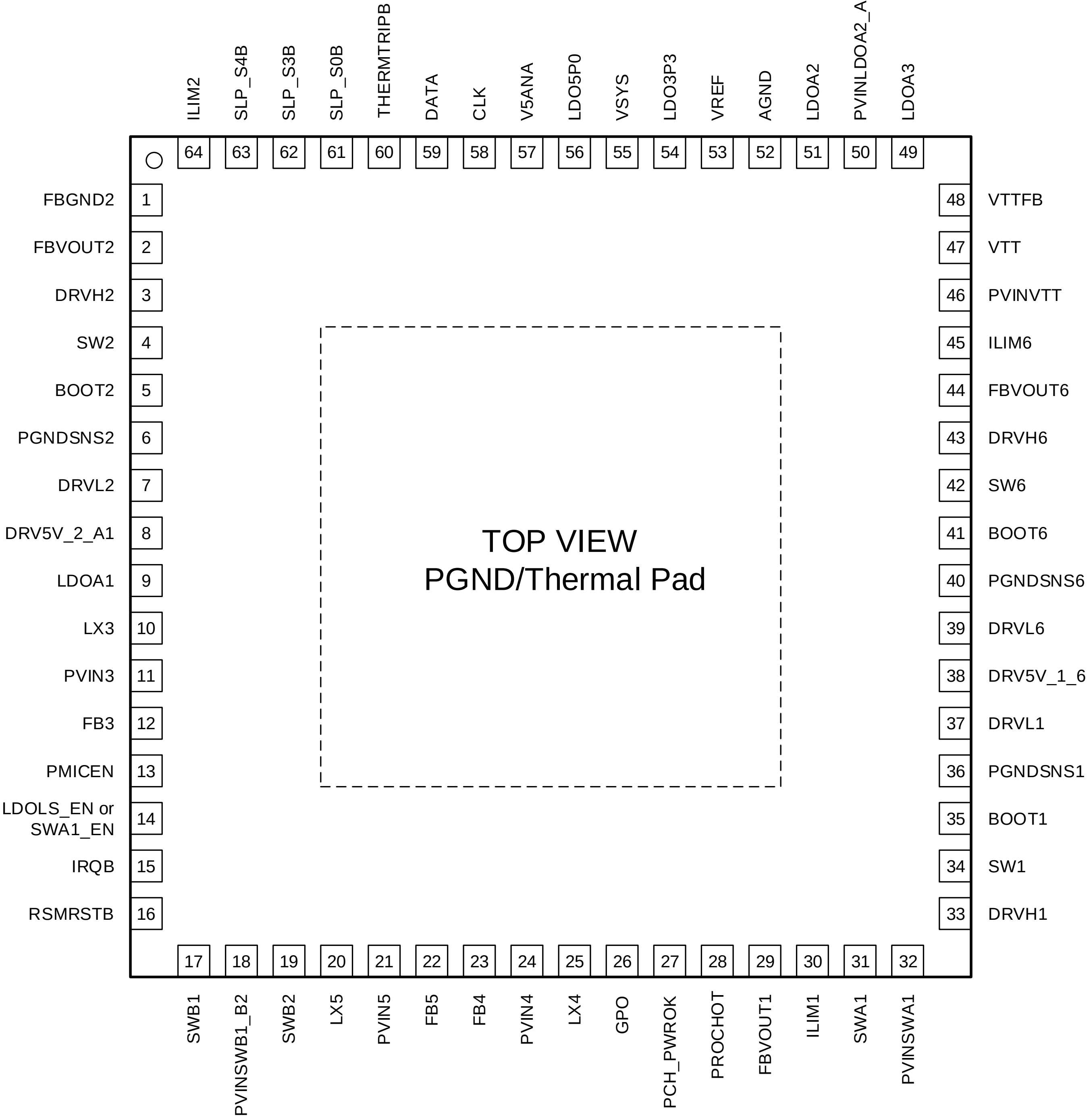
Table 3-1 summarizes the differences between the various TPS65094x family OTPs.

Table 3-1. Summary of TPS65094x OTP Differences

	TPS650940	TPS650941	TPS650942	TPS650944	TPS650945
DDR	LPDDR4	LPDDR3	DDR3L	LPDDR4	LPDDR4
BUCK6 Voltage	1.1 V	1.2 V	1.35 V	1.1 V	1.1 V
VTT Disabled	Yes	No	No	Yes	Yes
VTT I_{OCP} (minimum)	0.95 A	0.95 A	1.8 A	1.8 A	0.95 A
SWB1_2 controlled by SLP_S4B (V1P8U)	Yes	Yes	No	Yes	Yes
SWB1_2 controlled by SLP_S3B	No	No	Yes	No	No
Pin 14 Usage	LDOLS_EN	LDOLS_EN	LDOLS_EN	SWA1_EN	LDOLS_EN
LDOA1 Always On	No	No	No	Yes	No
LDOA1 Default Voltage	3.3 V	3.3 V	3.3 V	1.8 V	3.3 V
LDOA2 Default Voltage	1.2 V	1.2 V	1.2 V	0.7 V	1.2 V
LDOA3 Default Voltage	1.25 V	1.25 V	1.25 V	0.7 V	1.25 V
PMICEN Low Forces Reset	Yes	Yes	Yes	No	Yes
DEVICEID Register	8h	29h	1Ah	0Bh	8h
BUCK3-5 Mode	Auto	Auto	Auto	Auto	Forced PWM

4 Pin Configuration and Functions

RSK Package
64-Pin VQFN With Thermal Pad
Top View



NOTE: The thermal pad must be connected to the system power ground plane.

Pin Functions

PIN		I/O	SUPPLY, OP VOLTAGE LEVEL	DESCRIPTION
NO.	NAME			
SMPS REGULATORS				
1	FBGND2	I		Remote negative feedback sense for BUCK2 controller. Connect to VCCGI VSS SENSE sent from the SoC to the PMIC.
2	FBVOUT2	I		Remote positive feedback sense for BUCK2 controller. Connect to VCCGI VCC SENSE sent from the SoC to the PMIC.
3	DRVH2	O	VSYS + 5 V	High-side gate driver output for BUCK2 controller
4	SW2	I		Switch node connection for BUCK2 controller
5	BOOT2	I	VSYS + 5 V	Bootstrap pin for BUCK2 controller. Connect a 100-nF ceramic capacitor between this pin and SW2 pin.
6	PGNDSNS2	I		Power GND connection for BUCK2. Connect to ground terminal of external low-side FET.
7	DRVL2	O	5 V	Low-side gate driver output for BUCK2 controller
8	DRV5V_2_A1	I	5 V	5-V supply to BUCK2 gate driver and LDOA1. Bypass to ground with a 2.2-µF (typical) ceramic capacitor. Shorted on board to LDO5P0 pin.
10	LX3	O		Switch node connection for BUCK3 converter. Connect to a 0.47-µH (typical) inductor with less than 50-mΩ DCR.
11	PVIN3	I	5 V	Power input to BUCK3 converter. Bypass to ground with a 10-µF (typical) ceramic capacitor.
12	FB3	I		Remote feedback sense for BUCK3 converter. Connect to positive terminal of output capacitor.
20	LX5	O		Switch node connection for BUCK5 converter. Connect to a 0.47-µH (typical) inductor with less than 50-mΩ DCR.
21	PVIN5	I	5 V	Power input to BUCK5 converter. Bypass to ground with a 10-µF (typical) ceramic capacitor.
22	FB5	I		Remote feedback sense for BUCK5 converter. Connect to positive terminal of output capacitor.
23	FB4	I		Remote feedback sense for BUCK4 converter. Connect to positive terminal of output capacitor.
24	PVIN4	I	5 V	Power input to BUCK4 converter. Bypass to ground with a 10-µF (typical) ceramic capacitor.
25	LX4	O		Switch node connection for BUCK4 converter. Connect to a 0.47-µH (typical) inductor with less than 50-mΩ DCR.
29	FBVOUT1	I		Remote feedback sense for BUCK1 controller. Connect to VNN VCC SENSE sent from the SoC to the PMIC.
30	ILIM1	I		Current limit set pin for BUCK1 controller. Fit a resistor from this pin to ground to set current limit of external low-side FET.
33	DRVH1	O	VSYS + 5 V	High-side gate driver output for BUCK1 controller
34	SW1	I		Switch node connection for BUCK1 controller
35	BOOT1	I	VSYS + 5 V	Bootstrap pin for BUCK1 controller. Connect a 100-nF ceramic capacitor between this pin and SW1 pin.
36	PGNDSNS1	I		Power GND connection for BUCK1. Connect to ground terminal of external low-side FET.
37	DRVL1	O	5 V	Low-side gate driver output for BUCK1 controller
38	DRV5V_1_6	I	5 V	5-V supply to BUCK1 and BUCK6 gate drivers. Bypass to ground with a 2.2-µF (typical) ceramic capacitor. Shorted on board to LDO5P0 pin.
39	DRVL6	O	5 V	Low-side gate driver output for BUCK6 controller
40	PGNDSNS6	I		Power GND connection for BUCK6. Connect to ground terminal of external low-side FET.
41	BOOT6	I	VSYS + 5 V	Bootstrap pin for BUCK6 controller. Connect a 100-nF ceramic capacitor between this pin and SW6 pin.
42	SW6	I		Switch node connection for BUCK6 controller
43	DRVH6	O	VSYS + 5 V	High-side gate driver output for BUCK6 controller

Pin Functions (continued)

PIN		I/O	SUPPLY, OP VOLTAGE LEVEL	DESCRIPTION
NO.	NAME			
44	FBVOUT6	I		Remote feedback sense for BUCK6 controller. Connect to positive terminal of output capacitor.
45	ILIM6	I		Current limit set pin for BUCK6 controller. Fit a resistor from this pin to ground to set current limit of external low-side FET.
64	ILIM2	I		Current limit set pin for BUCK2 controller. Fit a resistor from this pin to ground to set current limit of external low-side FET.
LDO and LOAD SWITCHES				
9	LDOA1	O	1.35–3.3 V	LDOA1 output. Bypass to ground with a 4.7-µF (typical) ceramic capacitor. Leave floating when not in use.
17	SWB1	O	0.5–3.3 V (1.8-V Typical)	Output of load switch B1. Bypass to ground with a 0.1-µF (typical) ceramic capacitor. Short with SWB2.
18	PVINSWB1_B2	I	0.5–3.3 V (1.8-V Typical)	Power supply to load switch B1 and B2. Bypass to ground with a 1-µF (typical) ceramic capacitor to improve transient performance. Connect to ground when not in use.
19	SWB2	O	0.5–3.3 V (1.8-V Typical)	Output of load switch B2. Bypass to ground with a 0.1-µF (typical) ceramic capacitor. Short with SWB1. Leave floating when not in use.
31	SWA1	O	0.5–3.3 V	Output of load switch A1. Bypass to ground with a 0.1-µF (typical) ceramic capacitor. Leave floating when not in use.
32	PVINSWA1	I	0.5–3.3 V	Power supply to load switch A1. Bypass to ground with a 1-µF (typical) ceramic capacitor to improve transient performance. Connect to ground when not in use.
46	PVINVTT	I	VDDQ	Power supply to VTT LDO. Bypass to ground with a 10-µF (minimum) ceramic capacitor. Connect to ground when not in use.
47	VTT	O	VDDQ / 2	Output of load VTT LDO. Bypass to ground with 2× 22-µF (minimum) ceramic capacitors. Leave floating when not in use.
48	VTTFB	I	VDDQ / 2	Remote feedback sense for VTT LDO. Connect to positive terminal of output capacitor. Short to GND when not in use.
49	LDOA3	O	0.7–1.5 V	Output of LDOA3. Bypass to ground with a 4.7-µF (typical) ceramic capacitor. Leave floating when not in use.
50	PVINLDOA2_A3	I	1.8 V	Power supply to LDOA2 and LDOA3. Bypass to ground with a 4.7-µF (typical) ceramic capacitor. Connect to ground when not in use.
51	LDOA2	O	0.7–1.5 V	Output of LDOA2. Bypass to ground with a 4.7-µF (typical) ceramic capacitor. Leave floating when not in use.
54	LDO3P3	O	3.3 V	Output of 3.3-V internal LDO. Bypass to ground with a 4.7-µF (typical) ceramic capacitor.
56	LDO5P0	O	5 V	Output of 5-V internal LDO or an internal switch that connects this pin to V5ANA. Bypass to ground with a 4.7-µF (typical) ceramic capacitor.
57	V5ANA	I	5 V	External 5-V supply input to internal load switch that connects this pin to LDO5P0 pin. Bypass this pin with an optional ceramic capacitor to improve transient performance.

Pin Functions (continued)

PIN		I/O	SUPPLY, OP VOLTAGE LEVEL	DESCRIPTION
NO.	**NAME**			
INTERFACE				
13	PMICEN	I		PMIC cold-boot pin. At assertion rising edge of the signal of this pin power state transitions from G3 to S4/S5. Driving the pin to *L* shuts down all VRs.
14	LDOLS_EN or SWA1_EN	I		Enable pin for LDOA2, LDOA3, and SWA1 when OTP is configured to LDOLS_EN. Enable pin for just SWA1 when OTP is configured to SWA1_EN. Resources turn on at assertion (H) and turn off at deassertion (L) of the pin. Optionally, when the pin is pulled low, the host can write to enable bits in Reg 0xA0–Reg 0xA1 to control the rails.
15	IRQB	O		Open-drain output interrupt pin. Refer to Section 6.6.3, *IRQ: PMIC Interrupt Register*, for definitions.
16	RSMRSTB	O		Open-drain output Always-ON-rail Power Good. It reflects a valid state whenever VSYS is available.
26	GPO	O		Open-drain output controlled by an I^2C register bit defined in Section 6.6.26, *GPO_CTRL: GPO Control Register,* by the user, which then can be used as an enable signal to an external VR.
27	PCH_PWROK	O		Open-drain output global Power Good. It reflects a valid state whenever VSYS is available.
28	PROCHOT	O		Optional open-drain output for indicating PMIC thermal event. Invert before connecting to SoC if used, otherwise leave floating. This pin is triggered when any of the PMIC die temperature sensors detects the T_{HOT} temperature.
58	CLK	I		I^2C clock
59	DATA	I/O		I^2C data
60	THERMTRIPB	I		Thermal shutdown signal from SoC
61	SLP_S0B	I		Power state pin. PMIC goes into Connected Standby at falling edge and exits from Connected Standby at rising edge.
62	SLP_S3B	I		Power state pin. PMIC goes into S3 at falling edge and exits from S3, transitions into S0 at rising edge.
63	SLP_S4B	I		Power state pin. PMIC goes into S4 at falling edge and exits from S4, transitions into S3 at rising edge.
REFERENCE				
53	VREF	O	1.25 V	Band-gap reference output. Stabilize it by connecting a 100-nF (typical) ceramic capacitor between this pin and quiet ground.
52	AGND	—		Analog ground. Do not connect to the thermal pad ground on top layer. Connect to ground of VREF capacitor.
55	VSYS	I		System voltage detection and input to internal LDOs (3.3 V and 5 V). Bypass to ground with a 1-µF (typical) ceramic capacitor.
THERMAL PAD				
—	Thermal pad	—		Connect to PCB ground plane using multiple vias for good thermal and electrical performance.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
ANALOG				
VSYS	Input voltage from battery	–0.3	28	V
PVIN3, PVIN4, PVIN5, LDO5P0, DRV5V_1_6, DRV5V_2_A1, DRVL1, DRVL2, DRVL6		–0.3	7	V
V5ANA		–0.3	6	V
PGNDSNS1, PGNDSNS2, PGNDSNS6, AGND, FBGND2		–0.3	0.3	V
DRVH1, DRVH2, DRVH6, BOOT1, BOOT2, BOOT6		–0.3	34	V
SW1, SW2, SW6		–5(2)	28	V
LX3, LX4, LX5		–2(3)	8	V
BOOTx to SWx	Differential voltage	–0.3	5.5	V
VREF, LDO3P3, FBVOUT1, FBVOUT2, FBVOUT6, FB3, FB4, FB5, ILIM1, ILIM2, ILIM6, PVINVTT, VTT, VTTFB, PVINSWA1, SWA1, PVINSWB1_B2, SWB1, SWB2, LDOA1		–0.3	3.6	V
PVINLDOA2_A3, LDOA2, LDOA3		–0.3	3.3	V
DIGITAL IOs				
DATA, CLK, PCH_PWROK, RSMRSTB, GPO		–0.3	3.6	V
PMICEN, SLP_S4B, SLP_S3B, SLP_S0B, LDOLS_EN, SWA1_EN, THERMTRIPB, IRQB, PROCHOT		–0.3	7	V
Storage temperature, T_{stg}		–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Transient for less than 5 ns.
(3) Transient for less than 20 ns.

5.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human Body Model (HBM), per ANSI/ESDA/JEDEC JS001(1)	±1000	V
		Charged Device Model (CDM), per JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
ANALOG					
VSYS		5.6	13	21	V
VREF		–0.3		1.3	V
PVIN3, PVIN4, PVIN5, LDO5P0, V5ANA, DRV5V_1_6, DRV5V_2_A1		–0.3	5	5.5	V
PGNDSNS1, PGNDSNS2, PGNDSNS6, AGND, FBGND2		–0.3		0.3	V
DRVH1, DRVH2, DRVH6, BOOT1, BOOT2, BOOT6		–0.3		26.5	V
DRVL1, DRVL2, DRVL6		–0.3		5.5	V
SW1, SW2, SW6		–1		21	V
LX3, LX4, LX5		–1		5.5	V
FBVOUT1, FBVOUT2, FBVOUT6, FB3, FB4, FB5		–0.3		3.6	V
LDO3P3, ILIM1, ILIM2, ILIM6, LDOA1		–0.3		3.3	V
PVINVTT		–0.3		VDDQ	V
VTT, VTTFB		–0.3		VDDQ / 2	V
PVINSWA1, SWA1		–0.3	3.3	3.6	V
PVINSWB1_B2, PVINLDOA2_A3, SWB1, SWB2		–0.3		1.8	V
LDOA2, LDOA3		–0.3		1.5	V
DIGITAL IOs					
DATA, CLK, PMICEN, SLP_S4B, SLP_S3B, LDOLS_EN, SWA1_EN, SLP_S0B, THERMTRIPB, PROCHOT, IRQB, RSMRSTB, PCH_PWROK, GPO		–0.3		3.3	V
CHIP					
T_A	Operating ambient temperature	–40	27	85	°C
T_J	Operating junction temperature	–40	27	125	°C

5.4 Thermal Information

THERMAL METRIC[(1)]		TPS65094x	UNIT
		RSK (VQFN)	
		64 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	11.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	4.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	4.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.7	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

5.5 Electrical Characteristics: Total Current Consumption

over recommended free-air temperature range and over recommended input voltage range (typical values are at T_A = 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SD}	PMIC shutdown current that includes I_Q for references, LDO5, LDO3P3, and digital core	V_{SYS} = 13 V, all functional output rails are disabled		65		µA

5.6 Electrical Characteristics: Reference and Monitoring System

over recommended free-air temperature range and over recommended input voltage range (typical values are at T_A = 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE						
V_{REF}	Band-gap reference voltage			1.25		V
	Accuracy		–0.5%		0.5%	
C_{VREF}	Band-gap output capacitor		0.047	0.1	0.22	µF
$V_{SYS\_UVLO\_5V}$	VSYS UVLO threshold for LDO5	V_{SYS} falling	5.24	5.4	5.56	V
$V_{SYS\_UVLO\_5V\_HYS}$	VSYS UVLO threshold hysteresis for LDO5	V_{SYS} rising above $V_{SYS\_UVLO\_5V}$		200		mV
$V_{SYS\_UVLO\_3V}$	VSYS UVLO threshold for LDO3P3	V_{SYS} falling	3.45	3.6	3.75	V
$V_{SYS\_UVLO\_3V\_HYS}$	VSYS UVLO threshold hysteresis for LDO3P3	V_{SYS} rising above $V_{SYS\_UVLO\_3V}$		150		mV
T_{CRIT}	Critical threshold of die temperature	T_J rising	130	145	160	°C
T_{CRIT_HYS}	Hysteresis of T_{CRIT}	T_J falling		10		°C
T_{HOT}	Hot threshold of die temperature	T_J rising	110	115	120	°C
T_{HOT_HYS}	Hysteresis of T_{HOT}	T_J falling		10		°C
LDO5						
V_{IN}	Input voltage at V_{SYS} pin			13	21	V
V_{OUT}	DC output voltage	I_{OUT} = 10 mA	4.9	5	5.1	V
I_{OUT}	DC output current			100	180	mA
I_{OCP}	Overcurrent protection	Measured with output shorted to ground	200			mA
V_{TH_PG}	Power Good assertion threshold in percentage of target V_{OUT}	V_{OUT} rising		94%		
$V_{TH\_PG\_HYS}$	Power Good deassertion hysteresis	V_{OUT} rising or falling		4%		
I_Q	Quiescent current	V_{IN} = 13 V, I_{OUT} = 0 A		20		µA
C_{OUT}	External output capacitance		2.7	4.7	10	µF
V5ANA-to-LDO5P0 LOAD SWITCH						
R_{DSON}	On resistance	V_{IN} = 5 V, measured from V5ANA pin to LDO5P0 pin at I_{OUT} = 200 mA			1	Ω
V_{TH_PG}	Power Good threshold for external 5-V supply	V_{V5ANA} rising		4.7		V
$V_{TH\_HYS\_PG}$	Power Good threshold hysteresis for external 5-V supply	V_{V5ANA} falling		100		mV
I_{LKG}	Leakage current	Switch disabled, V_{V5ANA} = 5 V, V_{LDO5} = 0 V			10	µA
LDO3P3						
V_{IN}	Input voltage at V_{SYS} pin			13	21	V
V_{OUT}	DC output voltage	I_{OUT} = 10 mA		3.3		V
	Accuracy	V_{IN} = 13 V, I_{OUT} = 10 mA	–3%		3%	
I_{OUT}	DC output current				40	mA
I_{OCP}	Overcurrent protection	Measured with output shorted to ground	70			mA
V_{TH_PG}	Power Good assertion threshold in percentage of target V_{OUT}	V_{OUT} rising		92%		
$V_{TH\_PG\_HYS}$	Power Good deassertion hysteresis	V_{OUT} falling		3%		
I_Q	Quiescent current	V_{IN} = 13 V, I_{OUT} = 0 A		20		µA
C_{OUT}	External output capacitance		2.2	4.7	10	µF

5.7 Electrical Characteristics: Buck Controllers

over recommended input voltage range, T_A = –40°C to +85°C and T_A = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BUCK1						
V_{IN}	Power input voltage for external HSD FET		5.6	13	21	V
V_{OUT}	DC output voltage	Step size		10		mV
		BUCK1_VID[6:0] = 0000000		0		V
		BUCK1_VID[6:0] = 0000001		0.5		
		BUCK1_VID[6:0] = 0000010		0.51		
		⋮		⋮		
		BUCK1_VID[6:0] = 0110011 (default)		1.00		
		⋮		⋮		
		BUCK1_VID[6:0] = 1110101		1.66		
		BUCK1_VID[6:0] = 1110110–1111111		1.67		
	DC output voltage accuracy	V_{OUT} ≥ 1 V, I_{OUT} = 100 mA to 5 A	–2%		2%	
		V_{OUT} = 0.75 V, I_{OUT} = 100 mA to 2.1 A	–2.5%		2.5%	
		V_{OUT} ≤ 0.6 V, I_{OUT} = 10 mA	–3.5%		3.5%	
	Total output voltage accuracy (DC + ripple) in DCM	I_{OUT} = 10 mA, V_{OUT} ≤ 0.785 V, V_{SYS} = 13 V	–20		40	mV
		I_{OUT} = 10 mA, V_{OUT} ≤ 0.785 V, V_{SYS} = 21 V	–20		55	
SR(V_{OUT})	Output DVS slew rate		2.5	3.125		mV/µs
I_{LIM_LSD}	Low-side output valley current limit accuracy (programmed by external resistor R_{LIM})	See Section 6.3.3.4, *Current Limit,* for details.	–15%		15%	
V_{TH_ZC}	Low-side current zero crossing detection threshold		–11		11	mV
I_{LIMREF}	Source current out of ILIM1 pin	T = 25°C	45	50	55	µA
V_{LIM}	Voltage at ILIM1 pin	$V_{LIM} = R_{LIM} \times I_{LIMREF}$	0.2		2.25	V
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation	V_{OUT} ≥ 1 V, I_{OUT} = 5 A	–0.5%		0.5%	
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	V_{IN} = 13 V, V_{OUT} ≥ 1 V, I_{OUT} = 0 A to 5 A, referenced to V_{OUT} at I_{OUT} = 5 A	0%		1%	
ΔV_{OUT_TR}(1)	Load transient regulation	DC + AC at sense point, V_{IN} = 13 V, V_{OUT} = 1.00 V, I_{OUT} = 1.5 A to 5 A and 5 A to 1.5 A with 1 µs of t_r and t_f	–50		50	mV
		DC + AC at sense point, V_{IN} = 13 V, V_{OUT} = 0.75 V, I_{OUT} = 0.3 A to 1.5 A and 1.5 A to 0.3 A with 1 µs of t_r and t_f				
V_{TH_PG}	Power Good deassertion threshold in percentage of target V_{OUT}	V_{OUT} rising		108%		
		V_{OUT} falling		92%		
$V_{TH\_HYS\_PG}$	Power Good reassertion hysteresis entering back into V_{TH_PG}	V_{OUT} rising or falling		3%		
C_{OUT}	External output capacitance	Recommended amount to meet transient specification	180	220		µF
L_{SW}	External output inductance		0.376	0.47	0.564	µH

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(1) Frequency of transient load current ranges from 0 to 1 MHz with duty cycle of 50%. For cases where duty cycle and frequency are limited by t_r and t_f, the highest frequency is set by 1 / (t_r + t_f), where t_r is rise time (0% to 100%) and t_f is fall time (100% to 0%).

Electrical Characteristics: Buck Controllers *(continued)*

over recommended input voltage range, T_A = –40°C to +85°C and T_A = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{DSON_DRVH}	Driver DRVH resistance	Source, IDRVH = –50 mA		3		Ω
		Sink, IDRVH = 50 mA		2		
R_{DSON_DRVL}	Driver DRVL resistance	Source, IDRVL = –50 mA		3		Ω
		Sink, IDRVL = 50 mA		0.4		
R_{DIS}	Output auto-discharge resistance	BUCK1_DIS[1:0] = 01		100		Ω
		BUCK1_DIS[1:0] = 10		200		
		BUCK1_DIS[1:0] = 11		500		
C_{BOOT}	Bootstrap capacitance			100		nF
R_{ON_BOOT}	Bootstrap switch ON resistance				20	Ω
BUCK2						
V_{IN}	Power input voltage for external HSD FET		5.6	13	21	V
V_{OUT}	DC output voltage	Step size		10		mV
		BUCK2_VID[6:0] = 0000000 (default)		0		V
		BUCK2_VID[6:0] = 0000001		0.5		
		BUCK2_VID[6:0] = 0000010		0.51		
		⋮		⋮		
		BUCK2_VID[6:0] = 1110101		1.66		
		BUCK2_VID[6:0] = 1110110–1111111		1.67		
	DC output voltage accuracy	V_{OUT} ≥ 1 V, I_{OUT} = 100 mA to 21 A	–2%		2%	
		V_{OUT} = 0.75 V, I_{OUT} = 100 mA to 6.3 A	–2.5%		2.5%	
		V_{OUT} ≤ 0.6 V, I_{OUT} = 10 mA	–3.5%		3.5%	
	Total output voltage accuracy (DC + ripple) in DCM	I_{OUT} = 10 mA, V_{OUT} ≤ 0.765 V	–20		40	mV
SR(V_{OUT})	Output DVS slew rate		2.5	3.125		mV/µs
I_{LIM_LSD}	Low-side output valley current limit accuracy (programmed by external resistor R_{LIM})	See Section 6.3.3.4, *Current Limit,* for details.	–15%		15%	
V_{TH_ZC}	Low-side current zero crossing detection threshold		–11		11	mV
I_{LIMREF}	Source current out of ILIM2 pin	T = 25°C	45	50	55	µA
V_{LIM}	Voltage at ILIM2 pin	$V_{LIM} = R_{LIM} \times I_{LIMREF}$	0.2		2.25	V
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation	V_{OUT} ≥ 1 V, I_{OUT} = 21 A	–0.5%		0.5%	
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	V_{IN} = 13 V, 1 V ≤ V_{OUT} ≤ 1.3 V, I_{OUT} = 0 A to 21 A, referenced to V_{OUT} at I_{OUT} = 21 A	0%		1%	
ΔV_{OUT_TR} (1)	Load transient regulation	DC + AC at sense point, V_{IN} = 13 V, V_{OUT} = 1 V, I_{OUT} = 1 A to 21 A and 21 A to 1 A with 1 µs of t_r and t_f	–160		30 (2)	mV
		DC + AC at sense point, V_{IN} = 13 V, V_{OUT} = 0.75 V, I_{OUT} = 1 A to 3.3 A and 3.3 A to 1 A with 1 µs of t_r and t_f	–50		50 (2)	
V_{TH_PG}	Power Good deassertion threshold in percentage of target V_{OUT}	V_{OUT} rising		108%		
		V_{OUT} falling		92%		

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(2) Additional overshoot of up to 100 mV is allowed as long as it lasts less than 50 µs.

Electrical Characteristics: Buck Controllers *(continued)*

over recommended input voltage range, T_A = –40°C to +85°C and T_A = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{TH\_HYS\_PG}$	Power Good reassertion hysteresis entering back into V_{TH_PG}	V_{OUT} rising or falling		3%		
L_{SW}	External output inductance		0.176	0.22	0.264	µH
C_{OUT}	External output capacitance	Recommended amount to meet transient specification	440	550		µF
R_{DSON_DRVH}	Driver DRVH resistance	Source, IDRVH = –50 mA		3		Ω
		Sink, IDRVH = 50 mA		2		
R_{DSON_DRVL}	Driver DRVL resistance	Source, IDRVL = –50 mA		3		Ω
		Sink, IDRVL = 50 mA		0.4		
R_{DIS}	Output auto-discharge resistance	BUCK2_DIS[1:0] = 01		100		Ω
		BUCK2_DIS[1:0] = 10		200		
		BUCK2_DIS[1:0] = 11		500		
C_{BOOT}	Bootstrap capacitance			100		nF
R_{ON_BOOT}	Bootstrap switch ON resistance				20	Ω
BUCK6						
V_{IN}	Power input voltage for external HSD FET		5.6	13	21	V
V_{OUT}	DC output voltage	Step size		10		mV
		BUCK6_VID[6:0] = 0000000		0		V
		BUCK6_VID[6:0] = 0000001		0.5		
		BUCK6_VID[6:0] = 0000010		0.51		
		⋮		⋮		
		BUCK6_VID[6:0] = 0111101 (TPS650940 and TPS650944 default)		1.1		
		⋮		⋮		
		BUCK6_VID[6:0] = 1000111 (TPS650941 default)		1.2		
		⋮		⋮		
		BUCK6_VID[6:0] = 1010110 (TPS650942 default)		1.35		
		⋮		⋮		
		BUCK6_VID[6:0] = 1110101		1.66		
		BUCK6_VID[6:0] = 1110110–1111111		1.67		
	DC output voltage accuracy	V_{OUT} ≥ 1 V, I_{OUT} = 100 mA to 7 A	–2%		2%	
I_{LIM_LSD}	Low-side output valley current limit accuracy (programmed by external resistor R_{LIM})	See Section 6.3.3.4, *Current Limit*, for details.	–15%		15%	
V_{TH_ZC}	Low-side current zero crossing detection threshold		–11		11	mV
I_{LIMREF}	Source current out of ILIM6 pin	T = 25°C	45	50	55	µA
V_{LIM}	Voltage at ILIM6 pin	$V_{LIM} = R_{LIM} \times I_{LIMREF}$	0.2		2.25	V
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation	V_{OUT} ≥ 1 V, I_{OUT} = 7 A	–0.5%		0.5%	
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	V_{IN} = 13 V, V_{OUT} ≥ 1 V, I_{OUT} = 0 A to 7 A, referenced to V_{OUT} at I_{OUT} = 7 A	0%		1%	
ΔV_{OUT_TR}	Load transient regulation	DC + AC at sense point, V_{IN} = 13 V, VOUT = 1.35 V, I_{OUT} = 2.1 A to 7 A and 7 A to 2.1 A with 1.96 µs of t_r and t_f (2.5 A/µs)	–5%		5%	

Electrical Characteristics: Buck Controllers *(continued)*

over recommended input voltage range, T_A = –40°C to +85°C and T_A = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{TH_PG}	Power Good deassertion threshold in percentage of target V_{OUT}	V_{OUT} rising		108%		
		V_{OUT} falling		92%		
$V_{TH\_HYS\_PG}$	Power Good reassertion hysteresis entering back into V_{TH_PG}	V_{OUT} rising or falling		3%		
L_{SW}	External output inductance		0.376	0.47	0.564	µH
C_{OUT}	External output capacitance	Recommended amount to meet transient specification	150	220		µF
R_{DSON_DRVH}	Driver DRVH resistance	Source, IDRVH = –50 mA		3		Ω
		Sink, IDRVH = 50 mA		2		
R_{DSON_DRVL}	Driver DRVL resistance	Source, IDRVL = –50 mA		3		Ω
		Sink, IDRVL = 50 mA		0.4		
R_{DIS}	Output auto-discharge resistance	BUCK6_DIS[1:0] = 01		100		Ω
		BUCK6_DIS[1:0] = 10		200		
		BUCK6_DIS[1:0] = 11		500		
C_{BOOT}	Bootstrap capacitance			100		nF
R_{ON_BOOT}	Bootstrap switch ON resistance				20	Ω

5.8 Electrical Characteristics: Synchronous Buck Converters

over recommended input voltage range, T_A = –40°C to +85°C and T_A = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BUCK3						
V_{IN}	Power input voltage		4.5	5	5.5	V
V_{OUT}	DC output voltage	Step size		25		mV
		BUCK3_VID[6:0] = 0000000		0		V
		BUCK3_VID[6:0] = 0000001		0.65		
		BUCK3_VID[6:0] = 0000010		0.675		
		⋮		⋮		
		BUCK3_VID[6:0] = 0010001 (default)		1.05		
		⋮		⋮		
		BUCK3_VID[6:0] = 1110101		3.55		
		BUCK3_VID[6:0] = 1110110–1111111		3.575		
	DC output voltage accuracy	V_{OUT} = 1.05 V, I_{OUT} = 1.5 A	–2%		2%	
		V_{OUT} = 1.05 V, I_{OUT} = 100 mA	–2.5%		2.5%	
$SR(V_{OUT})$	Output DVS slew rate		2.5	3.125		mV/µs
I_{OUT}	Continuous DC output current				3	A
I_{IND_LIM}	HSD FET current limit		4.3		7	A
I_Q	Quiescent current	V_{IN} = 5 V, V_{OUT} = 1 V		35		µA
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation	V_{OUT} = 1.05 V, I_{OUT} = 1.5 A	–0.5%		0.5%	
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	V_{IN} = 5 V, V_{OUT} = 1.05 V, I_{OUT} = 0 A to 3 A, referenced to V_{OUT} at I_{OUT} = 1.5 A	–0.2%		2%	
ΔV_{OUT_TR} (1)	Load transient regulation	DC + AC at sense point, V_{IN} = 5 V, V_{OUT} = 1.05 V, I_{OUT} = 0.9 A to 3 A and 3 A to 0.9 A with slew rate of 2.5 A/µs	–5%		7%	
V_{TH_PG}	Power Good deassertion threshold in percentage of target V_{OUT}	V_{OUT} rising		108%		
		V_{OUT} falling		92%		
$V_{TH\_HYS\_PG}$	Power Good reassertion hysteresis entering back into V_{TH_PG}	V_{OUT} rising or falling		3%		
L_{SW}	Output inductance		0.376	0.47	0.564	µH
C_{IN}	Input bypass capacitance		2.5	10	12	µF
C_{OUT}	Output filtering capacitance		61.6	88	110	µF
R_{DIS}	Output auto-discharge resistance	BUCK3_DIS[1:0] = 01		100		Ω
		BUCK3_DIS[1:0] = 10		200		
		BUCK3_DIS[1:0] = 11		500		

(1) Frequency of transient load current ranges from 0 to 1 MHz with duty cycle of 50%. For cases where duty cycle and frequency are limited by t_r and t_f, the highest frequency is set by 1 / (t_r + t_f), where t_r is rise time (0% to 100%) and t_f is fall time (100% to 0%).

Electrical Characteristics: Synchronous Buck Converters *(continued)*

over recommended input voltage range, T_A = –40°C to +85°C and T_A = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BUCK4						
V_{IN}	Power input voltage		4.5	5	5.5	V
V_{OUT}	DC output voltage	Step size		25		mV
		BUCK4_VID[6:0] = 0000000		0		V
		BUCK4_VID[6:0] = 0000001		0.65		
		BUCK4_VID[6:0] = 0000010		0.675		
		⋮		⋮		
		BUCK4_VID[6:0] = 0101111 (default)		1.8		
		⋮		⋮		
		BUCK4_VID[6:0] = 1110101		3.55		
		BUCK4_VID[6:0] = 1110110–1111111		3.575		
	DC output voltage accuracy	V_{OUT} = 1.8 V, I_{OUT} = 1.5 A	–2%		2%	
		V_{OUT} = 1.8 V, I_{OUT} = 100 mA	–2.5%		2.5%	
I_{OUT}	Continuous DC output current				3	A
I_{IND_LIM}	HSD FET current limit		4.3		7	A
I_Q	Quiescent current	V_{IN} = 5 V, V_{OUT} = 1.8 V		35		µA
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation	V_{OUT} = 1.8 V, I_{OUT} = 1.5 A	–0.5%		0.5%	
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	V_{IN} = 5 V, V_{OUT} = 1.8 V, I_{OUT} = 0 A to 1.5 A, referenced to V_{OUT} at I_{OUT} = 0.75 A	–0.2%		0.65%	
ΔV_{OUT_TR} (1)	Load transient regulation	DC + AC at sense point, V_{IN} = 5 V, VOUT = 1.8 V, I_{OUT} = 0.45 A to 1.5 A and 1.5 A to 0.45 A with slew rate of 2.5 A/µs	–5%		5%	
V_{TH_PG}	Power Good deassertion threshold in percentage of target V_{OUT}	V_{OUT} rising		108%		
		V_{OUT} falling		92%		
$V_{TH\_HYS\_PG}$	Power Good reassertion hysteresis entering back into V_{TH_PG}	V_{OUT} rising or falling		3%		
L_{SW}	Output inductance		0.376	0.47	0.564	µH
C_{IN}	Input bypass capacitance		2.5	10	12	µF
C_{OUT}	Output filtering capacitance		46	66	110	µF
R_{DIS}	Output auto-discharge resistance	BUCK4_DIS[1:0] = 01		100		Ω
		BUCK4_DIS[1:0] = 10		200		
		BUCK4_DIS[1:0] = 11		500		

Electrical Characteristics: Synchronous Buck Converters *(continued)*

over recommended input voltage range, T_A = –40°C to +85°C and T_A = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BUCK5						
V_{IN}	Power input voltage		4.5	5	5.5	V
V_{OUT}	DC output voltage	Step size		10		mV
		BUCK5_VID[6:0] = 0000000		0		V
		BUCK5_VID[6:0] = 0000001		0.5		
		BUCK5_VID[6:0] = 0000010		0.51		
		⋮		⋮		
		BUCK5_VID[6:0] = 1001011 (default)		1.24		
		⋮		⋮		
		BUCK5_VID[6:0] = 1110101		1.66		
		BUCK4_VID[6:0] = 1110110–1111111		1.67		
	DC output voltage accuracy	V_{OUT} = 1.24 V, I_{OUT} = 1.5 A	–2%		2%	
		V_{OUT} = 1.24 V, I_{OUT} = 100 mA	–2.5%		2.5%	
I_{OUT}	Continuous DC output current				3.2	A
I_{IND_LIM}	HSD FET current limit		4.3		7	A
I_Q	Quiescent current	V_{IN} = 5 V, V_{OUT} = 1.24 V		35		µA
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation	V_{OUT} = 1.24 V, I_{OUT} = 1.5 A	–0.5%		0.5%	
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	V_{IN} = 5 V, V_{OUT} = 1.24 V, I_{OUT} = 0 A to 1.5 A, referenced to V_{OUT} at I_{OUT} = 0.75 A	–0.2%		1%	
ΔV_{OUT_TR} (1)	Load transient regulation	DC + AC at sense point, V_{IN} = 5 V, V_{OUT} = 1.24 V, I_{OUT} = 0.45 A to 1.5 A and 1.5 A to 0.45 A with slew rate of 2.5 A/µs	–5%		5%	
V_{TH_PG}	Power Good deassertion threshold in percentage of target V_{OUT}	V_{OUT} rising		108%		
		V_{OUT} falling		92%		
$V_{TH\_HYS\_PG}$	Power Good reassertion hysteresis entering back into V_{TH_PG}	V_{OUT} rising or falling		3		
L_{SW}	Output inductance		0.376	0.47	0.564	µH
C_{IN}	Input bypass capacitance		2.5	10	12	µF
C_{OUT}	Output filtering capacitance		31	44	110	µF
R_{DIS}	Output auto-discharge resistance	BUCK5_DIS[1:0] = 01		100		Ω
		BUCK5_DIS[1:0] = 10		200		
		BUCK5_DIS[1:0] = 11		500		

5.9 Electrical Characteristics: LDOs

over recommended input voltage range, T_A = –40°C to +85°C and T_A = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LDOA1						
V_{IN}	Input voltage		4.5	5	5.5	V
V_{OUT}	DC output voltage	I_{OUT} = 10 mA, LDOA1_SEL[3:0] = 0000		1.35		V
		LDOA1_SEL[3:0] = 0001		1.5		
		LDOA1_SEL[3:0] = 0010		1.6		
		LDOA1_SEL[3:0] = 0011		1.7		
		LDOA1_SEL[3:0] = 0100 (TPS650944 default)		1.8		
		LDOA1_SEL[3:0] = 0101		1.9		
		LDOA1_SEL[3:0] = 0110		2		
		LDOA1_SEL[3:0] = 0111		2.1		
		LDOA1_SEL[3:0] = 1000		2.3		
		LDOA1_SEL[3:0] = 1001		2.4		
		LDOA1_SEL[3:0] = 1010		2.5		
		LDOA1_SEL[3:0] = 1011		2.7		
		LDOA1_SEL[3:0] = 1100		2.85		
		LDOA1_SEL[3:0] = 1101		3		
		LDOA1_SEL[3:0] = 1110 (TPS650940, TPS650941, and TPS650942 default)		3.3		
V_{OUT}	Accuracy	I_{OUT} = 0 to 200 mA	–2%		2%	
I_{OUT}	DC output current				200	mA
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation	I_{OUT} = 40 mA	–0.5%		0.5%	
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	I_{OUT} = 10 mA to 200 mA	–2%		2%	
I_{OCP}	Overcurrent protection	V_{IN} = 5 V, Measured with output shorted to ground	500			mA
V_{TH_PG}	Power Good deassertion threshold in percentage of target V_{OUT}	V_{OUT} rising		108%		
		V_{OUT} falling		92%		
$V_{TH\_HYS\_PG}$	Power Good reassertion hysteresis entering back into V_{TH_PG}	V_{OUT} rising or falling		3%		
I_Q	Quiescent current	I_{OUT} = 0 A		23		µA
C_{OUT}	External output capacitance		2.7	4.7	10	µF
	ESR				100	mΩ
R_{DIS}	Output auto-discharge resistance	LDOA1_DIS[1:0] = 01		100		Ω
		LDOA1_DIS[1:0] = 10		190		
		LDOA1_DIS[1:0] = 11		450		

Electrical Characteristics: LDOs *(continued)*

over recommended input voltage range, T_A = –40°C to +85°C and T_A = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LDOA2						
V_{IN}	Power input voltage		V_{OUT} + V_{DROP} (1)	1.8	1.98	V
V_{OUT}	DC output voltage in normal operating mode	LDOA2_VID[3:0] = 0000 (TPS650944 default)		0.7		V
		LDOA2_VID[3:0] = 0001		0.75		
		LDOA2_VID[3:0] = 0010		0.8		
		LDOA2_VID[3:0] = 0011		0.85		
		LDOA2_VID[3:0] = 0100		0.9		
		LDOA2_VID[3:0] = 0101		0.95		
		LDOA2_VID[3:0] = 0110		1		
		LDOA2_VID[3:0] = 0111		1.05		
		LDOA2_VID[3:0] = 1000		1.1		
		LDOA2_VID[3:0] = 1001		1.15		
		LDOA2_VID[3:0] = 1010 (TPS650940, TPS650941, and TPS650942 default)		1.2		
		LDOA2_VID[3:0] = 1011		1.25		
		LDOA2_VID[3:0] = 1100		1.3		
		LDOA2_VID[3:0] = 1101		1.35		
		LDOA2_VID[3:0] = 1110		1.4		
		LDOA2_VID[3:0] = 1111		1.5		
V_{OUT}	DC output voltage accuracy	I_{OUT} = 0 to 600 mA	–2%		3%	
I_{OUT}	DC output current				600	mA
V_{DROP}	Dropout voltage	V_{OUT} = 0.99 × V_{OUT_NOM}, I_{OUT} = 600 mA			350	mV
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation	I_{OUT} = 300 mA	–0.5%		0.5%	
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	I_{OUT} = 10 mA to 600 mA	–2%		2%	
I_{OCP}	Overcurrent protection	Measured with output shorted to ground	0.65	1.25		A
V_{TH_PG}	Power Good assertion threshold in percentage of target V_{OUT}	V_{OUT} rising		108%		
		V_{OUT} falling		92%		
$V_{TH\_HYS\_PG}$	Power Good deassertion hysteresis	V_{OUT} falling		3%		
I_Q	Quiescent current	I_{OUT} = 0 A		20		µA
PSRR	Power supply rejection ratio	f = 1 kHz, V_{IN} = 1.8 V, V_{OUT} = 1.2 V, I_{OUT} = 300 mA, C_{OUT} = 2.2 µF to 4.7 µF		48		dB
		f = 10 kHz, V_{IN} = 1.8 V, V_{OUT} = 1.2 V, I_{OUT} = 300 mA, C_{OUT} = 2.2 µF to 4.7 µF		30		dB
C_{OUT}	External output capacitance		2.2	4.7	10	µF
	ESR				100	mΩ
R_{DIS}	Output auto-discharge resistance	LDOA2_DIS[1:0] = 01		80		Ω
		LDOA2_DIS[1:0] = 10		180		
		LDOA2_DIS[1:0] = 11		475		

(1) The minimum value must be equal to or greater than 1.62 V.

Electrical Characteristics: LDOs *(continued)*

over recommended input voltage range, T_A = –40°C to +85°C and T_A = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LDOA3						
V_{IN}	Power input voltage		V_{OUT} + V_{DROP}(1)	1.8	1.98	V
V_{OUT}	DC output voltage in normal operating mode	LDOA3_VID[3:0] = 0000 (TPS650944 default)		0.7		V
		LDOA3_VID[3:0] = 0001		0.75		
		LDOA3_VID[3:0] = 0010		0.8		
		LDOA3_VID[3:0] = 0011		0.85		
		LDOA3_VID[3:0] = 0100		0.9		
		LDOA3_VID[3:0] = 0101		0.95		
		LDOA3_VID[3:0] = 0110		1		
		LDOA3_VID[3:0] = 0111		1.05		
		LDOA3_VID[3:0] = 1000		1.1		
		LDOA3_VID[3:0] = 1001		1.15		
		LDOA3_VID[3:0] = 1010		1.2		
		LDOA3_VID[3:0] = 1011 (TPS650940, TPS650941, and TPS650942 default)		1.25		
		LDOA3_VID[3:0] = 1100		1.3		
		LDOA3_VID[3:0] = 1101		1.35		
		LDOA3_VID[1:0] = 1110		1.4		
		LDOA3_VID[1:0] = 1111		1.5		
V_{OUT}	DC output voltage accuracy	I_{OUT} = 0 to 600 mA	–2%		3%	
I_{OUT}	DC output current				600	mA
I_{OCP}	Overcurrent protection	Measured with output shorted to ground	0.65	1.25		A
V_{DROP}	Dropout voltage	V_{OUT} = 0.99 × V_{OUT_NOM}, I_{OUT} = 600 mA			350	mV
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation	I_{OUT} = 300 mA	–0.5%		0.5%	
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	I_{OUT} = 10 mA to 600 mA	–2%		2%	
V_{TH_PG}	Power Good assertion threshold in percentage of target V_{OUT}	V_{OUT} rising		108%		
		V_{OUT} falling		92%		
$V_{TH\_HYS\_PG}$	Power Good deassertion hysteresis	V_{OUT} falling		3%		
I_Q	Quiescent current	I_{OUT} = 0 A		20		µA
PSRR	Power supply rejection ratio	f = 1 kHz, V_{IN} = 1.8 V, V_{OUT} = 1.2 V, I_{OUT} = 300 mA, C_{OUT} = 2.2 µF to 4.7 µF		48		dB
		f = 10 kHz, V_{IN} = 1.8 V, V_{OUT} = 1.2 V, I_{OUT} = 300 mA, C_{OUT} = 2.2 µF to 4.7 µF		30		
C_{OUT}	External output capacitance		2.2	4.7	10	µF
	ESR				100	mΩ
R_{DIS}	Output auto-discharge resistance	LDOA3_DIS[1:0] = 01		80		Ω
		LDOA3_DIS[1:0] = 10		180		
		LDOA3_DIS[1:0] = 11		475		

Electrical Characteristics: LDOs *(continued)*

over recommended input voltage range, T_A = –40°C to +85°C and T_A = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VTT LDO						
V_{IN}	Power input voltage			VDDQ	3.3	V
V_{OUT}	DC output voltage	Measured at VTTFB pin		V_{IN} / 2		V
	DC output voltage accuracy	Relative to V_{IN} / 2, I_{OUT} = 100 mA, 1.1 V ≤ V_{IN} ≤ 1.5 V	–10		10	mV
I_{OUT}	DC Output Current (RMS Value Over Operation)	1.1 V ≤ V_{IN} ≤ 1.5 V	–500	0	500	mA
	Pulsed Current (Duty Cycle Limited to Remain Below DC RMS Specification)	source(+) and sink(–): LPDDR3 and LPDDR4 OTPs, 1.1 V ≤ V_{IN} ≤ 1.5 V	–500		500	mA
		source(+) and sink(–): DDR3L OTPs, 1.1 V ≤ V_{IN} ≤ 1.5 V	–1800		1800	
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation	Relative to V_{IN} / 2, I_{OUT} ≤ 10 mA, 1.1 V ≤ V_{IN} ≤ 1.5 V	–10		10	mV
		Relative to V_{IN} / 2, I_{OUT} ≤ 500 mA, 1.1 V ≤ V_{IN} ≤ 1.5 V	–20		20	
		Relative to V_{IN} / 2, I_{OUT} ≤ 1200 mA, 1.1 V ≤ V_{IN} ≤ 1.5 V	–30		30	
		Relative to V_{IN} / 2, I_{OUT} ≤ 1800 mA, 1.1 V ≤ V_{IN} ≤ 1.5 V	–40		40	
ΔV_{OUT_TR}	Load transient regulation	DC + AC at sense point, 1.1 V ≤ V_{IN} ≤ 1.5 V, (I_{OUT} = 0 to 350 mA and 350 mA to 0) AND (0 to –350 mA and –350 mA to 0) with 1 µs of rise and fall time C_{OUT} = 40 µF	–5%		5%	
I_{OCP}	Overcurrent protection	Measured with output shorted to ground: OTPs with VTT I_{LIM} = 0.95 A	0.95			A
		Measured with output shorted to ground: OTPs with VTT I_{LIM} = 1.8 A	1.8			
V_{TH_PG}	Power Good deassertion threshold in percentage of target V_{OUT}	V_{OUT} rising		110%		
		V_{OUT} falling		95%		
$V_{TH\_HYS\_PG}$	Power Good reassertion hysteresis entering back into V_{TH_PG}	V_{OUT} rising or falling		5%		
I_Q	Total ground current	V_{IN} = 1.2 V, I_{OUT} = 0 A			240	µA
I_{LKG}	OFF leakage current	V_{IN} = 1.2 V, disabled			1	µA
C_{IN}	External input capacitance		10			µF
C_{OUT}	External output capacitance		35			µF

5.10 Electrical Characteristics: Load Switches

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SWA1						
V_{IN}	Input voltage range		0.5	1.8	3.3	V
I_{OUT}	DC output current				300	mA
R_{DSON}	ON resistance	V_{IN} = 1.8 V, measured from PVINSWA1 pin to SWA1 pin at I_{OUT} = $I_{OUT(MAX)}$		60	93	mΩ
		V_{IN} = 3.3 V, measured from PVINSWA1 pin to SWA1 pin at I_{OUT} = $I_{OUT(MAX)}$		100	165	
V_{TH_PG}	Power Good deassertion threshold in percentage of target V_{OUT}	V_{OUT} rising		108%		
		V_{OUT} falling		92%		
$V_{TH\_HYS\_PG}$	Power Good reassertion hysteresis entering back into V_{TH_PG}	V_{OUT} rising or falling		2%		
I_{INRUSH}	Inrush current upon turnon	V_{IN} = 3.3 V, C_{OUT} = 0.1 µF			10	mA
I_Q	Quiescent current	V_{IN} = 3.3 V, I_{OUT} = 0 A		10.5		µA
		V_{IN} = 1.8 V, I_{OUT} = 0 A		9		
I_{LKG}	Leakage current	Switch disabled, V_{IN} = 1.8 V		7	370	nA
		Switch disabled, V_{IN} = 3.3 V		10	900	
C_{OUT}	External output capacitance			0.1		µF
R_{DIS}	Output auto-discharge resistance	SWA1_DIS[1:0] = 01		100		Ω
		SWA1_DIS[1:0] = 10		200		
		SWA1_DIS[1:0] = 11		500		
SWB1_2						
V_{IN}	Input voltage range		0.5	1.8	3.3	V
I_{OUT}	DC current per output				400	mA
R_{DSON}	ON resistance per output	V_{IN} = 1.8 V, measured from PVINSWB1_B2 pin to SWB1 or SWB2 pin at I_{OUT} = $I_{OUT(MAX)}$		68	92	mΩ
		V_{IN} = 3.3 V, measured from PVINSWB1_B2 pin to SWB1 or SWB2 pin at I_{OUT} = $I_{OUT(MAX)}$		75	125	
V_{TH_PG}	Power Good deassertion threshold in percentage of target V_{OUT}	V_{OUT} rising		108%		
		V_{OUT} falling		92%		
$V_{TH\_HYS\_PG}$	Power Good reassertion hysteresis entering back into V_{TH_PG}	V_{OUT} rising or falling		2%		
I_{INRUSH}	Inrush current upon turning on	V_{IN} = 3.3 V, C_{OUT} = 0.1 µF			10	mA
I_Q	Quiescent current	V_{IN} = 3.3 V, I_{OUT} = 0 A		10.5		µA
		V_{IN} = 1.8 V, I_{OUT} = 0 A		9		
I_{LKG}	Leakage current	Switch disabled, V_{IN} = 1.8 V		7	460	nA
		Switch disabled, V_{IN} = 3.3 V		10	1150	
C_{OUT}	External output capacitance			0.1		µF
R_{DIS}	Output auto-discharge resistance	SWBx_DIS[1:0] = 01		100		Ω
		SWBx_DIS[1:0] = 10		200		
		SWBx_DIS[1:0] = 11		500		

5.11 Digital Signals: I^2C Interface

over recommended free-air temperature range and over recommended input voltage range (typical values are at T_A = 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage	V_{PULL_UP} = 1.8 V			0.4	V
V_{IH}	High-level input voltage		1.2			V
V_{IL}	Low-level input voltage				0.4	V
I_{LKG}	Leakage current	V_{PULL_UP} = 1.8 V		0.01	0.3	µA
$R_{PULL\text{-}UP}$	Pullup resistance	Standard mode			8.5	kΩ
		Fast mode			2.5	
		Fast mode plus			1	
C_{OUT}	Total load capacitance per pin				50	pF

5.12 Digital Input Signals (LDOLS_EN, SWA1_EN, THERMTRIPB, PMICEN, SLP_S3B, SLP_S4B, SLP_S0B)

over recommended free-air temperature range and over recommended input voltage range (typical values are at T_A = 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		0.85			V
V_{IL}	Low-level input voltage				0.4	V

5.13 Digital Output Signals (IRQB, RSMRSTB, PCH_PWROK, PROCHOT)

Over recommended free-air temperature range and over recommended input voltage range (typical values are at T_A = 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage	I_{OL} < 2 mA			0.4	V
I_{LKG}	Leakage current	V_{PULL_UP} = 1.8 V			0.35	µA

5.14 Timing Requirements

over recommended free-air temperature range and over recommended input voltage range (typical values are at T_A = 25°C) (unless otherwise noted)

		MIN	NOM	MAX	UNIT
I^2C INTERFACE					
f_{CLK}	Clock frequency (standard mode)			100	kHz
	Clock frequency (fast mode)			400	
	Clock frequency (fast mode plus)			1000	
t_r	Rise time (standard mode)			1000	ns
	Rise time (fast mode)			300	
	Rise time (fast mode plus)			120	
t_f	Rise time (standard mode)			300	ns
	Rise time (fast mode)			300	
	Rise time (fast mode plus)			120	

5.15 Switching Characteristics

over operating free-air temperature range and over recommended input voltage range (typical values are at T_A = 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BUCK CONTROLLERS						
t_{PG}	Total turnon time	Measured from enable going high to when output reaches 90% of target value.		550	850	µs
$T_{ON,MIN}$	Minimum ON time of DRVH			50		ns
T_{DEAD}	Driver dead-time	DRVH off to DRVL on		15		ns
		DRVL off to DRVH on		30		
f_{SW}	Switching frequency	Continuous-conduction mode, V_{IN} = 13 V, V_{OUT} ≥ 1 V		1000		kHz
BUCK CONVERTERS						
t_{PG}	Total turnon time	Measured from enable going high to when output reaches 90% of target value. V_{OUT} = 1 V, C_{OUT} = 88 µF		250	1000	µs
f_{SW}	Switching frequency	Continuous-conduction mode, BUCK3 V_{OUT} = 1 V, I_{OUT} = 1 A		1.6		MHz
		Continuous-conduction mode, BUCK3 V_{OUT} = 1.05 V, I_{OUT} = 1 A		1.7		
		Continuous-conduction mode, BUCK4 V_{OUT} = 1.8 V, I_{OUT} = 1 A		2.5		
		Continuous-conduction mode, BUCK5 V_{OUT} = 1.24 V, I_{OUT} = 1 A		2.4		
		Continuous-conduction mode, BUCK5 V_{OUT} = 1.35 V, I_{OUT} = 1 A		2.5		
LDOAx						
$t_{STARTUP}$	Start-up time	Measured from enable going high to when output reaches 95% of final value, V_{OUT} = 1.2 V, C_{OUT} = 4.7 µF		180		µs
VTT LDO						
$t_{STARTUP}$	Start-up time	Measured from enable going high to PG assertion, V_{OUT} = 0.675 V, C_{OUT} = 40 µF		22		µs
SWA1						
$t_{TURN-ON}$	Turnon time	Measured from enable going high to reach 95% of final value, V_{IN} = 3.3 V, C_{OUT} = 0.1 µF		0.85		ms
		Measured from enable going high to reach 95% of final value, V_{IN} = 1.8 V, C_{OUT} = 0.1 µF		0.63		
SWB1_2						
$t_{TURN-ON}$	Turnon time	Measured from enable going high to reach 95% of final value, V_{IN} = 3.3 V, C_{OUT} = 0.1 µF		1.1		ms
		Measured from enable going high to reach 95% of final value, V_{IN} = 1.8 V, C_{OUT} = 0.1 µF		0.82		

5.16 Typical Characteristics

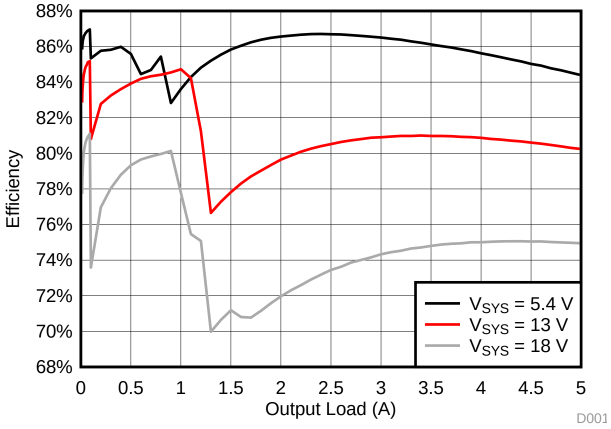

Figure 5-1. BUCK1 (VNN) Efficiency at V_{OUT} = 1 V

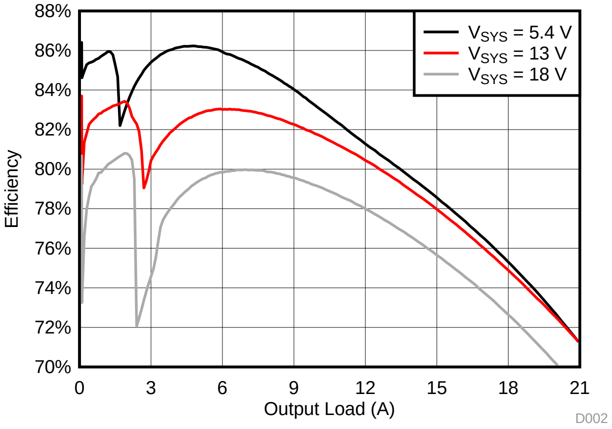

Figure 5-2. BUCK2 (VCCGI) Efficiency at V_{OUT} = 1 V

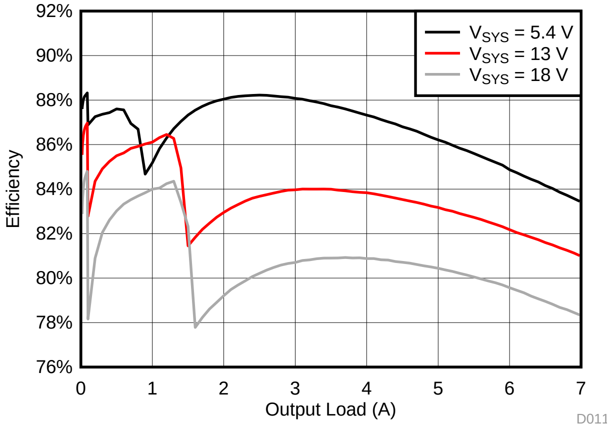

Figure 5-3. BUCK6 (VDDQ) Efficiency at V_{OUT} = 1.2 V

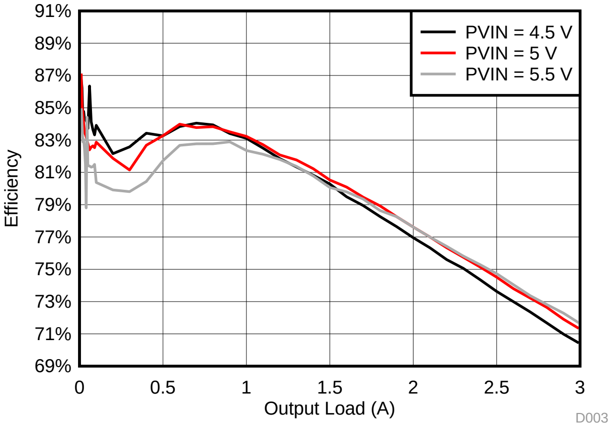

Figure 5-4. BUCK3 (VCCRAM) Efficiency at V_{OUT} = 1.05 V

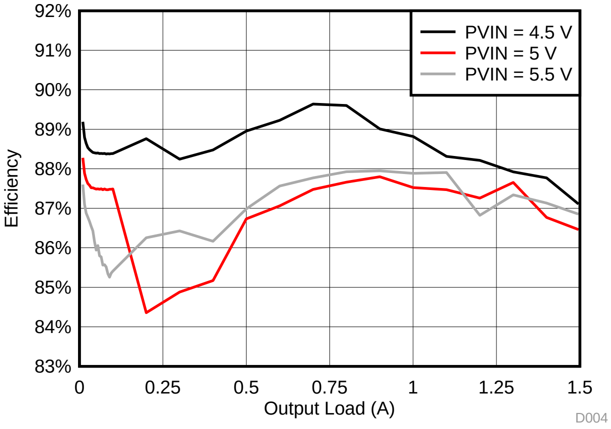

Figure 5-5. BUCK4 (V1P8A) Efficiency at V_{OUT} = 1.8 V

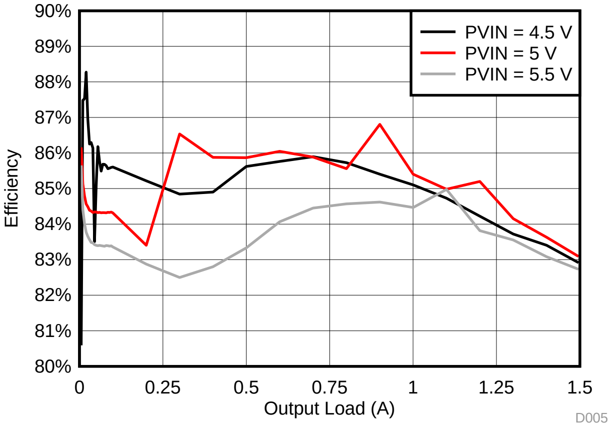

Figure 5-6. BUCK5 (V1P24A) Efficiency at V_{OUT} = 1.24 V

6 Detailed Description

6.1 Overview

The TPS65094x device provides all the necessary power supplies for the Intel Reference Designs. For an overview of the different OTP configurations, consult Table 3-1. The following VRs are integrated: three step-down controllers (BUCK1, BUCK2, and BUCK6), three step-down converters (BUCK3, BUCK4, and BUCK5), a sink and source LDO (VTT LDO), three low-voltage V_{IN} LDOs (LDOA1–LDOA3), and three load switches that are managed by power-up sequence logic to provide the proper power rails, sequencing, and protection. All VRs have a built-in discharge resistor, and the value can be changed by the DISCHCNT1–DISCHCNT3 and LDOA1_CTRL registers. When enabling a VR, the PMIC automatically disconnects the discharge resistor for that rail without any I^2C command. Table 6-1 summarizes the key characteristics of the voltage rails.

Table 6-1. Summary of Voltage Regulators

RAIL	TYPE	INPUT VOLTAGE (V)		OUTPUT VOLTAGE RANGE (V)			TYPICAL APPLICATION CURRENT (mA)
		MIN	MAX	MIN	TYP	MAX	
BUCK1 (VNN)	Step-down controller	4.5	21	0.5	1.05	1.67	5000
BUCK2 (VCCGI)	Step-down controller	4.5	21	0.5	1	1.67	21000
BUCK3 (VCCRAM)	Step-down converter	4.5	5.5	0.65	1.05	3.575	3000
BUCK4 (V1P8A)	Step-down converter	4.5	5.5	0.65	1.8	3.575	1500
BUCK5 (V1P24A)	Step-down converter	4.5	5.5	0.5	1.24	1.67	1900
BUCK6 (VDDQ)	Step-down controller	4.5	21	0.5	OTP dependent	1.67	7000
LDOA1	LDO	4.5	5.5	1.35	OTP dependent	3.3	200(1)
LDOA2	LDO	1.62	1.98	0.7	OTP dependent	1.5	600
LDOA3	LDO	1.62	1.98	0.7	OTP dependent	1.5	600
SWA1	Load switch	0.5	3.3				300
SWB1_2(2)	Load switch	0.5	3.3				800 (combined)
VTT	Sink and source LDO	BUCK6 output			V_{BUCK6} / 2		OTP dependent

(1) When powered from a 5-V supply through the DRV5V_2_A1 pin. Otherwise, maximum current is limited by maximum I_{OUT} of LDO5.
(2) For LPDDR3 and LPDDR4 memory, SWB1_2 is configured to V1P8U and controlled by SLP_S4B. For DDR3L memory, SWB1_2 is configured to either V3P3S or V1P8S and controlled by SLP_S3B.

6.2 Functional Block Diagram

Figure 6-1 shows a functional block diagram of the PMIC.

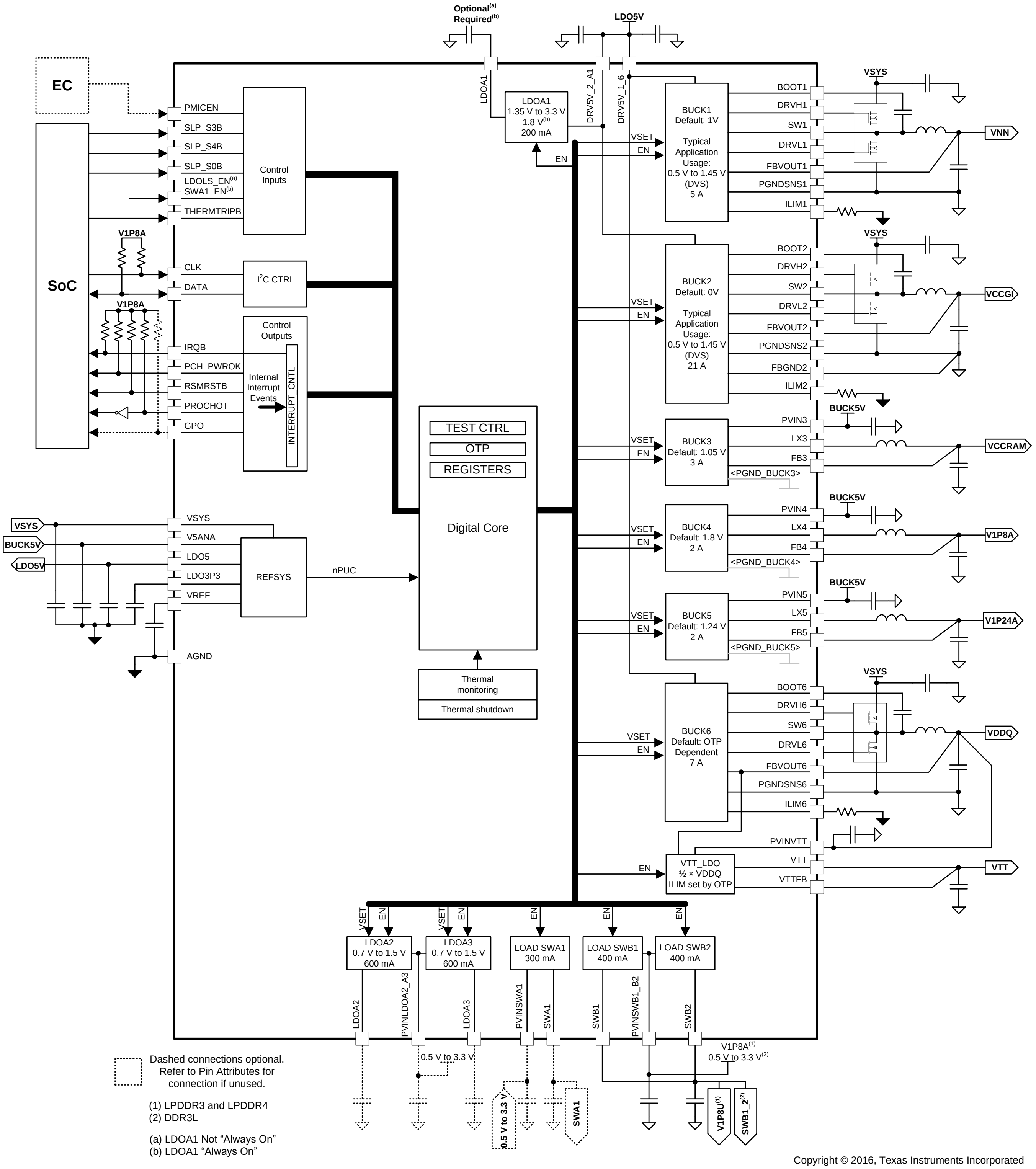

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Figure 6-1. PMIC Functional Block Diagram

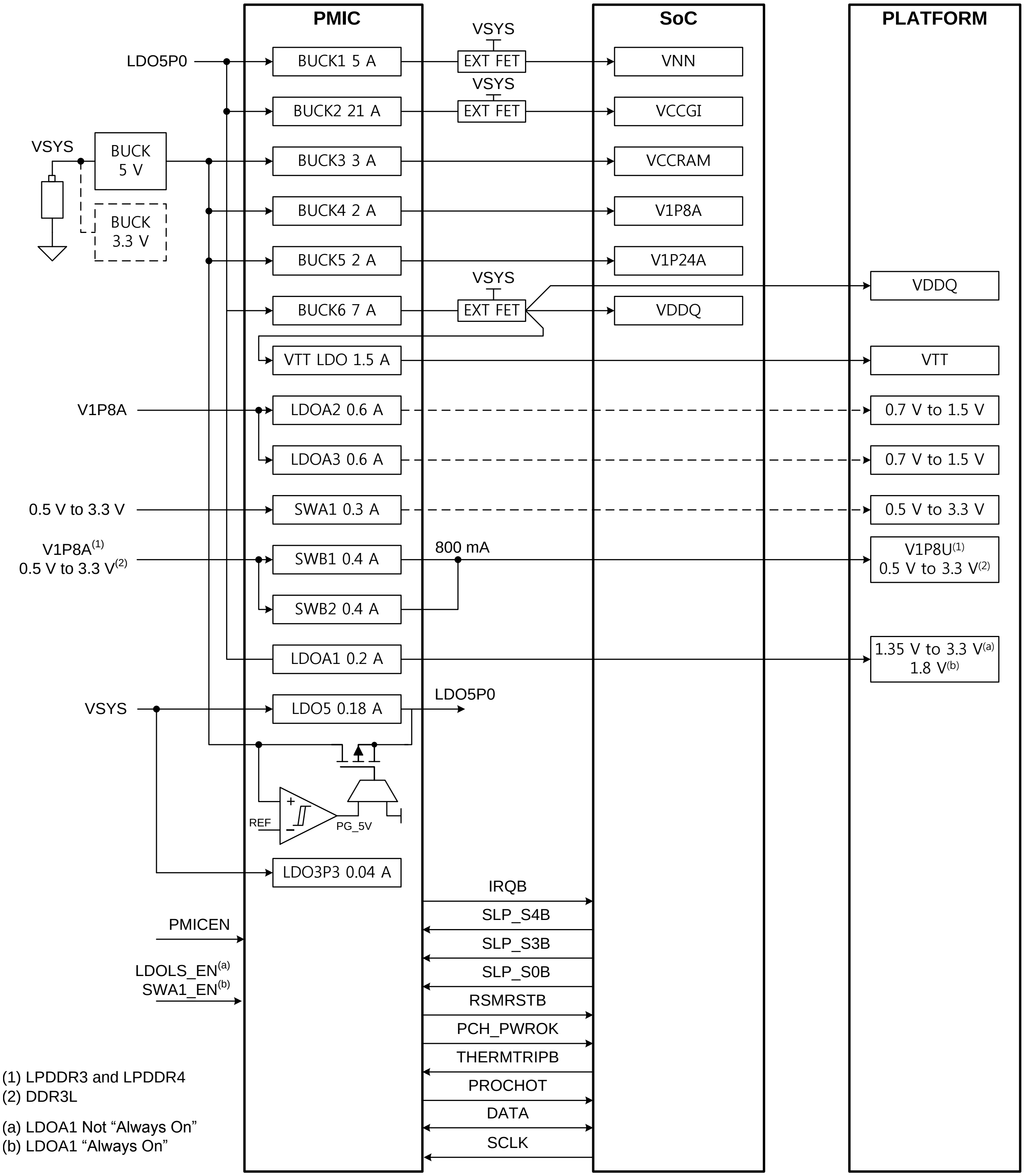

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Figure 6-2. Apollo Lake Power Map

6.3 Feature Description

6.3.1 *Power Good (PGOOD)*

The TPS65094x device provides information on status of VRs through two Power Good signals or pins. Table 6-2 defines which signals are required to assert the PGOOD signals.

Table 6-2. Power Good Summary

POWER GOOD[1]	QUALIFYING SIGNALS (LOGICAL AND)										
	UVLO (VSYS > 5.6 V)	PMICEN	THERMTRIPB	SLP_S4B	SLP_S3B	BUCK1_PG (VNN)	BUCK4_PG (V1P8A)	BUCK5_PG (V1P24A)	BUCK6_PG (VDDQ)	BUCK3_PG (VCCRAM)	BUCK2_PG (VCCGI)
RSMRSTB	✓	✓	✓			✓	✓	✓			
PCH_PWROK	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

(1) All Power Good signals must immediately deassert at the loss of any of the qualifying signals, or at the occurrence of a fault condition.

6.3.2 *Register Reset Conditions*

All registers are reset if any of the following conditions are met:

- VSYS pin voltage drops below 5.4 V
- Falling edge of PMICEN for OTPs where LDOA1 is not "Always On"
- Falling edge of THERMTRIPB while RSMRSTB = 1
- Power fault of any regulator where xx_FLTMSK = 0 (see Section 6.6.27, *PWR_FAULT_MASK1 Register*, and Section 6.6.28, *PWR_FAULT_MASK2 Register*)
- PMIC critical temperature shutdown
- Software shutdown (writing 1 to the SDWN bit in the FORCESHUTDN register, see Figure 6-35)

Additionally, BUCK1 and BUCK2 VID registers are reset on the falling edge of SLP_S0IXB and SLP_S3B.

6.3.3 *SMPS Voltage Regulators*

The buck controllers integrate gate drivers for external power stages with programmable current limit (set by an external resistor at ILIMx pin), which allows for optimal selection of external passive components based on the desired system load. The buck converters include integrated power stage and require a minimum number of pins for power input, inductor, and output voltage feedback input. Combined with high-frequency switching, all these features allow use of inductors in small form factor, thus reducing the total cost and size of the system.

BUCK3–BUCK6 have selectable auto- and forced-PWM mode through the BUCKx_MODE bit in the BUCKxCTRL register. In default auto mode, the VR automatically switches between PWM and PFM depending on the output load to maximize efficiency. The host cannot select Forced PWM mode for other SMPS VRs as they stay in auto mode at all times.

See Table 6-3 and Table 6-4 for the full voltage tables for all SMPS regulators.

Table 6-3. 10-mV Step-Size V_{OUT} Range (BUCK1, BUCK2, BUCK5, BUCK6)

VID Bits	V_{OUT}	VID Bits	V_{OUT}	VID Bits	V_{OUT}
0000000	0	0101011	0.92	1010110	1.35
0000001	0.50	0101100	0.93	1010111	1.36
0000010	0.51	0101101	0.94	1011000	1.37
0000011	0.52	0101110	0.95	1011001	1.38
0000100	0.53	0101111	0.96	1011010	1.39
0000101	0.54	0110000	0.97	1011011	1.40
0000110	0.55	0110001	0.98	1011100	1.41
0000111	0.56	0110010	0.99	1011101	1.42
0001000	0.57	0110011	1.00	1011110	1.43
0001001	0.58	0110100	1.01	1011111	1.44
0001010	0.59	0110101	1.02	1100000	1.45
0001011	0.60	0110110	1.03	1100001	1.46
0001100	0.61	0110111	1.04	1100010	1.47
0001101	0.62	0111000	1.05	1100011	1.48
0001110	0.63	0111001	1.06	1100100	1.49
0001111	0.64	0111010	1.07	1100101	1.50
0010000	0.65	0111011	1.08	1100110	1.51
0010001	0.66	0111100	1.09	1100111	1.52
0010010	0.67	0111101	1.10	1101000	1.53
0010011	0.68	0111110	1.11	1101001	1.54
0010100	0.69	0111111	1.12	1101010	1.55
0010101	0.70	1000000	1.13	1101011	1.56
0010110	0.71	1000001	1.14	1101100	1.57
0010111	0.72	1000010	1.15	1101101	1.58
0011000	0.73	1000011	1.16	1101110	1.59
0011001	0.74	1000100	1.17	1101111	1.60
0011010	0.75	1000101	1.18	1110000	1.61
0011011	0.76	1000110	1.19	1110001	1.62
0011100	0.77	1000111	1.20	1110010	1.63
0011101	0.78	1001000	1.21	1110011	1.64
0011110	0.79	1001001	1.22	1110100	1.65
0011111	0.80	1001010	1.23	1110101	1.66
0100000	0.81	1001011	1.24	1110110	1.67
0100001	0.82	1001100	1.25	1110111	1.67
0100010	0.83	1001101	1.26	1111000	1.67
0100011	0.84	1001110	1.27	1111001	1.67
0100100	0.85	1001111	1.28	1111010	1.67
0100101	0.86	1010000	1.29	1111011	1.67
0100110	0.87	1010001	1.30	1111100	1.67
0100111	0.88	1010010	1.31	1111101	1.67
0101000	0.89	1010011	1.32	1111110	1.67
0101001	0.90	1010100	1.33	1111111	1.67
0101010	0.91	1010101	1.34		

Table 6-4. 25-mV Step-Size V_{OUT} Range (BUCK3, BUCK4)

VID Bits	V_{OUT}	VID Bits	V_{OUT}	VID Bits	V_{OUT}
0000000	0	0101011	1.700	1010110	2.775
0000001	0.650	0101100	1.725	1010111	2.800
0000010	0.675	0101101	1.750	1011000	2.825
0000011	0.700	0101110	1.775	1011001	2.850
0000100	0.725	0101111	1.800	1011010	2.875
0000101	0.750	0110000	1.825	1011011	2.900
0000110	0.775	0110001	1.850	1011100	2.925
0000111	0.800	0110010	1.875	1011101	2.950
0001000	0.825	0110011	1.900	1011110	2.975
0001001	0.850	0110100	1.925	1011111	3.000
0001010	0.875	0110101	1.950	1100000	3.025
0001011	0.900	0110110	1.975	1100001	3.050
0001100	0.925	0110111	2.000	1100010	3.075
0001101	0.950	0111000	2.025	1100011	3.100
0001110	0.975	0111001	2.050	1100100	3.125
0001111	1.000	0111010	2.075	1100101	3.150
0010000	1.025	0111011	2.100	1100110	3.175
0010001	1.050	0111100	2.125	1100111	3.200
0010010	1.075	0111101	2.150	1101000	3.225
0010011	1.100	0111110	2.175	1101001	3.250
0010100	1.125	0111111	2.200	1101010	3.275
0010101	1.150	1000000	2.225	1101011	3.300
0010110	1.175	1000001	2.250	1101100	3.325
0010111	1.200	1000010	2.275	1101101	3.350
0011000	1.225	1000011	2.300	1101110	3.375
0011001	1.250	1000100	2.325	1101111	3.400
0011010	1.275	1000101	2.350	1110000	3.425
0011011	1.300	1000110	2.375	1110001	3.450
0011100	1.325	1000111	2.400	1110010	3.475
0011101	1.350	1001000	2.425	1110011	3.500
0011110	1.375	1001001	2.450	1110100	3.525
0011111	1.400	1001010	2.475	1110101	3.550
0100000	1.425	1001011	2.500	1110110	3.575
0100001	1.450	1001100	2.525	1110111	3.575
0100010	1.475	1001101	2.550	1111000	3.575
0100011	1.500	1001110	2.575	1111001	3.575
0100100	1.525	1001111	2.600	1111010	3.575
0100101	1.550	1010000	2.625	1111011	3.575
0100110	1.575	1010001	2.650	1111100	3.575
0100111	1.600	1010010	2.675	1111101	3.575
0101000	1.625	1010011	2.700	1111110	3.575
0101001	1.650	1010100	2.725	1111111	3.575
0101010	1.675	1010101	2.750		

6.3.3.1 Controller Overview

The controllers are fast-reacting, high-frequency, scalable output power controllers capable of driving two external N-MOSFETs. They use a D-CAP2 control scheme that optimizes transient responses at high load currents for such applications as CORE and DDR supplies. The output voltage is compared with internal reference voltage after divider resistors. The PWM comparator determines the timing to turn on the high-side MOSFET. The PWM comparator response maintains a very small PWM output ripple voltage. Because the device does not have a dedicated oscillator for control loop on board, switching cycle is controlled by the adaptive ON time circuit. The ON time is controlled to meet the target switching frequency by feed-forwarding the input and output voltage into the ON time one-shot timer.

The D-CAP2 control scheme has an injected ripple from the SW node that is added to the reference voltage to simulate output ripple, which eliminates the need for ESR-induced output ripple from D-CAP™ mode control. Thus, low-ESR output capacitors (such as low-cost ceramic MLCC capacitors) can be used with the controllers.

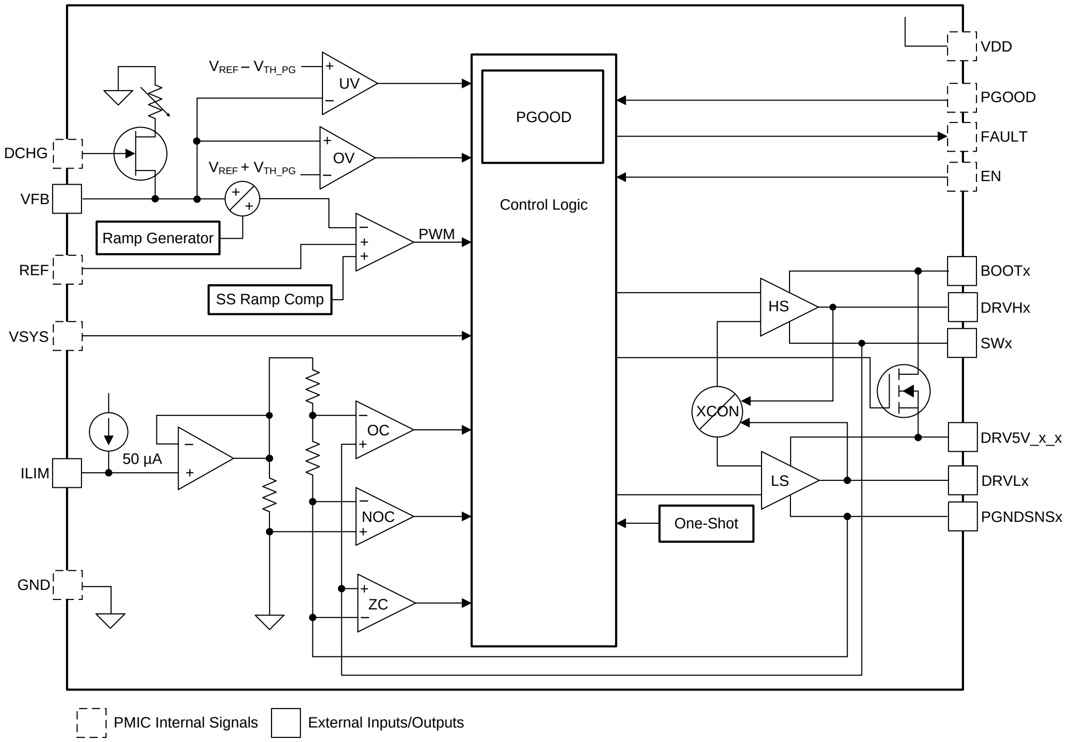

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Figure 6-3. Controller Block Diagram

6.3.3.2 Converter Overview

The PMIC synchronous step-down DC-DC converters include a unique hysteretic PWM control scheme which enables a high switching frequency converter, excellent transient and AC load regulation, as well as operation with cost-competitive external components. The controller topology supports forced PWM mode as well as power-save mode operation. Power-save mode operation, or PFM mode, reduces the quiescent current consumption and ensures high conversion efficiency at light loads by skipping switch pulses. In forced PWM mode, the device operates on a quasi-fixed frequency, avoids pulse skipping, and allows filtering of the switch noise by external filter components. The PMIC device offers fixed output voltage options featuring smallest solution size by using only three external components per converter.

A significant advantage of PMIC compared to other hysteretic PWM controller topologies is the excellent capability of the AC load transient regulation. When the output voltage falls below the threshold of the error comparator, a switch pulse is initiated, and the high-side switch is turned on. The high-side switch remains turned on until a minimum ON-time of t_{ONmin} expires and the output voltage trips the threshold of the error comparator or the inductor current reaches the high-side switch current limit. When the high-side switch turns off, the low-side switch rectifier is turned on and the inductor current ramps down until the high-side switch turns on again or the inductor current reaches zero. In forced PWM mode operation, negative inductor current is allowed to enable continuous conduction mode even at no load condition.

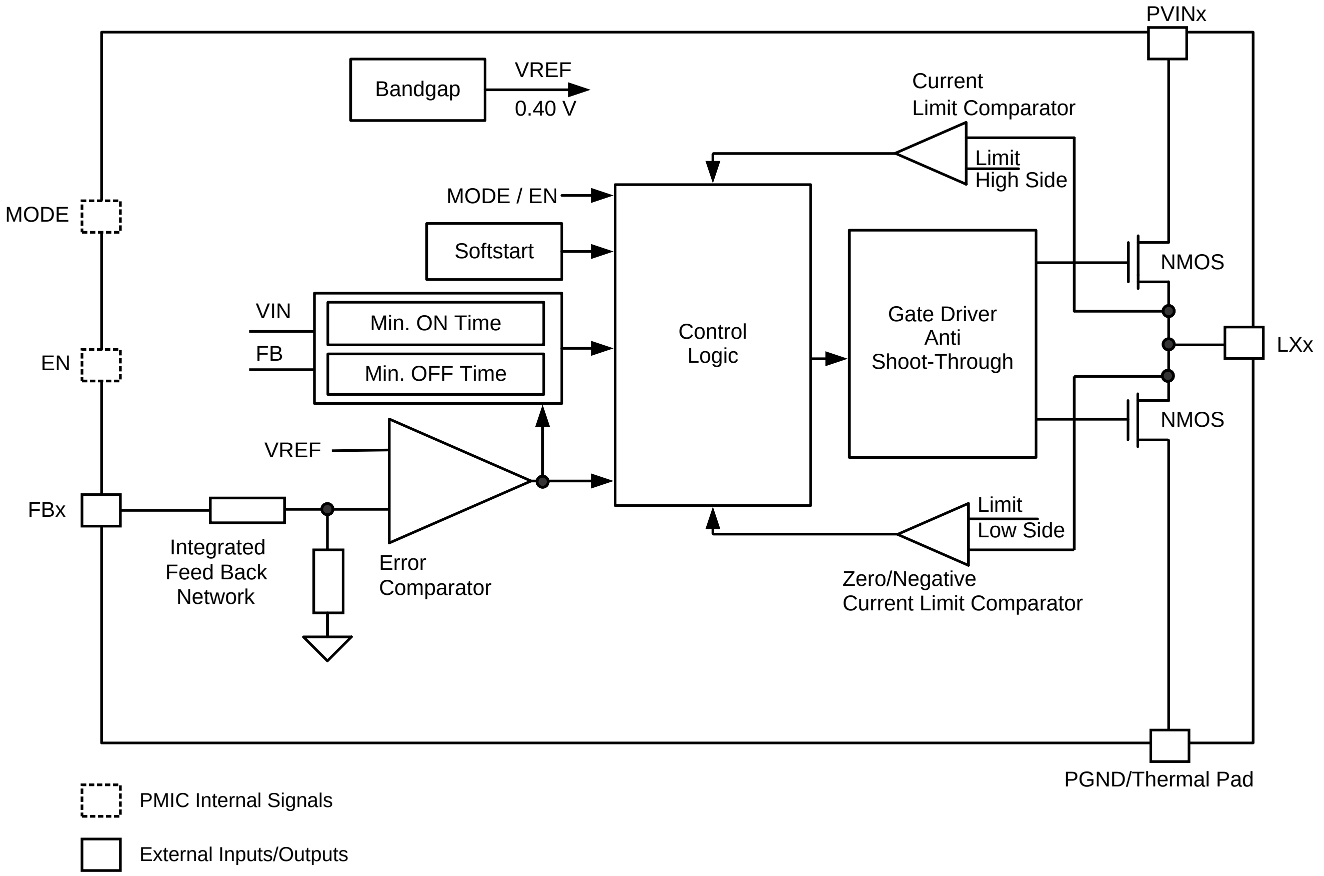


Figure 6-4. Converter Block Diagram

6.3.3.3 DVS

BUCK1–BUCK6 and LDOA1–3 support dynamic voltage scaling (DVS) for maximum system efficiency. The VR outputs can slew up and down in either 10-mV or 25-mV steps using the 7-bit voltage ID (VID) defined in Section 5.7, *Electrical Characteristics: Buck Controllers,* and Section 5.8, *Electrical Characteristics: Synchronous Buck Converters*. DVS slew rate is minimum 2.5 mV/µs. To meet the minimum slew rate, VID progresses to the next code at 3-µs (nom) interval per 10-mV step. When DVS is active, the VR is forced into PWM mode to ensure the output keeps track of VID code with minimal delay. Additionally, PGOOD is masked when DVS is in progress. Figure 6-5 shows an example of slew down and up from one VID to another.

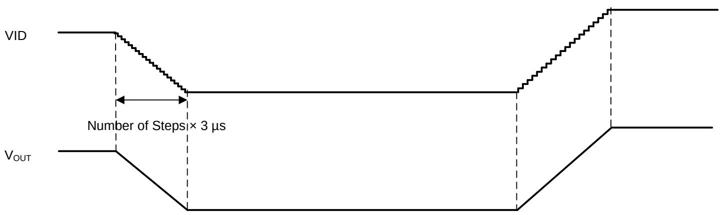


Figure 6-5. DVS Timing Diagram I

As shown in Figure 6-6, if a BUCKx_VID[6:0] is set to 7b000 0000, the output voltage slews down to 0.5 V first, and then drifts down to 0 V as the SMPS stops switching. Subsequently, if a BUCKx_VID[6:0] is set to a value (neither 7b000 0000 nor 7b000 0001) when the output voltage is less than 0.5 V, the VR ramps up to 0.5 V first with soft-start kicking in, then it slews up to the target voltage in the aforementioned slew rate.

NOTE

A fixed 200 µs of soft-start time is reserved for V_{OUT} to reach 0.5 V. In this case, however, the SMPS is not forced into PWM mode because it otherwise could cause V_{OUT} to droop momentarily if V_{OUT} is drifting above 0.5 V for any reason.

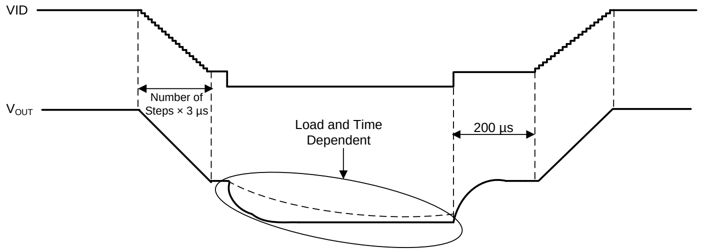


Figure 6-6. DVS Timing Diagram II

6.3.3.4 Current Limit

The buck controllers (BUCK1, BUCK2, and BUCK6) have inductor-valley current-limit architecture and the current limit is programmable by an external resistor at the ILIMx pin. Equation 1 shows the calculation for a desired resistor value, depending on specific application conditions. I_{LIMREF} is the current source out of the ILIMx pin that is typically 50 µA, and R_{DSON} is the maximum channel resistance of the low-side FET. The scaling factor is 1.3 to take into account all errors and temperature variations of R_{DSON}, I_{LIMREF}, and R_{ILIM}. Finally, 8 is another scaling factor associated with I_{LIMREF}.

$$R_{ILIM} = \frac{R_{DSON} \times 8 \times 1.3 \times \left(I_{LIM} - \frac{I_{ripple(min)}}{2} \right)}{I_{LIMREF}}$$

where

- I_{LIM} is the target current limit. An appropriate margin must be allowed when determining I_{LIM} from maximum output DC load current.
- $I_{ripple(min)}$ is the minimum peak-to-peak inductor ripple current for a given V_{OUT}. (1)

$$I_{ripple(min)} = \frac{V_{OUT}\left(V_{IN(MIN)} - V_{OUT}\right)}{L_{max} \times V_{IN(MIN)} \times f_{sw(max)}}$$

where

- L_{max} is maximum inductance
- $f_{sw(max)}$ is maximum switching frequency
- $V_{IN(MIN)}$ minimum input voltage to the external power stage (2)

The buck converter limit inductor peak current cycle-by-cycle to I_{IND_LIM} is specified in Section 5.8, *Electrical Characteristics: Synchronous Buck Converters*.

6.3.4 LDOs and Load Switches

6.3.4.1 VTT LDO

Powered from the BUCK6 output (VDDQ), the VTT LDO tracks VDDQ and regulates to half of the VDDQ voltage for proper DDR termination. The LDO current limit is OTP dependent, and it is designed specifically to power DDR memory. The VTT LDO is enabled by assertion (L → H) of the SLP_S0B pin and is disabled by deassertion (H → L) of the same pin. The LDO core is a transconductance amplifier with large gain, and it drives a current output stage that either sources or sinks current depending on the deviation of VTTFB pin voltage from the target regulation voltage.

6.3.4.2 LDOA1–LDOA3

The TPS65094x device integrates three optional general-purpose LDOs. LDOA1 is powered from a 5-V supply through the DRV5V_2_A1 pin and it can be factory configured to be an Always-On rail as long as a valid power supply is available at VSYS. See Table 6-5 for LDOA1 output voltage options. LDOA2 and LDOA3 share a power input pin (PVINLDOA2_A3). The output regulation voltages are set by writing to LDOAx_VID[3:0] bits (Reg 0x9A, 0x9B, and 0xAE). See Table 6-6 for LDOA2 and LDOA3 output voltage options. LDOA1 is controlled by LDOA1CTRL register. LDOA2 and LDOA3 can be controlled either by the LDOLS_EN pin or by writing to the LDOA2_EN bit (Reg 0xA0) and the LDOA3_EN bit (Reg 0xA1) as long as LDOLS_EN is low.

Table 6-5. LDOA1 Output Voltage Options

VID Bits	V_{OUT}	VID Bits	V_{OUT}	VID Bits	V_{OUT}	VID Bits	V_{OUT}
0000	1.35	0100	1.8	1000	2.3	1100	2.85
0001	1.5	0101	1.9	1001	2.4	1101	3.0
0010	1.6	0110	2.0	1010	2.5	1110	3.3
0011	1.7	0111	2.1	1011	2.7	1111	Not Used

Table 6-6. LDOA2 and LDOA3 Output Voltage Options

VID Bits	V_{OUT}	VID Bits	V_{OUT}	VID Bits	V_{OUT}	VID Bits	V_{OUT}
0000	0.70	0100	0.90	1000	1.10	1100	1.30
0001	0.75	0101	0.95	1001	1.15	1101	1.35
0010	0.80	0110	1.00	1010	1.20	1110	1.40
0011	0.85	0111	1.05	1011	1.25	1111	1.50

6.3.4.3 Load Switches

The PMIC features three general-purpose load switches. SWA1 has a power input pin (PVINSWA1), while SWB1 and SWB2 share a power input pin (PVINSWB1_B2). All switches have built-in slew rate control during start-up to limit the inrush current.

Table 6-7 lists the control signals for enabling and disabling each LDO and load switch.

Table 6-7. Summary of LDO and Load Switch Control

CONTROL SIGNAL	RAIL
SLP_S4B or SLP_S3B(1)	SWB1_2
LDOLS_EN(2)	LDOA2, LDOA3, SWA1
SWA1_EN(3)	SWA1
SLP_S0B(4)	VTT LDO

(1) For LPDDR3 and LPDDR4 memory, SWB1_2 is configured to V1P8U and controlled by SLP_S4B. For DDR3L memory, SWB1_2 is configured to either V3P3S or V1P8S and controlled by SLP_S3B.
(2) When LDOLS_EN = 0, the user can write to enable bits in Reg 0xA0–Reg 0xA1 to enable or disable the rails. Alternatively, all of them could be factory configured to be part of sequence along with other voltage rails. Pin name changed to SWA1_EN when LDOA1 is factory programmed to always on.
(3) When SWA1_EN = 0, the user can write to enable bits in Reg 0xA0–Reg 0xA1 to enable or disable the rails. Alternatively, all of them could be factory configured to be part of sequence along with other voltage rails. Pin name changed to LDOLS_EN when LDOA1 is not factory programmed to always on.
(4) BUCK6_PG should be asserted as well.

6.3.5 Power Sequencing and VR Control

When a valid power source is available at VSYS (VSYS ≥ 5.6 V), internal analog blocks including LDO5 and LDO3P3 are enabled. For part numbers with LDOA1 set as an always on rail, the PMIC leaves reset and I^{2}C communication is available as soon as LDO3P3 and LDO5 power goods are confirmed. For part numbers with LDOA1 set as a general-purpose LDO, the PMIC remains in reset until PMICEN is set high. Five input pins of the TPS65094x device are driven by a host or by external-controller (EC) defined power states that transition from one to another in sequence.

Table 6-8 shows various system-level power states. Also, Table 6-9 summarizes a list of active rails in each power state. The sequencing for the transitions between these states is described in the following sections.

If a rail is either disabled by I^{2}C or OTP programming, then it is not enabled by the following sequences. For example, VTT LDO is not enabled for LPDDR4 OTPs.

Table 6-8. Power State and Corresponding I/O Status

POWER STATE	SIGNALS TO PMIC					SIGNALS FROM PMIC	
	PMICEN	SLP_S4B (1)	SLP_S3B (1)	SLP_S0B (2)	THERMTRIPB (3)	RSMRSTB	PCH_PWROK
G3	0	0	0	0	0	0	0
S4/S5	1	0	0	1	1	1	0
S3	1	1	0	1	1	1	0
S0iX	1	1	1	0	1	1	1
S0	1	1	1	1	1	1	1

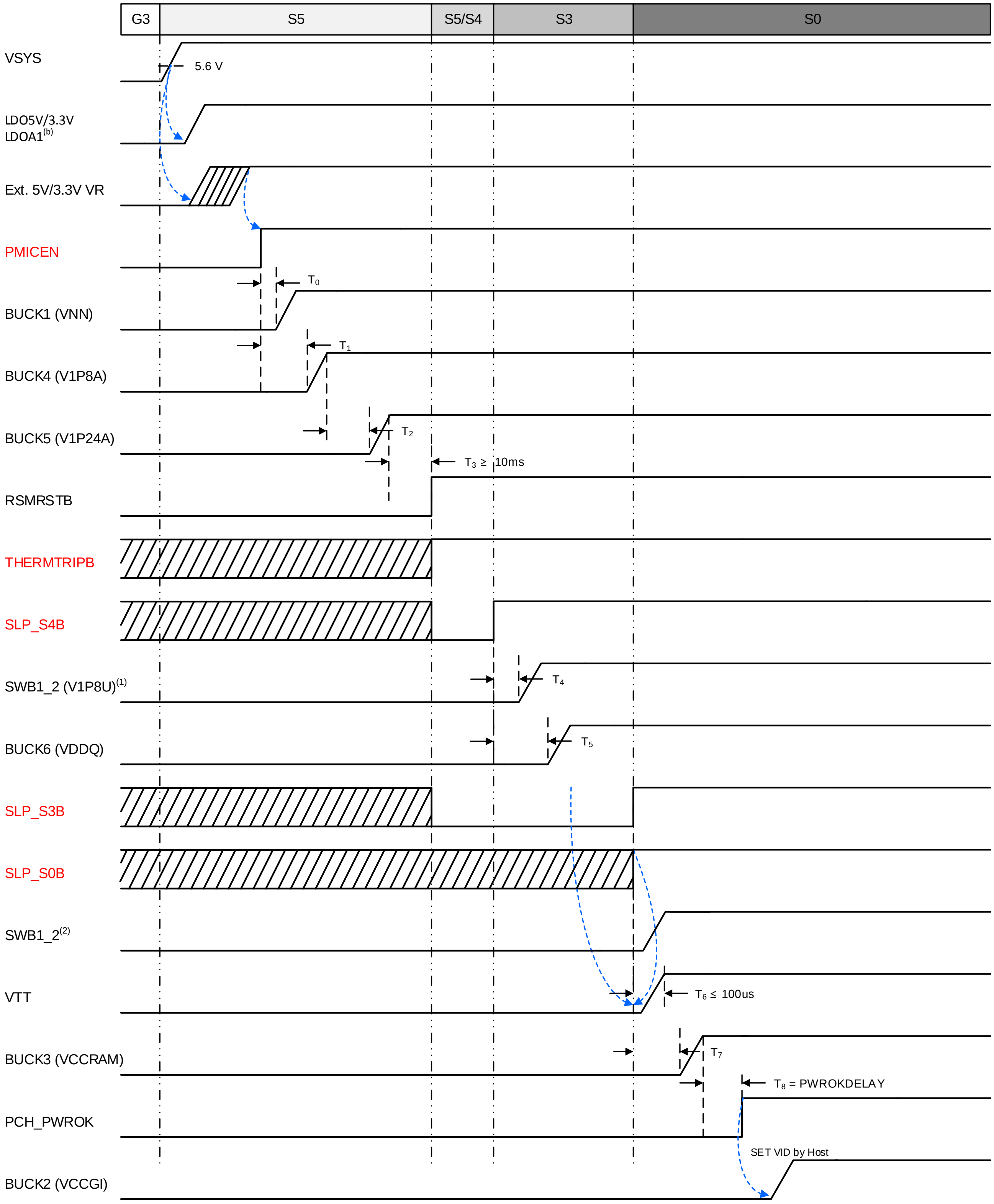
(1) When PMIC is first enabled, SLP_S4B and SLP_S3B are to be treated as if they are low (actual state of signal ignored) until the deassertion of RSMRSTB (L → H).
(2) When PMIC is first enabled, SLP_S0B are to be treated as if they are high (actual state of signal ignored) until the assertion of PCH_PWROK (L → H).
(3) THERMTRIPB is to be treated as if it is high (actual state of signal ignored) until the deassertion of RSMRSTB (L → H).

Table 6-9. Active Rails in Each Power State

POWER STATE	ACTIVE RAILS
S4/S5	BUCK1 (VNN), BUCK4 (V1P8A), BUCK5 (V1P24A)
S3	Rails in S4/S5 + SWB1_2 (V1P8U) (1), BUCK6 (VDDQ)
S0	Rails in S3 + SWB1_2 (2), VTT, BUCK2 (VCCGI), BUCK3 (VCCRAM)
S0iX	Rails in S0 – BUCK1 (VNN), BUCK2 (VCCGI), BUCK3 (VCCRAM), VTT

(1) For LPDDR3 and LPDDR4
(2) For DDR3L

6.3.5.1 Cold Boot



(1) LPDDR3 and LPDDR4
(2) DDR3L

(a) LDOA1 Not "Always On"
(b) LDOA1 "Always On"

Figure 6-7. Cold Boot Sequence

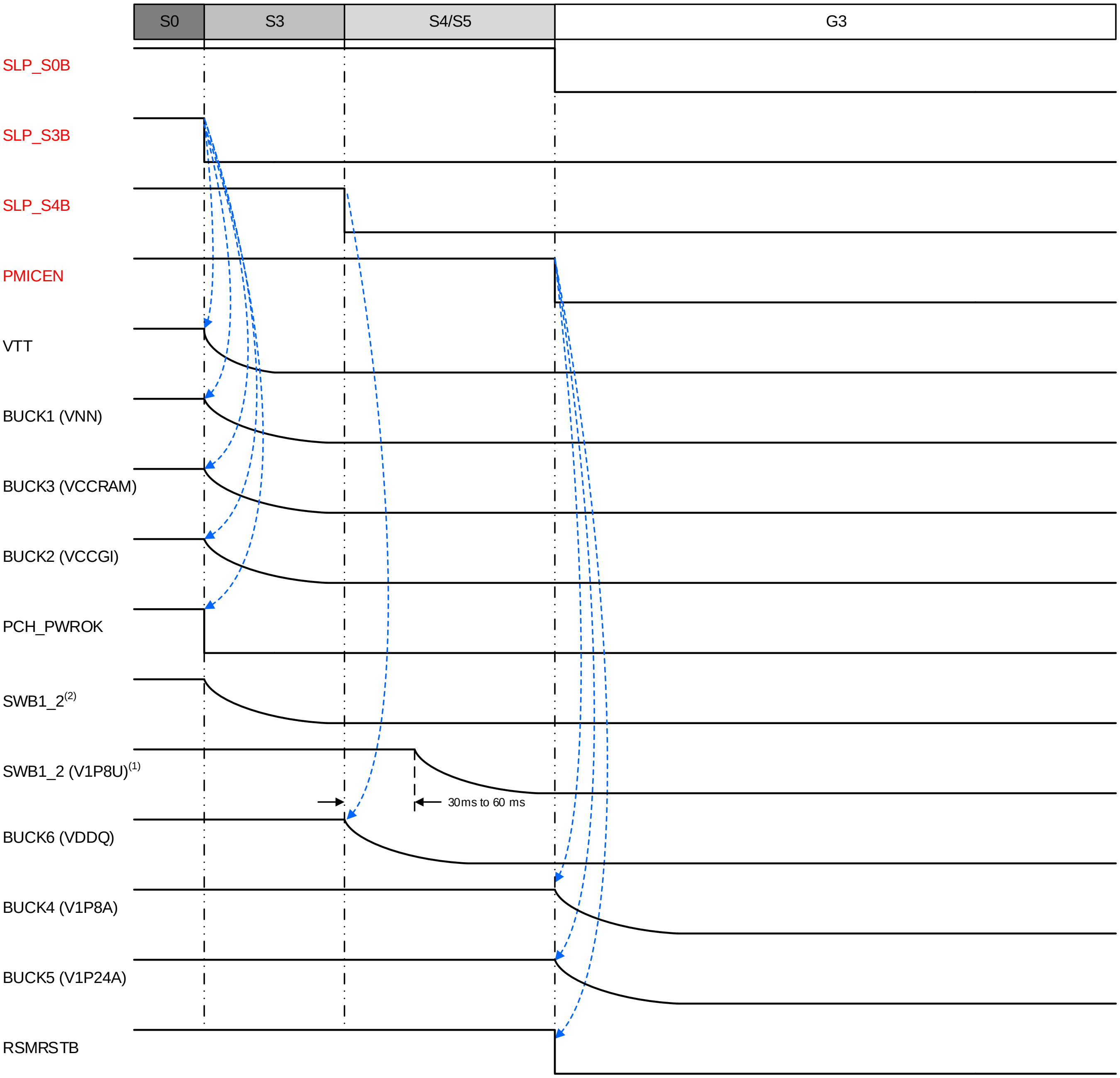
As V_{SYS} crosses above $V_{SYS\_UVLO\_5V}$ + $V_{SYS\_UVLO+5V\_HYS}$, the cold-boot sequence is initiated by pulling the PMICEN pin high followed by driving the remaining control pins high in order. SLP_S3B and SLP_S4B may go high at the same time. SLP_S0B is not defined until the first transition to S0 after RSMRSTB deassertion. SLP_S0B is defined for all Sx power-state transitions after the first transition to S0.

Table 6-10 lists definitions of the timing delays. These timing delays also apply to the subsequent sequences. T0 to T10 are factory programmable to 0 ms, 2 ms, 4 ms, 8 ms, 16 ms, 24 ms, 32 ms, or 64 ms.

Table 6-10. Definition of Delays During Cold Boot Sequence

DELAY	DESCRIPTION	TYP VALUE	UNIT
T0	PMICEN to BUCK1 (VNN) enable	0	ms
T1	PMICEN to BUCK4 (V1P8A) enable	4	ms
T2	BUCK4 PG to BUCK5 (V1P24A) enable	0	ms
T3	BUCK5 PG to RSMRSTB deassertion	10	ms
T4	SLP_S4B deassertion to SWB1_2 (V1P8U) enable	0	ms
T5	SLP_S4B deassertion to BUCK6 (VDDQ) enable	4	ms
T6	Logical AND of BUCK6 PG, SLP_S0B, SLP_S3B, and SLP_S4B to VTT enable	0	ms
T7	SLP_S0B deassertion to BUCK3 (VCCRAM) enable	2	ms
T8	Logical AND of all PGs (except BUCK2) to PCH_PWROK assertion. User selectable from POK_DELAY register.	100	ms

6.3.5.2 Cold OFF



(1) LPDDR3 and LPDDR4
(2) DDR3L

Figure 6-8. Cold OFF Sequence

Cold OFF sequence is initiated by pulling the SLP_S3B pin low in the S0 state, followed by SLP_S4B, SLP_S0B, and PMICEN.

6.3.5.3 Connected Standby Entry and Exit

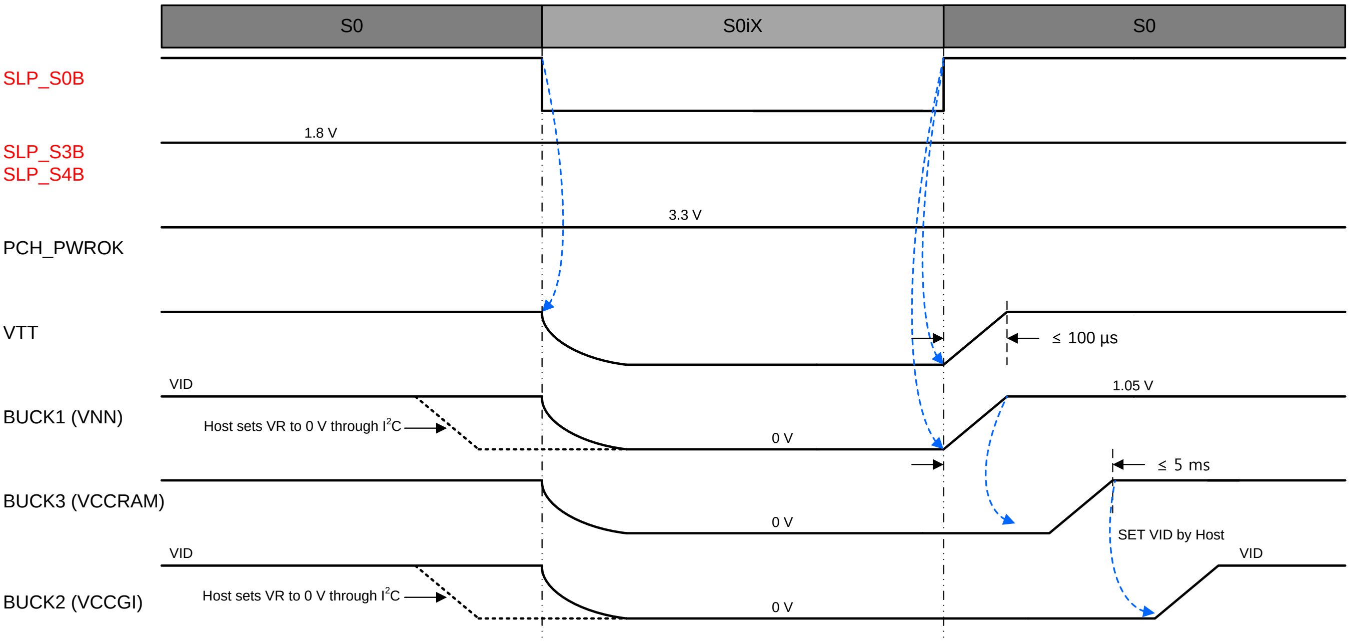


Figure 6-9. Connected Standby Entry and Exit Sequence

S0 to S0iX (Connected Standby) entry and exit occurs when SLP_S0B is pulled low and high, respectively. In Connected Standby state, VTT LDO is turned off, but all PGOODs remain asserted. BUCK1–BUCK3 are not disabled, but instead stop switching while BUCK4–BUCK6 remain in regulation. SWB1_2 also stays enabled. On entry, BUCK2 and BUCK3 decay to 0 V with their VID registers retaining the last programmed values to which the BUCKs ramp back up on exit. The host can write to BUCK2CTRL and BUCK3CTRL registers regardless of the state of the SLP_S0B pin while SLP_S3B and SLP_S4B are high, which means that BUCK2 and BUCK3 can be changed to ramp to a different voltage upon exiting S0iX than they had when entering S0iX state. BUCK1 ramps back up to the default value (1.05 V).

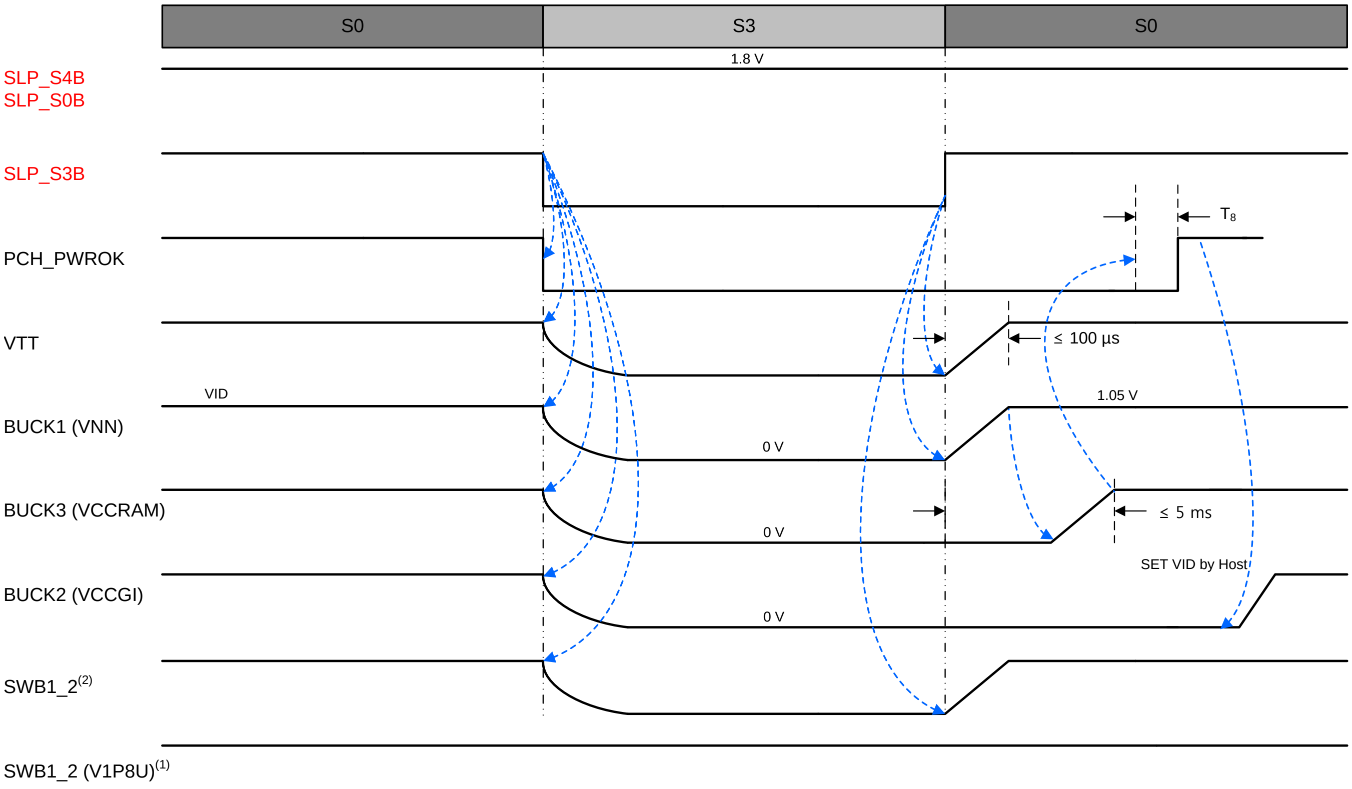
Table 6-11 summarizes status of each VR in Connected Standby state.

Table 6-11. Summary of Rails on Connected Standby Entry and Exit

VR	S0 → S0IX	S0IX → S0
BUCK1 (VNN)	0 V	1.05 V
BUCK2 (VCCGI)	0 V	0 V
BUCK3 (VCCRAM)	0 V	1.05 V
BUCK4 (V1P8A)	VID value	VID value
BUCK5 (V1P24A)	VID value	VID value
BUCK6 (VDDQ)	OTP dependent	OTP dependent
VTT LDO (VTT)	OFF	VDDQ / 2
SWB1_2	ON	ON

6.3.5.4 S0 to S3 Entry and Exit

Assertion of SLP_S3B (H → L) triggers S3 entry. Deassertion of SLP_S3B causes S3 exit and S0 entry as depicted in Figure 6-10. On S3 exit, BUCK1–BUCK3 behave exactly the same way as they do on S0iX exit, which is explained in Section 6.3.5.3, *Connected Standby Entry and Exit.*

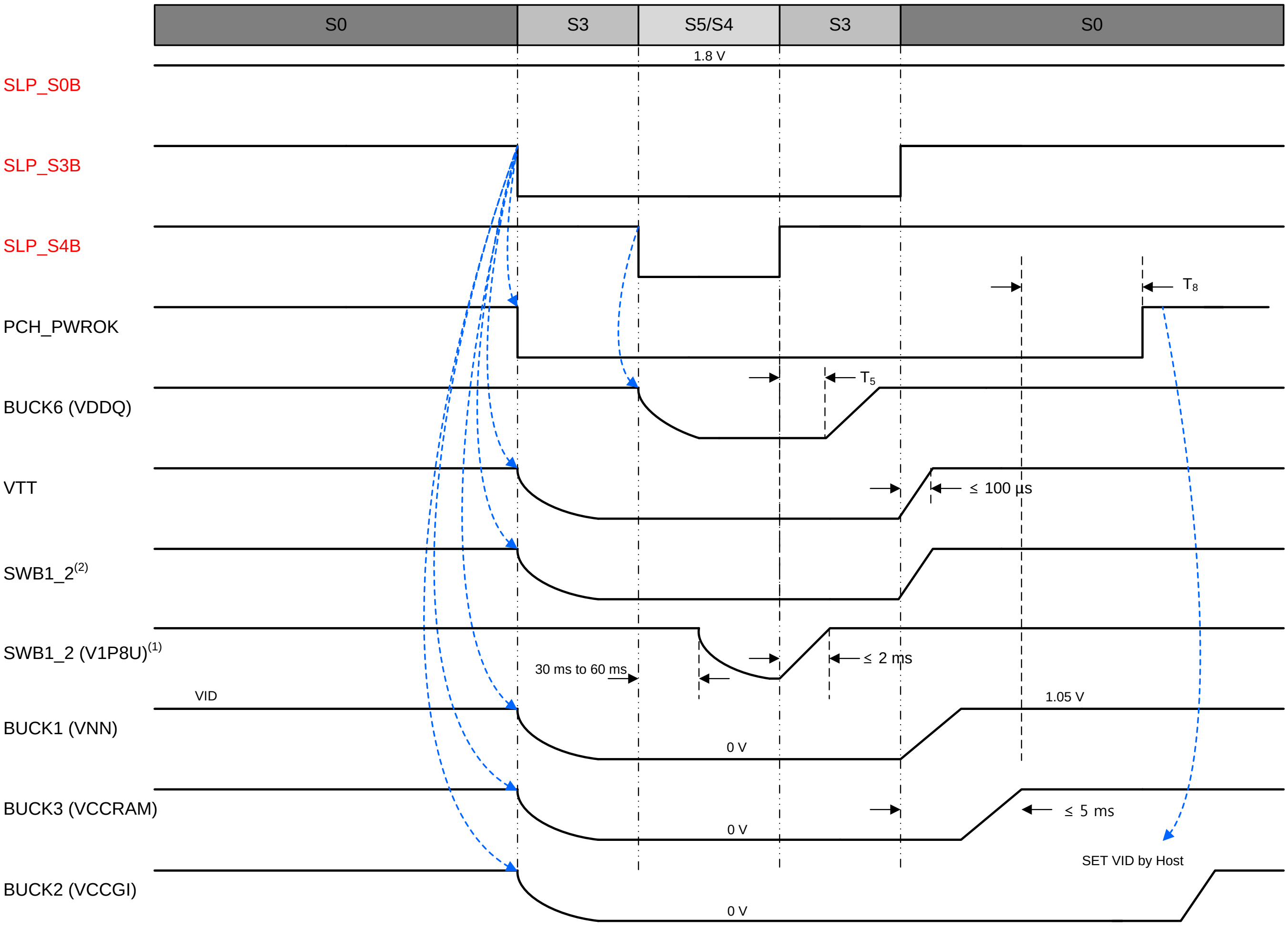


(1) LPDDR3 and LPDDR4
(2) DDR3L

Figure 6-10. S3 Entry and Exit Sequence

6.3.5.5 S0 to S4/5 Entry and Exit

Assertion of the SLP_S4B (H → L) after the S3 entry pushes the sequence further down to S4/5 where SWB1_2 (for LPDDR3 or LPDDR4) and BUCK6 are disabled. Any rails not shown are essentially the same as the S0 to S3 entry and exit case described in Figure 6-11.



(1) LPDDR3 and LPDDR4
(2) DDR3L

Figure 6-11. S4/5 Entry and Exit Sequence

6.3.5.6 Emergency Shutdown

When V_{SYS} crosses below $V_{SYS\_UVLO\_5V}$, all Power Good pins are deasserted; after 444 ns (nominal) of delay, all VRs shut down (see Figure 6-12). Upon shutdown, all internal discharge resistors are set to 100 Ω to ensure timely decay of all VR outputs. VSYS crossing above $V_{SYS\_UVLO\_5V}$ + $V_{SYS\_UVLO\_5V\_HYS}$ and assertion of PMICEN is required to re-enable the VRs.

Other conditions that cause emergency shutdown are the following:

- The die temperature rising above the critical temperature threshold (T_{CRIT})
- Falling edge of THERMTRIPB
- Deassertion of Power Good of any rail or failure to reach power good within 10 ms of enable (configurable)

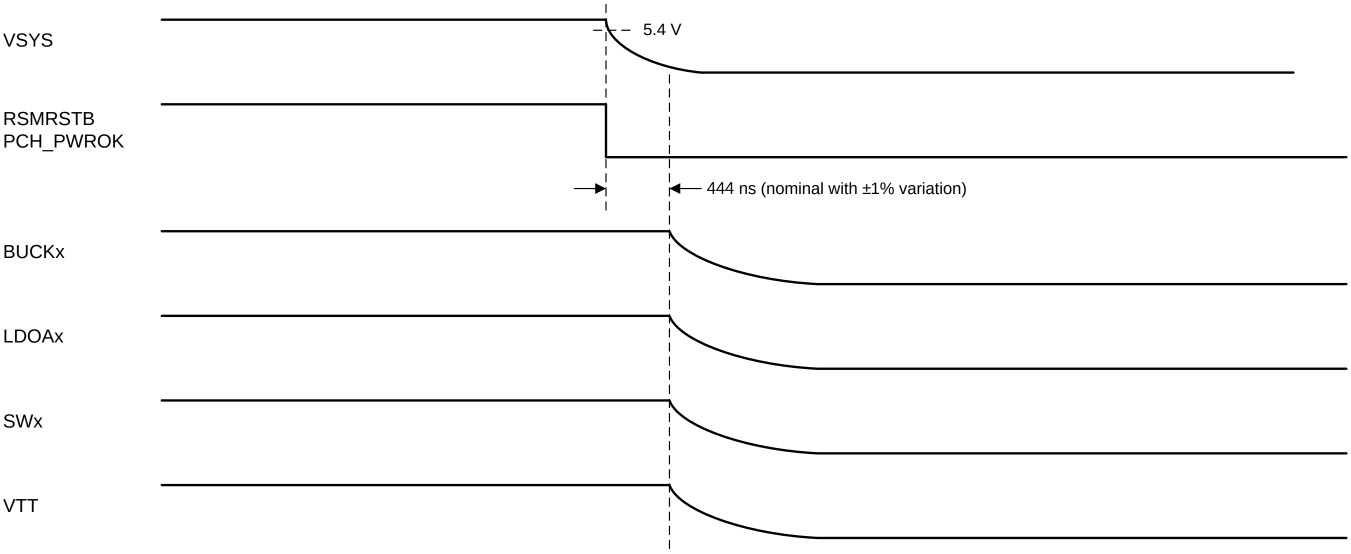


Figure 6-12. Emergency Shutdown Sequence

6.4 Device Functional Modes

6.4.1 Off Mode

When power supply at the VSYS pin is less than $V_{SYS\_UVLO\_5V}$ (5.4-V nominal) + $V_{SYS\_UVLO\_5V\_HYS}$ (0.2-V nominal), the device is in off mode, where all output rails are disabled. If the supply voltage is greater than $V_{SYS\_UVLO\_3V}$ (3.6-V nominal) + $V_{SYS\_UVLO\_3V\_HYS}$ (0.15-V nominal) while it is still less than $V_{SYS\_UVLO\_5V}$ + $V_{SYS\_UVLO\_5V\_HYS}$, then the internal band-gap reference (VREF pin) along with LDO3P3 are enabled and regulated at target values.

6.4.2 Standby Mode

When power supply at the VSYS pin rises above $V_{SYS\_UVLO\_5V}$ + $V_{SYS\_UVLO\_5V\_HYS}$, the device enters standby mode, where all internal reference and regulators (LDO3P3 and LDO5) are running, and I^2C interface and PMICEN pin are ready to respond. All default registers defined in Section 6.6, *Register Maps*, should now have been loaded from one-time programmable (OTP) memory. Quiescent current consumption in standby mode is specified in Section 5.5, *Electrical Characteristics: Total Current Consumption.*

6.4.3 Active Mode

The device proceeds to active mode when any output rail is enabled either through an input pin as discussed in Section 6.3.5, *Power Sequencing and VR Control*, or by writing to the EN bits through I^2C. Output regulation voltage can also be changed by writing to the VID bits defined in Section 6.6, *Register Maps.*

6.5 Programming

6.5.1 I^2C Interface

The I^2C interface is a 2-wire serial interface developed by NXP™ (formerly Philips Semiconductor) (see the I^2C-Bus Specification and user manual, Rev 4, 13 February 2012). The bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I^2C compatible devices connect to the I^2C bus through open-drain I/O pins, DATA and CLK. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the start and stop of data transfer. A slave device receives and/or transmits data on the bus under control of the master device.

The TPS65094x device works as a slave and supports the following data transfer modes, as defined in the I^2C-Bus Specification: standard mode (100 kbps), fast mode (400 kbps), and high-speed mode (1 Mbps). The interface adds flexibility to the power supply solution, enabling programming of most functions to new values depending on the instantaneous application requirements. Register contents are loaded when V_{SYS} higher than $V_{SYS\_UVLO\_5V}$ is applied to the TPS65094x device. The I^2C interface is running from an internal oscillator that is automatically enabled when there is an access to the interface.

The data transfer protocol for standard and fast modes are exactly the same, therefore, they are referred to as F/S-mode in this document. The protocol for high-speed mode is different from F/S-mode, and it is referred to as H/S-mode.

The TPS65094x device supports 7-bit addressing; however, 10-bit addressing and general call address are not supported. The default device address is 0x5E.

6.5.1.1 F/S-Mode Protocol

The master initiates data transfer by generating a START condition. The START condition exists when a high-to-low transition occurs on the SDA line while SCL is high (see Figure 6-13). All I^{2}C-compatible devices should recognize a START condition.

The master then generates the SCL pulses and transmits the 7-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 6-14). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see Figure 6-15), by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master identifies that the communication link with a slave has been established.

The master generates further SCL cycles to either transmit data to the slave (R/W bit = 0) or receive data from the slave (R/W bit = 1). In either case, the receiver must acknowledge the data sent by the transmitter. An acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. Any 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the master generates a STOP condition by pulling the SDA line from low to high while the SCL line is high (see Figure 6-13). This STOP condition releases the bus and stops the communication link with the addressed slave. All I^{2}C-compatible devices must recognize the STOP condition. Upon the receipt of a STOP condition, all devices detect that the bus is released, and they wait for a START condition followed by a matching address.

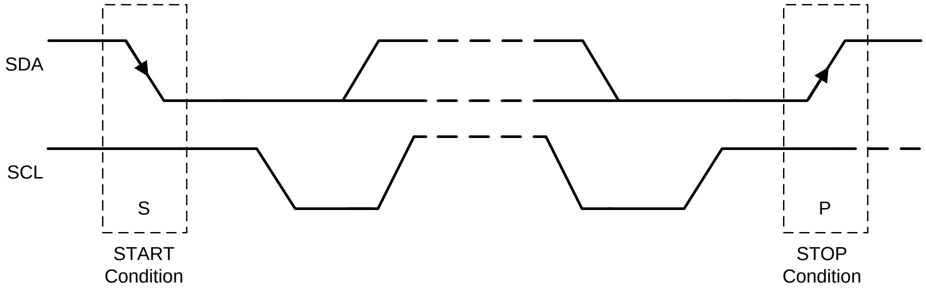


Figure 6-13. START and STOP Conditions

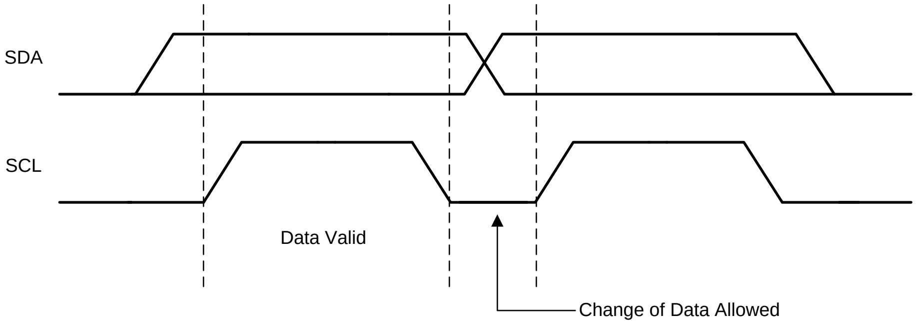


Figure 6-14. Bit Transfer on the I^{2}C Bus

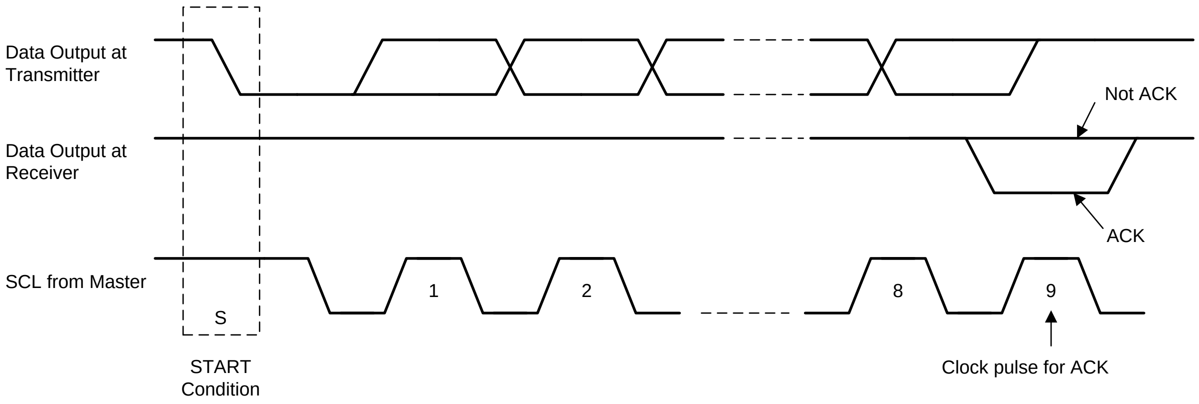


Figure 6-15. Acknowledge on the I^{2}C Bus

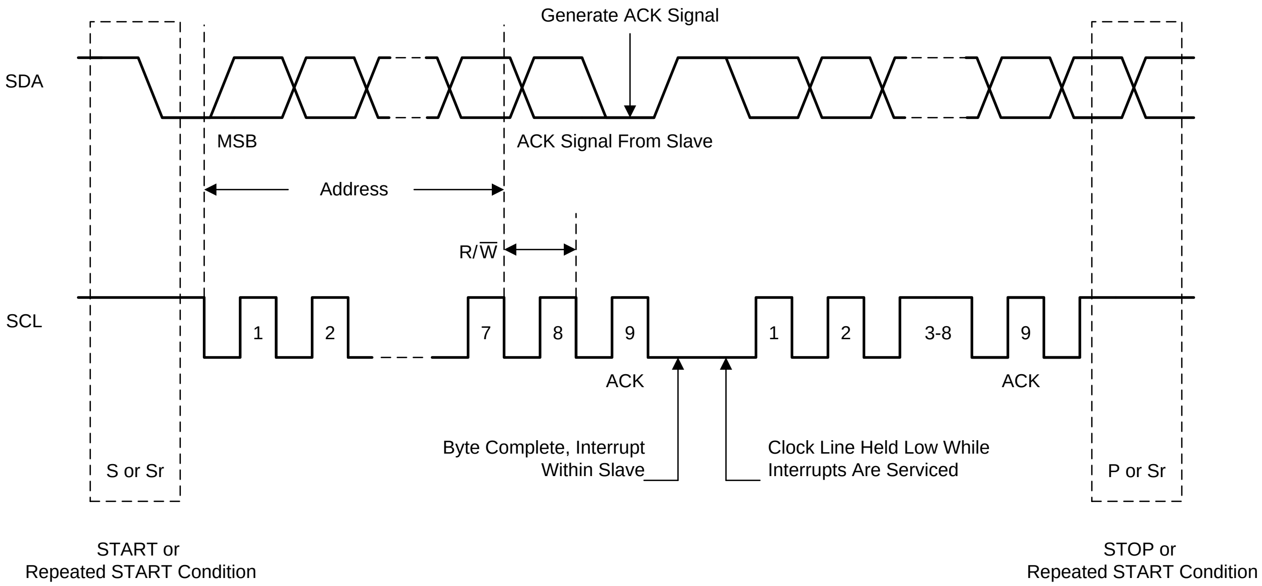


Figure 6-16. I^{2}C Bus Protocol

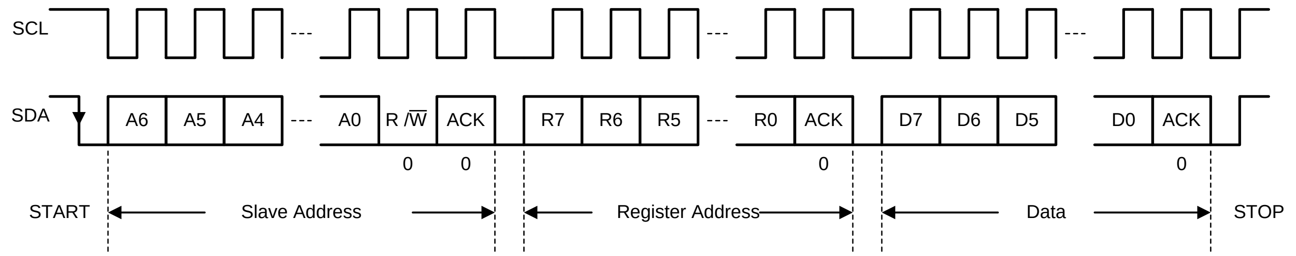


Figure 6-17. I^{2}C Interface WRITE to TPS65094x in F/S Mode

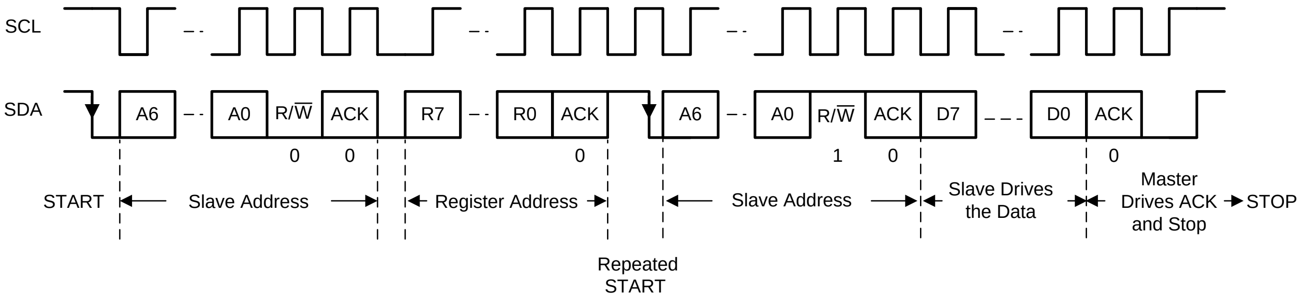


Figure 6-18. I^{2}C Interface READ from TPS65094x in F/S Mode (Only Repeated START is Supported)

6.6 Register Maps

Default value of RESERVED R/W bits must not be written to the opposite value.

6.6.1 *VENDORID: PMIC Vendor ID Register (offset = 00h) [reset = 0010 0010]*

Figure 6-19. VENDORID Register (offset = 00h) [reset = 0010 0010]

Bit	7	6	5	4	3	2	1	0
Bit Name	VENDORID[7]	VENDORID[6]	VENDORID[5]	VENDORID[4]	VENDORID[3]	VENDORID[2]	VENDORID[1]	VENDORID[0]
TPS65094x	0	0	1	0	0	0	1	0
Access	R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6-12. VENDORID Register Field Descriptions

Bit	Field	Type	Reset	Description
7–0	VENDORID[7:0]	R	00100010	Vendor identification register

6.6.2 *DEVICEID: PMIC Device and Revision ID Register (offset = 01h) [reset = OTP Dependent]*

Figure 6-20. DEVICEID Register (offset = 01h) [reset = OTP Dependent]

Bit	7	6	5	4	3	2	1	0
Bit Name	REVID[1]	REVID[0]	OTP_ VERSION[1]	OTP_ VERSION[0]	PART_ NUMBER[3]	PART_ NUMBER[2]	PART_ NUMBER[1]	PART_ NUMBER[0]
TPS650940	0	0	0	0	1	0	0	0
TPS650941	0	0	1	0	1	0	0	1
TPS650942	0	0	0	1	1	0	1	0
TPS650944	0	0	0	0	1	1	0	0
TPS650945	0	0	0	0	1	1	0	1
Access	R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6-13. DEVICEID Register Field Descriptions

Bit	Field	Type	Reset	Description
7–6	REVID[1:0]	R	OTP	Silicon revision ID
5–4	OTP_VERSION[1:0]	R	OTP	OTP variation ID **00**: A **01**: B **10**: C **11**: D
3–0	PART_NUMBER[3:0]	R	OTP	Device part number ID **1000**: TPS650940 **1001**: TPS650941 **1010**: TPS650942 **1011**: TPS650943 **1100**: TPS650944 **1101**: TPS650945 **1110**: TPS650946 **1111**: TPS650947 **0000**: TPS650948

6.6.3 IRQ: PMIC Interrupt Register (offset = 02h) [reset = 0000 0000]

Figure 6-21. IRQ Register (offset = 02h) [reset = 0000 0000]

Bit	7	6	5	4	3	2	1	0
Bit Name	VENDOR_ IRQ	RESERVED	RESERVED	RESERVED	ONOFFSRC	RESERVED	RESERVED	DIETEMP
TPS65094x	0	0	0	0	0	0	0	0
Access	R/W	R	R	R	R/W	R	R	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6-14. IRQ Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VENDOR_IRQ	R/W	0	Vendor-specific interrupt, indicating fault event occurrence. Asserted when either one of following conditions occurs: A. Deassertion of Power Good of any VR B. Overcurrent detection from BUCK1, BUCK2, BUCK6, or VTT LDO C. Die temperature crosses over the hot temperature threshold (T_{HOT}) D. Die temperature crosses over the critical temperature threshold (T_{CRIT}) **0**: Not asserted **1**: Asserted. Host to write 1 to clear.
3	ONOFFSRC	R/W	0	Asserted when PMIC shuts down. **0**: Not asserted. **1**: Asserted. Host to write 1 to clear.
0	DIETEMP	R/W	0	Die Temp interrupt. Asserted when PMIC die temperature crosses above the hot temperature threshold (T_{HOT}). **0**: Not asserted. **1**: Asserted. Host to write 1 to clear.

6.6.4 IRQ_MASK: PMIC Interrupt Mask Register (offset = 03h) [reset = 1111 1111]

Figure 6-22. IRQ_MASK Register (offset = 03h) [reset = 1111 1111]

Bit	7	6	5	4	3	2	1	0
Bit Name	MVENDOR_IRQ	RESERVED	RESERVED	RESERVED	MONOFFSRC	RESERVED	RESERVED	MDIETEMP
TPS65094x	1	1	1	1	1	1	1	1
Access	R/W	R	R	R	R/W	R	R	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6-15. IRQ_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MVENDOR_IRQ	R/W	1	Vendor-specific fault interrupt mask. **0**: Not masked **1**: Masked
3	MONOFFSRC	R/W	1	PMIC shutdown event interrupt mask **0**: Not masked **1**: Masked
0	MDIETEMP	R/W	1	Die temp interrupt mask. **0**: Not masked **1**: Masked

6.6.5 PMICSTAT: PMIC Status Register (offset = 04h) [reset = 0000 0000]

Figure 6-23. PMICSTAT Register (offset = 04h) [reset = 0000 0000]

Bit	7	6	5	4	3	2	1	0
Bit Name	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	SDIETEMP
TPS65094x	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6-16. PMICSTAT Register Field Descriptions

Bit	Field	Type	Reset	Description
0	SDIETEMP	R	0	PMIC die temperature status. **0**: PMIC die temperature is below T_{HOT}. **1**: PMIC die temperature is above T_{HOT}.

6.6.6 OFFONSRC: PMIC Power Transition Event Register (offset = 05h) [reset = 0000 0000]

Figure 6-24. OFFONSRC Register (offset = 05h) [reset = 0000 0000]

Bit	7	6	5	4	3	2	1	0
Bit Name	RESERVED	RESERVED	RESERVED	RESERVED	COLDOFF	UVLO	OCP	CRITTEMP
TPS65094x	0	0	0	0	0	0	0	0
Access	R	R	R	R	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6-17. OFFONSRC Register Field Descriptions

Bit	Field	Type	Reset	Description
3	COLDOFF	R/W	0	Set by PMIC cleared by host. Host writes 1 to this bit to clear it. **0** = Cleared **1** = PMIC was shut down by host through PMIC_EN pin.
2	UVLO	R/W	0	Set by PMIC cleared by host. Host writes 1 to this bit to clear it. **0** = Cleared **1** = PMIC was shut down due to a UVLO event (VSYS less 5.4 V). The setting of this bit sets the ONOFFSRC bit in the PMIC_IRQ register.
1	OCP	R/W	0	Set by PMIC cleared by host. Host writes 1 to this bit to clear it. **0** = Cleared **1** = PMIC shut down due to a power fault event. The setting of this bit sets the ONOFFSRC bit in the PMIC_IRQ register.
0	CRITTEMP	R/W	0	Set by PMIC cleared by host. Host writes 1 to this bit to clear it. **0** = Cleared **1** = PMIC shut down due to the rise of PMIC die temperature above critical temperature threshold (T_{CRIT}). The setting of this bit sets the ONOFFSRC bit in the PMIC_IRQ register.

6.6.7 BUCK1CTRL: BUCK1 Control Register (offset = 20h) [reset = 0011 1000]

Figure 6-25. BUCK1CTRL Register (offset = 20h) [reset = 0011 1000]

Bit	7	6	5	4	3	2	1	0
Bit Name	RESERVED	BUCK1_VID[6]	BUCK1_VID[5]	BUCK1_VID[4]	BUCK1_VID[3]	BUCK1_VID[2]	BUCK1_VID[1]	BUCK1_VID[0]
TPS65094x	0	0	1	1	1	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6-18. BUCK1CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
6–0	BUCK1_VID[6:0]	R/W	0111000 (1.05 V)	This field sets the BUCK1 regulator output regulation voltage in normal mode. Default = 1.05 V. Note that 0 V is a valid setting and all Power Goods stay high when VID is set to 0x00 and (or) SLP_S0B goes low. See Table 6-3 for full details.

6.6.8 BUCK2CTRL: BUCK2 Control Register (offset = 21h) [reset = 0000 0000]

Figure 6-26. BUCK2CTRL Register (offset = 21h) [reset = 0000 0000]

Bit	7	6	5	4	3	2	1	0
Bit Name	RESERVED	BUCK2_VID[6]	BUCK2_VID[5]	BUCK2_VID[4]	BUCK2_VID[3]	BUCK2_VID[2]	BUCK2_VID[1]	BUCK2_VID[0]
TPS65094x	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6-19. BUCK2CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
6–0	BUCK2_VID[6:0]	R/W	0000000 (0 V)	This field sets the BUCK2 regulator output regulation voltage in normal mode. Default = 0 V. Note that 0 V is a valid setting and all Power Goods must stay high when VID is set to 0x00 and (or) SLP_S0B goes low. See Table 6-3 for full details.

6.6.9 BUCK3CTRL: BUCK3 Control Register (offset = 23h) [reset = 0001 0001]

Figure 6-27. BUCK3CTRL Register (offset = 23h) [reset = 0001 0001]

Bit	7	6	5	4	3	2	1	0
Bit Name	RESERVED	BUCK3_VID[6]	BUCK3_VID[5]	BUCK3_VID[4]	BUCK3_VID[3]	BUCK3_VID[2]	BUCK3_VID[1]	BUCK3_VID[0]
TPS65094x	0	0	0	1	0	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6-20. BUCK3CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
6–0	BUCK3_VID[6:0]	R/W	0010001 (1.05 V)	This field sets the BUCK3 regulator output regulation voltage in normal mode. Default = 1.05 V. Note that 0 V is a valid setting and all Power Goods must stay high when VID is set to 0x00 and (or) SLP_S0B goes low. See Table 6-4 for full details.

6.6.10 BUCK4CTRL: BUCK4 Control Register (offset = 25h) [reset = 0011 1101]

Figure 6-28. BUCK4CTRL Register (offset = 25h) [reset = 0011 1101]

Bit	7	6	5	4	3	2	1	0
Bit Name	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	BUCK4_MODE	RESERVED
TPS650940, TPS650941, TPS65942, and TPS650944	0	0	1	1	1	1	0	1
TPS650945	0	0	1	1	1	1	1	1
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6-21. BUCK4CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
1	BUCK4_MODE	R/W	0	This field sets the BUCK4 regulator operating mode. **0** = Automatic mode **1** = Forced PWM mode

6.6.11 BUCK5CTRL: BUCK5 Control Register (offset = 26h) [reset = 0011 1101]

Figure 6-29. BUCK5CTRL Register (offset = 26h) [reset = 0011 1101]

Bit	7	6	5	4	3	2	1	0
Bit Name	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	BUCK5_MODE	RESERVED
TPS650940, TPS650941, TPS65942, and TPS650944	0	0	1	1	1	1	0	1
TPS650945	0	0	1	1	1	1	1	1
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6-22. BUCK5CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
1	BUCK5_MODE	R/W	0	This field sets the BUCK5 regulator operating mode. **0** = Automatic mode **1** = Forced PWM mode

6.6.12 BUCK6CTRL: BUCK6 Control Register (offset = 27h) [reset = 0011 1101]

Figure 6-30. BUCK6CTRL Register (offset = 27h) [reset = 0011 1101]

Bit	7	6	5	4	3	2	1	0
Bit Name	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	BUCK6_MODE	RESERVED
TPS65094x	0	0	1	1	1	1	0	1
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6-23. BUCK6CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
1	BUCK6_MODE	R/W	0	This field sets the BUCK6 regulator operating mode. **0** = Automatic mode **1** = Forced PWM mode

6.6.13 DISCHCNT1: Discharge Control1 Register (offset = 40h) [reset = 0101 0101]

All xx_DIS[1:0] bits automatically set to 00 when the corresponding VR is enabled. Discharge resistance values listed here are approximate.

Figure 6-31. DISCHCNT1 Register (offset = 40h) [reset = 0101 0101]

Bit	7	6	5	4	3	2	1	0
Bit Name	BUCK4_DIS[1]	BUCK4_DIS[0]	BUCK3_DIS[1]	BUCK3_DIS[0]	BUCK2_DIS[1]	BUCK2_DIS[0]	BUCK1_DIS[1]	BUCK1_DIS[0]
TPS65094x	0	1	0	1	0	1	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6-24. DISCHCNT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7–6	BUCK4_DIS[1:0]	R/W	01	BUCK4 discharge resistance **00**: No discharge **01**: 100 Ω **10**: 200 Ω **11**: 500 Ω
5–4	BUCK3_DIS[1:0]	R/W	01	BUCK3 discharge resistance **00**: No discharge **01**: 100 Ω **10**: 200 Ω **11**: 500 Ω
3–2	BUCK2_DIS[1:0]	R/W	01	BUCK2 discharge resistance **00**: No discharge **01**: 100 Ω **10**: 200 Ω **11**: 500 Ω
1–0	BUCK1_DIS[1:0]	R/W	01	BUCK1 discharge resistance **00**: No discharge **01**: 100 Ω **10**: 200 Ω **11**: 500 Ω

6.6.14 DISCHCNT2: Discharge Control2 Register (offset = 41h) [reset = 0101 0101]

All xx_DIS[1:0] bits automatically set to 00 when the corresponding VR is enabled. Discharge resistance values listed here are approximate.

Figure 6-32. DISCHCNT2 Register (offset = 41h) [reset = 0101 0101]

Bit	7	6	5	4	3	2	1	0
Bit Name	LDOA2_DIS[1]	LDOA2_DIS[0]	SWA1_DIS[1]	SWA1_DIS[0]	BUCK6_DIS[1]	BUCK6_DIS[0]	BUCK5_DIS[1]	BUCK5_DIS[0]
TPS65094x	0	1	0	1	0	1	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6-25. DISCHCNT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7–6	LDOA2_DIS[1:0]	R/W	01	LDOA2 discharge resistance **00**: No discharge **01**: 100 Ω **10**: 200 Ω **11**: 500 Ω
5–4	SWA1_DIS[1:0]	R/W	01	SWA1 discharge resistance **00**: No discharge **01**: 100 Ω **10**: 200 Ω **11**: 500 Ω
3–2	BUCK6_DIS[1:0]	R/W	01	BUCK6 discharge resistance **00**: No discharge **01**: 100 Ω **10**: 200 Ω **11**: 500 Ω
1–0	BUCK5_DIS[1:0]	R/W	01	BUCK5 discharge resistance **00**: No discharge **01**: 100 Ω **10**: 200 Ω **11**: 500 Ω

6.6.15 DISCHCNT3: Discharge Control3 Register (offset = 42h) [reset = 0000 0101]

All xx_DIS[1:0] bits automatically set to 00 when the corresponding VR is enabled. Discharge resistance values listed here are approximate.

Figure 6-33. DISCHCNT3 Register (offset = 42h) [reset = 0000 0101]

Bit	7	6	5	4	3	2	1	0
Bit Name	RESERVED	RESERVED	RESERVED	RESERVED	SWB1_DIS[1]	SWB1_DIS[0]	LDOA3_DIS[1]	LDOA3_DIS[0]
TPS65094x	0	0	0	0	0	1	0	1
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6-26. DISCHCNT3 Register Field Descriptions

Bit	Field	Type	Reset	Description
3–2	SWB1_DIS[1:0]	R/W	01	SWB1 discharge resistance **00**: No discharge **01**: 100 Ω **10**: 200 Ω **11**: 500 Ω
1–0	LDOA3_DIS[1:0]	R/W	01	LDOA3 discharge resistance **00**: No discharge **01**: 100 Ω **10**: 200 Ω **11**: 500 Ω

6.6.16 POK_DELAY: PCH_PWROK Delay Register (offset = 43h) [reset = 0000 0111]

Programmable Power Good delay for PCH_PWROK pin, measured from the moment when all VRs reach the regulation range to Power Good assertion.

Figure 6-34. POK_DELAY Register (Offset = 43h) [reset = 0000 0111]

Bit	7	6	5	4	3	2	1	0
Bit Name	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	PWROKDELAY [2]	PWROKDELAY [1]	PWROKDELAY [0]
TPS65094x	0	0	0	0	0	1	1	1
Access	R	R	R	R	R	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6-27. POK_DELAY Register Field Descriptions

Bit	Field	Type	Reset	Description
2–0	PWROKDELAY[2:0]	R/W	111	Programmable delay measured from the moment all rails have reached regulation voltage to assertion of PCH_PWROK. All values have ±10% variation. **000** = 2.5 ms **001** = 5.0 ms **010** = 10 ms **011** = 15 ms **100** = 20 ms **101** = 50 ms **110** = 75 ms **111** = 100 ms (default)

6.6.17 FORCESHUTDN: Force Emergency Shutdown Control Register (offset = 91h) [reset = 0000 0000]

Figure 6-35. FORCESHUTDN Register (offset = 91h) [reset = 0000 0000]

Bit	7	6	5	4	3	2	1	0
Bit Name	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	SDWN
TPS65094x	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6-28. FORCESHUTDN Register Field Descriptions

Bit	Field	Type	Reset	Description
0	SDWN	R/W	0	Forces reset of the PMIC. The bit is self-clearing. **0** = No action **1** = PMIC is forced to shut down.

6.6.18 BUCK4VID: BUCK4 VID Register (offset = 94h) [reset = 0010 1111]

Figure 6-36. BUCK4VID Register (offset = 94h) [reset = 0010 1111]

Bit	7	6	5	4	3	2	1	0
Bit Name	RESERVED	BUCK4_VID[6]	BUCK4_VID[5]	BUCK4_VID[4]	BUCK4_VID[3]	BUCK4_VID[2]	BUCK4_VID[1]	BUCK4_VID[0]
TPS65094x	0	0	1	0	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6-29. BUCK4VID Register Field Descriptions

Bit	Field	Type	Reset	Description
6–0	BUCK4_VID[6:0]	R/W	0101111 (1.80 V)	This field sets the BUCK4 regulator output regulation voltage in normal mode. Default = 1.80 V. Note that 0 V is a valid setting and all Power Goods must stay high when VID is set to 0x00. See Table 6-4 for full details.

6.6.19 BUCK5VID: BUCK5 VID Register (offset = 96h) [reset = 0100 1011]

Figure 6-37. BUCK5VID Register (Offset = 96h) [reset = 0100 1011]

Bit	7	6	5	4	3	2	1	0
Bit Name	RESERVED	BUCK5_VID[6]	BUCK5_VID[5]	BUCK5_VID[4]	BUCK5_VID[3]	BUCK5_VID[2]	BUCK5_VID[1]	BUCK5_VID[0]
TPS65094x	0	1	0	0	1	0	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6-30. BUCK5VID Register Field Descriptions

Bit	Field	Type	Reset	Description
6–0	BUCK5_VID[6:0]	R/W	1001011 (1.24 V)	This field sets the BUCK5 regulator output regulation voltage in normal mode. Default = 1.24 V. Note that 0 V is a valid setting and all Power Goods stay high when VID is set to 0x00. See Table 6-3 for full details.

6.6.20 BUCK6VID: BUCK6 VID Register (offset = 98h) [reset = OTP Dependent]

Figure 6-38. BUCK6VID Register (Offset = 98h) [reset = OTP Dependent]

Bit	7	6	5	4	3	2	1	0
Bit Name	RESERVED	BUCK6_VID[6]	BUCK6_VID[5]	BUCK6_VID[4]	BUCK6_VID[3]	BUCK6_VID[2]	BUCK6_VID[1]	BUCK6_VID[0]
TPS650940, TPS650944 and TPS650945	0	0	1	1	1	1	0	1
TPS650941	0	1	0	0	0	1	1	1
TPS650942	0	1	0	1	0	1	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6-31. BUCK6VID Register Field Descriptions

Bit	Field	Type	Reset	Description
6–0	BUCK6_VID[6:0]	R/W	TPS650940, TPS650944, and TPS650945: 0111101 (1.1 V) TPS650941: 1000111 (1.20 V) TPS650942: 1010110 (1.35 V)	This field sets the BUCK6 regulator output regulation voltage in normal mode. Default = OTP Dependent. Note that 0 V is a valid setting and all Power Goods stay high when VID is set to 0x00. See Table 6-3 for full details.

6.6.21 LDOA2VID: LDOA2 VID Register (offset = 9Ah) [reset = OTP Dependent]

LDOA2_SLPVID is used when SLP_S0B is low. Keep LDOA2_SLPVID equal to LDOA2_VID if sleep functionality is not desired.

Figure 6-39. LDOA2VID Register (offset = 9Ah) [reset = OTP Dependent]

Bit	7	6	5	4	3	2	1	0
Bit Name	LDOA2_ SLPVID[1]	LDOA2_ SLPVID[2]	LDOA2_ SLPVID[1]	LDOA2_ SLPVID[0]	LDOA2_VID[3]	LDOA2_VID[2]	LDOA2_VID[1]	LDOA2_VID[0]
TPS650940, TPS650941, TPS650942, and TPS650945	1	0	1	0	1	0	1	0
TPS650944	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6-32. LDOA2VID Register Field Descriptions

Bit	Field	Type	Reset	Description
7–4	LDOA2_SLPVID[3:0]	R/W	TPS650940, TPS650941, TPS650942, and TPS650945: 1010 (1.2 V) TPS650944: 0000 (0.7 V)	This field sets the LDOA2 regulator output regulation voltage in sleep mode. Default = OTP Dependent. See Table 6-6 for full details.
3–0	LDOA2_VID[3:0]	R/W	TPS650940, TPS650941, TPS650942, and TPS650945: 1010 (1.2 V) TPS650944: 0000 (0.7 V)	This field sets the LDOA2 regulator output regulation voltage in normal mode. Default = OTP Dependent. See Table 6-6 for full details.

6.6.22 LDOA3VID: LDOA3 VID Register (offset = 9Bh) [reset = OTP Dependent]

LDOA3_SLPVID is used when SLP_S0B is low. Keep LDOA3_SLPVID equal to LDOA3_VID if sleep functionality is not desired.

Figure 6-40. LDOA3VID Register (offset = 9Bh) [reset = OTP Dependent]

Bit	7	6	5	4	3	2	1	0
Bit Name	LDOA3_ SLPVID[3]	LDOA3_ SLPVID[2]	LDOA3_ SLPVID[1]	LDOA3_ SLPVID[0]	LDOA3_VID[3]	LDOA3_VID[2]	LDOA3_VID[1]	LDOA3_VID[0]
TPS650940, TPS650941, TPS650942, and TPS650945	1	0	1	1	1	0	1	1
TPS650944	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6-33. LDOA3VID Register Field Descriptions

Bit	Field	Type	Reset	Description
7–4	LDOA3_SLPVID[3:0]	R/W	TPS650940, TPS650941, TPS650942, and TPS650945: 1011 (1.25 V) TPS650944: 0000 (0.7 V)	This field sets the LDOA3 regulator output regulation voltage in sleep mode. Default = OTP Dependent. See Table 6-6 for full details.
3–0	LDOA3_VID[3:0]	R/W	TPS650940, TPS650941, TPS650942, and TPS650945: 1011 (1.25 V) TPS650944: 0000 (0.7 V)	This field sets the LDOA3 regulator output regulation voltage in normal mode. Default = OTP Dependent. See Table 6-6 for full details.

6.6.23 VR_CTRL1: BUCK1-3 Control Register (offset = 9Ch) [reset = 0000 0111]

Figure 6-41. VR_CTRL1 Register (offset = 9Ch) [reset = 0000 0111]

Bit	7	6	5	4	3	2	1	0
Bit Name	RESERVED	RESERVED	BUCK3_MODE	BUCK2_MODE	BUCK1_MODE	BUCK3_ DISABLEB	BUCK2_ DISABLEB	BUCK1_ DISABLEB
TPS650940, TPS650941, TPS650942, and TPS650944	0	0	0	0	0	1	1	1
TPS650945	0	0	1	0	0	1	1	1
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6-34. VR_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
5	BUCK3_MODE	R/W	0	This field sets the BUCK3 regulator operating mode. **0** = Automatic mode **1** = Forced PWM mode
4	BUCK2_MODE	R/W	0	This field sets the BUCK2 regulator operating mode. **0** = Automatic mode **1** = Forced PWM mode
3	BUCK1_MODE	R/W	0	This field sets the BUCK1 regulator operating mode. **0** = Automatic mode **1** = Forced PWM mode
2	BUCK3_DISABLEB	R/W	1	BUCK3 Active Low Disable bit. Writing 0 to this bit forces BUCK3 to turn off regardless of status of enable pins (PMICEN, SLP_Sx). Has priority over BUCK3_EN. **0**: Disabled **1**: BUCK3 operates normally.
1	BUCK2_DISABLEB	R/W	1	BUCK2 Active Low Disable bit. Writing 0 to this bit forces BUCK2 to turn off regardless of status of enable pins (PMICEN, SLP_Sx). Has priority over BUCK2_EN. **0**: Disabled **1**: BUCK2 operates normally.
0	BUCK1_DISABLEB	R/W	1	BUCK1 Active Low DISABLE bit. Writing 0 to this bit forces BUCK1 to turn off regardless of status of enable pins (PMICEN, SLP_Sx). Has priority over BUCK1_EN. **0**: Disabled **1**: BUCK1 operates normally.

6.6.24 VR_CTRL2: VR Enable Register (offset = 9Eh) [reset = 0000 0000]

Figure 6-42. VR_CTRL2 Register (offset = 9Eh) [reset = 0000 0000]

Bit	7	6	5	4	3	2	1	0
Bit Name	LDOA2_EN	SWA1_EN	BUCK6_EN	BUCK5_EN	BUCK4_EN	BUCK3_EN	BUCK2_EN	BUCK1_EN
TPS65094x	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6-35. VR_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDOA2_EN	R/W	0	LDOA2 Enable bit. **0**: Enabled if LDOLS_EN = 1 **1**: Enabled regardless of LDOLS_EN state
6	SWA1_EN	R/W	0	SWA1 Enable bit. **0**: Enabled if LDOLS_EN pin or SWA1_EN pin = 1 **1**: Enabled regardless of LDOLS_EN or SWA1_EN state

Table 6-35. VR_CTRL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	BUCK6_EN	R/W	0	BUCK6 Enable bit. **0**: BUCK6 operates normally. **1**: Enabled regardless of power sequencing
4	BUCK5_EN	R/W	0	BUCK5 Enable bit. **0**: BUCK5 operates normally. **1**: Enabled regardless of power sequencing
3	BUCK4_EN	R/W	0	BUCK4 Enable bit. **0**: BUCK4 operates normally. **1**: Enabled regardless of power sequencing
2	BUCK3_EN	R/W	0	BUCK3 Enable bit. BUCK3_DISABLEB has priority over BUCK3_EN. **0**: BUCK3 operates normally. **1**: Enabled regardless of power sequencing, unless BUCK3_DISABLEB = 0
1	BUCK2_EN	R/W	0	BUCK2 Enable bit. BUCK2_DISABLEB has priority over BUCK2_EN. **0**: BUCK2 operates normally. **1**: Enabled regardless of power sequencing, unless BUCK2_DISABLEB = 0
0	BUCK1_EN	R/W	0	BUCK1 Enable bit. BUCK1_DISABLEB has priority over BUCK1_EN. **0**: BUCK1 operates normally. **1**: Enabled regardless of power sequencing, unless BUCK1_DISABLEB = 0

6.6.25 VR_CTRL3: VR Enable/Disable Register (offset = 9Fh) [reset = 0111 0000]

Figure 6-43. VR_CTRL3 Register (Offset = 9Fh) [reset = 0111 0000]

Bit	7	6	5	4	3	2	1	0
Bit Name	RESERVED	SWB1_2_ DISABLEB	SWA1_ DISABLEB	VTT_ DISABLEB	VTT_EN	RESERVED	SWB1_2_EN	LDOA3_EN
TPS650940, TPS650944, and TPS650945	0	1	1	0	1	0	0	0
TPS650941 and TPS650942	0	1	1	1	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6-36. VR_CTRL3 Register Field Descriptions

Bit	Field	Type	Reset	Description
6	SWB1_2_DISABLEB	R/W	1	SWB1_2 Active Low Disable Bit. Writing 0 to this bit forces SWB1_2 to turn off regardless of status of enable pins (PMICEN, SLP_Sx). Has priority over SWB1_2_EN. **0**: Disabled **1**: SWB1_2 operates normally.
5	SWA1_DISABLEB	R/W	1	SWA1 Active Low Disable Bit. Writing 0 to this bit forces SWA1 to turn off regardless of status of enable pins (PMICEN, SLP_Sx). Has priority over SWA1_EN. **0**: Disabled **1**: SWA1 operates normally.
4	VTT_DISABLEB	R/W	TPS650940, TPS650944, and TPS650945: 0 TPS650941 and TPS650942: 1	VTT_LDO Active Low Disable Bit. Writing 0 to this bit forces VTT_LDO to turn off regardless of status of enable pins (PMICEN, SLP_Sx). Has priority over VTT_EN. **0**: Disabled **1**: VTT_LDO operates normally.
3	VTT_EN	R/W	TPS650940, TPS650944 and TPS650945: 1 TPS650941 and TPS650942: 0	VTT_LDO Enable bit. VTT_DISABLEB has priority over VTT_EN. **0**: VTT_LDO operates normally. **1**: Enabled regardless of power sequencing, unless VTT_DISABLEB = 0
1	SWB1_2_EN	R/W	0	SWB1_2_Enable bit. SWB1_2_DISABLEB has priority over SWB1_2_EN. **0**: SWB1_2 operates normally. **1**: Enabled regardless of power sequencing, unless SWB1_2_DISABLEB = 0
0	LDOA3_EN	R/W	0	LDOA3 Enable bit. **0**: Enabled if LDOLS_EN = 1 **1**: Enabled regardless of LDOLS_EN state

6.6.26 GPO_CTRL: GPO Control Register (offset = A1h) [reset = 0010 0000]

Figure 6-44. GPO_CTRL Register (offset = A1h) [reset = 0010 0000]

Bit	7	6	5	4	3	2	1	0
Bit Name	RESERVED	RESERVED	GPO_LVL	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
TPS65094x	0	0	1	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6-37. GPO_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
5	GPO_LVL	R/W	1	Open-drain GPO output level bit. **0**: The pin is driven to logic low. **1**: The pin is high impedance.

6.6.27 PWR_FAULT_MASK1: VR Power Fault Mask1 Register (offset = A2h) [reset = 1100 0000]

Figure 6-45. PWR_FAULT_MASK1 Register (offset = A2h) [reset = 1100 0000]

Bit	7	6	5	4	3	2	1	0
Bit Name	LDOA2_ FLTMSK	SWA1_ FLTMSK	BUCK6_ FLTMSK	BUCK5_ FLTMSK	BUCK4_ FLTMSK	BUCK3_ FLTMSK	BUCK2_ FLTMSK	BUCK1_ FLTMSK
TPS65094x	1	1	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6-38. PWR_FAULT_MASK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDOA2_FLTMSK	R/W	1	LDOA2 Power Fault Mask. When masked, power fault from LDOA2 does not cause PMIC shutdown. **0**: Not masked **1**: Masked
6	SWA1_FLTMSK	R/W	1	SWA1 Power Fault Mask. When masked, power fault from SWA1 does not cause PMIC shutdown. **0**: Not masked **1**: Masked
5	BUCK6_FLTMSK	R/W	0	BUCK6 Power Fault Mask. When masked, power fault from BUCK6 does not cause PMIC shutdown. **0**: Not masked **1**: Masked
4	BUCK5_FLTMSK	R/W	0	BUCK5 Power Fault Mask. When masked, power fault from BUCK5 does not cause PMIC shutdown. **0**: Not masked **1**: Masked
3	BUCK4_FLTMSK	R/W	0	BUCK4 Power Fault Mask. When masked, power fault from BUCK4 does not cause PMIC shutdown. **0**: Not masked **1**: Masked
2	BUCK3_FLTMSK	R/W	0	BUCK3 Power Fault Mask. When masked, power fault from BUCK3 does not cause PMIC shutdown. **0**: Not masked **1**: Masked
1	BUCK2_FLTMSK	R/W	0	BUCK2 Power Fault Mask. When masked, power fault from BUCK2 does not cause PMIC shutdown. **0**: Not masked **1**: Masked
0	BUCK1_FLTMSK	R/W	0	BUCK1 Power Fault Mask. When masked, power fault from BUCK1 does not cause PMIC shutdown. **0**: Not masked **1**: Masked

6.6.28 PWR_FAULT_MASK2: VR Power Fault Mask2 Register (offset = A3h) [reset = 0011 0111]

Figure 6-46. PWR_FAULT_MASK2 Register (offset = A3h) [reset = 0011 0111]

Bit	7	6	5	4	3	2	1	0
Bit Name	RESERVED	RESERVED	V5ANA_ FLTMSK	LDOA1_ FLTMSK	VTT_ FLTMSK	SWB1_2_ FLTMSK[1]	SWB1_2_ FLTMSK[0]	LDOA3_ FLTMSK
TPS65094x	0	0	1	1	0	1	1	1
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6-39. PWR_FAULT_MASK2 Register Field Descriptions

Bit	Field	Type	Reset	Description
5	V5ANA_FLTMSK	R/W	1	V5ANA Power Fault Mask. When masked, power fault from V5ANA does not cause PMIC shutdown. **0**: Not masked **1**: Masked
4	LDOA1_FLTMSK	R/W	1	LDOA1 Power Fault Mask. When masked, power fault from LDOA1 does not cause PMIC shutdown. **0**: Not masked **1**: Masked
3	VTT_FLTMSK	R/W	0	VTT LDO Power Fault Mask. When masked, power fault from VTT LDO does not cause PMIC shutdown. **0**: Not Masked **1**: Masked
2–1	SWB1_2_FLTMSK	R/W	11	SWB1_2 Power Fault Mask. When masked, power fault from SWB1_2 does not cause PMIC shutdown. **00**: Not masked **11**: Masked **01-10** = RESERVED
0	LDOA3_FLTMSK	R/W	1	LDOA3 Power Fault Mask. When masked, power fault from LDOA3 does not cause PMIC shutdown. **0**: Not masked **1**: Masked

6.6.29 DISCHCNT4: Discharge Control4 Register (offset = ADh) [reset = 0110 0001]

Figure 6-47. DISCHCNT4 Register (offset = ADh) [reset = 0110 0001]

Bit	7	6	5	4	3	2	1	0
Bit Name	RESERVED	RESERVED	RESERVED	VTT_DIS	RESERVED	RESERVED	RESERVED	RESERVED
TPS65094x	0	1	1	0	0	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6-40. DISCHNT4 Register Field Descriptions

Bit	Field	Type	Reset	Description
4	VTT_DIS	R/W	0	VTT_LDO discharge resistance **0** = No discharge **1** = 100 Ω

6.6.30 LDOA1CTRL: LDOA1 Control Register (offset = AEh) [reset = OTP Dependent]

Figure 6-48. LDOA1CTRL Register (offset = AEh) [reset = OTP Dependent]

Bit	7	6	5	4	3	2	1	0
Bit Name	LDOA1_DIS[1]	LDOA1_DIS[0]	LDOA1_SDWN_CONFIG	LDOA1_VID[3]	LDOA1_VID[2]	LDOA1_VID[1]	LDOA1_VID[0]	LDOA1_EN
TPS650940, TPS650941, TPS650942, and TPS650945	0	1	1	1	1	1	0	0
TPS650944	0	1	1	0	1	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6-41. LDOA1CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7–6	LDOA1_DIS[1:0]	R/W	01	LDOA1 discharge resistance **00**: No discharge **01**: 100 Ω **10**: 200 Ω **11**: 500 Ω
5	LDOA1_SDWN_CONFIG	R/W	1	Control for Disabling LDOA1 during Emergency Shutdown **0**: LDOA1 will turn off during Emergency Shutdown. **1**: LDOA1 will not turn off during Emergency Shutdown as long as LDOA1_EN = 1.
4–1	LDOA1_VID[3:0]	R/W	TPS650940, TPS650941, TPS650942, and TPS650945: 1110 (3.3 V) TPS650944: 0100 (1.8V)	This field sets the LDOA3 regulator output regulation voltage in normal mode. Default = OTP Dependent. See Table 6-5 for full details.
0	LDOA1_EN	R/W	TPS650940, TPS650941, TPS650942, and TPS650945: 0 TPS650944: 1	LDOA1 Enable Bit. **0**: Disable **1**: Enable

6.6.31 PG_STATUS1: Power Good Status1 Register (offset = B0h) [reset = 0000 0000]

Figure 6-49. PG_STATUS1 Register (offset = B0h) [reset = 0000 0000]

Bit	7	6	5	4	3	2	1	0
Bit Name	LDOA2_PGOOD	RESERVED	BUCK6_PGOOD	BUCK5_PGOOD	BUCK4_PGOOD	BUCK3_PGOOD	BUCK2_PGOOD	BUCK1_PGOOD
TPS65094x	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6-42. PG_STATUS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDOA2_PGOOD	R	0	LDOA2 Power Good status. **0**: The output is not in target regulation range. **1**: The output is in target regulation range.
5	BUCK6_PGOOD	R	0	BUCK6 Power Good status. **0**: The output is not in target regulation range. **1**: The output is in target regulation range.

Table 6-42. PG_STATUS1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	BUCK5_PGOOD	R	0	BUCK5 Power Good status. **0**: The output is not in target regulation range. **1**: The output is in target regulation range.
3	BUCK4_PGOOD	R	0	BUCK4 Power Good status. **0**: The output is not in target regulation range. **1**: The output is in target regulation range.
2	BUCK3_PGOOD	R	0	BUCK3 Power Good status. **0**: The output is not in target regulation range. **1**: The output is in target regulation range.
1	BUCK2_PGOOD	R	0	BUCK2 Power Good status. **0**: The output is not in target regulation range. **1**: The output is in target regulation range.
0	BUCK1_PGOOD	R	0	BUCK1 Power Good status. **0**: The output is not in target regulation range. **1**: The output is in target regulation range.

6.6.32 PG_STATUS2: Power Good Status2 Register (offset = B1h) [reset = 0000 0000]

Figure 6-50. PG_STATUS2 Register (offset = B1h) [reset = 0000 0000]

Bit	7	6	5	4	3	2	1	0
Bit Name	RESERVED	RESERVED	LDO5_PGOOD	LDOA1_PGOOD	VTT_PGOOD	RESERVED	RESERVED	LDOA3_PGOOD
TPS65094x	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6-43. PG_STATUS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
5	LDO5_PGOOD	R	0	LDO5 Power Good status. **0**: The output is not in target regulation range. **1**: The output is in target regulation range.
4	LDOA1_PGOOD	R	0	LDOA1 Power Good status. **0**: The output is not in target regulation range. **1**: The output is in target regulation range.
3	VTT_PGOOD	R	0	VTT LDO Power Good status. **0**: The output is not in target regulation range. **1**: The output is in target regulation range.
0	LDOA3_PGOOD	R	0	LDOA3 Power Good status. **0**: The output is not in target regulation range. **1**: The output is in target regulation range.

6.6.32.1 PWR_FAULT_STATUS1: Power Fault Status1 Register (offset = B2h) [reset = 0000 0000]

Figure 6-51. PWR_FAULT_STATUS1 Register (offset = B2h) [reset = 0000 0000]

Bit	7	6	5	4	3	2	1	0
Bit Name	LDOA2_PWRFLT	RESERVED	BUCK6_PWRFLT	BUCK5_PWRFLT	BUCK4_PWRFLT	BUCK3_PWRFLT	BUCK2_PWRFLT	BUCK1_PWRFLT
TPS65094x	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6-44. PWR_FAULT_STATUS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDOA2_PWRFLT	R	0	This fields indicates that LDOA2 has lost regulation. **0**: No Fault. **1**: Power fault has occurred. The host to write 1 to clear.
5	BUCK6_PWRFLT	R	0	This fields indicates that BUCK6 has lost regulation. **0**: No Fault. **1**: Power fault has occurred. The host to write 1 to clear.
4	BUCK5_PWRFLT	R	0	This fields indicates that BUCK5 has lost regulation. **0**: No Fault. **1**: Power fault has occurred. The host to write 1 to clear.
3	BUCK4_PWRFLT	R	0	This fields indicates that BUCK4 has lost regulation. **0**: No Fault. **1**: Power fault has occurred. The host to write 1 to clear.
2	BUCK3_PWRFLT	R	0	This fields indicates that BUCK3 has lost regulation. **0**: No Fault. **1**: Power fault has occurred. The host to write 1 to clear.
1	BUCK2_PWRFLT	R	0	This fields indicates that BUCK2 has lost regulation. **0**: No Fault. **1**: Power fault has occurred. The host to write 1 to clear.
0	BUCK1_PWRFLT	R	0	This fields indicates that BUCK1 has lost regulation. **0**: No Fault. **1**: Power fault has occurred. The host to write 1 to clear.

6.6.32.2 PWR_FAULT_STATUS2: Power Fault Status2 Register (offset = B3h) [reset = 0000 0000]

Figure 6-52. PWR_FAULT_STATUS2 Register (offset = B3h) [reset = 0000 0000]

Bit	7	6	5	4	3	2	1	0
Bit Name	RESERVED	RESERVED	RESERVED	LDOA1_ PWRFLT	VTT_ PWRFLT	RESERVED	RESERVED	LDOA3_ PWRFLT
TPS65094x	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6-45. PWR_FAULT_STATUS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
4	LDOA1_PWRFLT	R/W	0	This fields indicates that LDOA1 has lost regulation. **0**: No Fault. **1**: Power fault has occurred. The host to write 1 to clear.
3	VTT_PWRFLT	R/W	0	This fields indicates that VTT LDO has lost regulation. **0**: No Fault. **1**: Power fault has occurred. The host to write 1 to clear.
0	LDOA3_PWRFLT	R/W	0	This fields indicates that LDOA3 has lost regulation. **0**: No Fault. **1**: Power fault has occurred. The host to write 1 to clear.

6.6.33 TEMPHOT: Temperature Hot Status Register (offset = B5h) [reset = 0000 0000]

Asserted when an internal temperature sensor detects rise of die temperature above the HOT temperature threshold (T_{HOT}). There are five temperature sensors across the die.

Figure 6-53. TEMPHOT Register (offset = B5h) [reset = 0000 0000]

Bit	7	6	5	4	3	2	1	0
Bit Name	RESERVED	RESERVED	RESERVED	DIE_HOT	VTT_HOT	TOP-RIGHT _HOT	TOP-LEFT _HOT	BOTTOM-RIGHT_HOT
TPS65094x	0	0	0	0	0	0	0	0
Access	R	R	R	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6-46. TEMPHOT Register Field Descriptions

Bit	Field	Type	Reset	Description
4	DIE_HOT	R/W	0	Temperature of rest of die has exceeded T_{HOT}. **0**: Not asserted. **1**: Asserted. The host to write 1 to clear.
3	VTT_HOT	R/W	0	Temperature of VTT LDO has exceeded T_{HOT}. **0**: Not asserted. **1**: Asserted. The host to write 1 to clear.
2	TOP-RIGHT_HOT	R/W	0	Temperature of die top-right has exceeded T_{HOT}. Top-right corner of die from top view given pin 1 is in top-left corner. **0**: Not asserted. **1**: Asserted. The host to write 1 to clear.
1	TOP-LEFT_HOT	R/W	0	Temperature of die top-left has exceeded T_{HOT}. Top-left corner of die from top view given pin 1 is in top-left corner. **0**: Not asserted. **1**: Asserted. The host to write 1 to clear.
0	BOTTOM-RIGHT_HOT	R/W	0	Temperature of die bottom-right has exceeded T_{HOT}. Bottom-right corner of die from top view given pin 1 is in top-left corner. **0**: Not asserted. **1**: Asserted. The host to write 1 to clear.

7 Application and Implementation

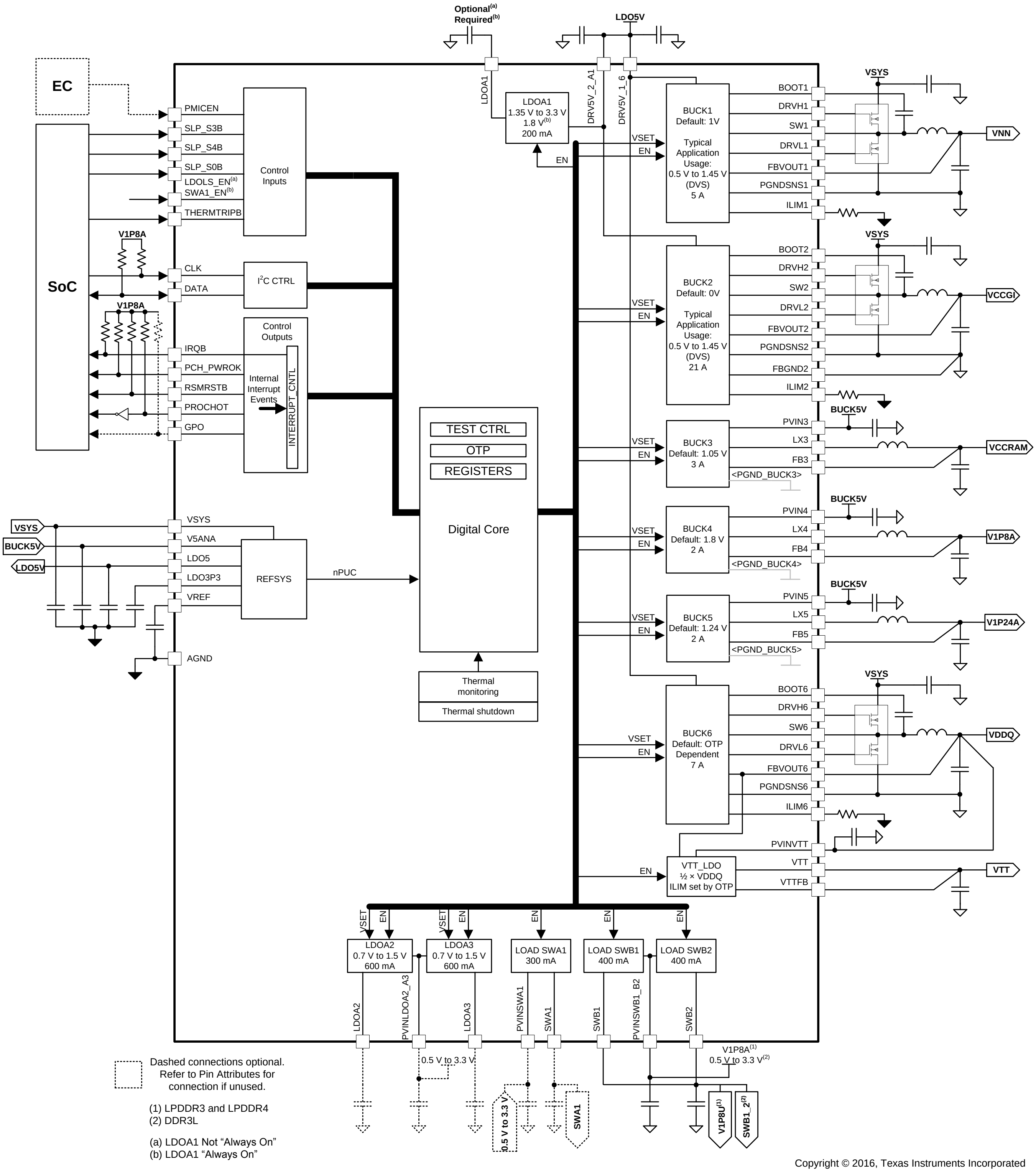
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

7.2 Typical Application

For a detailed description about application usage, refer to the *TPS65094x Design Guide* and to the *TPS65094x Schematic Checklist, Layout Checklist, and ILIM Calculator Tool*. The TPS65094x can be used in several different applications from computing, industrial interfacing, and much more. This section describes the general application information and provides a more detailed description on the TPS65094x device that powers the Intel Apollo Lake system. The functional block diagram for the device is shown in Figure 7-1, which outlines the typical external components necessary for proper device functionality.



Dashed connections optional. Refer to Pin Attributes for connection if unused.

(1) LPDDR3 and LPDDR4
(2) DDR3L

(a) LDOA1 Not "Always On"
(b) LDOA1 "Always On"

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Figure 7-1. Functional Block Diagram

7.2.1 Design Requirements

The TPS65094x device requires decoupling capacitors on the supply pins. Follow the values for recommended capacitance on these supplies given in the *Specifications* section. The controllers, converter, LDOs, and some other features can be adjusted to meet specific application requirements. Section 7.2.2, *Detailed Design Procedure,* describes how to design and adjust the external components to achieve desired performance.

7.2.2 Detailed Design Procedure

7.2.2.1 Controller Design Procedure

Designing the controller can be divided into the following steps:

1. Design the output filter.
2. Select the FETs.
3. Select the bootstrap capacitor.
4. Select the input capacitors.
5. Set the current limits.

Figure 7-2 shows a diagram of the controller. Controllers BUCK1, BUCK2, and BUCK6 require a 5-V supply and capacitors at their corresponding DRV5V_x_x pins. For most applications, the DRV5V_x_x input must come from the LDO5P0 pin to ensure uninterrupted supply voltage; a 2.2-µF, X5R, 20%, 10-V, or similar capacitor must be used for decoupling.

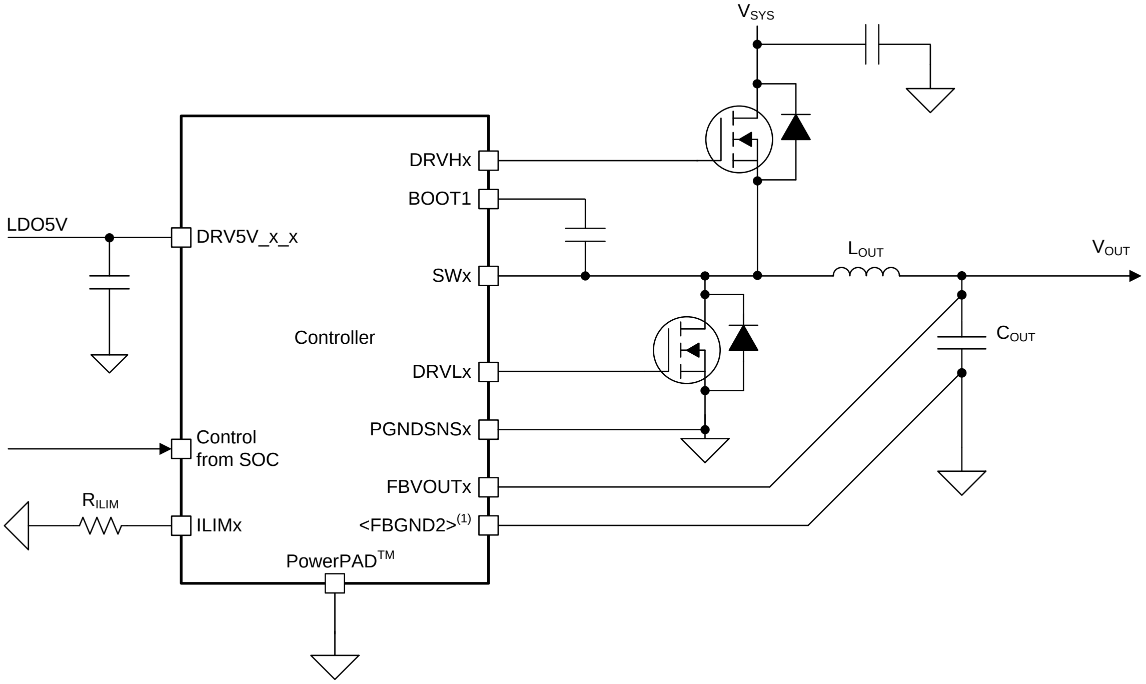


Figure 7-2. Controller Diagram

7.2.2.1.1 Selecting the Output Capacitors

TI recommends using ceramic capacitors with low ESR values to provide the lowest output voltage ripple. The output capacitor requires either an X7R or an X5R dielectric. Capacitors with Y5V or Z5U dielectrics display a wide variation in capacitance over temperature and become resistive at high frequencies.

At light load currents, the controller operates in PFM mode, and the output voltage ripple is dependent on the output-capacitor value and the PFM peak inductor current. Higher output-capacitor values minimize the voltage ripple in PFM mode. To achieve specified regulation performance and low output voltage ripple, the DC-bias characteristic of ceramic capacitors must be considered. The effective capacitance of ceramic capacitors drops with increasing DC bias voltage.

For the output capacitors of the BUCK controllers, TI recommends placing small ceramic capacitors between the inductor and load with many vias to the PGND plane. This solution typically provides the smallest and lowest cost solution available for DCAP2 controllers.

To meet the transient specifications, the output capacitance must equal or exceed the minimum capacitance listed in the electrical characteristics table for BUCK1, BUCK2, and BUCK6 (assuming quality layout techniques are followed). See Section 5.7, *Electrical Characteristics: Buck Controllers*.

7.2.2.1.2 Selecting the Inductor

An inductor must be placed between the external FETs and the output capacitors. Together, the inductor and output capacitors make the double-pole that contributes to stability. In addition, the inductor is responsible for the output ripple, efficiency, and transient performance. When the inductance increases, the ripple current decreases, which typically results in an increased efficiency. However, with an increase in inductance, the transient performance decreases. Finally, the inductor selected must be rated for appropriate saturation current, core losses, and DC resistance (DCR).

Equation 3 shows the calculation for the recommended inductance for the controller.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{sw} \times I_{OUT(MAX)} \times K_{IND}}$$

where

- V_{OUT} is the typical output voltage.
- V_{IN} is the typical input voltage.
- f_{SW} is the typical switching frequency.
- $I_{OUT(MAX)}$ is the maximum load current.
- K_{IND} is the ratio of $I_{Lripple}$ to the $I_{OUT(MAX)}$. For this application, TI recommends that K_{IND} is set to a value from 0.2 to 0.4. (3)

With the chosen inductance value and the peak current for the inductor in steady state operation, $I_{L(max)}$ can be calculated using Equation 4. The rated saturation current of the inductor must be higher than the $I_{L(MAX)}$ current.

$$I_{L(MAX)} = I_{OUT(MAX)} + \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times V_{IN} \times f_{sw} \times L} \tag{4}$$

Following the previous equations, Table 7-1 lists the preferred inductor selected for the controllers..

Table 7-1. Recommended Inductors

MANUFACTURER	PART NUMBER	VALUE	SIZE	HEIGHT
Cyntec	PIMB061H	0.47 µH	6.8 mm × 7.3 mm	1.8 mm
Cyntec	PIMB062D	0.22 µH	6.8 mm × 7.3 mm	2.4 mm

7.2.2.1.3 Selecting the FETs

This controller is designed to drive two NMOS FETs. Typically, lower R_{DSON} values are better for improving the overall efficiency of the controller. However, higher gate-charge thresholds result in lower efficiency, so the two must be balanced for optimal performance. As the R_{DSON} for the low-side FET decreases, the minimum current limit increases; therefore, ensure selection of the appropriate values for the FETs, inductor, output capacitors, and current-limit resistor. TI's CSD87331Q3D, CSD87381P, and CSD87588N devices are recommended for the controllers, depending on the required maximum current.

7.2.2.1.4 Bootstrap Capacitor

To ensure the internal high-side gate drivers are supplied with a stable low-noise supply voltage, a capacitor must be connected between the SWx pins and the respective BOOTx pins. TI recommends placing ceramic capacitors with the value of 0.1 µF for the controllers. During testing, a 0.1-µF, size 0402, 10-V capacitor is used for the controllers.

TI recommends reserving a small resistor in series with the bootstrap capacitor in case the turnon and turnoff of the FETs must be slowed to reduce voltage ringing on the switch node, which is a common practice for controller design.

7.2.2.1.5 Selecting the Input Capacitors

Due to the nature of the switching controller with a pulsating input current, a low-ESR input capacitor is required for best input-voltage filtering and also for minimizing the interference with other circuits caused by high input-voltage spikes. For the controller, a typical 2.2-µF capacitor can be used for the DRV5V_x_x pin to handle the transients on the driver. For the FET input, 10 µF of input capacitance (after derating) is recommended for most applications. To achieve the low-ESR requirement, a ceramic capacitor is recommended. However, the voltage rating and DC-bias characteristic of ceramic capacitors must be considered. For better input-voltage filtering, the input capacitor can be increased without any limit.

7.2.2.1.5.1 Setting the Current Limit

The current-limiting resistor value must be chosen based on Equation 1.

NOTE

Use the correct value for the ceramic capacitor capacitance after derating to achieve the recommended input capacitance.

TI recommends placing a ceramic capacitor as close as possible to the FET across the respective VSYS and PGND pins of the FETs. The preferred capacitors for the controllers are two Murata GRM21BR61E226ME44: 22 µF, 0805, 25 V, ±20%, or similar capacitors.

7.2.2.2 Converter Design Procedure

Designing the converter has only the following two steps:

1. Design the output filter.
2. Select the input capacitors.

The converter must be supplied by a 5-V source. Figure 7-3 shows a diagram of the converter.

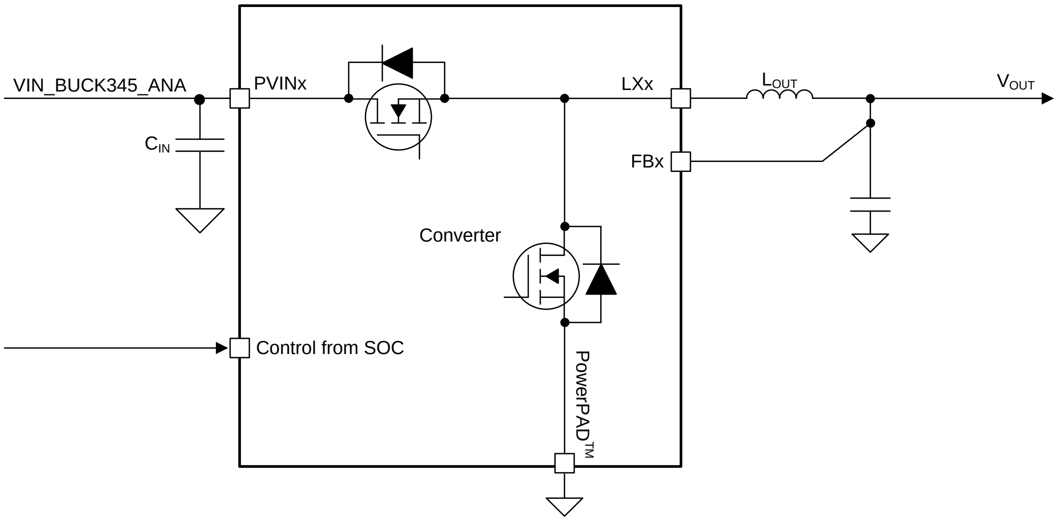


Figure 7-3. Converter Diagram

7.2.2.2.1 Selecting the Inductor

An inductor must be placed between the external FETs and the output capacitors. Together, the inductor and output capacitors form a double-pole in the control loop that contributes to stability. In addition, the inductor is responsible for the output ripple, efficiency, and transient performance. When the inductance increases, the ripple current decreases, which typically results in an increase in efficiency. However, with an increase in inductance, the transient performance decreases. Finally, the inductor selected must be rated for appropriate saturation current, core losses, and DCR.

> **NOTE**
>
> Internal parameters for the converters are optimized for a 0.47-µH inductor; however, it is possible to use other inductor values as long as they are chosen carefully and thoroughly tested.

Equation 5 shows the calculation for the recommended inductance for the converter.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{sw} \times I_{OUT(MAX)} \times K_{IND}} \quad (5)$$

where

- V_{OUT} is the typical output voltage.
- V_{IN} is the typical input voltage.
- f_{SW} is the typical switching frequency.
- $I_{OUT(MAX)}$ is the maximum load current.
- K_{IND} is the ratio of $I_{Lripple}$ to the $I_{OUT(MAX)}$. For this application, TI recommends that K_{IND} is set to a value from 0.2 to 0.4.

With the chosen inductance value and the peak current for the inductor in steady state operation, $I_{L(MAX)}$ can be calculated using Equation 6. The rated saturation current of the inductor must be higher than the $I_{L(MAX)}$ current.

$$I_{L(MAX)} = I_{OUT(MAX)} + \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times V_{IN} \times f_{sw} \times L} \quad (6)$$

Following these equations, Table 7-2 lists the preferred inductor selected for the converters.

Table 7-2. Recommended Inductors

MANUFACTURER	PART NUMBER	VALUE	SIZE	HEIGHT
Cyntec	PIFE32251B-R47MS	0.47 µH	3.2 mm × 2.5 mm	1.2 mm

7.2.2.2.2 Selecting the Output Capacitors

TI recommends using ceramic capacitors with low-ESR values are recommended to provide the lowest output voltage ripple. The output capacitor requires either an X7R or an X5R rating. Y5V and Z5U capacitors, aside from the wide variation in capacitance overtemperature, become resistive at high frequencies.

At light load currents, the converter operates in PFM mode and the output voltage ripple is dependent on the output-capacitor value and the PFM peak inductor current. Higher output-capacitor values minimize the voltage ripple in PFM mode. To achieve specified regulation performance and low output voltage ripple, the DC-bias characteristic of ceramic capacitors must be considered. The effective capacitance of ceramic capacitors drops with increasing DC-bias voltage.

For the output capacitors of the BUCK converters, TI recommends placing small ceramic capacitors between the inductor and load with many vias to the PGND plane. This solution typically provides the smallest and lowest-cost solution available for DCAP2 controllers.

To meet the transient specifications, the output capacitance must equal or exceed the minimum capacitance listed for BUCK3, BUCK4, and BUCK5 (assuming quality layout techniques are followed).

7.2.2.2.3 Selecting the Input Capacitors

Due to the nature of the switching converter with a pulsating input current, a low-ESR input capacitor is required for best input-voltage filtering and for minimizing the interference with other circuits caused by high input-voltage spikes. For the PVINx pin, 2.5 µF of input capacitance (after derating) is required for most applications. A ceramic capacitor is recommended to achieve the low-ESR requirement. However, the voltage rating and DC-bias characteristic of ceramic capacitors must be considered. For better input-voltage filtering, the input capacitor can be increased without any limit.

NOTE

Use the correct value for the ceramic capacitor capacitance after derating to achieve the recommended input capacitance.

The preferred capacitor for the converters is one Samsung CL05A106MP5NUNC: 10 µF, 0402, 10 V, ±20%, or similar capacitor.

7.2.2.3 LDO Design Procedure

The VTT LDO must handle the fast load transients from the DDR memory for termination. Therefore, TI recommends using ceramic capacitors to maintain a high amount of capacitance with low ESR on the VTT LDO outputs and inputs. The preferred output capacitors for the VTT LDO are the GRM188R60J226MEA0 from Murata (22 µF, 0603, 6.3 V, ±20%, or similar capacitors). The preferred input capacitor for the VTT LDO is the CL05A106MP5NUNC from Samsung (10 µF, 0402, 10 V, ±20%, or similar capacitor).

The remaining LDOs must have input and output capacitors chosen based on the values in Section 5.9, *Electrical Characteristics: LDOs.*

7.2.3 Application Curves

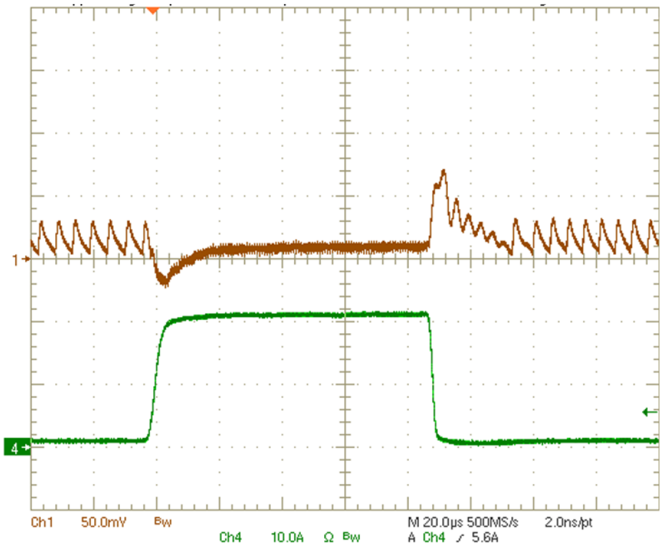


Figure 7-4. BUCK2 Controller Load Transient

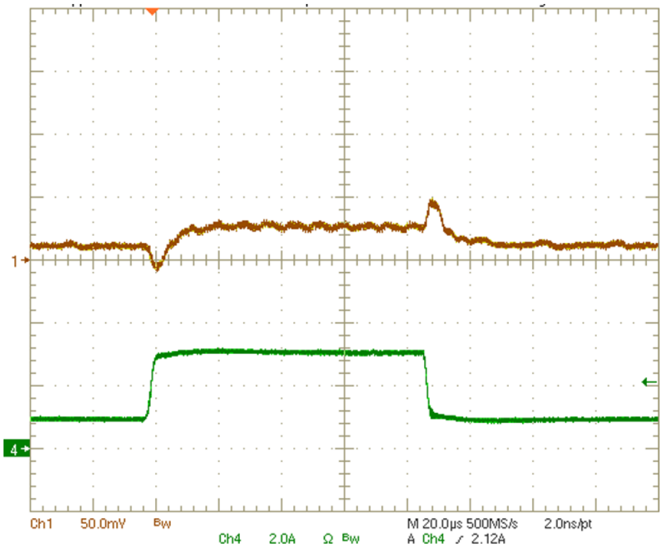


Figure 7-5. BUCK3 Converter Load Transient

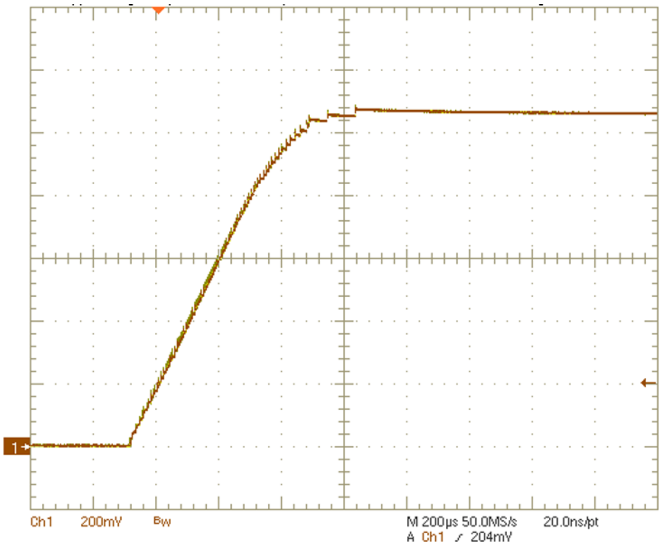


Figure 7-6. BUCK2 Controller Start-Up

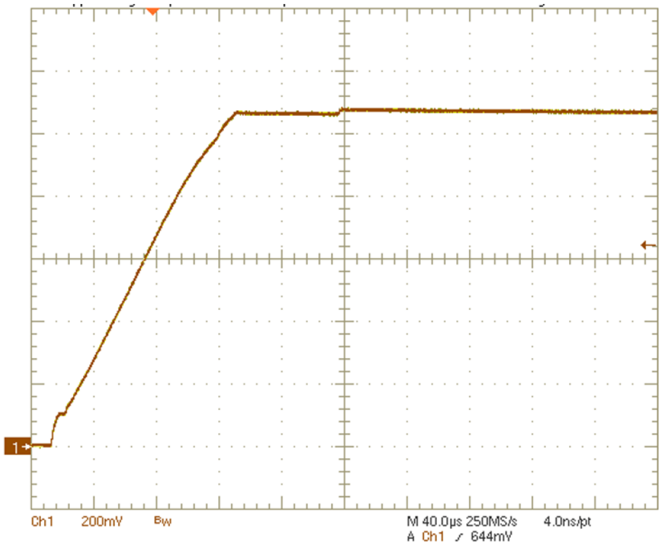
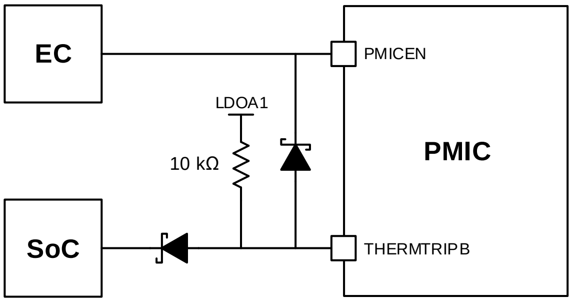


Figure 7-7. BUCK3 Converter Start-Up

7.3 Specific Application for TPS650944

For the TPS650944 device, if register reset is desired when the PMICEN pin is pulled low, an alternate reset condition can be used. There are two simple options. The first option is to write 1 to the SDWN bit in the FORCESHUTDN register (see Section 6.6.17, *FORCESHUTDN: Force Emergency Shutdown Control Register*) to force power rails to turn off and reset all registers. The second option is to use the falling edge detection of the THERMTRIPB pin to trigger the device reset. In this case, when the PMICEN pin is pulled low, the THERMTRIPB pin on PMIC should be pulled low simultaneously, which can be done in several ways. One approach is to connect a low-voltage Schottky diode between the PMICEN and THERMTRIPB pins. Because the THERMTRIPB SoC pin is push-pull configured, a second diode is needed to prevent shorting the SoC pin to GND. An example can be seen in Figure 7-8. Both diodes must have a forward voltage below PMIC V_{IL} (0.4 V) at the appropriate current. Another approach is to route the THERMTRIPB signal from SoC through the EC and tie PMICEN and THERMTRIPB together at the PMIC.



NOTE: Not applicable if LDOA1 is not configured to "Always On"

Figure 7-8. PMICEN and THERMTRIPB Connection Option for LDOA1 "Always On" Spins

For the TPS650944 device, if both the PVINSWA1 and PVINSWB1_B2 pins are tied to 2.5 V, LDOA2 and LDOA3 will turn on if all VRs and load switches are enabled and have released their Power Good signals. To avoid LDOA2 and LDOA3 turning on unexpectedly, TI recommends using voltages other than 2.5 V on both SWA1 and SWB1_2.

7.4 Do's and Don'ts

- Connect the LDO5V output to the DRV5V_x_x inputs for situations where an external 5-V supply is not initially available or is not available the entire time PMIC is on. If the external 5-V supply is always present, then DRV5V_x_x can be directly connected to remove the V5ANA-to-LDO5P0 load switch R_{DSON}.
- Ensure that none of the control pins are potentially floating.
- Include 0-Ω resistors on the DRVH and BOOT pins of controllers on prototype boards, which allows for slowing the controllers if the system is unable to handle the noise generated by the large switching or if switching voltage is too large due to layout.
- Do not connect the V5ANA power input to a different source other than PVINx. A mismatch here causes reference circuits to regulate incorrectly.
- Do not supply the V5ANA power input before the VSYS. Reference biasing of the internal FETs may turn on the HS FET and pass the input to the output until VSYS is biased.

8 Power Supply Recommendations

This device is designed to work with several different input voltages. The minimum voltage on the VSYS pin is 5.6 V for the device to start up; however, this is a low-power rail. The input to the FETs must be from 5.4 V to 21 V as long as the proper BOM choices are made. Input to the converters must be 5 V. For the device to output maximum power, the input power must be sufficient. For the controllers, VIN must be able to supply up to 5 A (typically), though less is acceptable with higher voltages or less usage. For the converters, PVINx must be able to supply 2 A (typically).

A best practice here is to determine power usage by the system and back-calculate the necessary power input based on expected efficiency values.

9 Layout

9.1 Layout Guidelines

For a detailed description regarding layout recommendations, refer to the *TPS65094x Design Guide* and to the *TPS65094x Schematic Checklist, Layout Checklist, and ILIM Calculator Tool*. For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator can have stability problems and EMI issues. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitors, output capacitors, and inductors must be placed as close as possible to the device. Use a common-ground node for power ground and use a different, isolated node for control ground to minimize the effects of ground noise. Connect these ground nodes close to the AGND pin by one or two vias. Use of the design guide is highly encouraged in addition to the following list of other basic requirements:

- Do not allow the AGND, PGNDSNSx, or FBGND2 to connect to the thermal pad on the top layer.
- To ensure proper sensing based on FET R_{DSON}, PGNDSNSx must not connect to PGND until very close to the PGND pin of the FET.
- All inductors, input/output capacitors, and FETs for the converters and controller must be on the same board layer as the device.
- To achieve the best regulation performance, place feedback connection points near the output capacitors and minimize the control feedback loop as much as possible.
- Bootstrap capacitors must be placed close to the device.
- The input and output capacitors of the internal reference regulators must be placed close to the device pins.
- Route DRVHx and SWx as a differential pair. Ensure that there is a PGND path routed in parallel with DRVLx, which provides optimal driver loops.

9.2 Layout Example

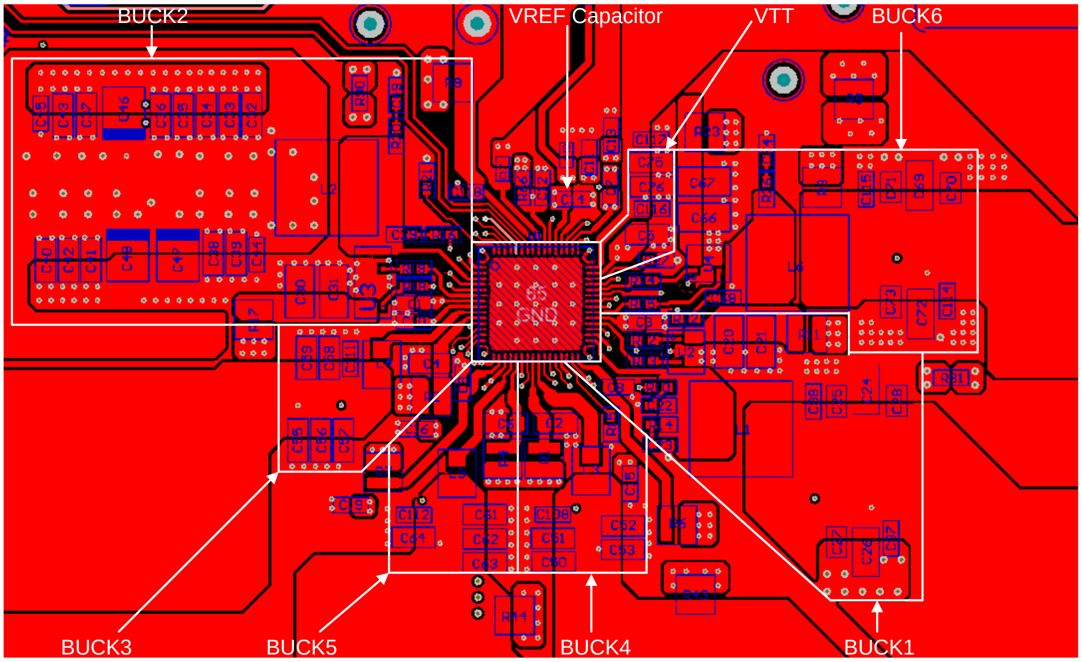


Figure 9-1. EVM Layout Example With All Components on the Top Layer

10 Device and Documentation Support

10.1 Device Support

10.1.1 Third-Party Products Disclaimer

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10.1.2 Development Support

See the following for development support:

TPS65094x Schematic Checklist, Layout Checklist, and ILIM Calculator Tool

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation see the following:

- *TPS65094x Design Guide*
- *TPS65094x Evaluation Module*

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Package Option Addendum

11.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish(3)	MSL Peak Temp (4)	Op Temp (°C)	Device Marking(5) (6)
TPS650945RSKR	ACTIVE	VQFN	RSK	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	T650945 PG1.0
TPS650945RSKT	ACTIVE	VQFN	RSK	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	T650945 PG1.0

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(4) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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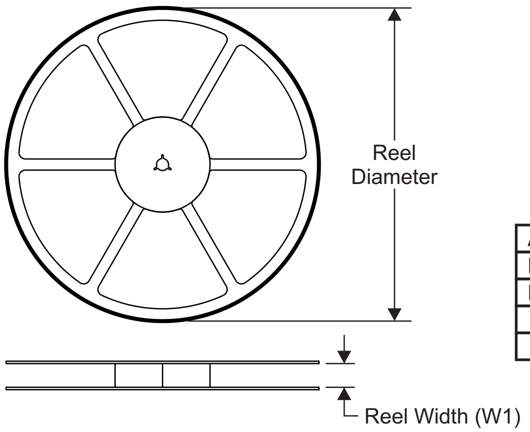
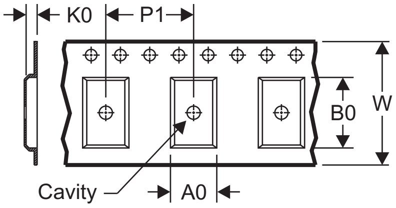
11.1.2 Tape and Reel Information

REEL DIMENSIONS

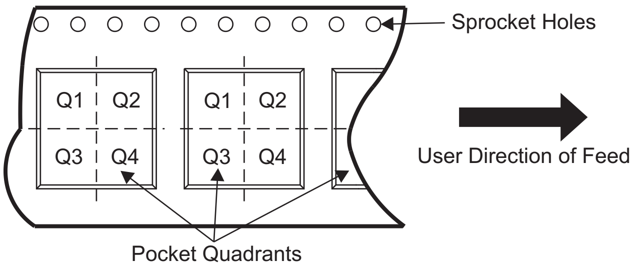


TAPE DIMENSIONS



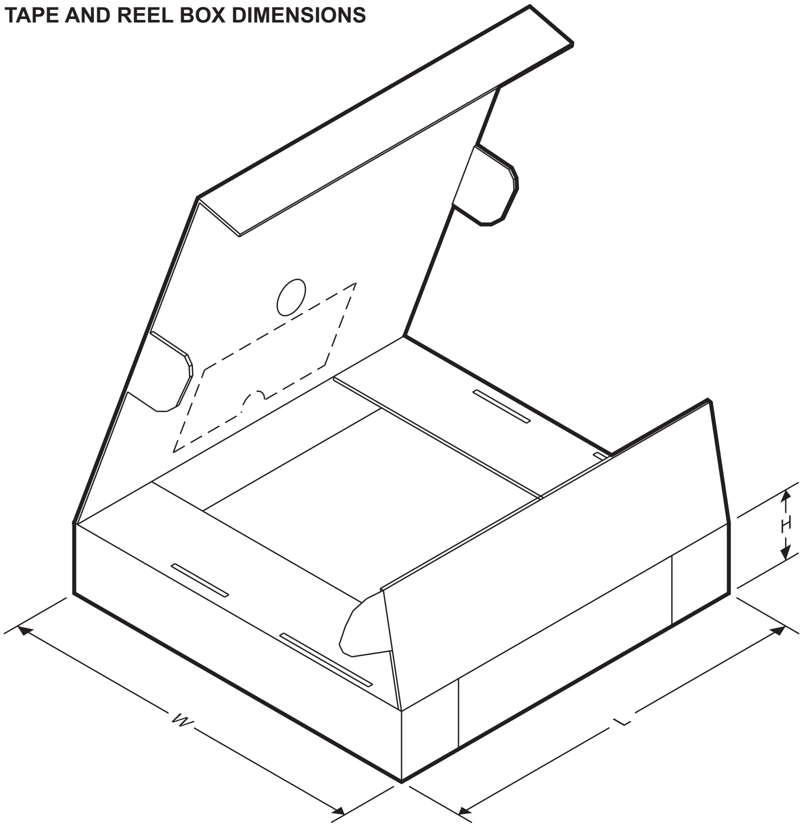
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS650945RSKR	VQFN	RSK	64	2000	330.0	16.4	8.3	8.3	1.1	12.0	16.0	Q2
TPS650945RSKT	VQFN	RSK	64	250	180.0	16.4	8.3	8.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS650945RSKR	VQFN	RSK	64	2000	367.0	367.0	38.0
TPS650945RSKT	VQFN	RSK	64	250.0	210.0	185.0	35.0

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS650940A0RSKR	ACTIVE	VQFN	RSK	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	T650940A0 PG1.0	Samples
TPS650940A0RSKT	ACTIVE	VQFN	RSK	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	T650940A0 PG1.0	Samples
TPS650941A0RSKR	ACTIVE	VQFN	RSK	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	T650941A0 PG1.0	Samples
TPS650941A0RSKT	ACTIVE	VQFN	RSK	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	T650941A0 PG1.0	Samples
TPS650942A0RSKR	ACTIVE	VQFN	RSK	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	T650942A0 PG1.0	Samples
TPS650942A0RSKT	ACTIVE	VQFN	RSK	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	T650942A0 PG1.0	Samples
TPS650944A0RSKR	ACTIVE	VQFN	RSK	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	T650944A0 PG1.0	Samples
TPS650944A0RSKT	ACTIVE	VQFN	RSK	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	T650944A0 PG1.0	Samples
TPS650945A0RSKR	ACTIVE	VQFN	RSK	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	T650945A0 PG1.0	Samples
TPS650945A0RSKT	ACTIVE	VQFN	RSK	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	T650945A0 PG1.0	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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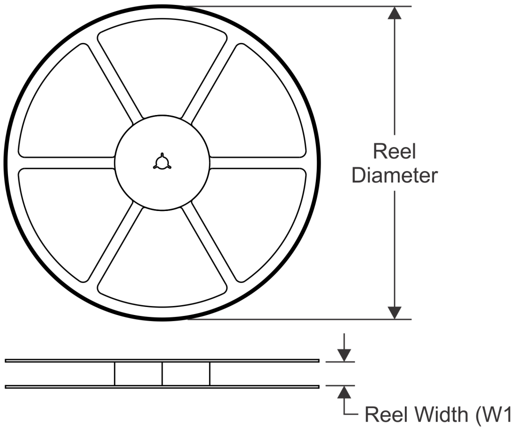
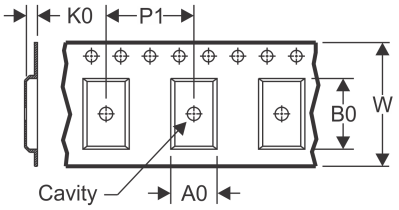
TAPE AND REEL INFORMATION

REEL DIMENSIONS

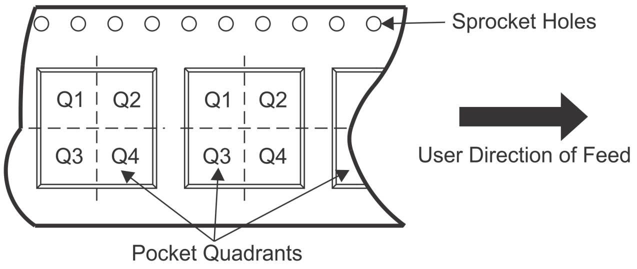


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

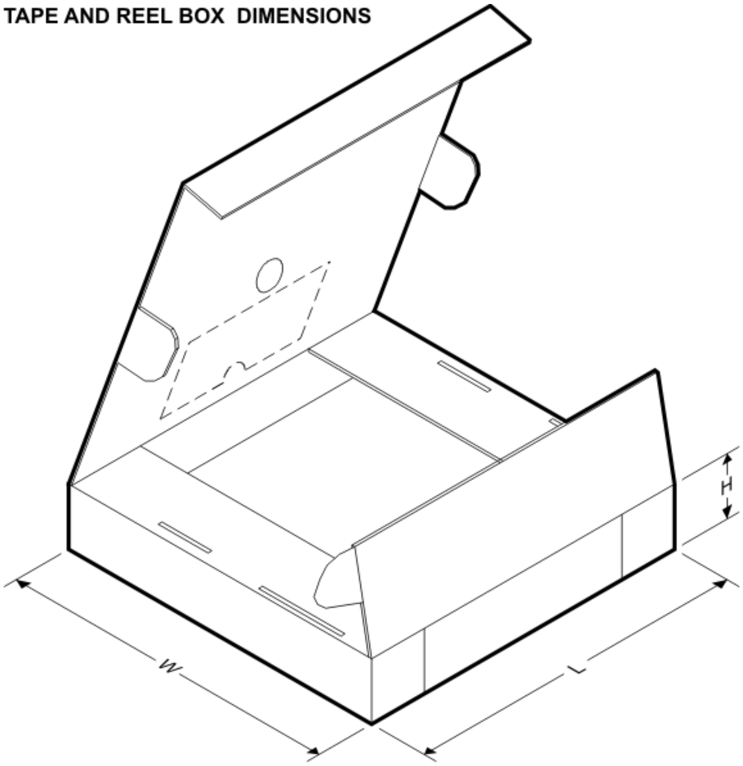
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS650940A0RSKR	VQFN	RSK	64	2000	330.0	16.4	8.3	8.3	1.1	12.0	16.0	Q2
TPS650940A0RSKT	VQFN	RSK	64	250	180.0	16.4	8.3	8.3	1.1	12.0	16.0	Q2
TPS650941A0RSKR	VQFN	RSK	64	2000	330.0	16.4	8.3	8.3	1.1	12.0	16.0	Q2
TPS650941A0RSKT	VQFN	RSK	64	250	180.0	16.4	8.3	8.3	1.1	12.0	16.0	Q2
TPS650942A0RSKR	VQFN	RSK	64	2000	330.0	16.4	8.3	8.3	1.1	12.0	16.0	Q2
TPS650942A0RSKT	VQFN	RSK	64	250	180.0	16.4	8.3	8.3	1.1	12.0	16.0	Q2
TPS650944A0RSKR	VQFN	RSK	64	2000	330.0	16.4	8.3	8.3	1.1	12.0	16.0	Q2
TPS650944A0RSKT	VQFN	RSK	64	250	180.0	16.4	8.3	8.3	1.1	12.0	16.0	Q2
TPS650945A0RSKR	VQFN	RSK	64	2000	330.0	16.4	8.3	8.3	1.1	12.0	16.0	Q2
TPS650945A0RSKT	VQFN	RSK	64	250	180.0	16.4	8.3	8.3	1.1	12.0	16.0	Q2

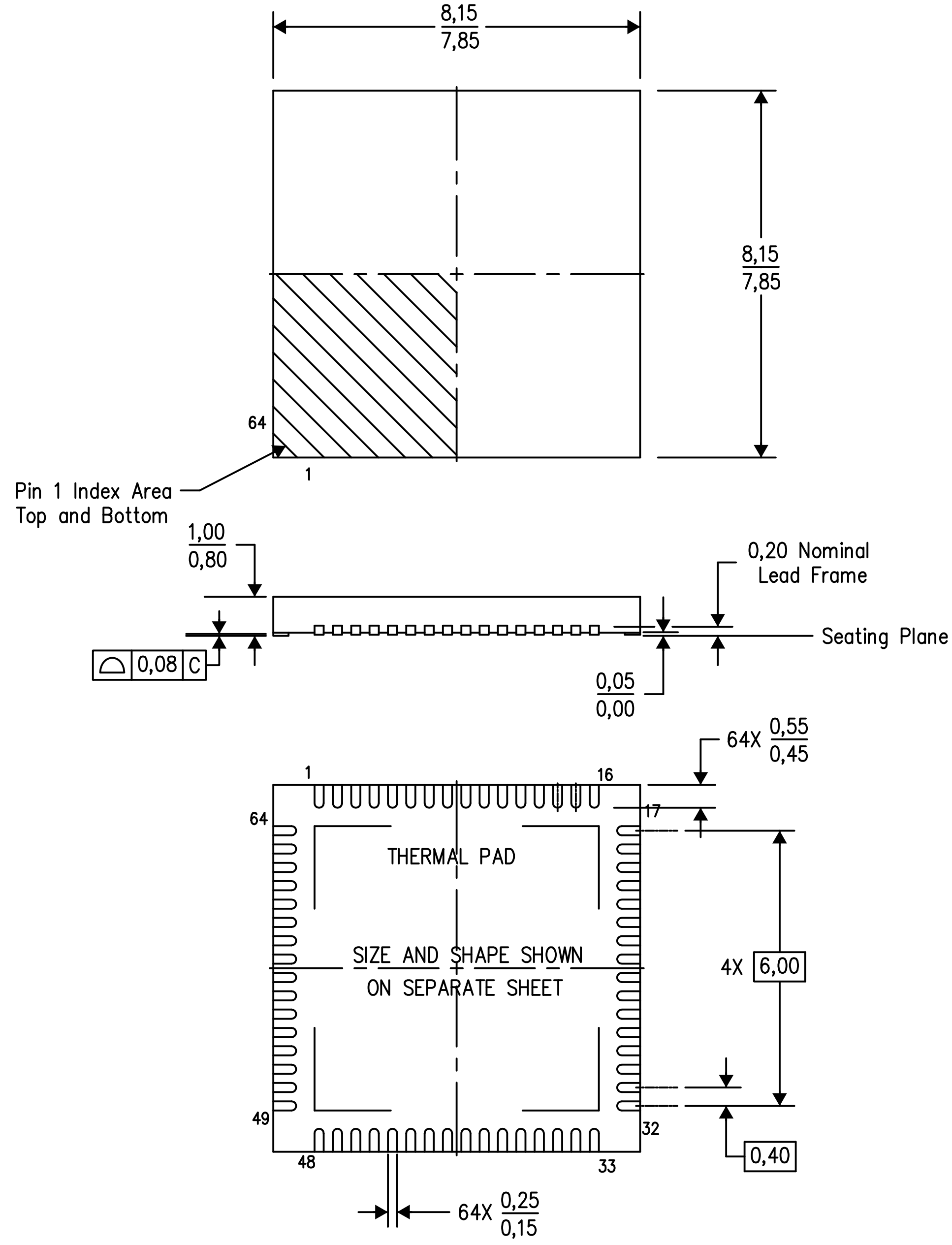
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS650940A0RSKR	VQFN	RSK	64	2000	367.0	367.0	38.0
TPS650940A0RSKT	VQFN	RSK	64	250	210.0	185.0	35.0
TPS650941A0RSKR	VQFN	RSK	64	2000	367.0	367.0	38.0
TPS650941A0RSKT	VQFN	RSK	64	250	210.0	185.0	35.0
TPS650942A0RSKR	VQFN	RSK	64	2000	367.0	367.0	38.0
TPS650942A0RSKT	VQFN	RSK	64	250	210.0	185.0	35.0
TPS650944A0RSKR	VQFN	RSK	64	2000	367.0	367.0	38.0
TPS650944A0RSKT	VQFN	RSK	64	250	210.0	185.0	35.0
TPS650945A0RSKR	VQFN	RSK	64	2000	367.0	367.0	38.0
TPS650945A0RSKT	VQFN	RSK	64	250	210.0	185.0	35.0

RSK (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD



Bottom View

4207547/C 04/12

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No–Lead) Package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

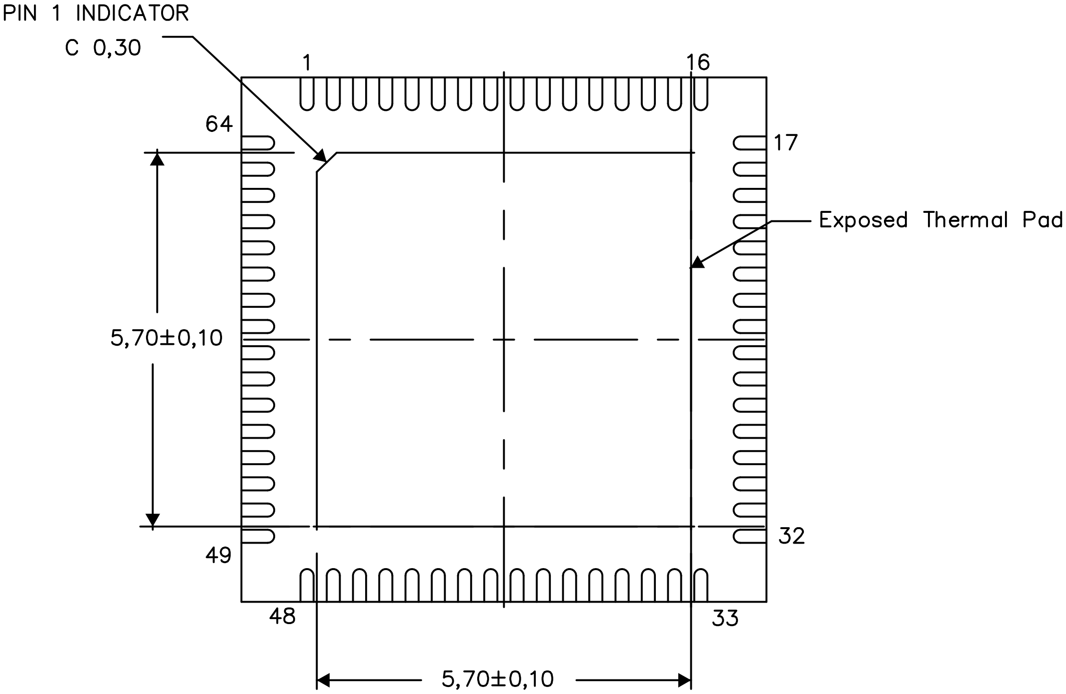
RSK (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



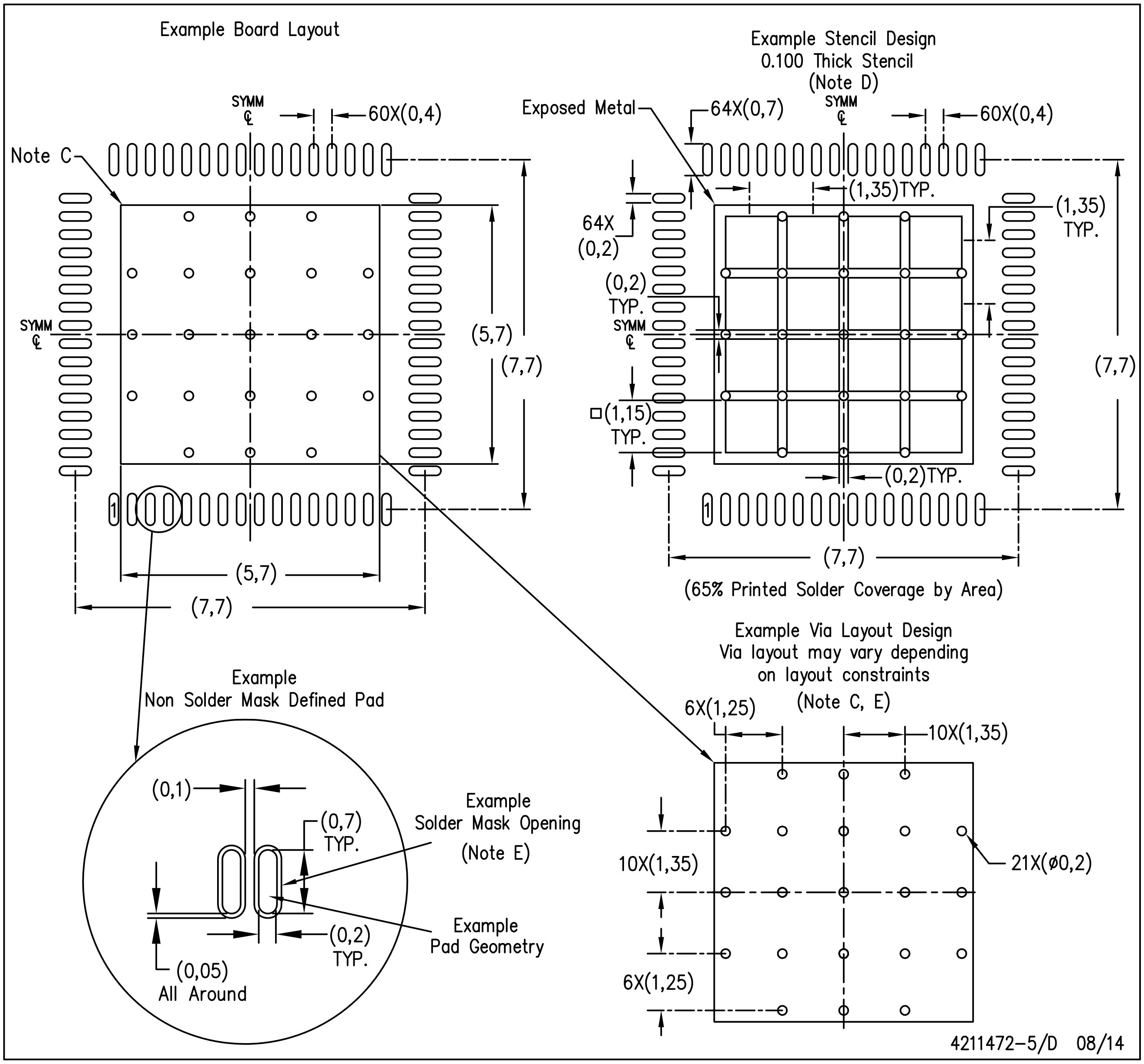
Bottom View

Exposed Thermal Pad Dimensions

4208001–5/H 08/14

NOTE: A. All linear dimensions are in millimeters

RSK (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for any larger diameter vias placed in the thermal pad.

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