MEC1618/MEC1618i

Low Power 32-bit Microcontroller with Embedded Flash

Product Features

- 3.3V Operation
- ACPI Compliant
- LPC Interface
  - LPC I/O Cycles Decoded
- VTR (standby) and VBAT (Power Planes)
  - Low Standby Current in Sleep Mode
- Configuration Register Set
  - Compatible with ISA Plug-and-Play Standard
  - EC-Programmable Base Address
- ARC-625D Embedded Controller (EC)
  - 16 KB Single Cycle 32-bit Wide Dual-ported SRAM, Accessible as Closely Coupled Data Memory and Instruction Memory
  - 32 x 32 x 64 Fast Multiply
  - Divide Assist and Saturation Arithmetic
  - Maskable Interrupt Aggregator/Accelerator Interface
  - Maskable Hardware Wake-Up Events
  - Sleep mode
  - JTAG Debug Port, Includes JTAG Master
  - MCU Serial Debug Port
  - 8-Channel DMA Interface Supports SMBus Controllers and EC/Host GP-SPI Controllers
  - Delay Register
  - Boot ROM
- Embedded Flash
  - 192 KB user space 32-bit Access, 30 ns Access Time, 10 K Cycles Endurance
  - 1 KB EEPROM Emulation, 40 ns Access Time, 250 K Cycles Endurance
  - Programmable by LPC, EC and JTAG Interfaces
  - Flash Security Enhancements
    - 4K Boot Block Protection
    - Direct JTAG and Direct LPC-protected (2) Pages at or Near Top of Memory for Password Protection
- Legacy Support
  - Fast GATEA20 & Fast CPU_RESET
- System to EC Message Interface
  - 8042 Style Host Interface
  - Embedded Memory Interface
    - Host Serial or Parallel IRQ Source
    - Provides Two Windows to On-Chip SRAM for Host Access

- Two Register Mailbox Command Interface
- Host Access of Virtual Registers Without EC Intervention
- Mailbox Registers Interface
  - Thirty-two 8-Bit Scratch Registers
  - Two Register Mailbox Command Interface
  - Two Register SMI Source Interface
- ACPI Embedded Controller Interface
  - Four Instances
  - 1 or 4 Byte Full Duplex Bidirectional Data Transfer Capable
- ACPI Power Management Interface
  - SCI Event-Generating Functions
- BIOS Debug Port
  - ISA Port 80 Plug-in Card Emulation
  - 2 Instances
  - Time Stamping Option
- Battery Backed Resources
  - Power-Fail Status Register
  - 32 KHz Clock Generator
  - Week Alarm Timer Interface with Programmable Wake-up from 1ms to 45 Days
  - VBAT-Powered Control Interface
    - 6 Latched Inputs
    - GPIO Capable
  - VBAT-Backed 64 Byte Memory
- Three EC-based SMBus 2.0 Host Controllers
  - Allows Master or Dual Slave Operation
  - Controllers are Fully Operational on Standby Power
  - DMA-driven I^2C Network Layer Hardware
  - I^2C Datalink Compatibility Mode
  - Multi-Master Capable
  - Supports Clock Stretching
  - Programmable Bus Speeds
  - 400 KHz Capable
  - Hardware Bus Access "Fairness" Interface
  - SMBus Time-outs Interface
  - 12 Port Flexible Multiplexing
  - Port Isolation
- PECI Interface 3.0
- Keyboard Matrix Scan Interface
  - 18 x 8 Interrupt/Wake Capable Multiplexed Keyboard Scan Matrix
  - Row Predrive Option

MEC1621/MEC1621i

- Three independent Hardware Driven PS/2 Ports
  - Fully functional on Main and/or Suspend Power
  - PS/2 Edge Wake Capable
- 133 General Purpose I/O Pins
  - 8 GPIO Pass-Through Port (GPTP)
- 3-pin LED Interface
  - Programmable Blink Rates
  - Piecewise Linear Breathing LED Output Controller
  - Operational in EC Sleep States
- Programmable 16-bit Counter/Timer Interface
  - Four Wake-capable 16-bit Auto-reloading Counter/Timer Instances
  - Four Operating Modes per Instance: Timer, One-shot, Event and Measurement.
  - 4 External Inputs, 4 External Outputs
- Hibernation Timer Interface
  - Two 32.768 KHz Driven Timers
  - Programmable Wake-up from 0.5ms to 128 Minutes
- System Watch Dog Timer (WDT)
- Input Capture and Compare Timer
  - 32-bit Free-running timer
  - Six 32-bit Capture Registers
  - Two 32-bit Compare Registers
  - Capture, Compare and Overflow Interrupts
- BC-Link™ Interconnection Bus
  - Two High Speed and one Low Speed Bus Masters Controllers
- Two General Purpose Serial Peripheral Interface Controllers (ECGP-SPI)
  - One 3-pin EC-driven Full Duplex Serial Communication Interface
  - One 4-pin EC/Host-driven Full Duplex Serial Communication Interface to SPI Flash Interface
  - Flexible Clock Rates
  - SPI Burst Capable
- FAN Support
  - 16 Programmable Pulse-Width Modulator Outputs
    –Multiple Clock Rates
    –16-Bit 'On' & 16-Bit 'Off' Counters
  - 6 Fan Tachometers
  - 6 x 2 Capture/Compare Timer Interface

- ADC Interface
  - 10-bit Conversion in 10μs
  - 16 Channels
  - Integral Non-Linearity of ±0.5 LSB; Differential Non-Linearity of ±0.5 LSB
- HDMI-CEC Interface Controller
- Two Pin Debug Port with Standard 16C550A Register Interface
  - Accessible from Host and EC
  - Programmable Input/output Pin Polarity Inversion
  - Programmable Main Power or Standby Power Functionality
  - Standard Baud Rates to 115.2 Kbps, Custom Baud Rates to 2 Mbps
- Resistor/Capacitor Identification Detection (RC_ID)
  - Single Pin Interface to External Inexpensive RC Circuit
  - Replacement for Multiple GPIO's
  - Provides 8 Quantized States on One Pin
- Integrated Standby Power Reset Generator
- Gang Programmer Interface
  - JTAG Enabled
  - Supports Mass Programming and Mass Verify
  - JTAG Mass Erase
- Clock Generator
  - VBAT powered 32.768 KHz Oscillator ±2% Accuracy
    –VBAT powered 32.768 KHz external input
    –External Clock Auto Detect Option
  - Operational on Suspend Power
  - Programmable Clock Power Management Control & Distribution
  - 20.27 MHz (nom) Oscillator
- Package:
  - 156 Pin LFBGA RoHS Compliant package

Tool Requirements:

Metaware version 8.7 or newer must be used.

Description

The MEC1618/MEC1618i is the mixed signal base component of a multi-device advanced I/O controller architecture. The MEC1618/MEC1618i incorporates a high-performance 32-bit ARC 625D embedded microcontroller with a 192 Kilobyte Embedded Flash Subsystem, 16 Kilobytes of SRAM and a 1 Kilobyte EEPROM Emulation. The MEC1609 communicates with the system host using the Intel® Low Pin Count bus.

The MEC1618/MEC1618i is the EC Base Component of a split-architecture Advanced I/O Controller system which uses BC-Link™ communication protocol to access up to three companion components. The BC-Link™ protocol is peer-to-peer providing communication between the MEC1618/MEC1618i embedded controller and registers located in a companion.

The MEC1618/MEC1618i is directly powered by two separate suspend supply planes (VBAT and VTR) and senses a third runtime power plane (VCC) to provide "instant on" and system power management functions. The MEC1618/MEC1618i also contains an integrated VTR Reset Interface and a system Power Management Interface that supports low-power states and can drive state changes as a result of hardware wake events as defined by the MEC1618/MEC1618i Wake Interface.

The MEC1618/MEC1618i defines a software development system interface that includes an MCU Serial Debug Port, a two pin serial debug port with a 16C550A register interface that is accessible to the EC or to the LPC host and can operate up to 2 MB/s, a flexible Flash programming interface, a BIOS Debug Port, Gang Programmer Interface, and a JTAG interface. The EC can also drive the JTAG interface as a master.

A top-level block diagram of the MEC1618/MEC1618i is shown below in .

MEC1621/MEC1621i

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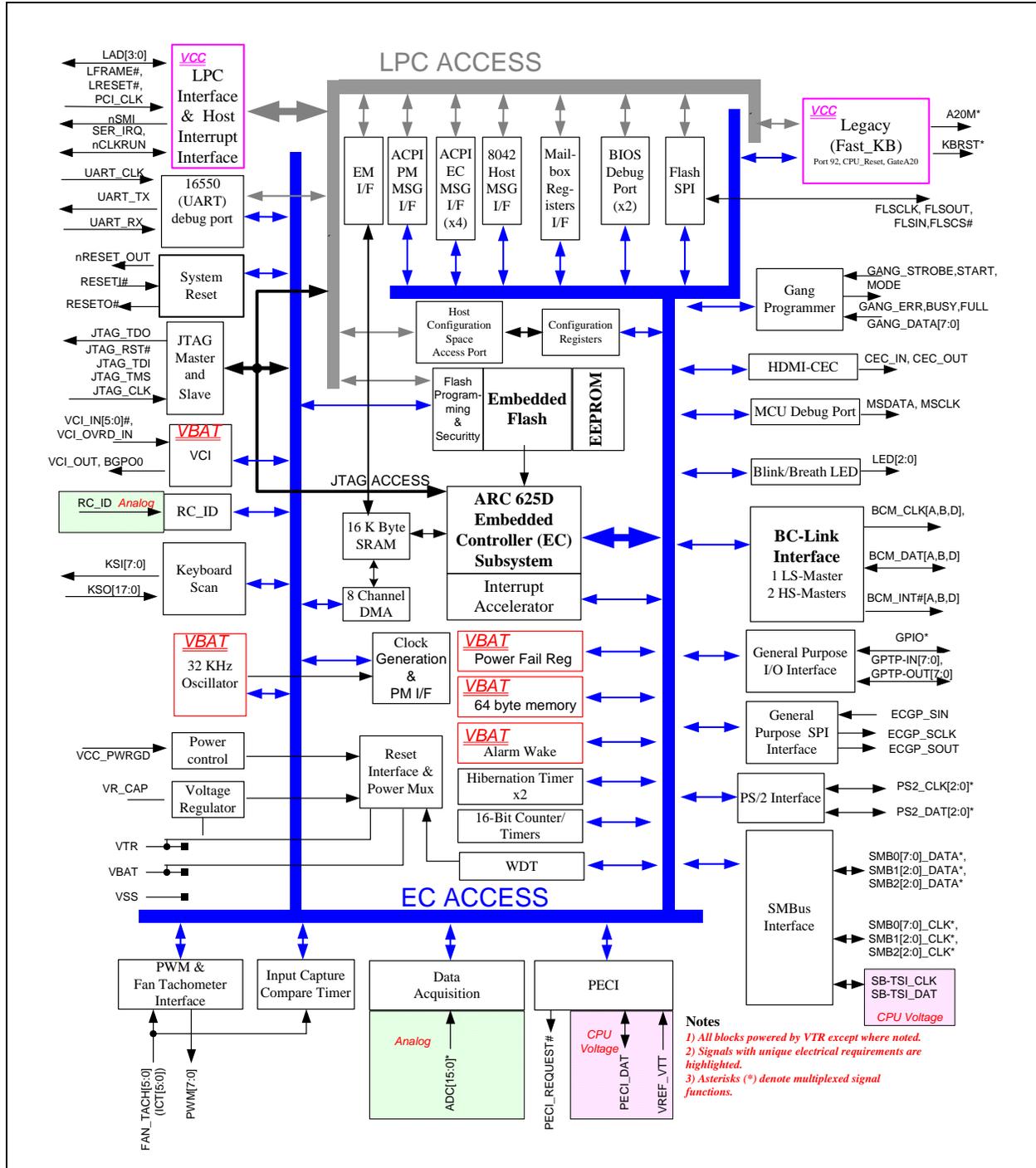- Your local Microchip sales office (see last page)

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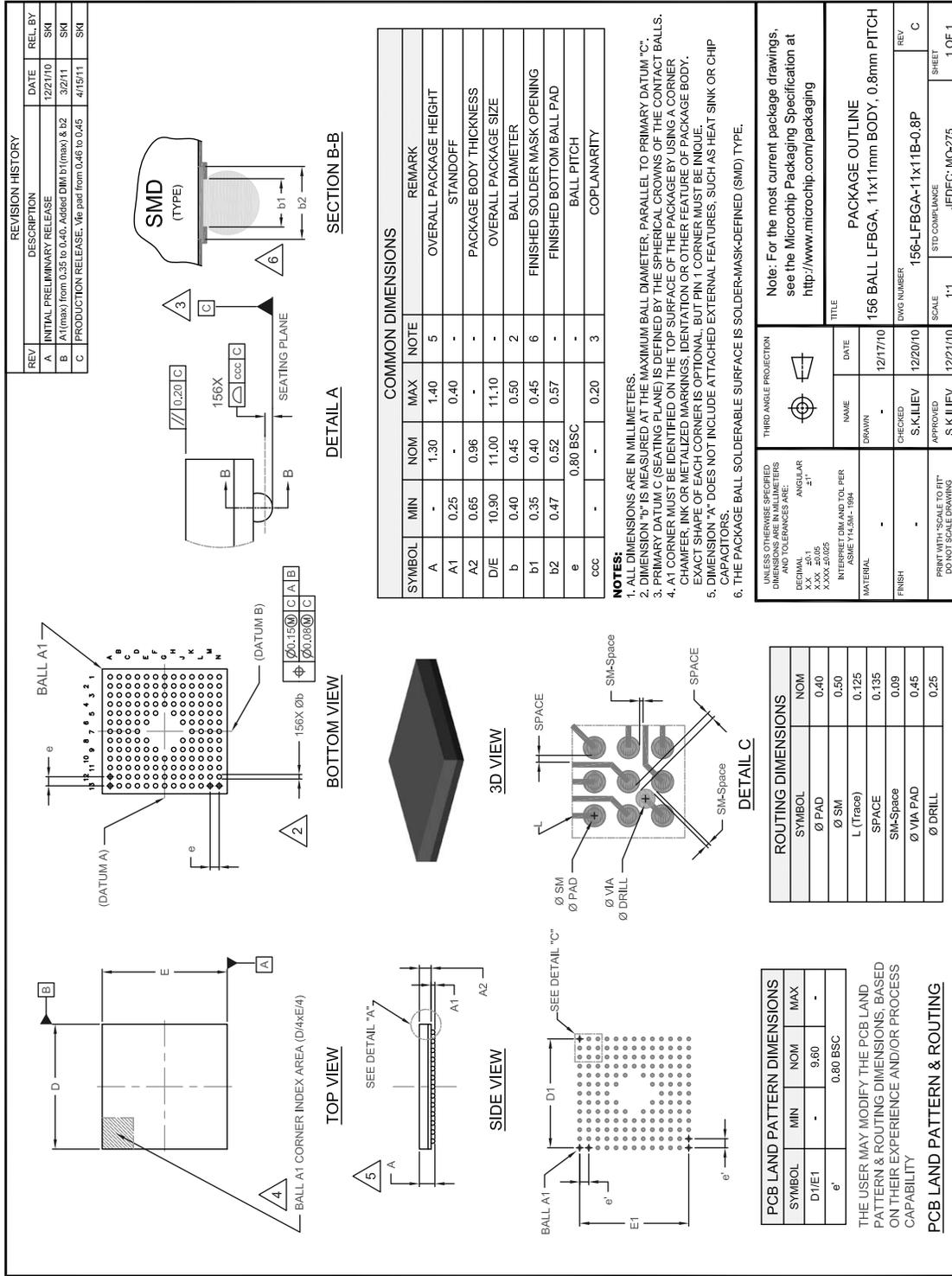
Block Diagram

FIGURE 1: **MEC1618/MEC1618i Block Diagram**

Package Outline

FIGURE 2: 156-BALL LFBGA, 11MM X 11MM BODY, 0.8MM PITCH

COMMON DIMENSIONS

SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	-	1.30	1.40	5	OVERALL PACKAGE HEIGHT
A1	0.25	-	0.40	-	STANDOFF
A2	0.65	0.96	-	-	PACKAGE BODY THICKNESS
D/E	10.90	11.00	11.10	-	OVERALL PACKAGE SIZE
b	0.40	0.45	0.50	2	BALL DIAMETER
b1	0.35	0.40	0.45	6	FINISHED SOLDER MASK OPENING
b2	0.47	0.52	0.57	-	FINISHED BOTTOM BALL PAD
e		0.80 BSC		-	BALL PITCH
ccc	-	-	0.20	3	COPLANARITY

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER, PARALLEL TO PRIMARY DATUM "C".
3. PRIMARY DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE CONTACT BALLS.
4. A1 CORNER MUST BE IDENTIFIED ON THE TOP SURFACE OF THE PACKAGE BY USING A CORNER CHAMFER, INK OR METALIZED MARKINGS, IDENTATION OR OTHER FEATURE OF PACKAGE BODY. EXACT SHAPE OF EACH CORNER IS OPTIONAL, BUT PIN 1 CORNER MUST BE INIQUE.
5. DIMENSION "A" DOES NOT INCLUDE ATTACHED EXTERNAL FEATURES, SUCH AS HEAT SINK OR CHIP CAPACITORS.
6. THE PACKAGE BALL SOLDERABLE SURFACE IS SOLDER-MASK-DEFINED (SMD) TYPE.

SECTION B-B

SMD (TYPE)

DETAIL A

SEATING PLANE

156X

BALL A1

(DATUM B)

BOTTOM VIEW

156X Øb

3D VIEW

DETAIL C

ROUTING DIMENSIONS

SYMBOL	NOM
Ø PAD	0.40
Ø SM	0.50
L (Trace)	0.125
SPACE	0.135
SM-Space	0.09
Ø VIA PAD	0.45
Ø DRILL	0.25

TOP VIEW

SIDE VIEW

PCB LAND PATTERN DIMENSIONS

SYMBOL	MIN	NOM	MAX
D1/E1	-	9.60	-
e'		0.80 BSC	

THE USER MAY MODIFY THE PCB LAND PATTERN & ROUTING DIMENSIONS, BASED ON THEIR EXPERIENCE AND/OR PROCESS CAPABILITY

PCB LAND PATTERN & ROUTING

BALL A1 CORNER INDEX AREA (D/4xE/4)

THIRD ANGLE PROJECTION

Note: For the most current package drawings, see the Microchip Packaging Specification at http://www.microchip.com/packaging

	NAME	DATE
DRAWN	-	12/17/10
CHECKED	S.K.ILIEV	12/20/10
APPROVED	S.K.ILIEV	12/21/10

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS AND TOLERANCES ARE:
DECIMAL: X.X ±0.1, X.XX ±0.05, X.XXX ±0.025
ANGULAR ±1°
INTERPRET DIM AND TOL PER ASME Y14.5M - 1994

TITLE PACKAGE OUTLINE
156 BALL LFBGA, 11x11mm BODY, 0.8mm PITCH

DWG NUMBER 156-LFBGA-11x11B-0.8P
REV C

STD COMPLIANCE JEDEC: MO-275

SCALE 1:1
SHEET 1 OF 1

PRINT WITH "SCALE TO FIT" DO NOT SCALE DRAWING

APPENDIX A: PRODUCT BRIEF REVISION HISTORY

TABLE A-1:   REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00001772A (06-05-14)	Document Release	

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PART NO.   **[X]** - **XXX** - **[X]**(1)

| Device | Temperature Range | Package | Tape and Reel Option |

Device: MEC1618, MEC1618i

Temperature Range:
Blank = 0°C to +85°C (Extended Commercial)
i = -40°C to +85°C (Industrial)

Package: AJZP = 156-pin LFBGA

Tape and Reel Option:
Blank = Standard packaging (tray)
TR = Tape and Reel(1)

Examples:

a) MEC1618-AJZP
156-pin LFBGA (11mm x 11mm, 0.8mm pitch)
RoHS Compliant package

b) MEC1618i-AJZP
156-pin LFBGA (11mm x 11mm, 0.8mm pitch)
RoHS Compliant package
with Industrial Temperature rating

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option. Reel size is 4,000.

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