MX25L6473E

HIGH PERFORMANCE

SERIAL FLASH SPECIFICATION

Contents

64M-BIT [x 1/x 2/x 4] CMOS MXSMIO® (SERIAL MULTI I/O) FLASH MEMORY

1. FEATURES

GENERAL

- Serial Peripheral Interface compatible -- Mode 0 and Mode 3
- 67,108,864 x 1 bit structure or 33,554,432 x 2 bits (two I/O mode) structure or 16,777,216 x 4 bits (four I/O mode) structure
- 2048 Equal Sectors with 4K bytes each
  - Any Sector can be erased individually
- 256 Equal Blocks with 32K bytes each
  - Any Block can be erased individually
- 128 Equal Blocks with 64K bytes each
  - Any Block can be erased individually
- Power Supply Operation
  - 2.7 to 3.6 volt for read, erase, and program operations
- Latch-up protected to 100mA from -1V to Vcc +1V
- Permanent fixed QE bit, QE =1 and 4 I/O mode is enabled

PERFORMANCE

- High Performance
  VCC = 2.7~3.6V
  - Normal read
    - 50MHz
  - Fast read
    - 1 I/O: 104MHz with 8 dummy cycles
    - 2 I/O: 86MHz with 4 dummy cycles for 2READ instruction
    - 4 I/O: Up to 104MHz
    - Configurable dummy cycle number for 4 I/O read operation
  - Fast program time: 0.7ms(typ.) and 3ms(max.)/page (256-byte per page)
  - Byte program time: 12us (typical)
  - Continuous Program mode (automatically increase address under word program mode)
  - Fast erase time: 30ms (typ.)/sector (4K-byte per sector) ; 0.25s(typ.) /block (64K-byte per block); 20s(typ.) / chip
- Low Power Consumption
  - Low active read current: 19mA(max.) at 104MHz, 10mA(max.) at 33MHz
  - Low active programming current: 15mA (typ.)
  - Low active sector erase current: 10mA (typ.)
  - Low standby current: 15uA (typ.)
  - Deep power down current: 1uA (typ.)
- Typical 100,000 erase/program cycles
- 20 years data retention

SOFTWARE FEATURES

- Input Data Format
  - 1-byte Command code
- Advanced Security Features
  - BP0-BP3 block group protect
  - Flexible individual block protect when OTP WPSEL=1
  - Additional 4K bits secured OTP for unique identifier
- Auto Erase and Auto Program Algorithms
  - Automatically erases and verifies data at selected sector
  - Automatically programs and verifies data at selected page by an internal algorithm that automatically times the program pulse width (Any page to be programmed should have page in the erased state first.)
- Status Register Feature
- Electronic Identification
  - JEDEC 1-byte Manufacturer ID and 2-byte Device ID
  - RES command for 1-byte Device ID
  - The REMS,REMS2, REMS4 commands for 1-byte Manufacturer ID and 1-byte Device ID
- Support Serial Flash Discoverable Parameters (SFDP) mode

HARDWARE FEATURES

- SCLK Input
  - Serial clock input
- SI/SIO0
  - Serial Data Input or Serial Data Input/Output for 2 x I/O mode and 4 x I/O mode
- SO/SIO1
  - Serial Data Output or Serial Data Input/Output for 2 x I/O mode and 4 x I/O mode
- SIO2
  - Serial data Input/Output for 4 x I/O mode
- SIO3
  - Serial data Input/Output for 4 x I/O mode
- PACKAGE
  - 16-pin SOP (300mil)
  - 8-pin SOP (200mil)
  - 8-pin VSOP (200mil)
  - 8-WSON (6x5mm)
  - **All devices are RoHS Compliant and Halogen-free**

2. GENERAL DESCRIPTION

MX25L6473E is 64Mb bits serial Flash memory, which is configured as 8,388,608 x 8 internally. When it is in two or four I/O mode, the structure becomes 33,554,432 bits x 2 or 16,777,216 bits x 4. MX25L6473E feature a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus while it is in single I/O mode. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input.

MX25L6473E, MXSMIO® (Serial Multi I/O) flash memory, provides sequential read operation on whole chip and multi-I/O features.

When it is in dual I/O mode, the SI pin and SO pin become SIO0 pin and SIO1 pin for address/dummy bits input and data output. When it is in quad I/O mode, the SI pin, SO pin become SIO0 pin and SIO1 pin, SIO2 pin and SIO3 pin for address/dummy bits input and data Input/Output.

After program/erase command is issued, auto program/ erase algorithms which program/ erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page (256 bytes) basis, or word basis for Continuous Program mode, and erase command is executed on sector (4K-byte), block (32K-byte/64K-byte), or whole chip basis.

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit.

When the device is not in operation and CS# is high, it is put in standby mode.

The MX25L6473E utilizes Macronix's proprietary memory cell, which reliably stores memory contents even after 100,000 program and erase cycles.

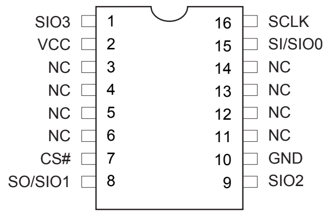
Table 1. Read Performance

Numbers of Dummy Cycles	4 I/O
6	86*
8	104

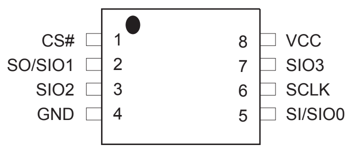
Note: *means default status

3. PIN CONFIGURATION

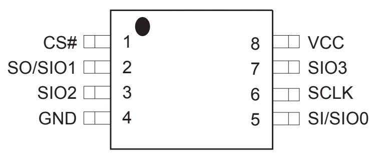
16-PIN SOP (300mil)



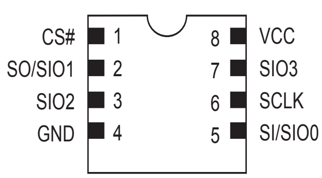
8-PIN SOP (200mil)



8-PIN VSOP (200mil)



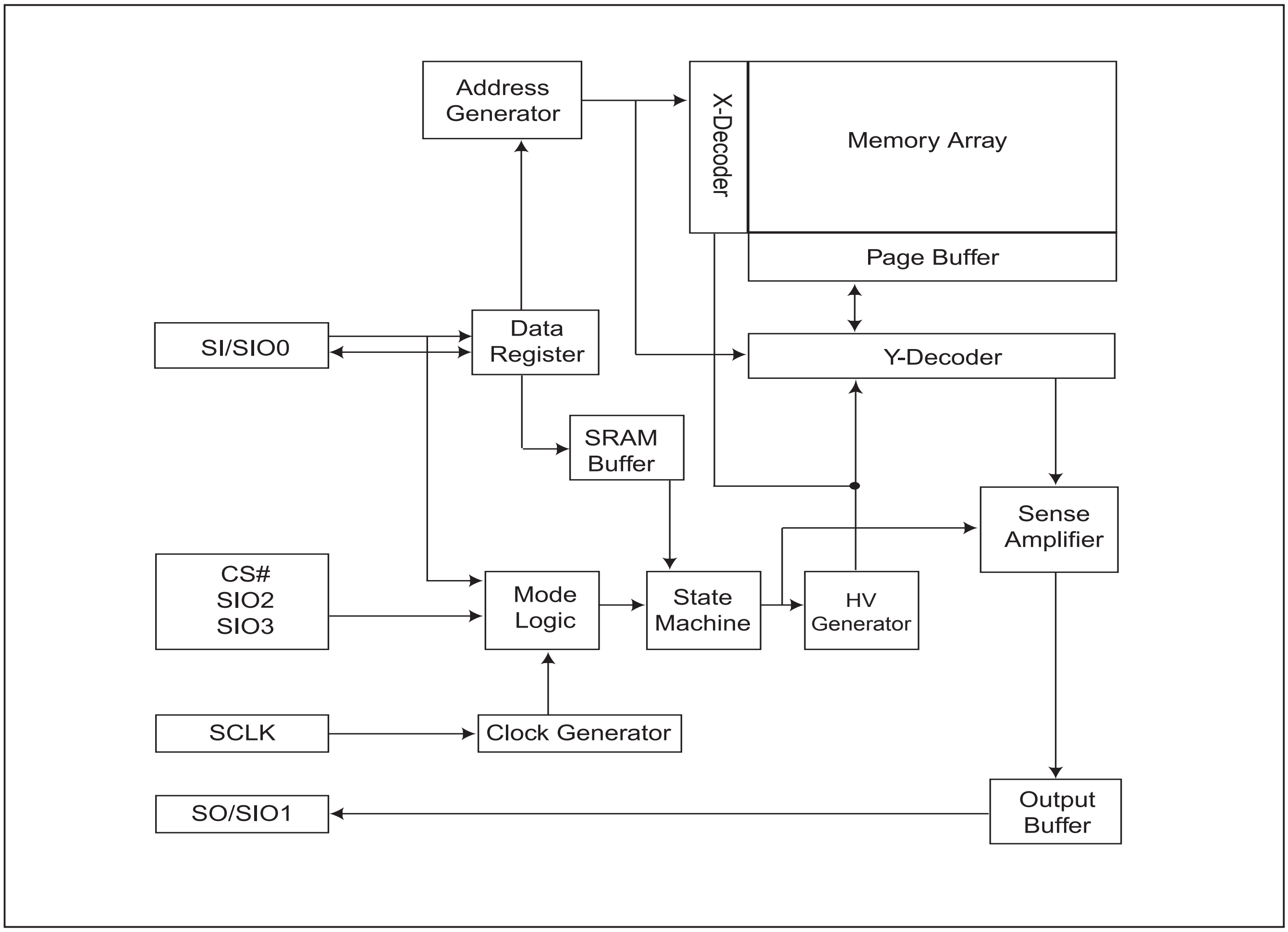
8-WSON (6x5mm)



4. PIN DESCRIPTION

SYMBOL	DESCRIPTION
CS#	Chip Select
SI/SIO0	Serial Data Input (for 1xI/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O mode)
SO/SIO1	Serial Data Output (for 1xI/O)/Serial Data Input & Output (for 2xI/O or 4xI/O mode)
SCLK	Clock Input
SIO2	Serial Data Input & Output (for 4xI/O mode)
SIO3	Serial data Input/Output for 4 x I/O mode
VCC	+ 3.0V Power Supply
GND	Ground
NC	No Connection

5. BLOCK DIAGRAM



6. DATA PROTECTION

During power transition, there may be some false system level signals which result in inadvertent erasure or programming. The device is designed to protect itself from these accidental write cycles.

The state machine will be reset as standby mode automatically during power up. In addition, the control register architecture of the device constrains that the memory contents can only be changed after specific command sequences have completed successfully.

In the following, there are several features to protect the system from the accidental write cycles during VCC power-up and power-down or from system noise.

- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.

- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before other command to change data. The WEL bit will return to reset stage under following situation:
  - Power-up
  - Write Disable (WRDI) command completion
  - Write Status Register (WRSR) command completion
  - Page Program (PP, 4PP) command completion
  - Continuous Program mode (CP) instruction completion
  - Sector Erase (SE) command completion
  - Block Erase (BE, BE32K) command completion
  - Chip Erase (CE) command completion
  - Single Block Lock/Unlock (SBLK/SBULK) instruction completion
  - Gang Block Lock/Unlock (GBLK/GBULK) instruction completion

- Deep Power Down Mode: By entering deep power down mode, the flash device also is under protected from writing all commands except Release from Deep Power Down mode command (RDP) and Read Electronic Signature command (RES).

I. Block lock protection

- The Software Protected Mode (SPM) uses (BP3, BP2, BP1, BP0) bits to allow part of memory to be protected as read only. The protected area definition is shown as table of *"Table 2. Protected Area Sizes"*, the protected areas are more flexible which may protect various areas by setting value of BP0-BP3 bits.

- MX25L6473E provides individual block (or sector) write protect & unprotect. User may enter the mode with WPSEL command and conduct individual block (or sector) write protect with SBLK instruction, or SBULK for individual block (or sector) unprotect. Under the mode, user may conduct whole chip (all blocks) protect with GBLK instruction and unlock the whole chip with GBULK instruction.

Table 2. Protected Area Sizes

Protected Area Sizes (TB bit = 0)

Status bit				Protect Level
BP3	BP2	BP1	BP0	64Mb
0	0	0	0	0 (none)
0	0	0	1	1 (1block, block 127th)
0	0	1	0	2 (2blocks, block 126th-127th)
0	0	1	1	3 (4blocks, block 124th-127th)
0	1	0	0	4 (8blocks, block 120th-127th)
0	1	0	1	5 (16blocks, block 112th-127th)
0	1	1	0	6 (32blocks, block 96th-127th)
0	1	1	1	7 (64blocks, block 64th-127th)
1	0	0	0	8 (128blocks, protect all)
1	0	0	1	9 (128blocks, protect all)
1	0	1	0	10 (128blocks, protect all)
1	0	1	1	11 (128blocks, protect all)
1	1	0	0	12 (128blocks, protect all)
1	1	0	1	13 (128blocks, protect all)
1	1	1	0	14 (128blocks, protect all)
1	1	1	1	15 (128blocks, protect all)

Protected Area Sizes (TB bit = 1)

Status bit				Protect Level
BP3	BP2	BP1	BP0	64Mb
0	0	0	0	0 (none)
0	0	0	1	1 (1block, block 0th)
0	0	1	0	2 (2blocks, block 0th-1st)
0	0	1	1	3 (4blocks, block 0th-3rd)
0	1	0	0	4 (8blocks, block 0th-7th)
0	1	0	1	5 (16blocks, block 0th-15th)
0	1	1	0	6 (32blocks, block 0th-31st)
0	1	1	1	7 (64blocks, block 0th-63rd)
1	0	0	0	8 (128blocks, protect all)
1	0	0	1	9 (128blocks, protect all)
1	0	1	0	10 (128blocks, protect all)
1	0	1	1	11 (128blocks, protect all)
1	1	0	0	12 (128blocks, protect all)
1	1	0	1	13 (128blocks, protect all)
1	1	1	0	14 (128blocks, protect all)
1	1	1	1	15 (128blocks, protect all)

Note: The device is ready to accept a Chip Erase instruction if, and only if, all Block Protect (BP3, BP2, BP1, BP0) are 0.

II. Additional 4K-bit secured OTP for unique identifier: to provide 4K-bit One-Time Program area for setting device unique serial number - Which may be set by factory or system maker.

- Security register bit 0 indicates whether the chip is locked by factory or not.
- To program the 4K-bit secured OTP by entering 4K-bit secured OTP mode (with ENSO command), and going through normal program procedure, and then exiting 4K-bit secured OTP mode by writing EXSO command.
- Customer may lock-down the customer lockable secured OTP by writing WRSCUR(write security register) command to set customer lock-down bit1 as "1". Please refer to table of *"Table 8. Security Register Definition"* for security register bit definition and table of *"Table 3. 4K-bit Secured OTP Definition"* for address range definition.

Note: Once lock-down whatever by factory or customer, it cannot be changed any more. While in 4K-bit Secured OTP mode, array access is not allowed.

Table 3. 4K-bit Secured OTP Definition

Address range	Size	Standard Factory Lock	Customer Lock
xxx000~xxx00F	128-bit	ESN (electrical serial number)	Determined by customer
xxx010~xxx1FF	3968-bit	N/A	

7. MEMORY ORGANIZATION

Table 4. Memory Organization

individual 16 sectors lock/unlock unit:4K-byte

individual block lock/unlock unit:64K-byte

Block(64K-byte)	Block(32K-byte)	Sector (4K-byte)	Address Range	
127	255	2047	7FF000h	7FFFFFh
		⋮		
		2040	7F8000h	7F8FFFh
	254	2039	7F7000h	7F7FFFh
		⋮		
		2032	7F0000h	7F0FFFh
126	253	2031	7EF000h	7EFFFFh
		⋮		
		2024	7E8000h	7E8FFFh
	252	2023	7E7000h	7E7FFFh
		⋮		
		2016	7E0000h	7E0FFFh
125	251	2015	7DF000h	7DFFFFh
		⋮		
		2008	7D8000h	7D8FFFh
	250	2007	7D7000h	7D7FFFh
		⋮		
		2000	7D0000h	7D0FFFh

individual block lock/unlock unit:64K-byte

2	5	47	02F000h	02FFFFh
		⋮		
		40	028000h	028FFFh
	4	39	027000h	027FFFh
		⋮		
		32	020000h	020FFFh
1	3	31	01F000h	01FFFFh
		⋮		
		24	018000h	018FFFh
	2	23	017000h	017FFFh
		⋮		
		16	010000h	010FFFh
0	1	15	00F000h	00FFFFh
		⋮		
		8	008000h	008FFFh
	0	7	007000h	007FFFh
		⋮		
		0	000000h	000FFFh

individual block lock/unlock unit:64K-byte

individual 16 sectors lock/unlock unit:4K-byte

8. DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.

2. When incorrect command is inputted to this LSI, this LSI becomes standby mode and keeps the standby mode until next CS# falling edge. In standby mode, SO pin of this LSI should be High-Z.

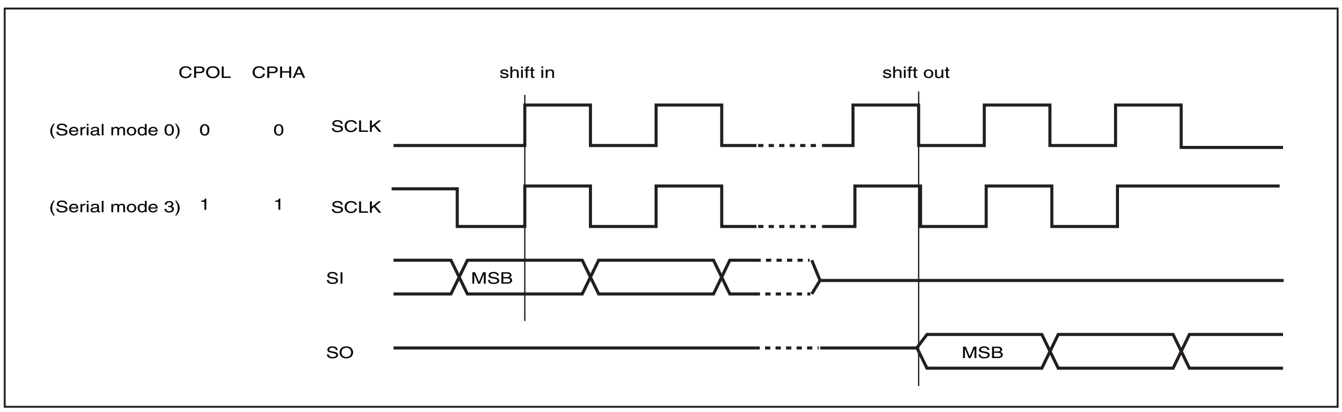
3. When correct command is inputted to this LSI, this LSI becomes active mode and keeps the active mode until next CS# rising edge.

4. For standard single data rate serial mode, input data is latched on the rising edge of Serial Clock(SCLK) and data shifts out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown as *"Figure 1. Serial Modes Supported (for Normal Serial mode)"*.

5. For the following instructions: RDID, RDSR, RDSCUR, READ, FAST_READ, RDSFDP, 2READ, DREAD, 4READ, QREAD, RDBLOCK, RES, REMS, REMS2, and REMS4 the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, SE, BE, BE32K, HPM, CE, PP, CP, 4PP, RDP, DP, WPSEL, SBLK, SBULK, GBLK, GBULK, ENSO, EXSO, WRSCUR, ESRY and DSRY. The CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

6. During the progress of Write Status Register, Program, Erase operation, to access the memory array is neglected and not affect the current operation of Write Status Register, Program, Erase.

Figure 1. Serial Modes Supported (for Normal Serial mode)



Note:
CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

9. COMMAND DESCRIPTION

Table 5. Command Sets

Read Commands

I/O	1	1	1	2	2	4	4
Command	READ (normal read)	FAST READ (fast read data)	RDSFDP (Read SFDP)	2READ (2 x I/O read command)	DREAD (1I / 2O read command)	W4READ	4READ (4 x I/O read command)
1st byte	03 (hex)	0B (hex)	5A (hex)	BB (hex)	3B (hex)	E7 (hex)	EB (hex)
2nd byte	AD1(8)	AD1(8)	AD1	AD1(4)	AD1(8)	AD1(2)	AD1(2)
3rd byte	AD2(8)	AD2(8)	AD2	AD2(4)	AD2(8)	AD2(2)	AD2(2)
4th byte	AD3(8)	AD3(8)	AD3	AD3(4)	AD3(8)	AD3(2)	AD3(2)
5th byte		Dummy(8)	Dummy	Dummy(4)	Dummy(8)	Dummy(4)	Dummy*
Action	n bytes read out until CS# goes high	n bytes read out until CS# goes high	Read SFDP mode	n bytes read out by 2 x I/O until CS# goes high		Quad I/O read with 4 dummy cycles	Quad I/O read with configurable dummy cycles

I/O	4
Command	QREAD
1st byte	6B (hex)
2nd byte	AD1(8)
3rd byte	AD2(8)
4th byte	AD3(8)
5th byte	Dummy(8)
Action	

Note: *Dummy cycle number will be different, depending on the bit7 (DC) setting of Configuration Register. Please refer to *"Configuration Register"* Table

Other Commands

Command	WREN (write enable)	WRDI (write disable)	RDSR (read status register)	RDCR (read configuration register)	WRSR (write status/ configuration register)	4PP (quad page program)	SE (sector erase)
1st byte	06 (hex)	04 (hex)	05 (hex)	15 (hex)	01 (hex)	38 (hex)	20 (hex)
2nd byte					Values	AD1	AD1
3rd byte					Values	AD2	AD2
4th byte						AD3	AD3
Action	sets the (WEL) write enable latch bit	resets the (WEL) write enable latch bit	to read out the values of the status register	to read out the values of the configuration register	to write new values of the status register	quad input to program the selected page	to erase the selected sector

Command	BE 32K (block erase 32KB)	BE (block erase 64KB)	CE (chip erase)	PP (page program)	CP (continuous program)	DP (Deep power down)	RDP (Release from deep power down)
1st byte	52 (hex)	D8 (hex)	60 or C7 (hex)	02 (hex)	AD (hex)	B9 (hex)	AB (hex)
2nd byte	AD1	AD1		AD1	AD1		
3rd byte	AD2	AD2		AD2	AD2		
4th byte	AD3	AD3		AD3	AD3		
Action	to erase the selected 32KB block	to erase the selected 64KB block	to erase whole chip	to program the selected page	continuously program whole chip, the address is automatically increase	enters deep power down mode	release from deep power down mode

Command	RDID (read identific-ation)	RES (read electronic ID)	REMS (read electronic manufacturer & device ID)	REMS2 (read electronic manufacturer & device ID)	REMS4 (read electronic manufacturer & device ID)	ENSO (enter secured OTP)
1st byte	9F (hex)	AB (hex)	90 (hex)	EF (hex)	DF (hex)	B1 (hex)
2nd byte		x	x	x	x	
3rd byte		x	x	x	x	
4th byte		x	ADD (Note 2)	ADD	ADD	
Action	outputs JEDEC ID: 1-byte Manufacturer ID & 2-byte Device ID	to read out 1-byte Device ID	output the Manufacturer ID & Device ID	output the Manufacturer ID & Device ID	output the Manufacturer ID & device ID	to enter the 4K-bit secured OTP mode

Command	EXSO (exit secured OTP)	RDSCUR (read security register)	WRSCUR (write security register)	SBLK (single block lock	SBULK (single block unlock)	RDBLOCK (block protect read)	GBLK (gang block lock)
1st byte	C1 (hex)	2B (hex)	2F (hex)	36 (hex)	39 (hex)	3C (hex)	7E (hex)
2nd byte				AD1	AD1	AD1	
3rd byte				AD2	AD2	AD2	
4th byte				AD3	AD3	AD3	
Action	to exit the 4K-bit secured OTP mode	to read value of security register	to set the lock-down bit as "1" (once lock-down, cannot be update)	individual block (64K-byte) or sector (4K-byte) write protect	individual block (64K-byte) or sector (4K-byte) unprotect	read individual block or sector write protect status	whole chip write protect

COMMAND	GBULK (gang block unlock)	NOP (No Operation)	RSTEN (Reset Enable)	RST (Reset Memory)	WPSEL (Write Protect Selection)	ESRY (enable SO to output RY/BY#)	DSRY (disable SO to output RY/BY#)
1st byte	98 (hex)	00 (hex)	66 (hex)	99 (hex)	68 (hex)	70 (hex)	80 (hex)
2nd byte							
3rd byte							
4th byte							
Action	whole chip unprotect				to enter and enable individal block protect mode	to enable SO to output RY/BY# during CP mode	to disable SO to output RY/BY# during CP mode

COMMAND	Release Read Enhanced
1st byte	FF (hex)
2nd byte	
3rd byte	
4th byte	
5th byte	
Action	All these commands FFh, 00h, AAh or 55h will escape the performance mode

Note 1: The count base is 4-bit for ADD(2) and Dummy(2) because of 2 x I/O. And the MSB is on SI/SIO1 which is different from 1 x I/O condition.

Note 2: ADD=00H will output the manufacturer ID first and ADD=01H will output device ID first.

Note 3: It is not recommended to adopt any other code not in the command definition table, which will potentially enter the hidden mode.

Note 4: Before executing RST command, RSTEN command must be executed. If there is any other command to interfere, the reset operation will be disabled.

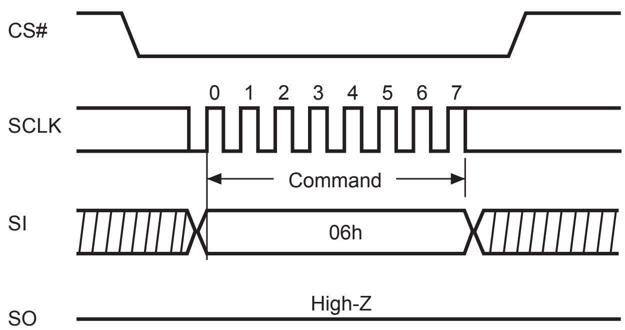
9-1. Write Enable (WREN)

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP, 4PP, CP, SE, BE, BE32K, CE, WRSR, WRSCUR, WPSEL, SBLK, SBULK, GBLK and GBULK, which are intended to change the device content, should be set every time after the WREN instruction setting the WEL bit.

The sequence of issuing WREN instruction is: CS# goes low→ sending WREN instruction code→ CS# goes high.

The SIO[3:1] are don't care in this mode.

Figure 2. Write Enable (WREN) Sequence (Command 06)



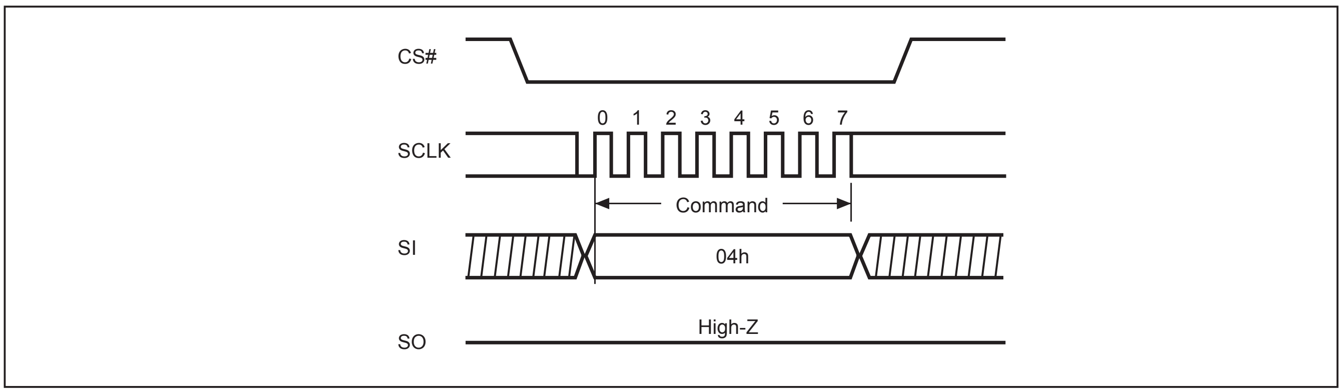
9-2. Write Disable (WRDI)

The Write Disable (WRDI) instruction is for resetting Write Enable Latch (WEL) bit.
The sequence of issuing WRDI instruction is: CS# goes low→ sending WRDI instruction code→ CS# goes high.

The WEL bit is reset by following situations:

- Power-up
- Write Disable (WRDI) instruction completion
- Write Status/Configuration Register (WRSR) instruction completion
- Page Program (PP, 4PP) instruction completion
- Sector Erase (SE) instruction completion
- Block Erase (BE, BE32K) instruction completion
- Chip Erase (CE) instruction completion
- Continuous Program mode (CP) instruction completion
- Single Block Lock/Unlock (SBLK/SBULK) instruction completion
- Gang Block Lock/Unlock (GBLK/GBULK) instruction completion

Figure 3. Write Disable (WRDI) Sequence (Command 04)



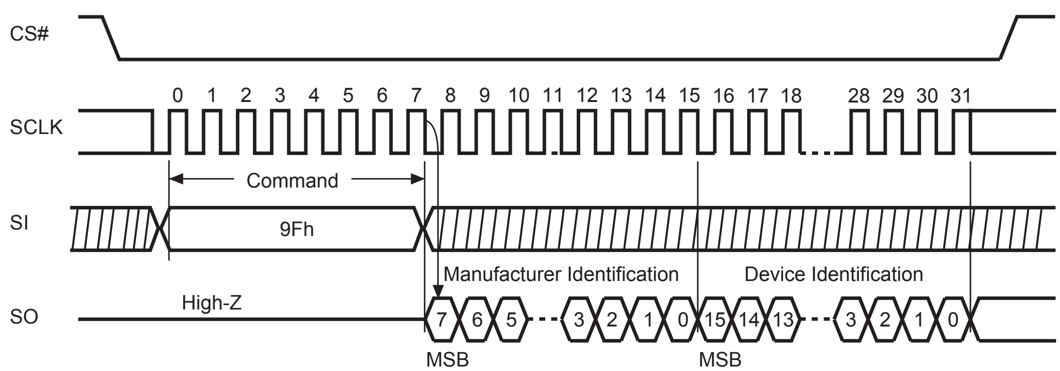
9-3. Read Identification (RDID)

The RDID instruction is for reading the Manufacturer ID of 1-byte and followed by Device ID of 2-byte.
The Macronix Manufacturer ID is C2(hex), the memory type ID is 20(hex) as the first-byte Device ID, and the individual Device ID of second-byte ID are listed as table of *"Table 7. ID Definitions"*.

The sequence of issuing RDID instruction is: CS# goes low→ sending RDID instruction code → 24-bits ID data out on SO→ to end RDID operation can use CS# to high at any time during data out.

While Program/Erase operation is in progress, it will not decode the RDID instruction, so there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

Figure 4. Read Identification (RDID) Sequence (Command 9F)



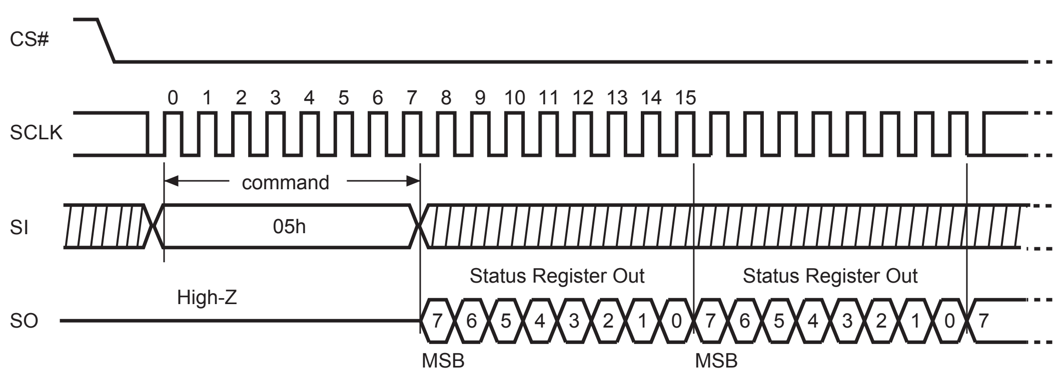
9-4. Read Status Register (RDSR)

The RDSR instruction is for reading Status Register. The Read Status Register can be read at any time (even in program/erase/write status register condition) and continuously. It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress.

The sequence of issuing RDSR instruction is: CS# goes low→ sending RDSR instruction code→ Status Register data out on SO.

The SIO[3:1] are don't care when during this mode.

Figure 5. Read Status Register (RDSR) Sequence (Command 05)



The definition of the status register bits is as below:

WIP bit. The Write in Progress (WIP) bit, a volatile bit, indicates whether the device is busy in program/erase/write status register progress. When WIP bit sets to 1, which means the device is busy in program/erase/write status register progress. When WIP bit sets to 0, which means the device is not in progress of program/erase/write status register cycle.

WEL bit. The Write Enable Latch (WEL) bit, a volatile bit, indicates whether the device is set to internal write enable latch. When WEL bit sets to "1", which means the internal write enable latch is set, the device can accept program/erase/write status register instruction. When WEL bit sets to 0, which means no internal write enable latch; the device will not accept program/erase/write status register instruction. The program/erase command will be ignored and will reset WEL bit if it is applied to a protected memory area. To ensure both WIP bit & WEL bit are both set to 0 and available for next program/erase/operations, WIP bit needs to be confirm to be 0 before polling WEL bit. After WIP bit confirmed, WEL bit needs to be confirm to be 0.

BP3, BP2, BP1, BP0 bits. The Block Protect (BP3, BP2, BP1, BP0) bits, non-volatile bits, indicate the protected area (as defined in *"Table 2. Protected Area Sizes"*) of the device to against the program/erase instruction without hardware protection mode being set. To write the Block Protect (BP3, BP2, BP1, BP0) bits requires the Write Status Register (WRSR) instruction to be executed. Those bits define the protected area of the memory to against Page Program (PP), Sector Erase (SE), Block Erase (BE) and Chip Erase (CE) instructions (only if all Block Protect bits set to 0, the CE instruction can be executed). The BP3, BP2, BP1, BP0 bits are "0" as default. Which is un-protected.

QE bit. The Quad Enable (QE) bit, a non-volatile bit which is permanently set to "1". The flash always performs Quad I/O mode.

SRWD bit. The Status Register Write Disable (SRWD) bit, non-volatile bit, default value is "0".

Status Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SRWD (status register write protect)	QE (Quad Enable)	BP3 (level of protected block)	BP2 (level of protected block)	BP1 (level of protected block)	BP0 (level of protected block)	WEL (write enable latch)	WIP (write in progress bit)
1=status register write disable 0=status register write enable	1= Quad Enable	(note 1)	(note 1)	(note 1)	(note 1)	1=write enable 0=not write enable	1=write operation 0=not in write operation
Non-volatile bit		Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

Note: See the *"Table 2. Protected Area Sizes"* .

Configuration Register

The Configuration Register is able to change the default status of Flash memory. Flash memory will be configured after the CR bit is set.

TB bit

The Top/Bottom (TB) bit is a non-volatile OTP bit. The Top/Bottom (TB) bit is used to configure the Block Protect area by BP bit (BP3, BP2, BP1, BP0), starting from TOP or Bottom of the memory array. The TB bit is defaulted as “0”, which means Top area protect. When it is set as “1”, the protect area will change to Bottom area of the memory device. To write the TB bits requires the Write Status Register (WRSR) instruction to be executed.

Configuration Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DC (Dummy Cycle)	Reserved	Reserved	Reserved	TB (top/bottom selected)	Reserved	Reserved	Reserved
(Note)	x	x	x	0=Top area protect 1=Bottom area protect (Default=0)	x	x	x
Volatile bit	x	x	x	OTP	x	x	x

Note: See *"Dummy Cycle and Frequency Table"*, with "Don't Care" on other Reserved Configuration Registers.

Dummy Cycle and Frequency Table

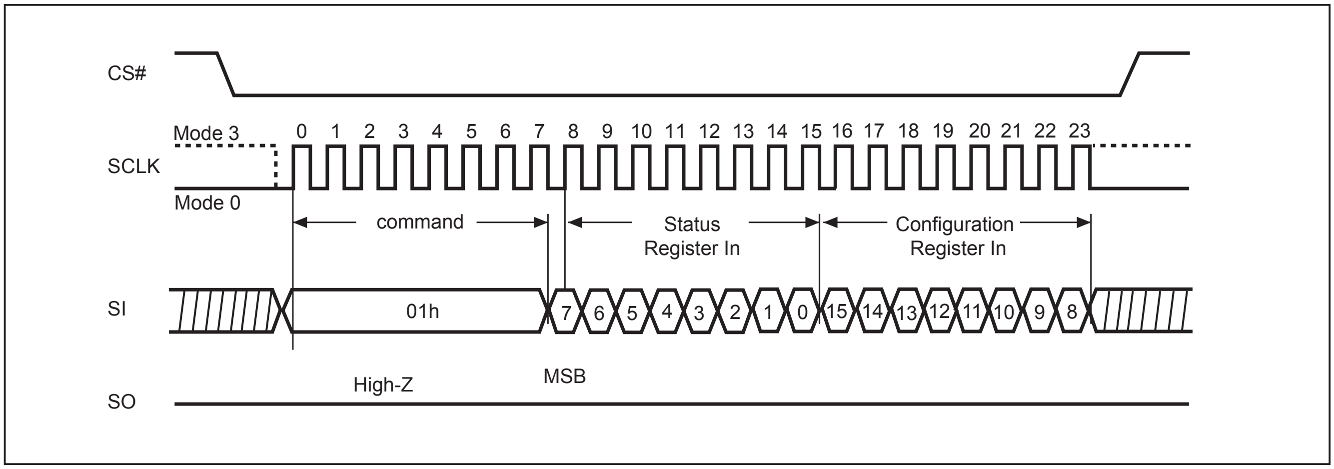
DC	Numbers of Dummy clock cycles	Quad I/O Fast Read
1	8	104
0 (default)	6	86

9-5. Write Status Register (WRSR)

The WRSR instruction is for changing the values of Status Register Bits and Configuration Register Bits. Before sending WRSR instruction, the Write Enable (WREN) instruction must be decoded and executed to set the Write Enable Latch (WEL) bit in advance. The WRSR instruction can change the value of Block Protect (BP3, BP2, BP1, BP0) bits to define the protected area of memory (as shown in *"Table 2. Protected Area Sizes"*). The WRSR can reset the Status Register Write Disable (SRWD) bit, but has no effect on bit1 (WEL) and bit0 (WIP) of the status register.

The sequence of issuing WRSR instruction is: CS# goes low→ sending WRSR instruction code→ Status Register data on SI→ CS# goes high.

Figure 6. Write Status Register (WRSR) Sequence (Command 01)



The CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked out during the Write Status Register cycle is in progress. The WIP sets 1 during the tW timing, and sets 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

Table 6. Protection Modes

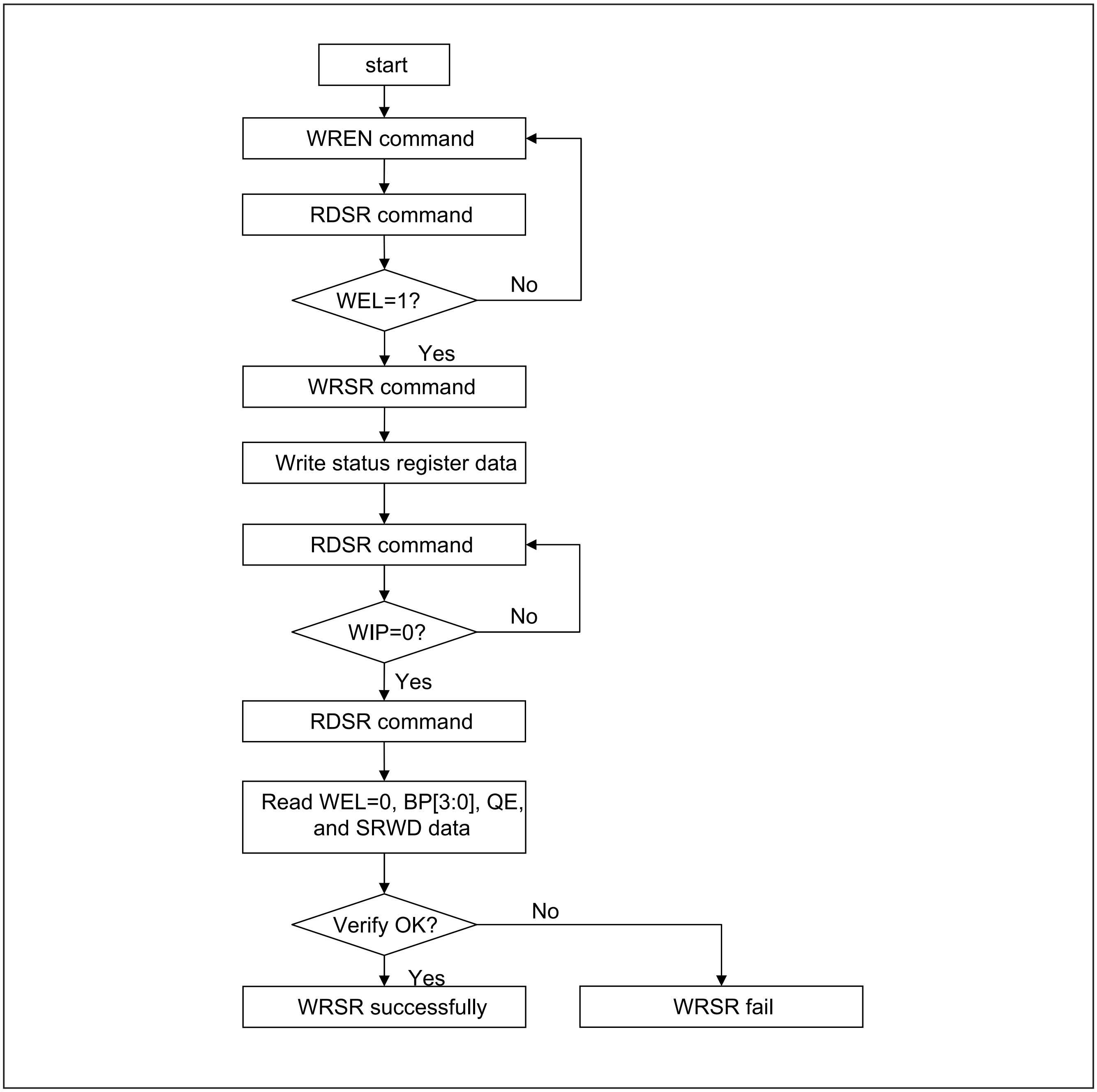
Mode	Status register condition	SRWD bit status	Memory
Software protection mode (SPM)	Status register can be written in (WEL bit is set to "1") and the SRWD, BP0-BP3 bits can be changed	SRWD bit=0	The protected area cannot be programmed or erased.

Note: As defined by the values in the Block Protect (BP3, BP2, BP1, BP0) bits of the Status Register, as shown in *"Table 2. Protected Area Sizes"*.

Software Protected Mode (SPM):

- When SRWD bit=0, the WREN instruction may set the WEL bit and can change the values of SRWD, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0, is at software protected mode (SPM).

Figure 7. WRSR flow

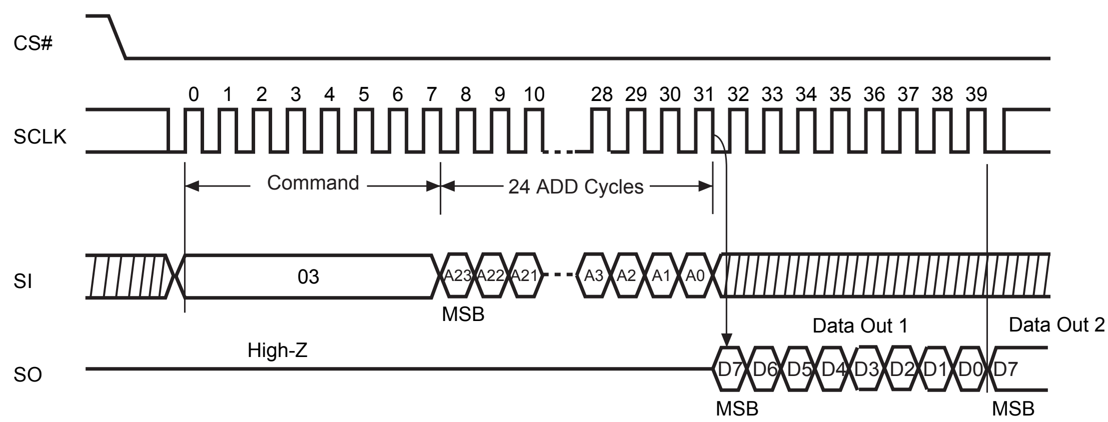


9-6. Read Data Bytes (READ)

The read instruction is for reading data out. The address is latched on rising edge of SCLK, and data shifts out on the falling edge of SCLK at a maximum frequency fR. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing READ instruction is: CS# goes low→ sending READ instruction code→3-byte address on SI →data out on SO→ to end READ operation can use CS# to high at any time during data out.

Figure 8. Read Data Bytes (READ) Sequence (Command 03)



9-7. Read Data Bytes at Higher Speed (FAST_READ)

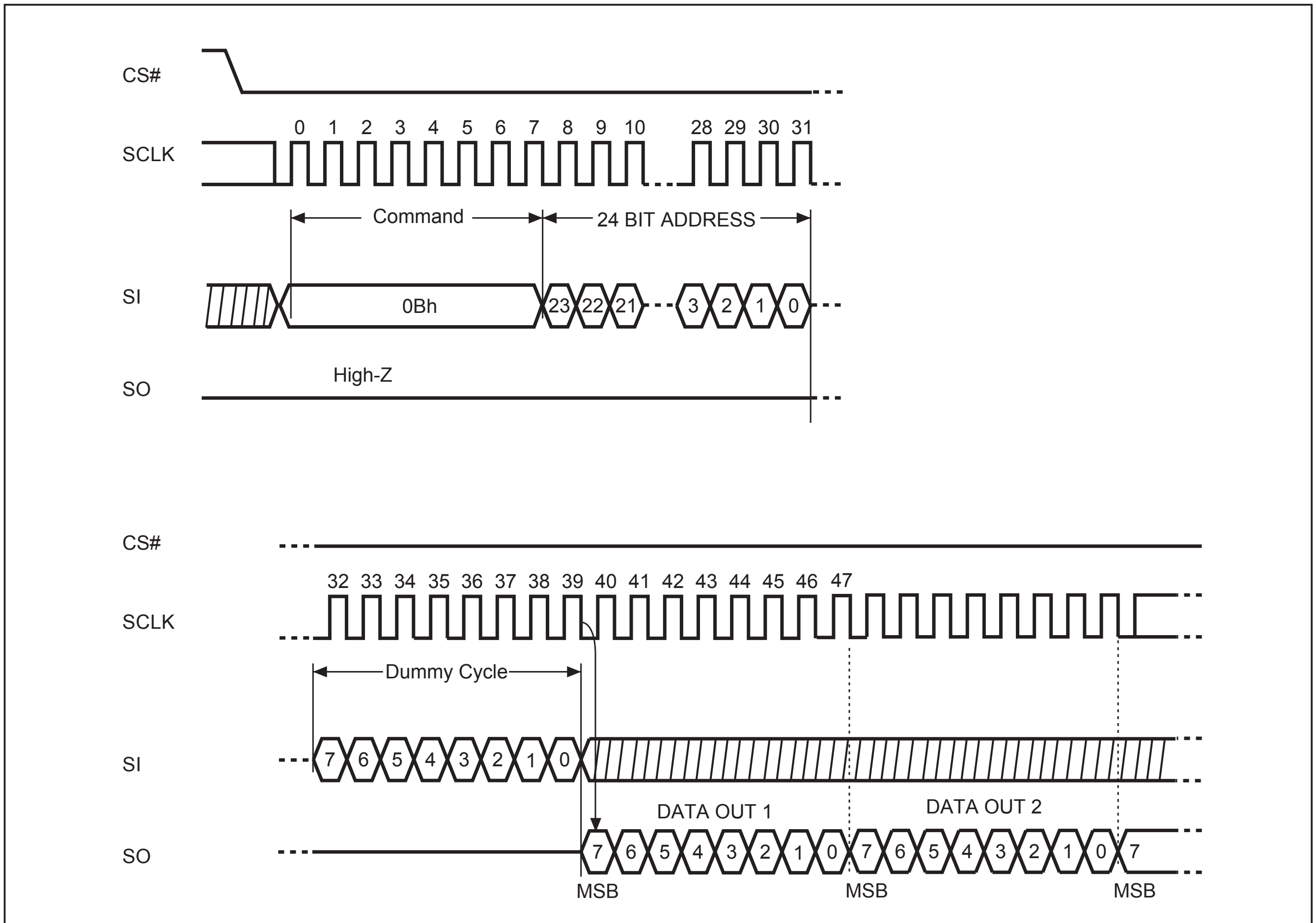
The FAST_READ instruction is for quickly reading data out. The address is latched on rising edge of SCLK, and data of each bit shifts out on the falling edge of SCLK at a maximum frequency fC. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FAST_READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing FAST_READ instruction is: CS# goes low→ sending FAST_READ instruction code→ 3-byte address on SI→1-dummy byte (default) address on SI→ data out on SO→ to end FAST_READ operation can use CS# to high at any time during data out.

In the performance-enhancing mode, P[7:4] must be toggling with P[3:0] ; likewise P[7:0]=A5h,5Ah,F0h or 0Fh can make this mode continue and reduce the next 4READ instruction. Once P[7:4] is no longer toggling with P[3:0]; likewise P[7:0]=FFh,00h,AAh or 55h and afterwards CS# is raised and then lowered, the system then will escape from performance enhance mode and return to normal operation.

While Program/Erase/Write Status Register cycle is in progress, FAST_READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 9. Read at Higher Speed (FAST_READ) Sequence (Command 0B) (104MHz)



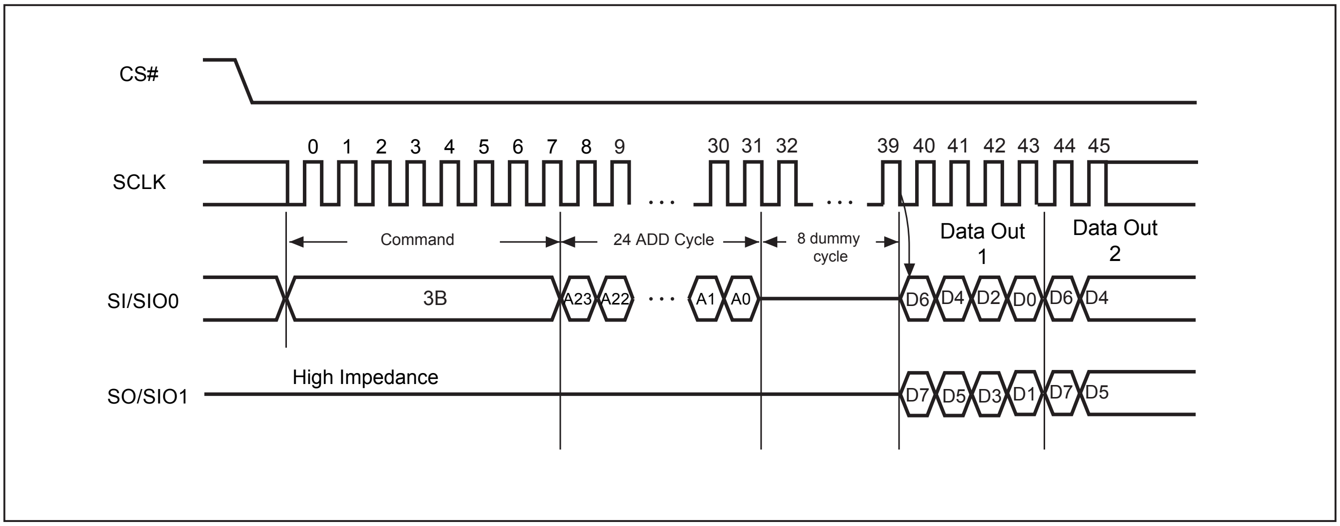
9-8. Dual Read Mode (DREAD)

The DREAD instruction enable double throughput of Serial Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single DREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing DREAD instruction, the following data out will perform as 2-bit instead of previous 1-bit.

The sequence of issuing DREAD instruction is: CS# goes low → sending DREAD instruction → 3-byte address on SI → 8-bit dummy cycle → data out interleave on SO1 & SO0 → to end DREAD operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, DREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 10. Dual Read Mode Sequence (Command 3B)



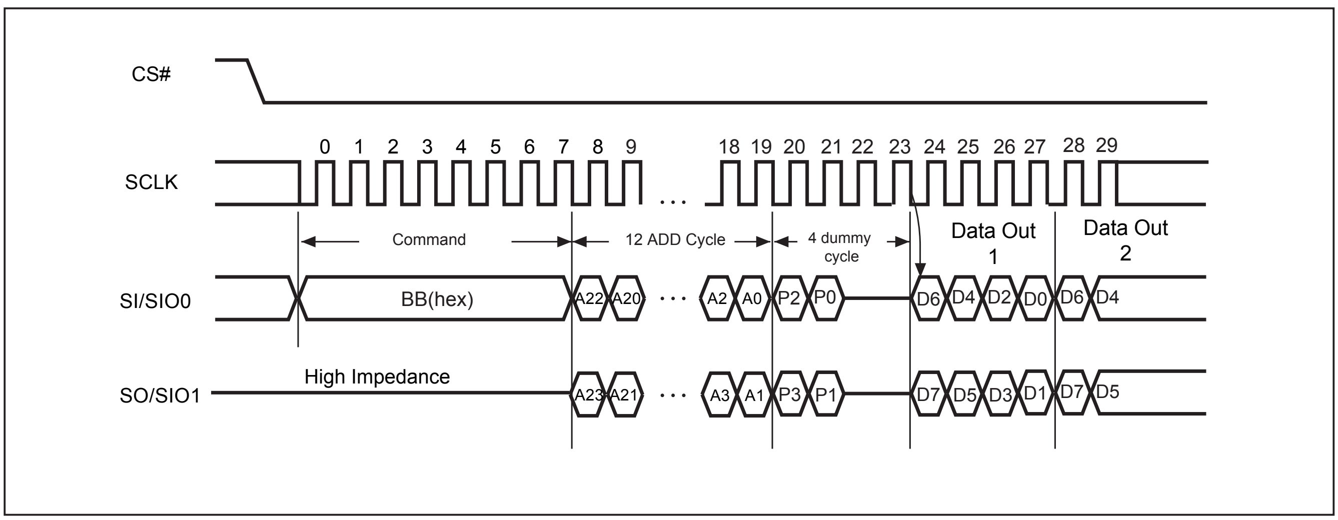
9-9. 2 x I/O Read Mode (2READ)

The 2READ instruction enables Double Transfer Rate of Serial Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 2READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 2READ instruction, the following address/dummy/data out will perform as 2-bit instead of previous 1-bit.

The sequence of issuing 2READ instruction is: CS# goes low→ sending 2READ instruction→ 24-bit address interleave on SIO1 & SIO0→ 4-bit dummy cycle on SIO1 & SIO0→ data out interleave on SIO1 & SIO0→ to end 2READ operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, 2READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 11. 2 x I/O Read Mode Sequence (Command BB)



Note: SI/SIO0 or SO/SIO1 should be kept "0h" or "Fh" in the first two dummy cycles. In other words, P2=P0 or P3=P1 is necessary.

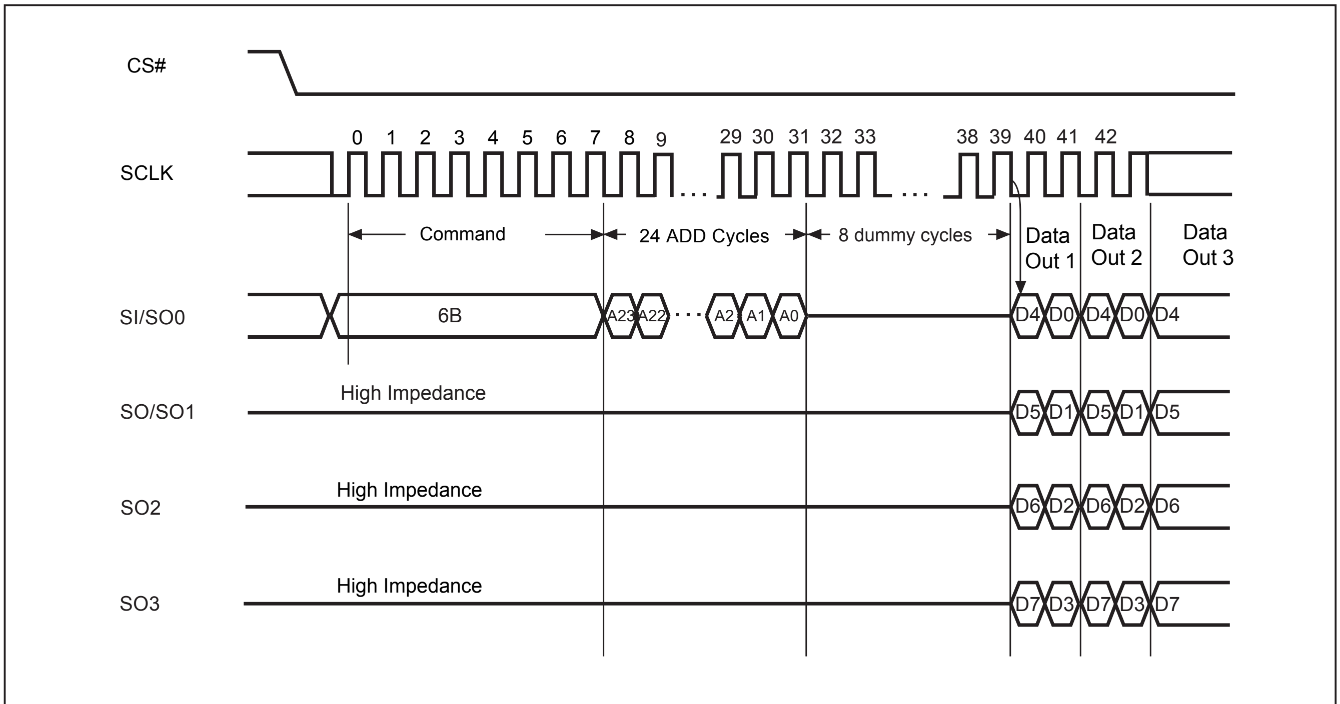
9-10. Quad Read Mode (QREAD)

The QREAD instruction enable quad throughput of Serial Flash in read mode. The address is latched on rising edge of SCLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fQ. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single QREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing QREAD instruction, the following data out will perform as 4-bit instead of previous 1-bit.

The sequence of issuing QREAD instruction is: CS# goes low→ sending QREAD instruction → 3-byte address on SI → 8-bit dummy cycle → data out interleave on SO3, SO2, SO1 & SO0→ to end QREAD operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, QREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 12. Quad Read Mode Sequence (Command 6B)



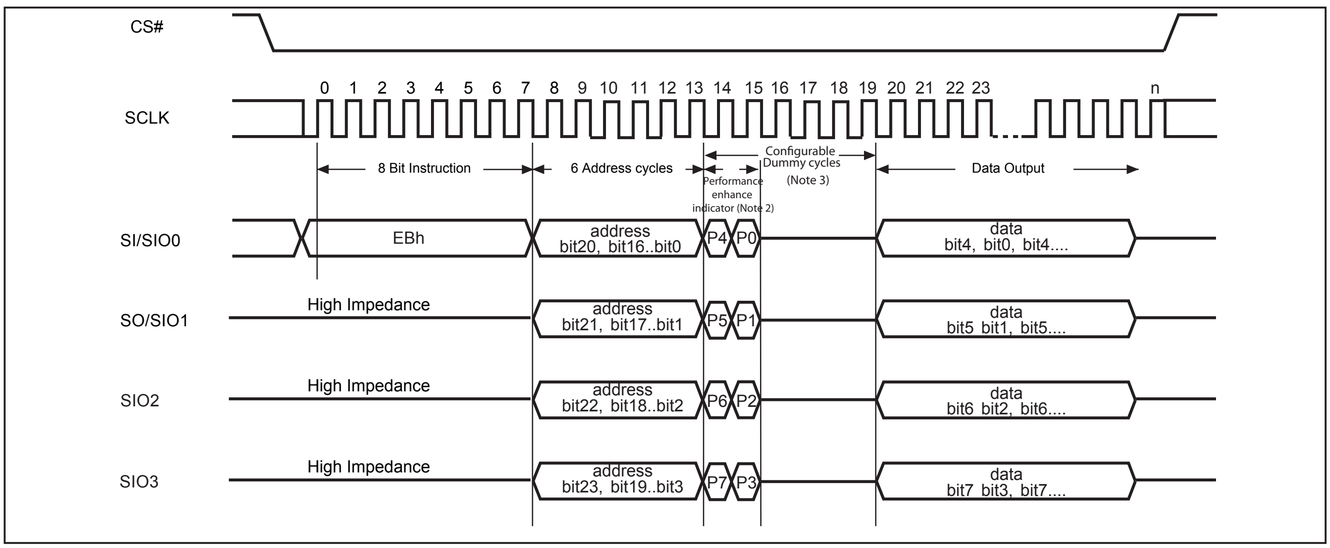
9-11. 4 x I/O Read Mode (4READ)

The 4READ instruction enables quad throughput of Serial Flash in read mode. The address is latched on rising edge of SCLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fQ. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 4READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 4READ instruction, the following address/dummy/data out will perform as 4-bit instead of previous 1-bit.

The sequence of issuing 4READ instruction is: CS# goes low→ sending 4READ instruction→ 24-bit address interleave on SIO3, SIO2, SIO1 & SIO0→2+4 dummy cycles (default)→data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end 4READ operation can use CS# to high at any time during data out.

W4READ instruction (E7) is also available for 4 I/O read. The sequence is similar to 4READ, but with only 4 dummy cycles. The clock rate runs at 54MHz.

Figure 13. 4 x I/O Read Mode Sequence (Command EB)



Note:
1. Hi-impedance is inhibited for the two clock cycles.
2. P7≠P3, P6≠P2, P5≠P1 & P4≠P0 (Toggling) is inhibited.
3. The Configurable Dummy Cycle is set by Configuration Register Bit. Please see *"Dummy Cycle and Frequency Table"*

Another sequence of issuing 4READ instruction especially useful in random access is : CS# goes low→ sending 4READ instruction→ 3-bytes address interleave on SIO3, SIO2, SIO1 & SIO0 →performance enhance toggling bit P[7:0]→ 4 dummy cycles (default)→ data out still CS# goes high → CS# goes low (reduce 4 Read instruction) → 24-bit random access address (Please refer to *"Figure 14. 4 x I/O Read enhance performance Mode Sequence (Command EB)"*).

In the performance-enhancing mode (Notes of *"Figure 14. 4 x I/O Read enhance performance Mode Sequence (Command EB)"*), P[7:4] must be toggling with P[3:0]; likewise P[7:0]=A5h, 5Ah, F0h or 0Fh can make this mode continue and reduce the next 4READ instruction. Once P[7:4] is no longer toggling with P[3:0]; likewise P[7:0]=FFh, 00h, AAh or 55h. These commands will reset the performance enhance mode. And afterwards CS# is raised and then lowered, the system then will return to normal operation.

While Program/Erase/Write Status Register cycle is in progress, 4READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

9-12. Performance Enhance Mode

The device could waive the command cycle bits if the two cycle bits after address cycle toggles. (Please note *"Figure 14. 4 x I/O Read enhance performance Mode Sequence (Command EB)"*)

Please be noticed that “EBh” and “E7h” commands support enhance mode. The performance enhance mode is not supported in dual I/O mode.

After entering enhance mode, following CSB go high, the device will stay in the read mode and treat CSB go low of the first clock as address instead of command cycle.

To exit enhance mode, a new fast read command whose first two dummy cycles is not toggle then exit. Or issue ”FFh” command to exit enhance mode.

9-13. Performance Enhance Mode Reset (FFh)

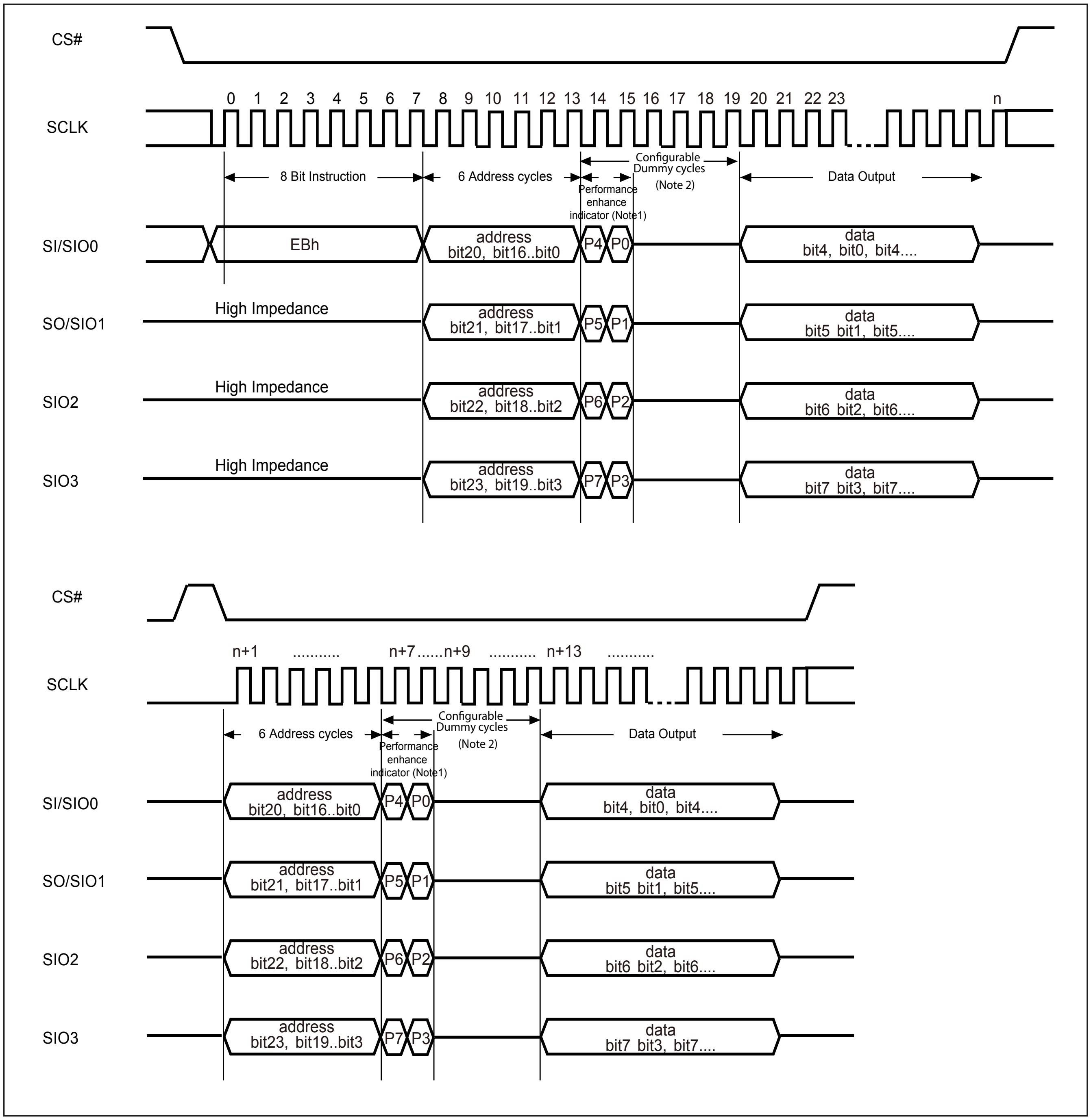
To conduct the Performance Enhance Mode Reset operation, FFh command code, 8 clocks, should be issued in 1I/O sequence.

If the system controller is being Reset during operation, the flash device will return to the standard operation.

Upon Reset of main chip, Instruction would be issued from the system. Instructions like Read ID (9Fh) or Fast Read (0Bh) would be issued.

The SIO[3:1] are don't care when during this mode.

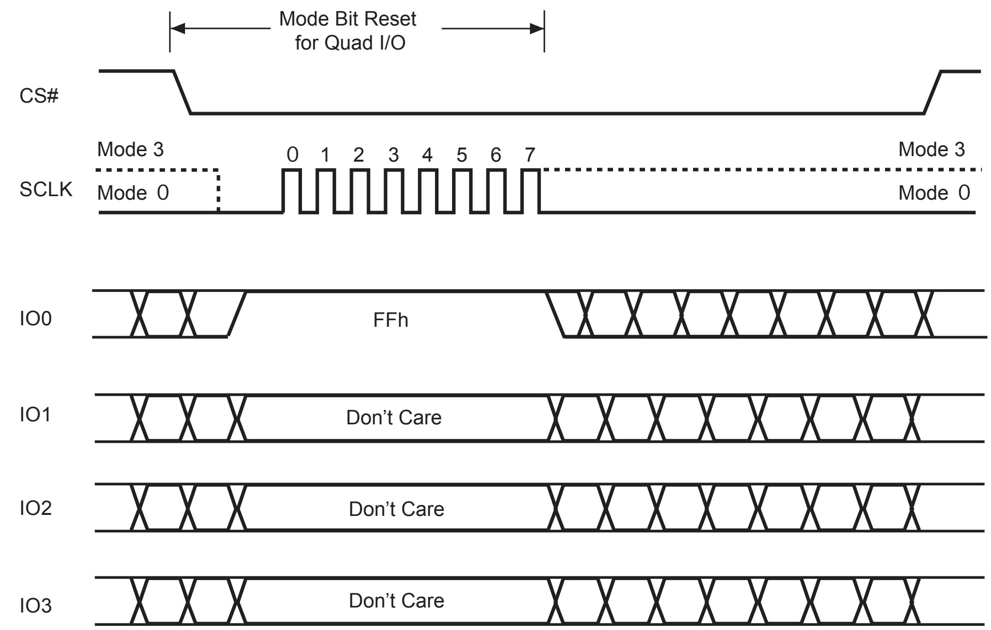
Figure 14. 4 x I/O Read enhance performance Mode Sequence (Command EB)



Note:

1. Performance enhance mode, if P7≠P3 & P6≠P2 & P5≠P1 & P4≠P0 (Toggling), ex: A5, 5A, 0F, if not using performance enhance recommend to keep 1 or 0 in performance enhance indicator.
   Reset the performance enhance mode, if P7=P3 or P6=P2 or P5=P1 or P4=P0, ex: AA, 00, FF
2. The Configurable Dummy Cycle is set by Configuration Register Bit. Please see *"Dummy Cycle and Frequency Table"*

Figure 15. Performance Enhance Mode Reset for Fast Read Quad I/O



9-14. Sector Erase (SE)

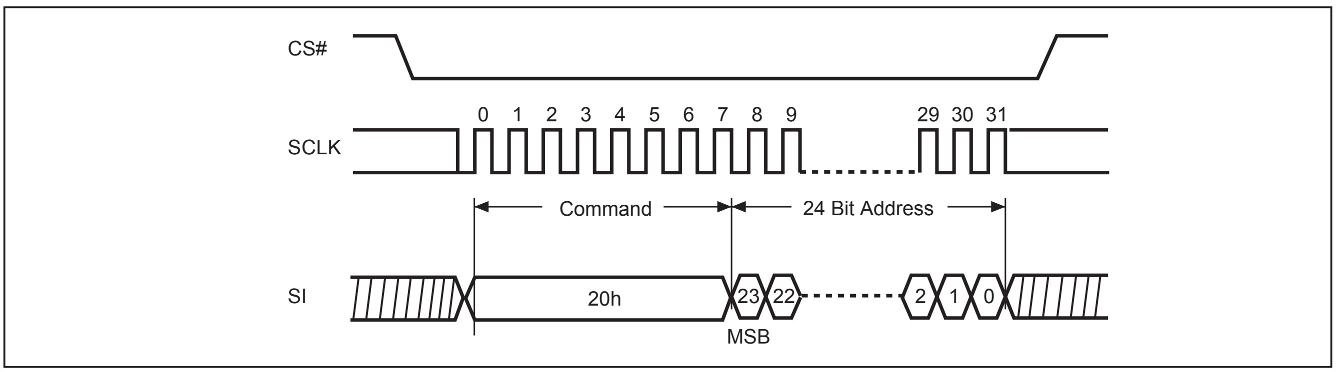
The Sector Erase (SE) instruction is for erasing the data of the chosen sector to be "1". The instruction is used for any 4K-byte sector. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Sector Erase (SE). Any address of the sector (see *"Table 4. Memory Organization"*) is a valid address for Sector Erase (SE) instruction. The CS# must go high exactly at the byte boundary (the latest eighth of address byte has been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing SE instruction is: CS# goes low → sending SE instruction code→ 3-byte address on SI →CS# goes high.

The SIO[3:1] are don't care when during this mode.

The self-timed Sector Erase Cycle time (tSE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked out during the Sector Erase cycle is in progress. The WIP sets 1 during the tSE timing, and sets 0 when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the sector is protected by BP3~0 (WPSEL=0) or by individual lock (WPSEL=1), the array data will be protected (no change) and the WEL bit still be reset.

Figure 16. Sector Erase (SE) Sequence (Command 20)



9-15. Block Erase (BE)

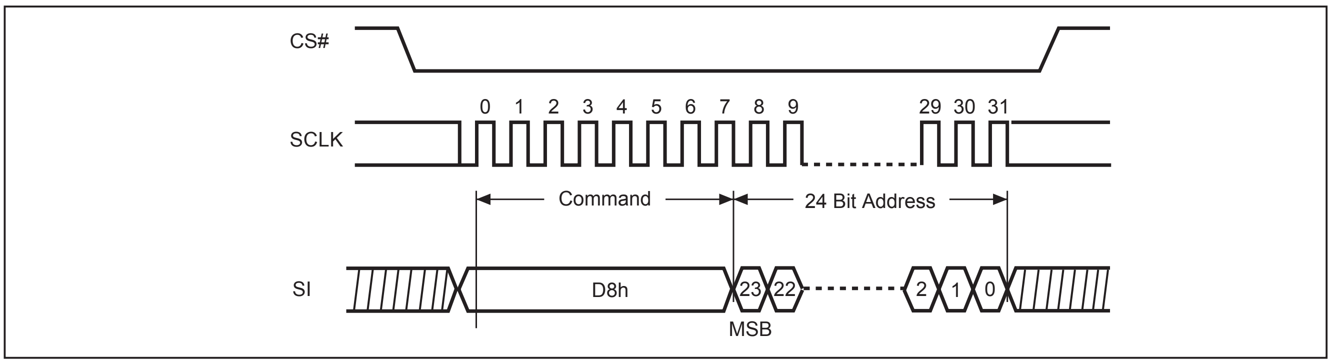
The Block Erase (BE) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 64K-byte block erase operation. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE). Any address of the block (see *"Table 4. Memory Organization"*) is a valid address for Block Erase (BE) instruction. The CS# must go high exactly at the byte boundary (the latest eighth of address byte has been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE instruction is: CS# goes low → sending BE instruction code → 3-byte address on SI → CS# goes high.

The SIO[3:1] are don't care when during this mode.

The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked out during the Sector Erase cycle is in progress. The WIP sets 1 during the tBE timing, and sets 0 when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the block is protected by BP3~0 (WPSEL=0) or by individual lock (WPSEL=1), the array data will be protected (no change) and the WEL bit still be reset.

Figure 17. Block Erase (BE) Sequence (Command D8)



9-16. Block Erase (BE32K)

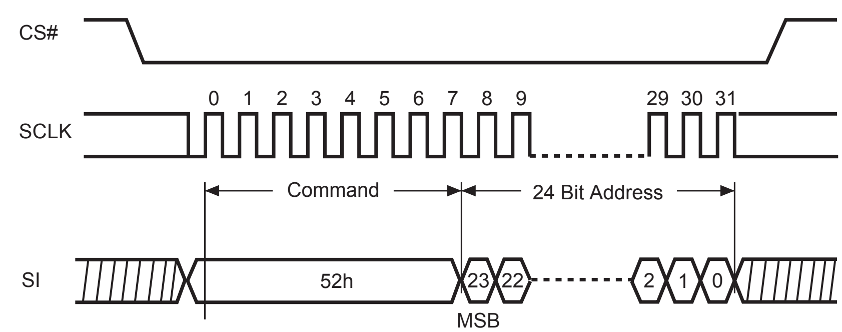
The Block Erase (BE32) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 32K-byte block erase operation. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE32). Any address of the block (see *"Table 4. Memory Organization"*) is a valid address for Block Erase (BE32) instruction. The CS# must go high exactly at the byte boundary (the latest eighth of address byte has been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE32 instruction is: CS# goes low → sending BE32 instruction code → 3-byte address on SI → CS# goes high.

The SIO[3:1] are don't care when during this mode.

The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked out during the Sector Erase cycle is in progress. The WIP sets 1 during the tBE timing, and sets 0 when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the block is protected by BP3~0 (WPSEL=0) or by individual lock (WPSEL=1), the array data will be protected (no change) and the WEL bit still be reset.

Figure 18. Block Erase 32KB (BE32K) Sequence (Command 52)



9-17. Chip Erase (CE)

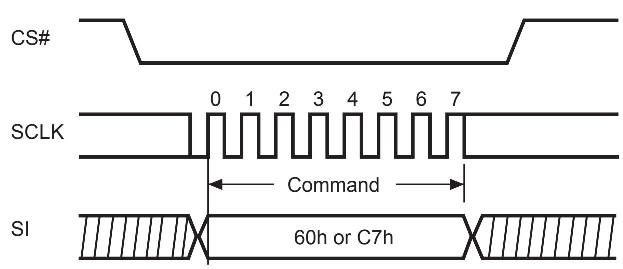
The Chip Erase (CE) instruction is for erasing the data of the whole chip to be "1". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Chip Erase (CE). The CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

The sequence of issuing CE instruction is: CS# goes low → sending CE instruction code → CS# goes high.

The SIO[3:1] are don't care when during this mode.

The self-timed Chip Erase Cycle time (tCE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked out during the Chip Erase cycle is in progress. The WIP sets 1 during the tCE timing, and sets 0 when Chip Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the chip is protected the Chip Erase (CE) instruction will not be executed, but WEL will be reset.

Figure 19. Chip Erase (CE) Sequence (Command 60 or C7)



9-18. Page Program (PP)

The Page Program (PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Page Program (PP). The device programs only the last 256 data bytes sent to the device. The last address byte (the 8 least significant address bits, A7-A0) should be set to 0 for 256 bytes page program. If A7-A0 are not all zero, transmitted data that exceed page length are programmed from the starting address (24-bit address that last 8 bit are all 0) of currently selected page. If the data bytes sent to the device exceeds 256, the last 256 data byte is programmed at the request page and previous data will be disregarded. If the data bytes sent to the device has not exceeded 256, the data will be programmed at the request address of the page. There will be no effort on the other data bytes of the same page.

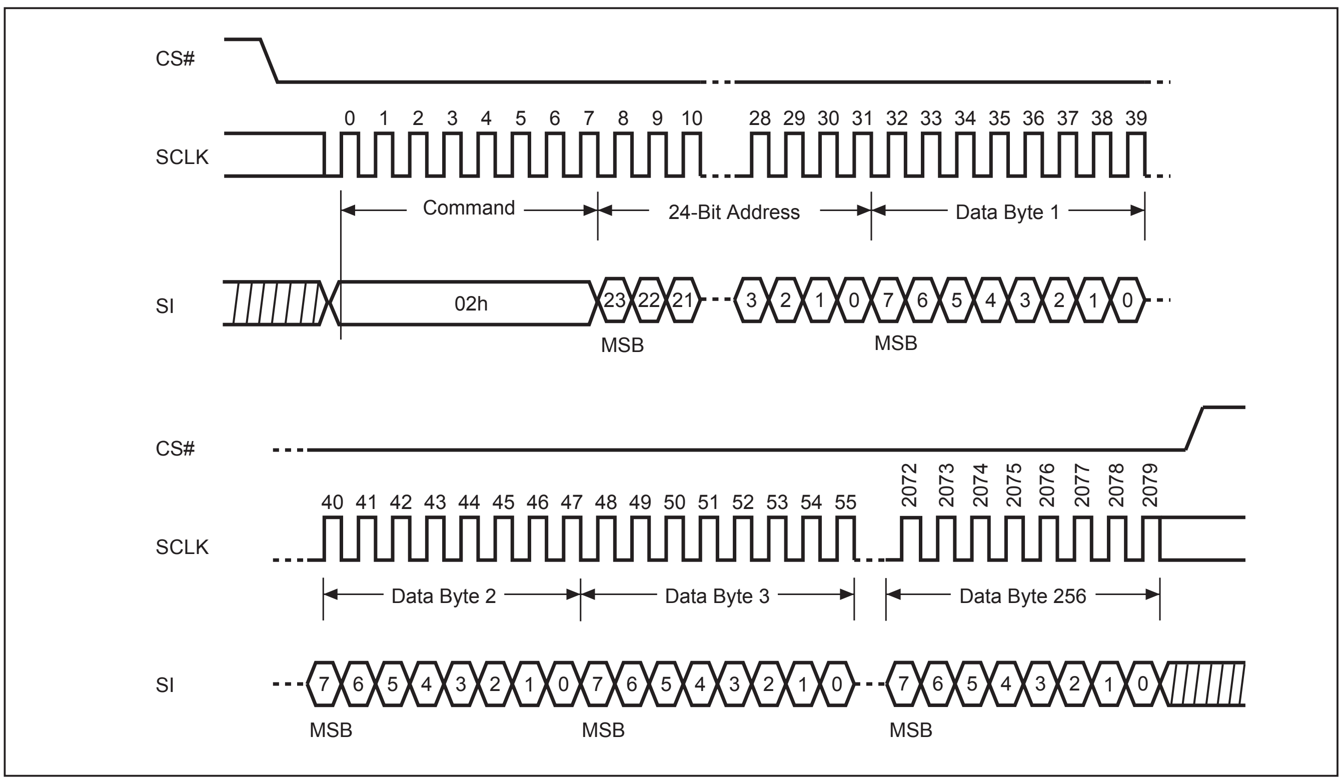
The sequence of issuing PP instruction is: CS# goes low→ sending PP instruction code→ 3-byte address on SI→ at least 1-byte on data on SI→ CS# goes high.

The CS# must be kept to low during the whole Page Program cycle; The CS# must go high exactly at the byte boundary (the latest eighth bit of data being latched in), otherwise, the instruction will be rejected and will not be executed.

The self-timed Page Program Cycle time (tPP) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked out during the Page Program cycle is in progress. The WIP sets 1 during the tPP timing, and sets 0 when Page Program Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the page is protected by BP3~0 (WPSEL=0) or by individual lock (WPSEL=1), the array data will be protected (no change) and the WEL bit will still be reset.

The SIO[3:1] are don't care when during this mode.

Figure 20. Page Program (PP) Sequence (Command 02)



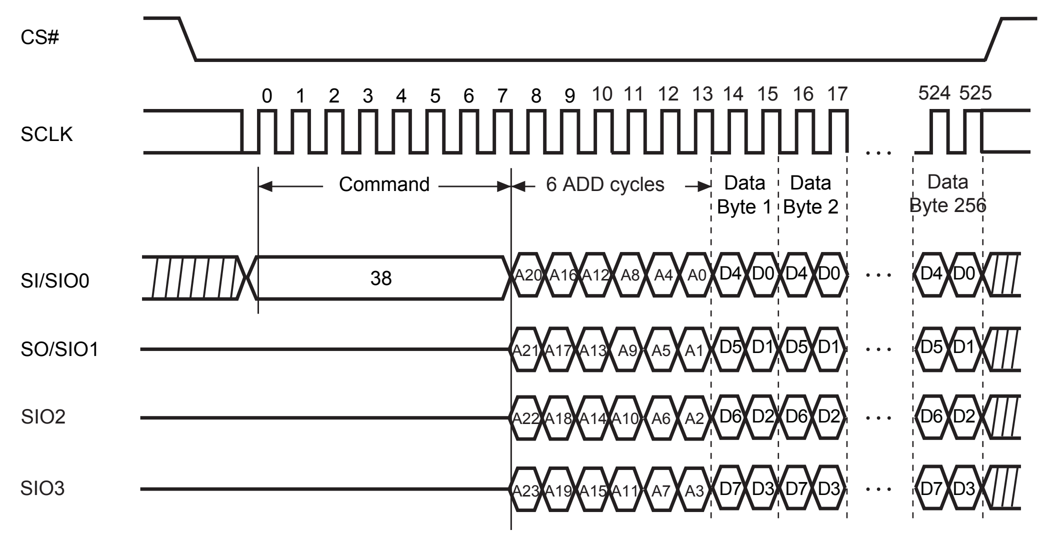
9-19. 4 x I/O Page Program (4PP)

The Quad Page Program (4PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit. The Quad Page Programming takes four pins: SIO0, SIO1, SIO2, and SIO3, which can raise programmer performance and the effectiveness of application of lower clock less than 104MHz. For system with faster clock, the Quad page program cannot provide more actual favors, because the required internal page program time is far more than the time data flows in. Therefore, we suggest that while executing this command (especially during sending data), user can slow the clock speed down to 104MHz below. The other function descriptions are as same as standard page program.

The sequence of issuing 4PP instruction is: CS# goes low→ sending 4PP instruction code→ 3-byte address on SIO[3:0]→ at least 1-byte on data on SIO[3:0]→ CS# goes high.

If the page is protected by BP3~0 (WPSEL=0) or by individual lock (WPSEL=1), the array data will be protected (no change) and the WEL bit will still be reset.

Figure 21. 4 x I/O Page Program (4PP) Sequence (Command 38)



The Program/Erase function instruction function flow is as follows:

Figure 22. Program/Erase Flow(1) with read array data

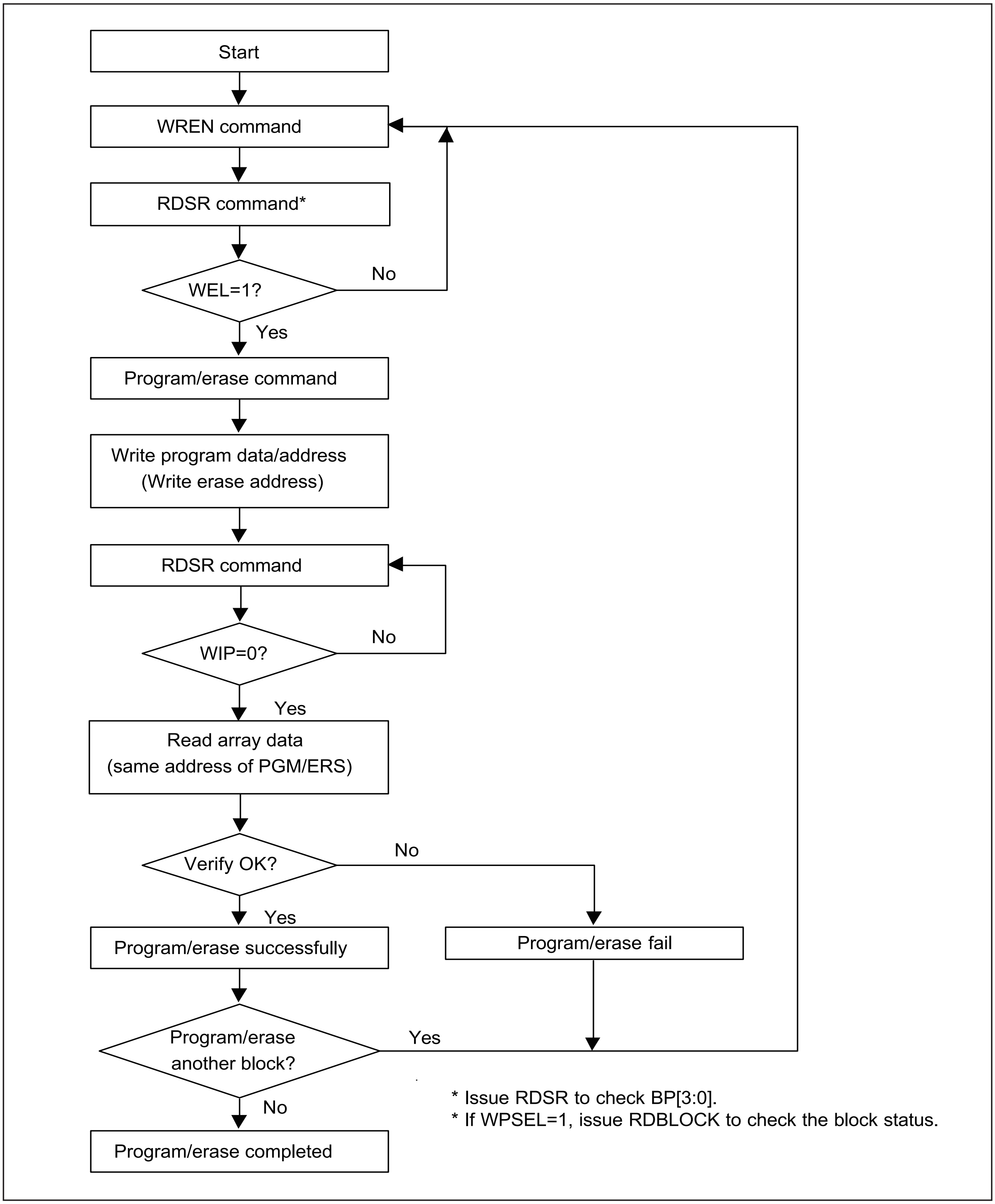
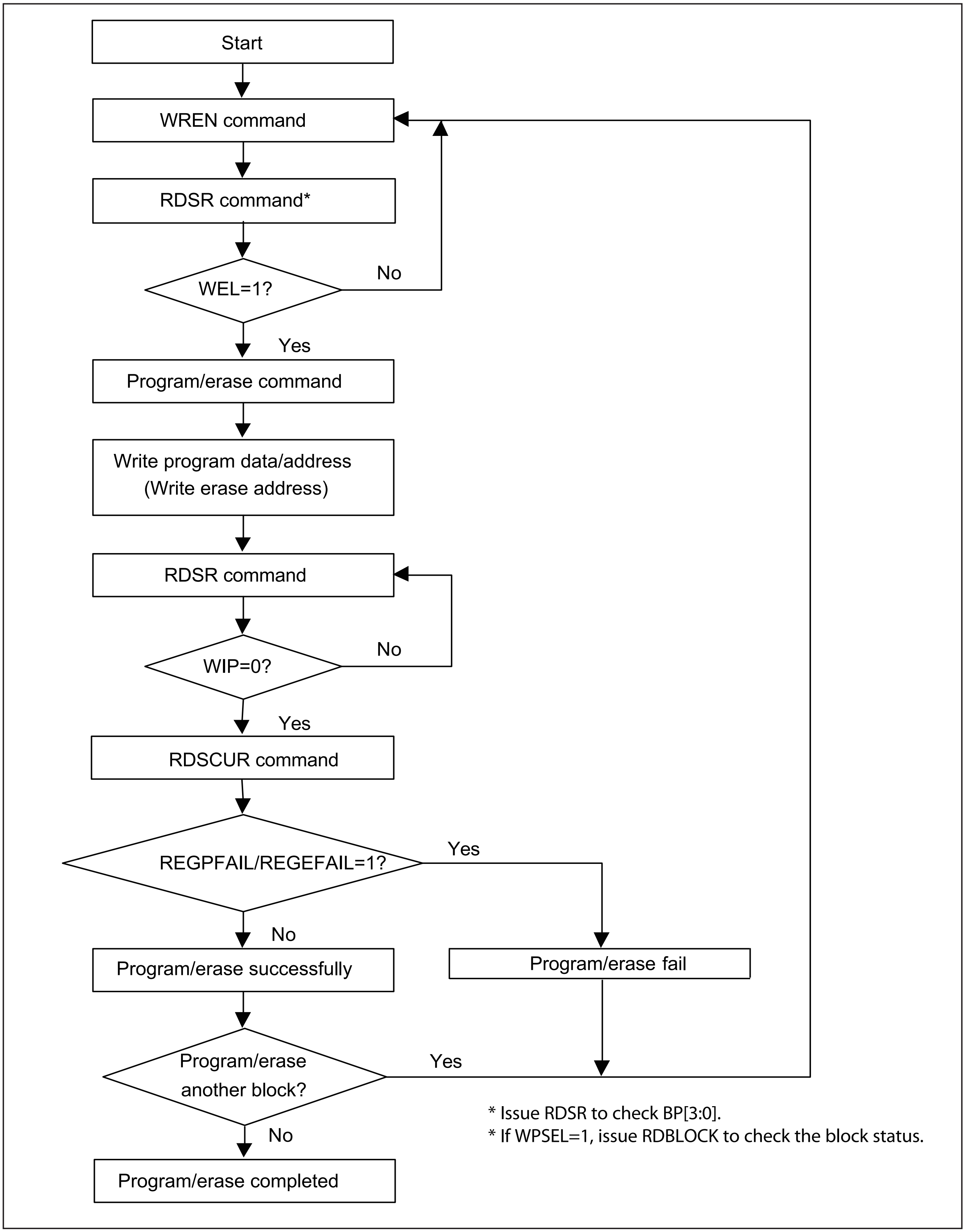


Figure 23. Program/Erase Flow(2) without read array data



9-20. Continuous Program mode (CP mode)

The CP mode may enhance program performance by automatically increasing address to the next higher address after each byte data has been programmed.

The Continuous Program (CP) instruction is for multiple bytes program to Flash. A write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Continuous Program (CP) instruction. CS# requires to go high before CP instruction is executing. After CP instruction and address input, two bytes of data is input sequentially from MSB(bit7) to LSB(bit0). The first byte data will be programmed to the initial address range with A0=0 and second byte data with A0=1. If only one byte data is input, the CP mode will not process. If more than two bytes data are input, the additional data will be ignored and only two byte data are valid. Any byte to be programmed should be in the erase state (FF) first. It will not roll over during the CP mode, once the last unprotected address has been reached, the chip will exit CP mode and reset write Enable Latch bit (WEL) as "0" and CP mode bit as "0". Please check the WIP bit status if it is not in write progress before entering next valid instruction. During CP mode, the valid commands are CP command (AD hex), WRDI command (04 hex), RDSR command (05 hex), and RDSCUR command (2B hex). And the WRDI command is valid after completion of a CP programming cycle, which means the WIP bit=0.

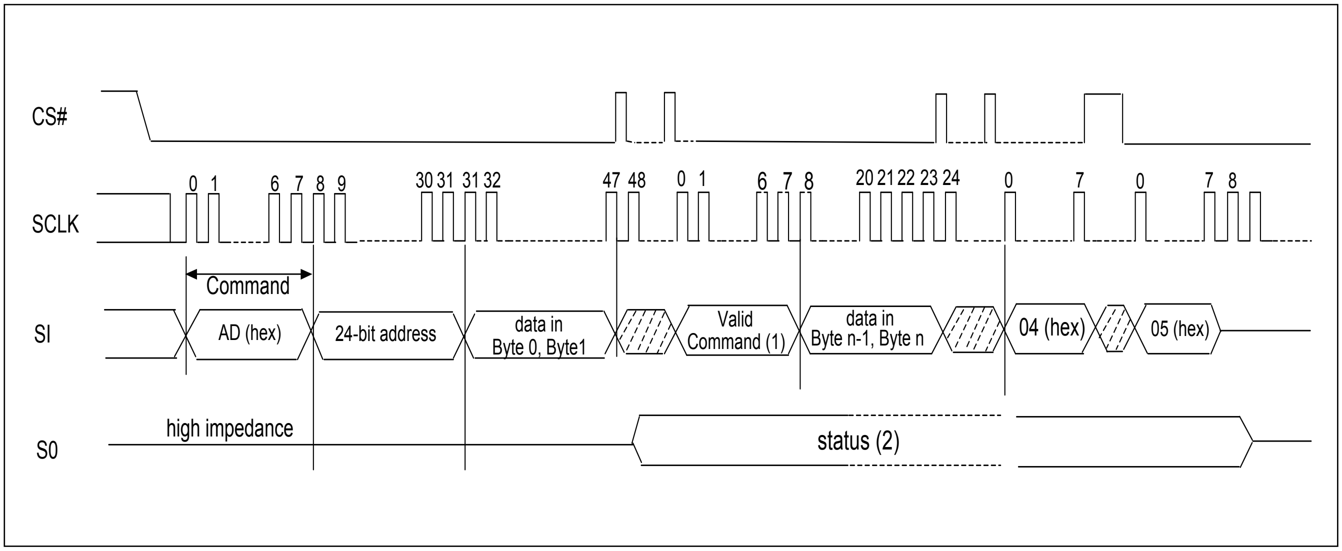
The sequence of issuing CP instruction is : CS# goes low → sending CP instruction code → 3-byte address on SI pin → two data bytes on SI → CS# goes high to low → sending CP instruction and then continue two data bytes are programmed → CS# goes high to low → till last desired two data bytes are programmed → CS# goes high to low →sending WRDI (Write Disable) instruction to end CP mode → send RDSR instruction to verify if CP mode word program ends, or send RDSCUR to check bit4 to verify if CP mode ends.

Three methods to detect the completion of a program cycle during CP mode:

1) Software method-I: by checking WIP bit of Status Register to detect the completion of CP mode.
2) Software method-II: by waiting for a tBP time out to determine if it may load next valid command or not.
3) Hardware method: by writing ESRY (enable SO to output RY/BY#) instruction to detect the completion of a program cycle during CP mode. The ESRY instruction must be executed before CP mode execution. Once it is enable in CP mode, the CS# goes low will drive out the RY/BY# status on SO, "0" indicates busy stage, "1" indicates ready stage, SO pin outputs tri-state if CS# goes high. DSRY (disable SO to output RY/BY#) instruction to disable the SO to output RY/BY# and return to status register data output during CP mode. Please note that the ESRY/DSRY commands are not accepted unless the completion of CP mode.

   If the page is protected by BP3~0 (WPSEL=0) or by individual lock (WPSEL=1), the array data will be protected (no change) and the WEL bit will still be reset.

Figure 24. Continously Program (CP) Mode Sequence with Hardware Detection (Command AD)



Notes:

(1) During CP mode, the valid commands are CP command (AD hex), WRDI command (04 hex), RDSR command (05 hex), RDSCUR command (2B hex), RSTEN command (66 hex) and RST command (99hex).

(2) Once an internal programming operation begins, CS# goes low will drive the status on the SO pin and CS# goes high will return the SO pin to tri-state.

(3) To end the CP mode, either reaching the highest unprotected address or sending Write Disable (WRDI) command (04 hex) may achieve it and then it is recommended to send RDSR command (05 hex) to verify if CP mode is ended. Please be noticed that Software reset and Hardware reset can end the CP mode.

9-21. Deep Power-down (DP)

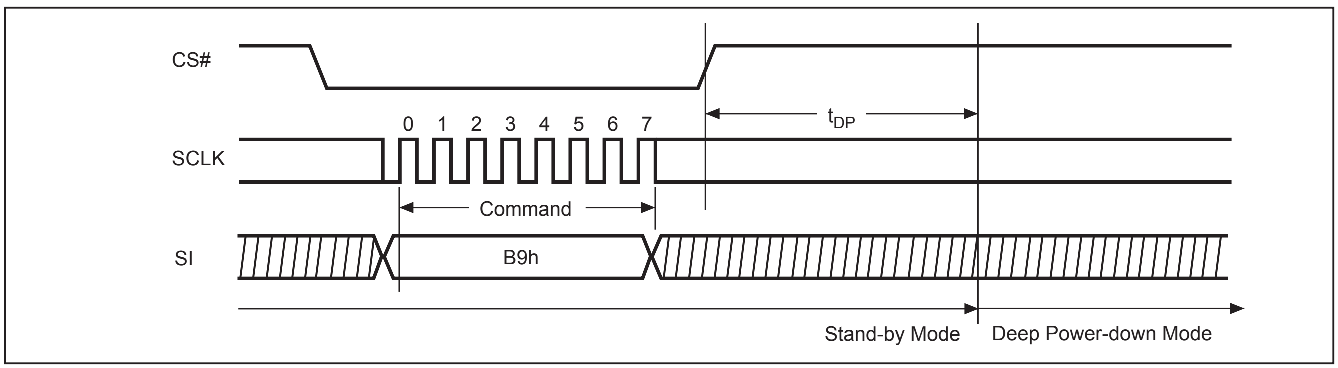
The Deep Power-down (DP) instruction is for setting the device on the minimizing the power consumption (to entering the Deep Power-down mode), the standby current is reduced from ISB1 to ISB2). The Deep Power-down mode requires the Deep Power-down (DP) instruction to enter, during the Deep Power-down mode, the device is not active and all Write/Program/Erase instructions are ignored. When CS# goes high, it's only in standby mode not deep power-down mode. It's different from Standby mode.

The sequence of issuing DP instruction is: CS# goes low→ sending DP instruction code→ CS# goes high.

The SIO[3:1] are don't care when during this mode.

Once the DP instruction is set, all instructions will be ignored except the Release from Deep Power-down mode (RDP) and Read Electronic Signature (RES) instruction. (those instructions allow the ID being reading out). When Power-down, the deep power-down mode automatically stops, and when power-up, the device automatically is in standby mode. For RDP instruction the CS# must go high exactly at the byte boundary (the latest eighth bit of instruction code has been latched-in); otherwise, the instruction will not be executed. As soon as Chip Select (CS#) goes high, a delay of tDP is required before entering the Deep Power-down mode and reducing the current to ISB2.

Figure 25. Deep Power-down (DP) Sequence (Command B9)



9-22. Release from Deep Power-down (RDP), Read Electronic Signature (RES)

The Release from Deep Power-down (RDP) instruction is terminated by driving Chip Select (CS#) High. When Chip Select (CS#) is driven High, the device is put in the standby Power mode. If the device was not previously in the Deep Power-down mode, the transition to the standby Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the standby Power mode is delayed by tRES2, and Chip Select (CS#) must remain High for at least tRES2(max), as specified in *"Table 13. AC Characteristics"*. Once in the standby mode, the device waits to be selected, so that it can receive, decode and execute instructions.

RES instruction is for reading out the old style of 8-bit Electronic Signature, whose values are shown as *"Table 7. ID Definitions"*. This is not the same as RDID instruction. It is not recommended to use for new design. For new design, please use RDID instruction. Even in Deep power-down mode, the RDP and RES are also allowed to be executed, only except the device is in progress of program/erase/write cycles; there's no effect on the current program/erase/write cycles in progress.

The SIO[3:1] are don't care when during this mode.

The RES instruction is ended by CS# goes high after the ID been read out at least once. The ID outputs repeatedly if continuously send the additional clock cycles on SCLK while CS# is at low. If the device was not previously in Deep Power-down mode, the device transition to standby mode is immediate. If the device was previously in Deep Power-down mode, there's a delay of tRES2 to transit to standby mode, and CS# must remain to high at least tRES2(max). Once in the standby mode, the device waits to be selected, so it can receive, decode, and execute instruction.

The RDP instruction is for releasing from Deep Power-down Mode.

Figure 26. Release from Deep Power-down and Read Electronic Signature (RES) Sequence (Command AB)

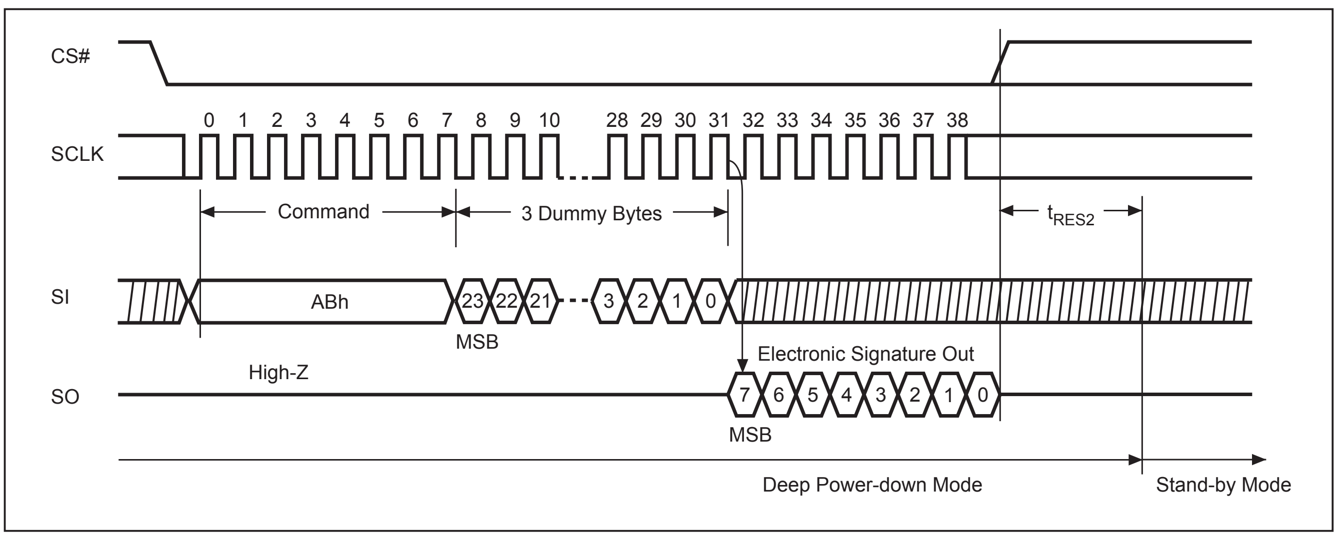
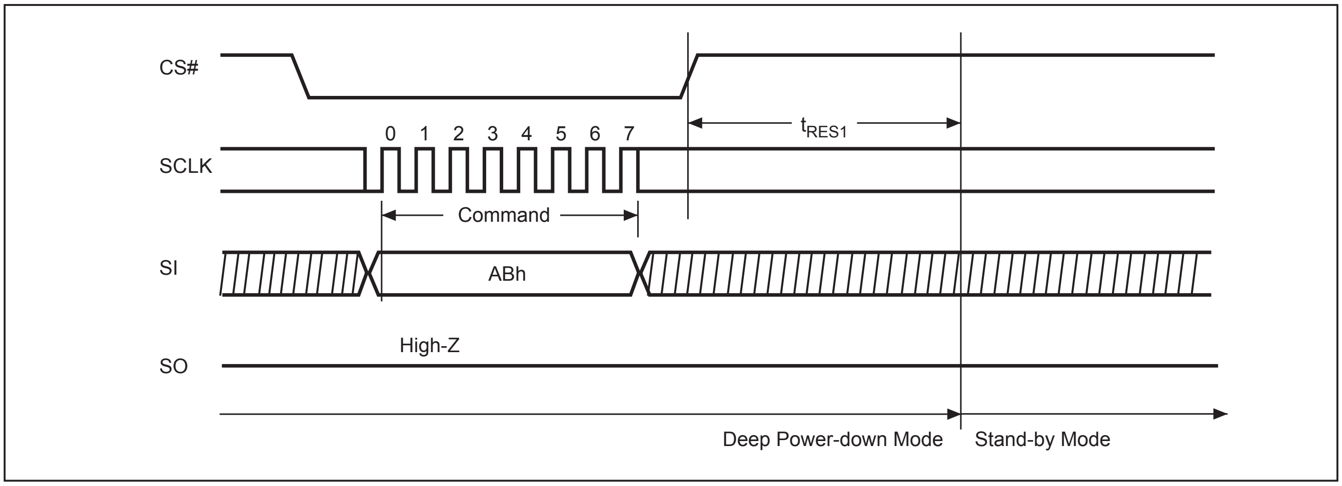


Figure 27. Release from Deep Power-down (RDP) Sequence (Command AB)

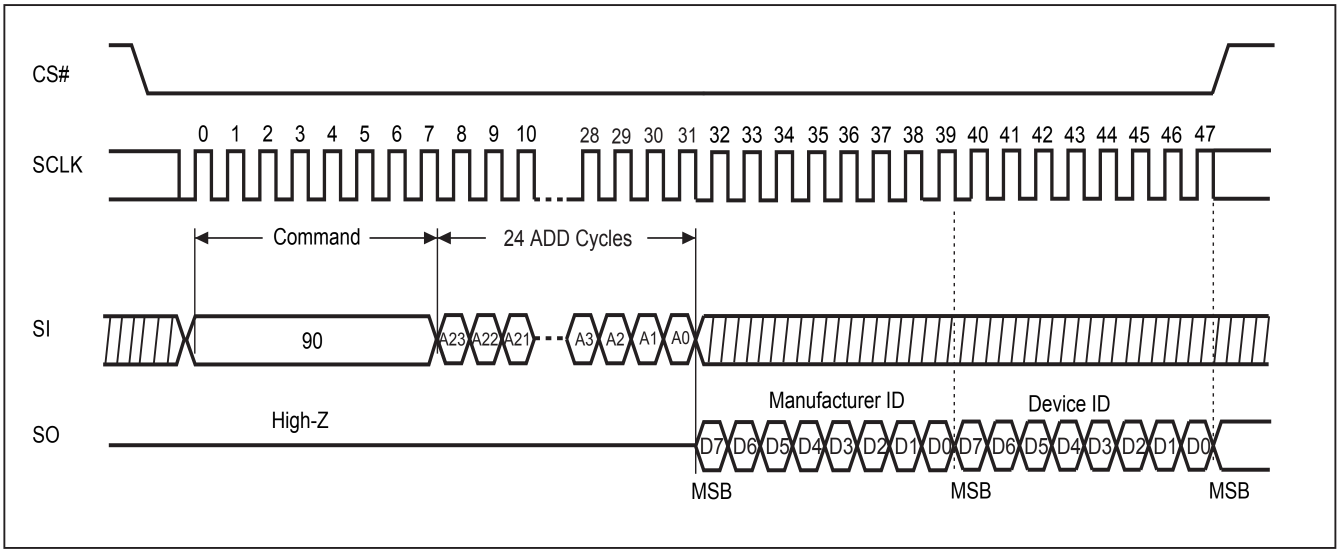


9-23. Read Electronic Manufacturer ID & Device ID (REMS), (REMS2), (REMS4)

The REMS, REMS2, and REMS4 instruction provides both the JEDEC assigned Manufacturer ID and the specific Device ID.

The instruction is initiated by driving the CS# pin low and shift the instruction code "90h", "DFh" or "EFh" followed by two dummy bytes and one byte address (A7~A0). After which, the Manufacturer ID for Macronix (C2h) and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in the figure below. The Device ID values are listed in *"Table 7. ID Definitions"*. If the one-byte address is initially set to 01h, then the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

Figure 28. Read Electronic Manufacturer & Device ID (REMS) Sequence (Command 90 or EF or DF)



Notes:

1. A0=0 will output the Manufacturer ID first and A0=1 will output Device ID first. A1~A23 are don't care.
2. Instruction is either 90(hex) or EF(hex) or DF(hex).

9-24. ID Read

User can execute this ID Read instruction to identify the Device ID and Manufacturer ID. The sequence of issue ID instruction is CS# goes low→sending ID instruction→Data out on SO→CS# goes high. Most significant bit (MSB) first.

After the command cycle, the device will immediately output data on the falling edge of SCLK. The manufacturer ID, memory type, and device ID data byte will be output continuously, until the CS# goes high.

Table 7. ID Definitions

Command Type	MX25L6473E		
RDID	manufacturer ID	memory type	memory density
	C2	20	17
RES	electronic ID		
	16		
REMS/REMS2/ REMS4	manufacturer ID	device ID	
	C2	16	

9-25. Enter Secured OTP (ENSO)

The ENSO instruction is for entering the additional 4K-bit Secured OTP mode. The additional 4K-bit Secured OTP is independent from main array, which may use to store unique serial number for system identifier. After entering the Secured OTP mode, and then follow standard read or program procedure to read out the data or update data. The Secured OTP data cannot be updated again once it is lock-down.

The sequence of issuing ENSO instruction is: CS# goes low→ sending ENSO instruction to enter Secured OTP mode→ CS# goes high.

The SIO[3:1] are don't care when during this mode.

Please note that WRSR/WRSCUR/WPSEL/SBLK/GBLK/SBULK/GBULK/CE/BE/SE/BE32K commands are not acceptable during the access of secure OTP region, once Security OTP is locked down, only read related commands are valid.

9-26. Exit Secured OTP (EXSO)

The EXSO instruction is for exiting the additional 4K-bit Secured OTP mode.
The sequence of issuing EXSO instruction is: CS# goes low→ sending EXSO instruction to exit Secured OTP mode→ CS# goes high.

The SIO[3:1] are don't care when during this mode.

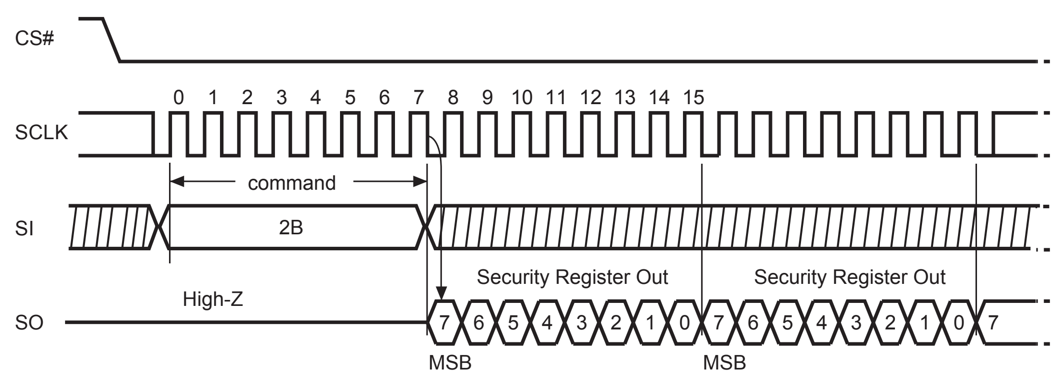
9-27. Read Security Register (RDSCUR)

The RDSCUR instruction is for reading the value of Security Register. The Read Security Register can be read at any time (even in program/erase/write status register/write security register condition) and continuously.

The sequence of issuing RDSCUR instruction is : CS# goes low→ sending RDSCUR instruction → Security Register data out on SO→ CS# goes high.

The SIO[3:1] are don't care when during this mode.

Figure 29. Read Security Register (RDSCUR) Sequence (Command 2B)



The definition of the Security Register is as below:

Secured OTP Indicator bit. The Secured OTP indicator bit shows the chip is locked by factory before ex- factory or not. When it is "0", it indicates non-factory lock; "1" indicates factory- lock.

Lock-down Secured OTP (LDSO) bit. By writing WRSCUR instruction, the LDSO bit may be set to "1" for customer lock-down purpose. However, once the bit is set to "1" (lock-down), the LDSO bit and the 4K-bit Secured OTP area cannot be updated any more. While it is in 4K-bit Secured OTP mode, array access is not allowed.

Continuous Program Mode (CP mode) bit. The Continuous Program Mode bit indicates the status of CP mode, "0" indicates not in CP mode; "1" indicates in CP mode.

Program Fail Flag bit. While a program failure happened, the Program Fail Flag bit would be set. If the program operation fails on a protected memory region or locked OTP region, this bit will also be set. This bit can be the failure indication of one or more program operations. This fail flag bit will be cleared automatically after the next successful program operation.

Erase Fail Flag bit. While an erase failure happened, the Erase Fail Flag bit would be set. If the erase operation fails on a protected memory region or locked OTP region, this bit will also be set. This bit can be the failure indication of one or more erase operations. This fail flag bit will be cleared automatically after the next successful erase operation.

Write Protection Select bit. The Write Protection Select bit indicates that WPSEL has been executed successfully. Once this bit has been set (WPSEL=1), all the blocks or sectors will be write-protected after the power-on every time. Once WPSEL has been set, it cannot be changed again, which means it's only for individual WP mode.

Table 8. Security Register Definition

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
WPSEL	E_FAIL	P_FAIL	Continuously Program mode (CP mode)	Reserved	Reserved	LDSO (lock-down 4K-bit Secured OTP)	4K-bit Secured OTP
0=normal WP mode 1=individual WP mode (default=0)	0=normal Erase succeed 1=indicate Erase failed (default=0)	0=normal Program succeed 1=indicate Program failed (default=0)	0=normal Program mode 1=CP mode (default=0)	-	-	0 = not lockdown 1 = lock-down (cannot program/ erase OTP)	0 = nonfactory lock 1 = factory lock
non-volatile bit	volatile bit	volatile bit	volatile bit	volatile bit	volatile bit	non-volatile bit	non-volatile bit
OTP	Read Only	Read Only	Read Only	Read Only	Read Only	OTP	Read Only

9-28. Write Security Register (WRSCUR)

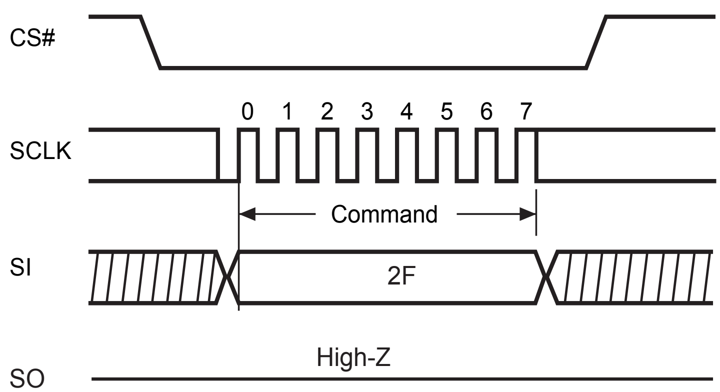
The WRSCUR instruction is for changing the values of Security Register Bits. The WREN instruction is required before sending WRSCUR instruction. The WRSCUR instruction may change the values of bit1 (LDSO bit) for customer to lock-down the 4K-bit Secured OTP area. Once the LDSO bit is set to "1", the Secured OTP area cannot be updated any more.

The sequence of issuing WRSCUR instruction is :CS# goes low→ sending WRSCUR instruction → CS# goes high.

The SIO[3:1] are don't care when during this mode.

The CS# must go high exactly at the boundary; otherwise, the instruction will be rejected and not executed.

Figure 30. Write Security Register (WRSCUR) Sequence (Command 2F)



9-29. Write Protection Selection (WPSEL)

There are two write protection methods, (1) BP protection mode (2) individual block protection mode. If WPSEL=0, flash is under BP protection mode. If WPSEL=1, flash is under individual block protection mode. The default value of WPSEL is “0”. WPSEL command can be used to set WPSEL=1. **Please note that WPSEL is an OTP bit. Once WPSEL is set to 1, there is no chance to recovery WPSEL back to “0”.** If the flash is put on BP mode, the individual block protection mode is disabled. Contrarily, if flash is on the individual block protection mode, the BP mode is disabled.

The SIO[3:1] are don't care when during this mode.

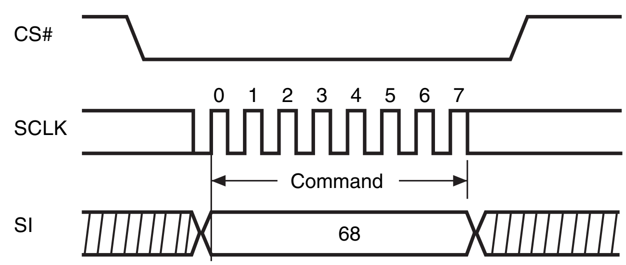
Every time after the system is powered-on, and the Security Register bit 7 is checked to be WPSEL=1, all the blocks or sectors will be write protected by default. User may only unlock the blocks or sectors via SBULK and GBULK instruction. Program or erase functions can only be operated after the Unlock instruction is conducted.

<u>BP protection mode, WPSEL=0:</u>
ARRAY is protected by BP3~BP0, where SRWD is bit 7 of status register that can be set by WRSR command.

Individual block protection mode, WPSEL=1:
Blocks are individually protected by their own SRAM lock bits which are set to “1” after power up. SBULK and SBLK command can set SRAM lock bit to “0” and “1”. When the system accepts and executes WPSEL instruction, the bit 7 in security register will be set. It will activate SBLK, SBULK, RDBLOCK, GBLK, GBULK, PBLK, RDPBLK etc instructions to conduct block lock protection and replace the original Software Protect Mode (SPM) use (BP3~BP0) indicated block methods.

The WREN (Write Enable) instruction is required before issuing WPSEL instruction.
The sequence of issuing WPSEL instruction is: CS# goes low → sending WPSEL instruction to enter the individual block protect mode → CS# goes high.

Figure 31. Write Protection Selection (WPSEL) Sequence (Command 68)



WPSEL instruction function flow is as follows:

Figure 32. BP and SRWD if WPSEL=0

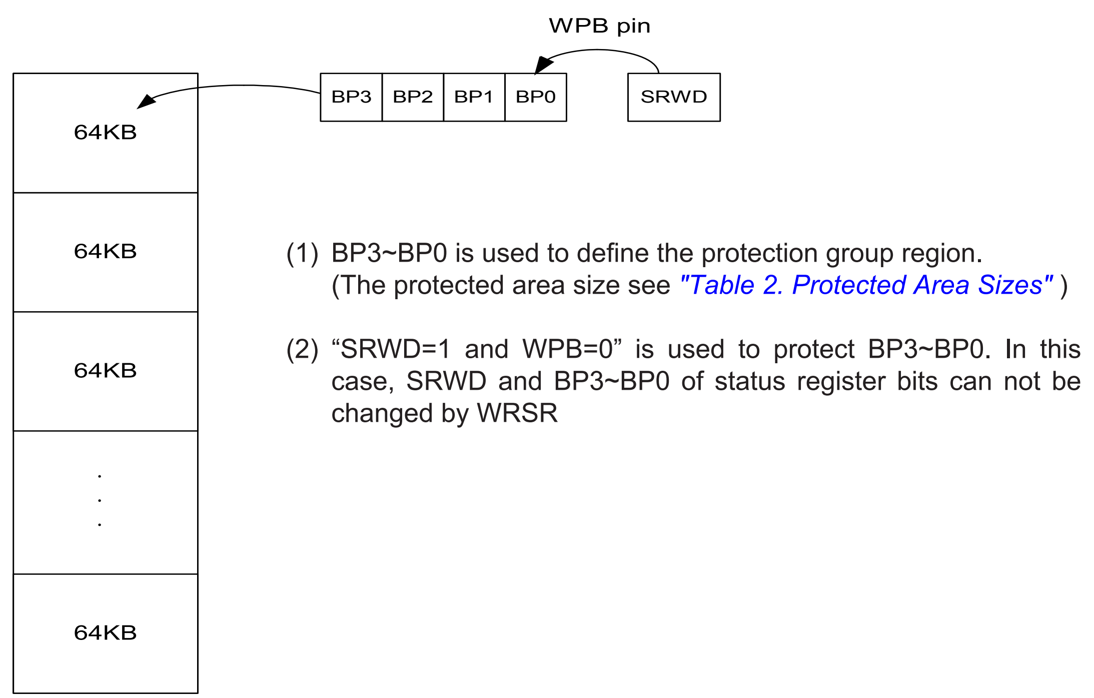
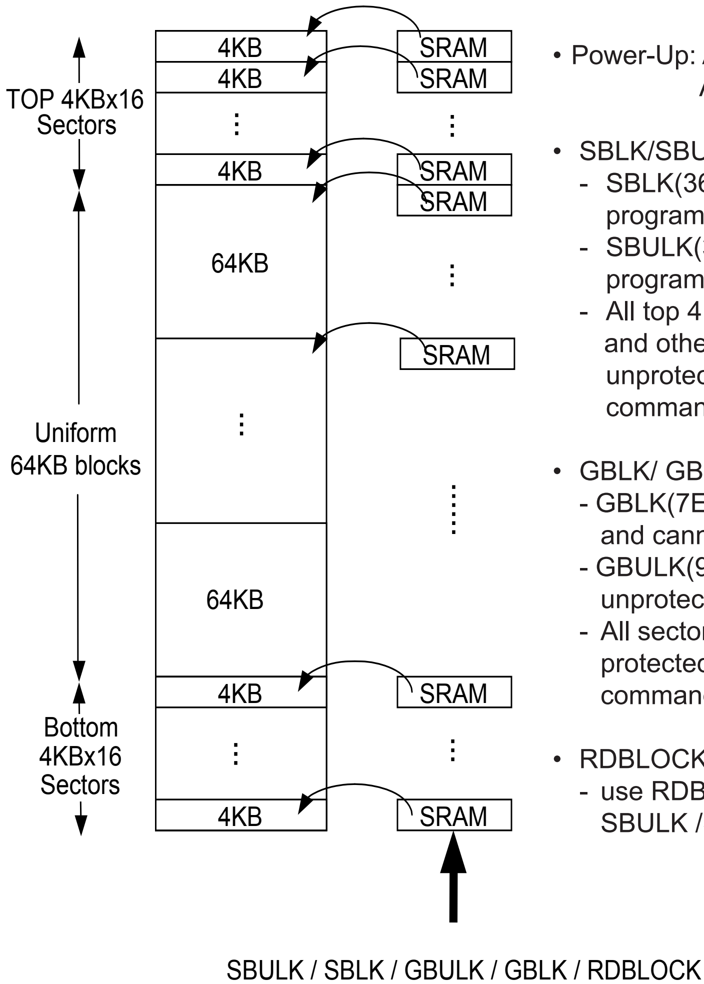
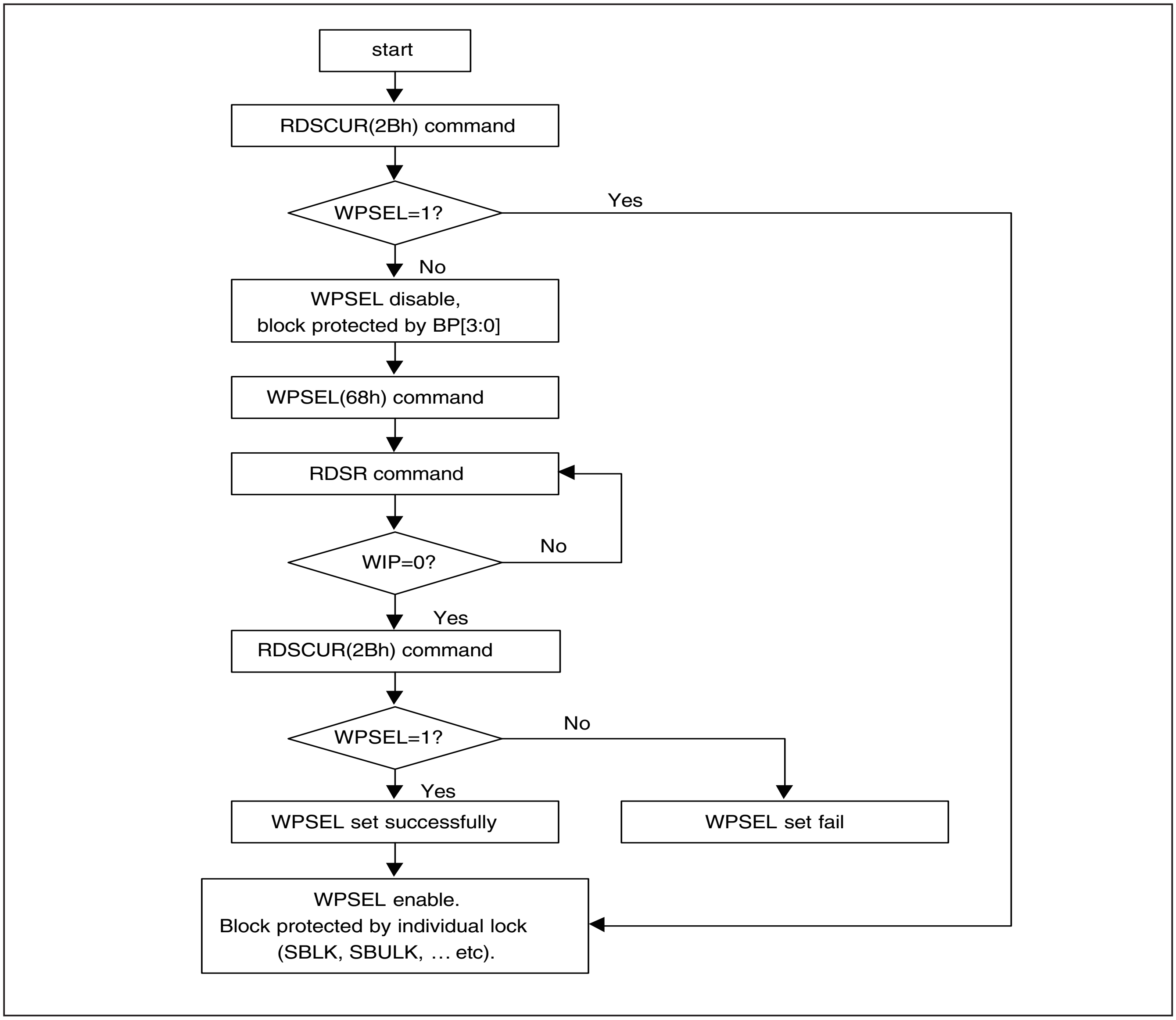


Figure 33. The individual block lock mode is effective after setting WPSEL=1



- Power-Up: All SRAM bits=1 (all blocks are default protected).
  All arrays cannot be programmed/erased
- SBLK/SBULK(36h/39h):
  - SBLK(36h) : Set SRAM bit=1 (protect) : array can not be programmed /erased
  - SBULK(39h): Set SRAM bit=0 (unprotect): array can be programmed /erased
  - All top 4KBx16 sectors and bottom 4KBx16 sectors and other 64KB uniform blocks can be protected and unprotected SRAM bits individually by SBLK/SBULK command set.
- GBLK/ GBULK(7Eh/98h):
  - GBLK(7Eh):Set all SRAM bits=1,whole chip are protected and cannot be programmed / erased.
  - GBULK(98h):Set all SRAM bits=0,whole chip are unprotected and can be programmed / erased.
  - All sectors and blocks SRAM bits of whole chip can be protected and unprotected at one time by GBLK/GBULK command set.
- RDBLOCK(3Ch):
  - use RDBLOCK mode to check the SRAM bits status after SBULK /SBLK/GBULK/GBLK command set.

Figure 34. WPSEL Flow



9-30. Single Block Lock/Unlock Protection (SBLK/SBULK)

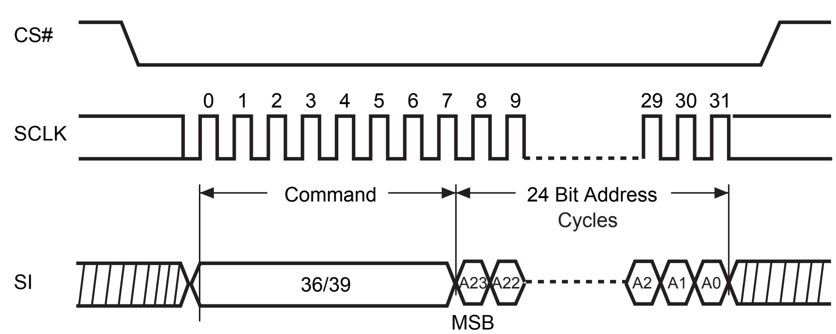
These instructions are only effective after WPSEL was executed. The SBLK instruction is for write protection a specified block(or sector) of memory, using A23-A16 or (A23-A12) address bits to assign a 64Kbytes block (or 4K bytes sector) to be protected as read only. The SBULK instruction will cancel the block (or sector) write protection state. This feature allows user to stop protecting the entire block (or sector) through the chip unprotect command (GBULK).

The WREN (Write Enable) instruction is required before issuing SBLK/SBULK instruction.
The sequence of issuing SBLK/SBULK instruction is: CS# goes low → send SBLK/SBULK (36h/39h) instruction → send 3 address bytes assign one block (or sector) to be protected on SI pin → CS# goes high.

The CS# must go high exactly at the byte boundary, otherwise the instruction will be rejected and not be executed.

The SIO[3:1] are don't care when during this mode.

Figure 35. Single Block Lock/Unlock Protection (SBLK/SBULK) Sequence (Command 36/39)



SBLK/SBULK instruction function flow is as follows:

Figure 36. Block Lock Flow

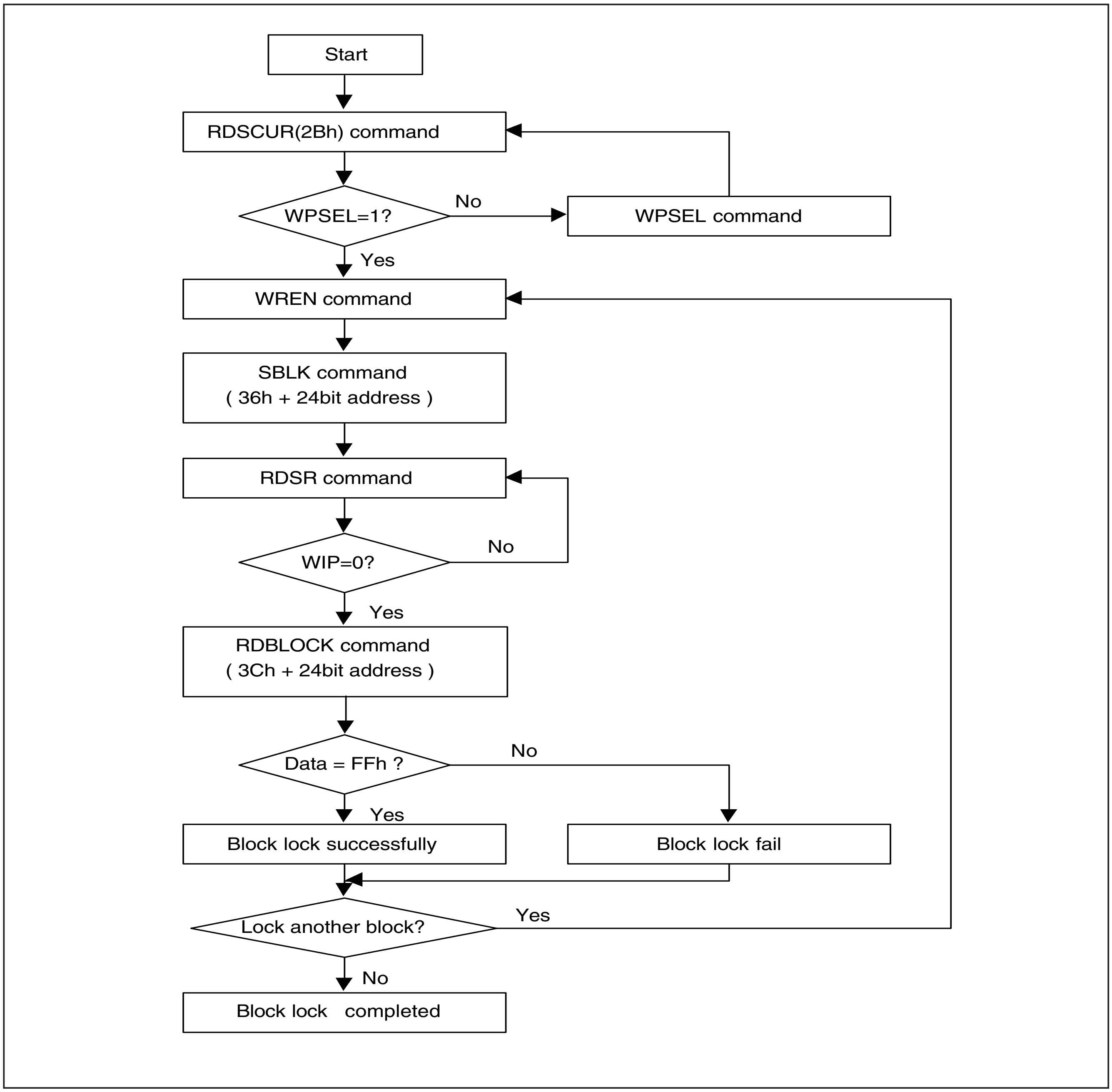
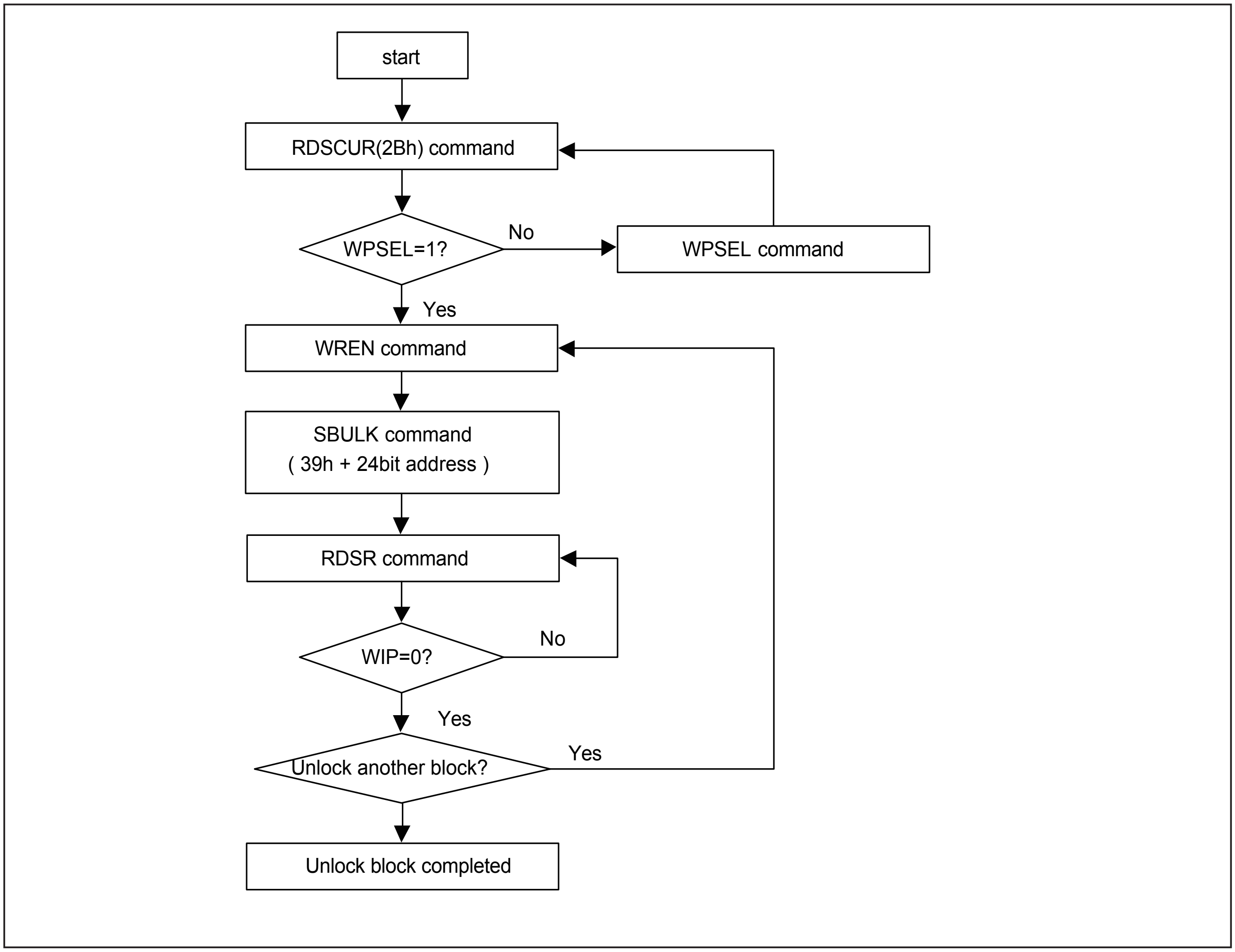


Figure 37. Block Unlock Flow



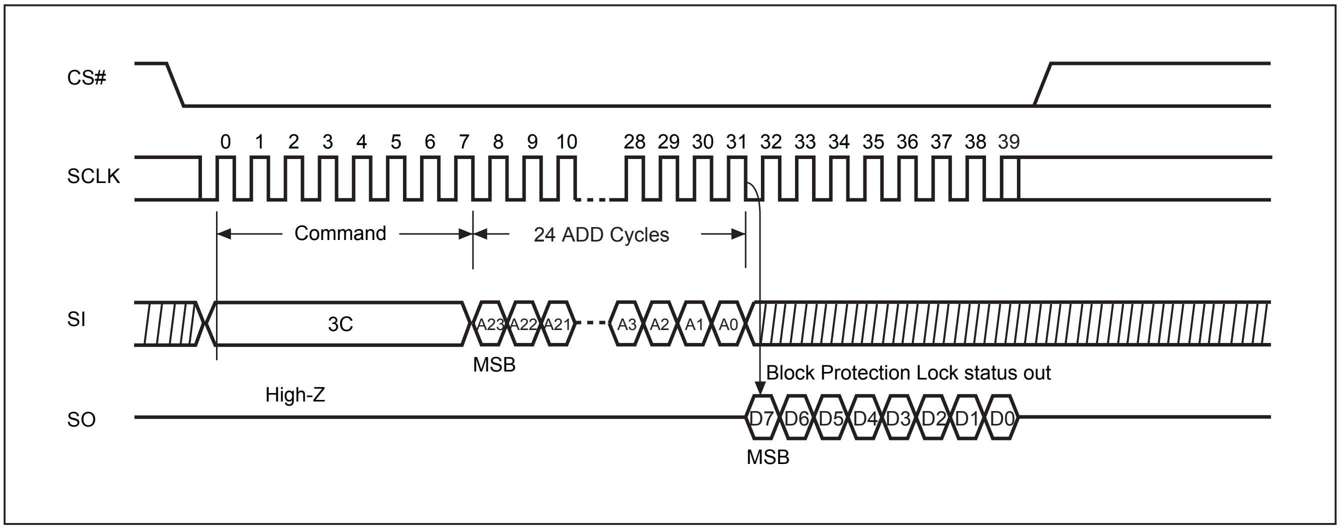
9-31. Read Block Lock Status (RDBLOCK)

This instruction is only effective after WPSEL was executed. The RDBLOCK instruction is for reading the status of protection lock of a specified block(or sector), using A23-A16 (or A23-A12) address bits to assign a 64K bytes block (4K bytes sector) and read protection lock status bit which the first byte of Read-out cycle. The status bit is"1" to indicate that this block has been protected, that user can read only but cannot write/program /erase this block. The status bit is "0" to indicate that this block hasn't be protected, and user can read and write this block.

The sequence of issuing RDBLOCK instruction is: CS# goes low → send RDBLOCK (3Ch) instruction → send 3 address bytes to assign one block on SI pin → read block's protection lock status bit on SO pin → CS# goes high.

The SIO[3:1] are don't care when during this mode.

Figure 38. Read Block Protection Lock Status (RDBLOCK) Sequence (Command 3C)



9-32. Gang Block Lock/Unlock (GBLK/GBULK)

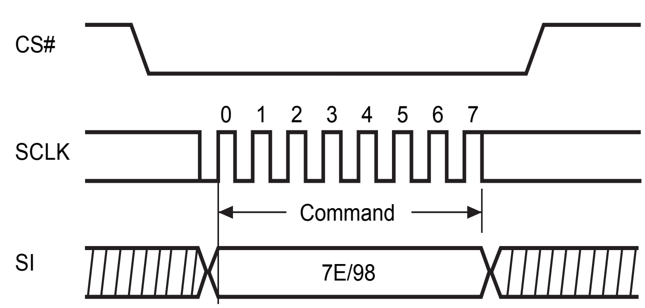
These instructions are only effective after WPSEL was executed. The GBLK/GBULK instruction is for enable/ disable the lock protection block of the whole chip.

The WREN (Write Enable) instruction is required before issuing GBLK/GBULK instruction.
The sequence of issuing GBLK/GBULK instruction is: CS# goes low → send GBLK/GBULK (7Eh/98h) instruction → CS# goes high.

The CS# must go high exactly at the byte boundary, otherwise, the instruction will be rejected and not be executed.

The SIO[3:1] are don't care when during this mode.

Figure 39. Gang Block Lock/Unlock (GBLK/GBULK) Sequence (Command 7E/98)



9-33. Enable SO to Output RY/BY# (ESRY)

The ESRY instruction is for outputting the ready/busy status to SO during CP mode.
The sequence of issuing ESRY instruction is: CS# goes low → sending ESRY instruction code → CS# goes high.
The CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

9-34. Disable SO to Output RY/BY# (DSRY)

The DSRY instruction is for resetting ESRY during CP mode. The ready/busy status will not output to SO after DSRY issued.
The sequence of issuing DSRY instruction is: CS# goes low → send DSRY instruction code → CS# goes high.
The CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

9-35. No Operation (NOP)

The “No Operation” command is only able to terminate the Reset Enable (RSTEN) command and will not affect any other command.
The SIO[3:1] are don't care when during this mode.

9-36. Software Reset (Reset-Enable (RSTEN) and Reset (RST))

The Software Reset operation combines two instructions: Reset-Enable (RSTEN) command and Reset (RST) command. It returns the device to standby mode.

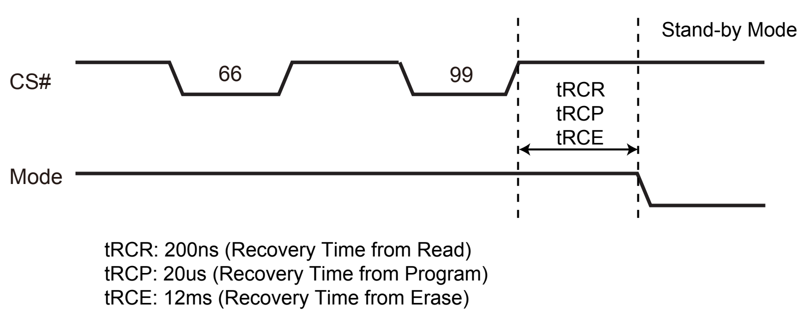
To execute Reset command (RST), the Reset-Enable (RSTEN) command must be executed first to perform the Reset operation. If there is any other command to interrupt after the Reset-Enable command, the Reset-Enable will be invalid.

The SIO[3:1] are don't care when during this mode.

If the Reset command is executed during program or erase operation, the operation will be disabled, the data under processing could be damaged or lost.

The reset time is different depending on the last operation. Longer latency time is required to recover from a program operation than from other operations.

Figure 40. Software Reset Recovery



9-37. Read SFDP Mode (RDSFDP)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI.

The sequence of issuing RDSFDP instruction is CS# goes low→send RDSFDP instruction (5Ah)→send 3 address bytes on SI pin→send 1 dummy byte on SI pin→read SFDP code on SO→to end RDSFDP operation can use CS# to high at any time during data out.

SFDP is a JEDEC Standard, JESD216.

Figure 41. Read Serial Flash Discoverable Parameter (RDSFDP) Sequence

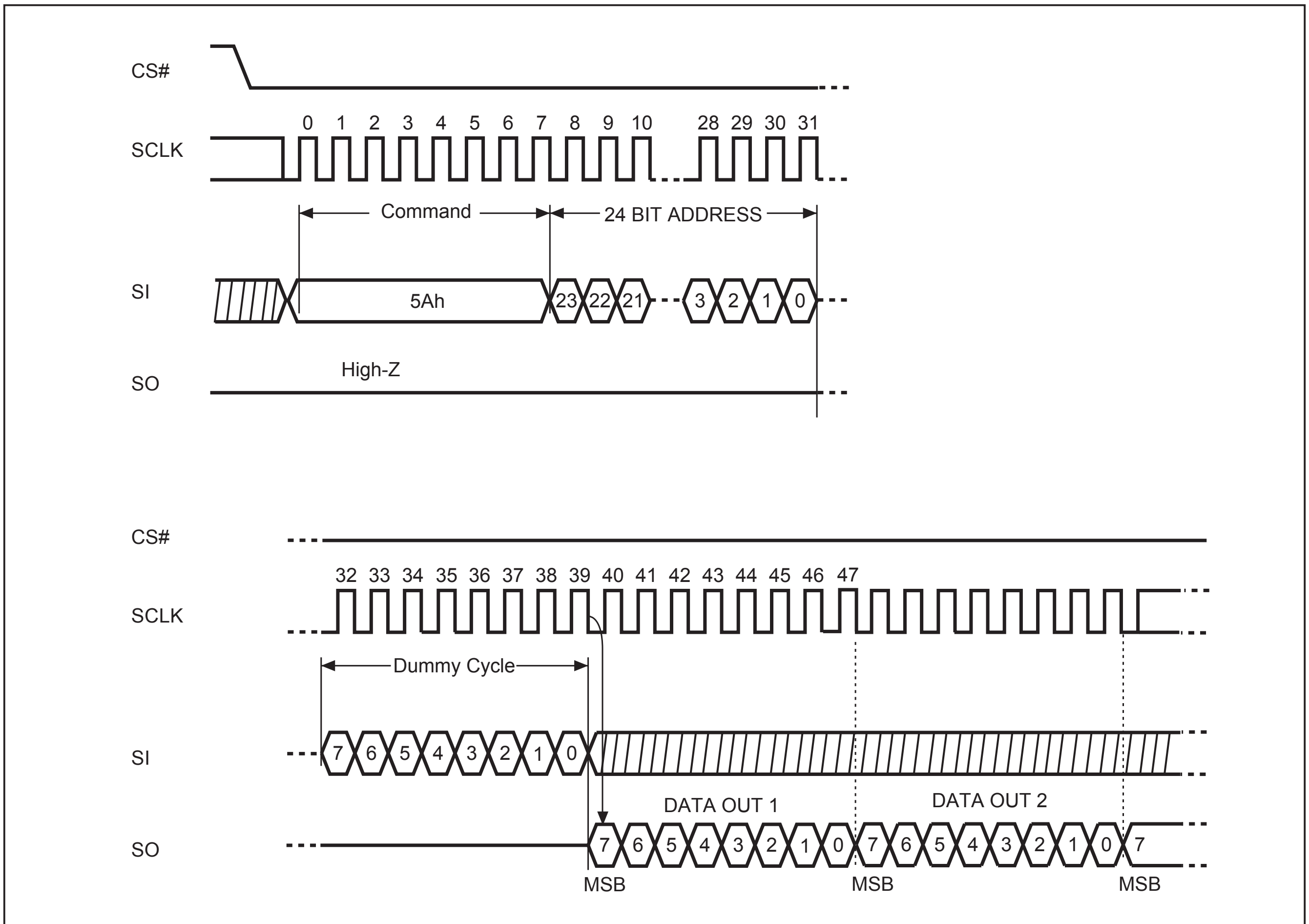


Table 9. Signature and Parameter Identification Data Values

Description	Comment	Add (h) (Byte)	DW Add (Bit)	Data (h/b) (Note1)	Data (h)
SFDP Signature	Fixed: 50444653h	00h	07:00	53h	53h
		01h	15:08	46h	46h
		02h	23:16	44h	44h
		03h	31:24	50h	50h
SFDP Minor Revision Number	Start from 00h	04h	07:00	00h	00h
SFDP Major Revision Number	Start from 01h	05h	15:08	01h	01h
Number of Parameter Headers	This number is 0-based. Therefore, 0 indicates 1 parameter header.	06h	23:16	01h	01h
Unused		07h	31:24	FFh	FFh
ID number (JEDEC)	00h: it indicates a JEDEC specified header.	08h	07:00	00h	00h
Parameter Table Minor Revision Number	Start from 00h	09h	15:08	00h	00h
Parameter Table Major Revision Number	Start from 01h	0Ah	23:16	01h	01h
Parameter Table Length (in double word)	How many DWORDs in the Parameter table	0Bh	31:24	09h	09h
Parameter Table Pointer (PTP)	First address of JEDEC Flash Parameter table	0Ch	07:00	30h	30h
		0Dh	15:08	00h	00h
		0Eh	23:16	00h	00h
Unused		0Fh	31:24	FFh	FFh
ID number (Macronix manufacturer ID)	it indicates Macronix manufacturer ID	10h	07:00	C2h	C2h
Parameter Table Minor Revision Number	Start from 00h	11h	15:08	00h	00h
Parameter Table Major Revision Number	Start from 01h	12h	23:16	01h	01h
Parameter Table Length (in double word)	How many DWORDs in the Parameter table	13h	31:24	04h	04h
Parameter Table Pointer (PTP)	First address of Macronix Flash Parameter table	14h	07:00	60h	60h
		15h	15:08	00h	00h
		16h	23:16	00h	00h
Unused		17h	31:24	FFh	FFh

Table 10. Parameter Table (0): JEDEC Flash Parameter Tables

Description	Comment	Add (h) (Byte)	DW Add (Bit)	Data (h/b) (Note1)	Data (h)
Block/Sector Erase sizes	00: Reserved, 01: 4KB erase, 10: Reserved, 11: not support 4KB erase	30h	01:00	01b	E5h
Write Granularity	0: 1Byte, 1: 64Byte or larger		02	1b	
Write Enable Instruction Required for Writing to Volatile Status Registers	0: not required 1: required 00h to be written to the status register		03	0b	
Write Enable Opcode Select for Writing to Volatile Status Registers	0: use 50h opcode, 1: use 06h opcode Note: If target flash status register is nonvolatile, then bits 3 and 4 must be set to 00b.		04	0b	
Unused	Contains 111b and can never be changed		07:05	111b	
4KB Erase Opcode		31h	15:08	20h	20h
(1-1-2) Fast Read (Note2)	0=not support 1=support	32h	16	1b	F1h
Address Bytes Number used in addressing flash array	00: 3Byte only, 01: 3 or 4Byte, 10: 4Byte only, 11: Reserved		18:17	00b	
Double Transfer Rate (DTR) Clocking	0=not support 1=support		19	0b	
(1-2-2) Fast Read	0=not support 1=support		20	1b	
(1-4-4) Fast Read	0=not support 1=support		21	1b	
(1-1-4) Fast Read	0=not support 1=support		22	1b	
Unused			23	1b	
Unused		33h	31:24	FFh	FFh
Flash Memory Density		37h:34h	31:00	03FF FFFFh	
(1-4-4) Fast Read Number of Wait states (Note3)	0 0000b: Wait states (Dummy Clocks) not support	38h	04:00	0 0100b	44h
(1-4-4) Fast Read Number of Mode Bits (Note4)	000b: Mode Bits not support		07:05	010b	
(1-4-4) Fast Read Opcode		39h	15:08	EBh	EBh
(1-1-4) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	3Ah	20:16	0 1000b	08h
(1-1-4) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	000b	
(1-1-4) Fast Read Opcode		3Bh	31:24	6Bh	6Bh

Description	Comment	Add (h) (Byte)	DW Add (Bit)	Data (h/b) (Note1)	Data (h)
(1-1-2) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	3Ch	04:00	0 1000b	08h
(1-1-2) Fast Read Number of Mode Bits	000b: Mode Bits not support		07:05	000b	
(1-1-2) Fast Read Opcode		3Dh	15:08	3Bh	3Bh
(1-2-2) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	3Eh	20:16	0 0100b	04h
(1-2-2) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	000b	
(1-2-2) Fast Read Opcode		3Fh	31:24	BBh	BBh
(2-2-2) Fast Read	0=not support 1=support	40h	00	0b	EEh
Unused			03:01	111b	
(4-4-4) Fast Read	0=not support 1=support		04	0b	
Unused			07:05	111b	
Unused		43h:41h	31:08	FFh	FFh
Unused		45h:44h	15:00	FFh	FFh
(2-2-2) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	46h	20:16	0 0000b	00h
(2-2-2) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	000b	
(2-2-2) Fast Read Opcode		47h	31:24	FFh	FFh
Unused		49h:48h	15:00	FFh	FFh
(4-4-4) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	4Ah	20:16	0 0000b	00h
(4-4-4) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	000b	
(4-4-4) Fast Read Opcode		4Bh	31:24	FFh	FFh
Sector Type 1 Size	Sector/block size = 2^N bytes (Note5) 0x00b: this sector type doesn't exist	4Ch	07:00	0Ch	0Ch
Sector Type 1 erase Opcode		4Dh	15:08	20h	20h
Sector Type 2 Size	Sector/block size = 2^N bytes 0x00b: this sector type doesn't exist	4Eh	23:16	0Fh	0Fh
Sector Type 2 erase Opcode		4Fh	31:24	52h	52h
Sector Type 3 Size	Sector/block size = 2^N bytes 0x00b: this sector type doesn't exist	50h	07:00	10h	10h
Sector Type 3 erase Opcode		51h	15:08	D8h	D8h
Sector Type 4 Size	Sector/block size = 2^N bytes 0x00b: this sector type doesn't exist	52h	23:16	00h	00h
Sector Type 4 erase Opcode		53h	31:24	FFh	FFh

Table 11. Parameter Table (1): Macronix Flash Parameter Tables

Description	Comment	Add (h) (Byte)	DW Add (Bit)	Data (h/b) (Note1)	Data (h)
Vcc Supply Maximum Voltage	2000h=2.000V 2700h=2.700V 3600h=3.600V	61h:60h	07:00 15:08	00h 36h	00h 36h
Vcc Supply Minimum Voltage	1650h=1.650V 2250h=2.250V 2350h=2.350V 2700h=2.700V	63h:62h	23:16 31:24	00h 27h	00h 27h
H/W Reset# pin	0=not support 1=support	65h:64h	00	0b	499Ch
H/W Hold# pin	0=not support 1=support		01	0b	
Deep Power Down Mode	0=not support 1=support		02	1b	
S/W Reset	0=not support 1=support		03	1b	
S/W Reset Opcode	Reset Enable (66h) should be issued before Reset Opcode		11:04	1001 1001b (99h)	
Program Suspend/Resume	0=not support 1=support		12	0b	
Erase Suspend/Resume	0=not support 1=support		13	0b	
Unused			14	1b	
Wrap-Around Read mode	0=not support 1=support		15	0b	
Wrap-Around Read mode Opcode		66h	23:16	FFh	FFh
Wrap-Around Read data length	08h:support 8B wrap-around read 16h:8B&16B 32h:8B&16B&32B 64h:8B&16B&32B&64B	67h	31:24	FFh	FFh
Individual block lock	0=not support 1=support	6Bh:68h	00	1b	C8D9h
Individual block lock bit (Volatile/Nonvolatile)	0=Volatile 1=Nonvolatile		01	0b	
Individual block lock Opcode			09:02	0011 0110b (36h)	
Individual block lock Volatile protect bit default protect status	0=protect 1=unprotect		10	0b	
Secured OTP	0=not support 1=support		11	1b	
Read Lock	0=not support 1=support		12	0b	
Permanent Lock	0=not support 1=support		13	0b	
Unused			15:14	11b	
Unused			31:16	FFh	FFh
Unused		6Fh:6Ch	31:00	FFh	FFh

Note 1: h/b is hexadecimal or binary.

Note 2: **(x-y-z)** means I/O mode nomenclature used to indicate the number of active pins used for the opcode (x), address (y), and data (z). At the present time, the only valid Read SFDP instruction modes are: (1-1-1), (2-2-2), and (4-4-4)

Note 3: **Wait States** is required dummy clock cycles after the address bits or optional mode bits.

Note 4: **Mode Bits** is optional control bits that follow the address bits. These bits are driven by the system controller if they are specified. (eg,read performance enhance toggling bits)

Note 5: 4KB=2^0Ch,32KB=2^0Fh,64KB=2^10h

Note 6: All unused and undefined area data is blank FFh.

10. POWER-ON STATE

The device is at below states when power-up:

- Standby mode (please note it is not Deep Power-down mode)
- Write Enable Latch (WEL) bit is reset

The device must not be selected during power-up and power-down stage unless the VCC achieves below correct level:

- VCC minimum at power-up stage and then after a delay of tVSL
- GND at power-down

Please note that a pull-up resistor on CS# may ensure a safe and proper power-up/down level.

An internal Power-on Reset (POR) circuit may protect the device from data corruption and inadvertent data change during power up state.

For further protection on the device, if the VCC does not reach the VCC minimum level, the correct operation is not guaranteed. The read, write, erase, and program command should be sent after the time delay:

- tVSL after VCC reached VCC minimum level

The device can accept read command after VCC reached VCC minimum and a time delay of tVSL.

Note:

- To stabilize the VCC level, the VCC rail decoupled by a suitable capacitor close to package pins is recommended. (generally around 0.1uF)

11. ELECTRICAL SPECIFICATIONS

11-1. Absolute Maximum Ratings

Rating		Value
Ambient Operating Temperature	Industrial grade	-40°C to 85°C
Storage Temperature		-65°C to 150°C
Applied Input Voltage		-0.5V to VCC+0.5V
Applied Output Voltage		-0.5V to VCC+0.5V
VCC to Ground Potential		-0.5V to 4.0V

NOTICE:
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
2. Specifications contained within the following tables are subject to change.
3. During voltage transitions, all pins may overshoot Vss to -2.0V and Vcc to +2.0V for periods up to 20ns, see the figures below.

Figure 42. Maximum Negative Overshoot Waveform

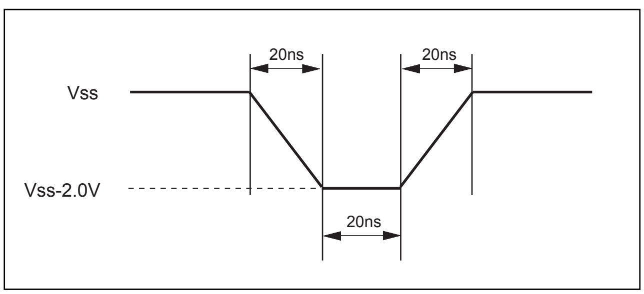
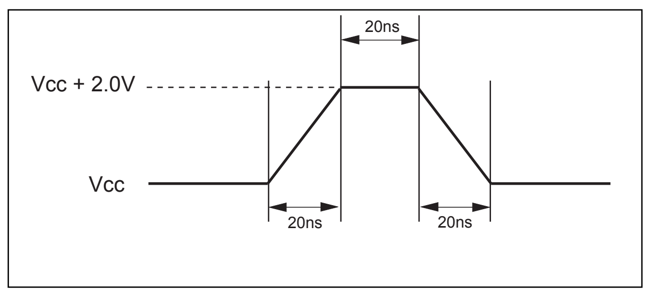


Figure 43. Maximum Positive Overshoot Waveform



11-2. Capacitance

TA = 25°C, f = 1.0 MHz

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
CIN	Input Capacitance			6	pF	VIN = 0V
COUT	Output Capacitance			8	pF	VOUT = 0V

Figure 44. Input Test Waveforms and Measurement Level

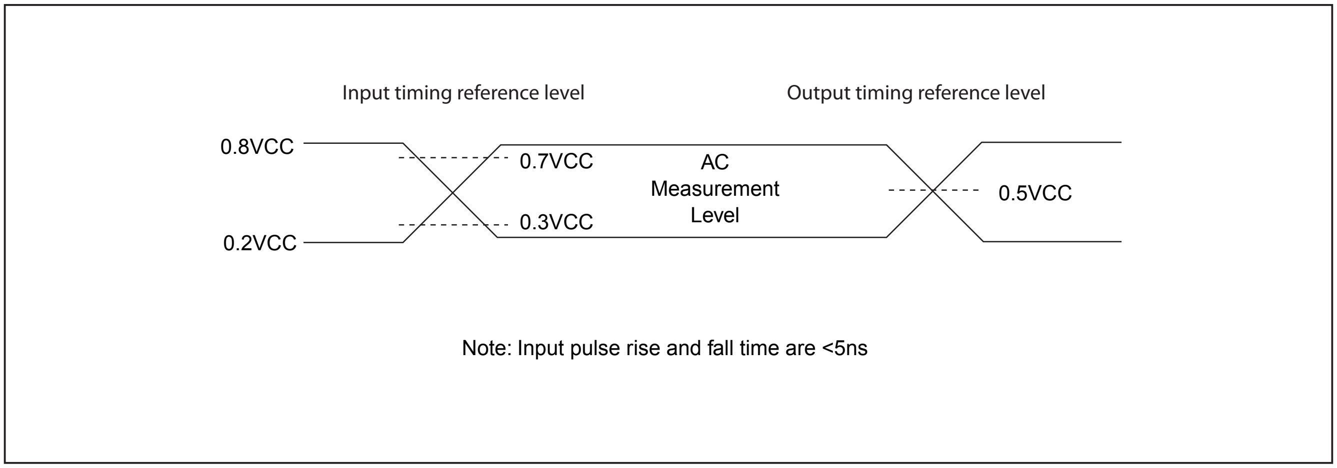


Figure 45. Output Loading

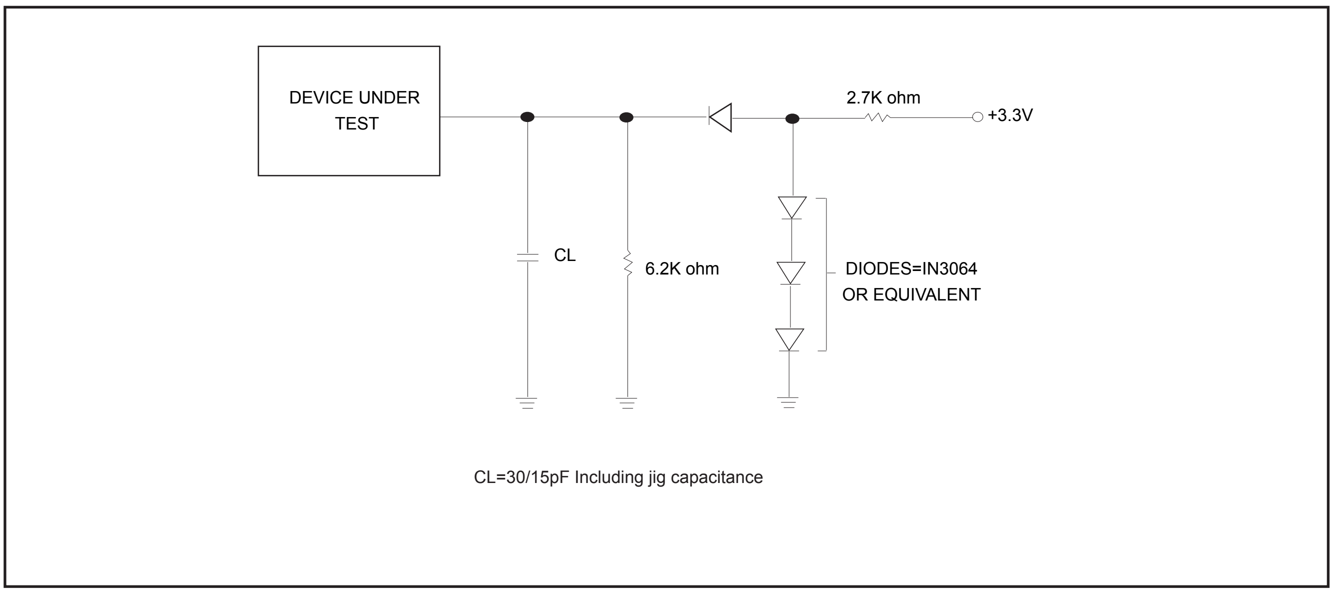


Table 12. DC Characteristics

Temperature = -40°C to 85°C for Industrial grade

Symbol	Parameter	Notes	Min.	Typ.	Max.	Units	Test Conditions
ILI	Input Load Current	1			± 2	uA	VCC = VCC Max, VIN = VCC or GND
ILO	Output Leakage Current	1			± 2	uA	VCC = VCC Max, VOUT = VCC or GND
ISB1	VCC Standby Current	1		15	50	uA	VIN = VCC or GND, CS# = VCC
ISB2	Deep Power-down Current			1	25	uA	VIN = VCC or GND, CS# = VCC
ICC1	VCC Read	1			35	mA	f=104MHz (4 x I/O read) SCLK=0.1VCC/0.9VCC, SO=Open
					19	mA	f=104MHz (1 x I/O read) SCLK=0.1VCC/0.9VCC, SO=Open
					25	mA	fQ=86MHz (4 x I/O read) SCLK=0.1VCC/0.9VCC, SO=Open
					20	mA	fT=86MHz (2 x I/O read) SCLK=0.1VCC/0.9VCC, SO=Open
					10	mA	f=33MHz, SCLK=0.1VCC/0.9VCC, SO=Open
ICC2	VCC Program Current (PP)	1		15	25	mA	Program in Progress, CS# = VCC
ICC3	VCC Write Status Register (WRSR) Current			15	20	mA	Program status register in progress, CS#=VCC
ICC4	VCC Sector Erase Current (SE)	1		10	25	mA	Erase in Progress, CS#=VCC
ICC5	VCC Chip Erase Current (CE)	1		15	25	mA	Erase in Progress, CS#=VCC
VIL	Input Low Voltage		-0.5		0.8	V	
VIH	Input High Voltage		0.7VCC		VCC+0.4	V	
VOL	Output Low Voltage				0.4	V	IOL = 1.6mA
VOH	Output High Voltage		VCC-0.2			V	IOH = -100uA

Notes :
1. Typical values at VCC = 3.3V, T = 25°C. These currents are valid for all product versions (package and speeds).
2. Typical value is calculated by simulation.
3. The value guaranteed by characterization, not 100% tested in production.

Table 13. AC Characteristics

Temperature = -40°C to 85°C for Industrial grade

Symbol	Alt.	Parameter			Min.	Typ.	Max.	Unit
fSCLK	fC	Clock Frequency for the following instructions: FAST_READ, RDSFDP, PP, SE, BE, CE, DP, RES, RDP, WREN, WRDI, RDID, RDSR, WRSR			D.C.		104	MHz
fRSCLK	fR	Clock Frequency for READ instructions					50	MHz
fTSCLK	fT	Clock Frequency for 2READ/DREAD instructions					86	MHz
	fQ	Clock Frequency for 4READ/QREAD instructions (4)					86	MHz
f4PP		Clock Frequency for 4PP (Quad page program)					104	MHz
tCH(1)	tCLH	Clock High Time		Others (fSCLK)	4.5			ns
				Normal Read (fRSCLK)	9			ns
tCL(1)	tCLL	Clock Low Time		Others (fSCLK)	4.5			ns
				Normal Read (fRSCLK)	9			ns
tCLCH		Clock Rise Time (peak to peak)			0.1			V/ns
tCHCL		Clock Fall Time (peak to peak)			0.1			V/ns
tSLCH	tCSS	CS# Active Setup Time (relative to SCLK)			4			ns
tCHSL		CS# Not Active Hold Time (relative to SCLK)			4			ns
tDVCH	tDSU	Data In Setup Time			2			ns
tCHDX	tDH	Data In Hold Time			3			ns
tCHSH		CS# Active Hold Time (relative to SCLK)			4			ns
tSHCH		CS# Not Active Setup Time (relative to SCLK)			4			ns
tSHSL	tCSH	CS# Deselect Time		Read	15			ns
				Write/Erase/Program	50			ns
tSHQZ	tDIS	Output Disable Time		2.7V-3.6V			10	ns
				3.0V-3.6V			8	ns
tCLQV	tV	Clock Low to Output Valid VCC=2.7V~3.6V	Loading: 10pF	1 I/O			5	ns
				2 I/O & 4 I/O			6	ns
			Loading: 15pF	1 I/O			6	ns
				2 I/O & 4 I/O			6	ns
			Loading: 30pF	1 I/O			7	ns
				2 I/O & 4 I/O			8	ns
tCLQX	tHO	Output Hold Time			1			ns
tWHSL(3)		Write Protect Setup Time			20			ns
tSHWL(3)		Write Protect Hold Time			100			ns
tDP		CS# High to Deep Power-down Mode					10	us
tRES1		CS# High to Standby Mode without Electronic Signature Read					100	us
tRES2		CS# High to Standby Mode with Electronic Signature Read					100	us

Symbol	Alt.	Parameter	Min.	Typ.	Max.	Unit
tW		Write Status Register Cycle Time			40	ms
tBP		Byte-Program		12	50	us
tPP		Page Program Cycle Time		0.7	3	ms
tSE		Sector Erase Cycle Time (4KB)		30	200	ms
tBE		Block Erase Cycle Time (32KB)		0.14	1.6	s
tBE		Block Erase Cycle Time (64KB)		0.25	2	s
tCE		Chip Erase Cycle Time		20	80	s
tWPS		Write Protection Selection Time			1	ms
tWSR		Write Security Register Time			1	ms

Notes:
1. tCH + tCL must be greater than or equal to 1/ fC.
2. The value guaranteed by characterization, not 100% tested in production.
3. Only applicable as a constraint for a WRSR instruction when SRWD is set at 1.
4. For 4READ instruction, when dummy cycle=6, clock rate is 86MHz (default), and when dummy cycle=8, clock rate is 104MHz.

12. TIMING ANALYSIS

Figure 46. Serial Input Timing

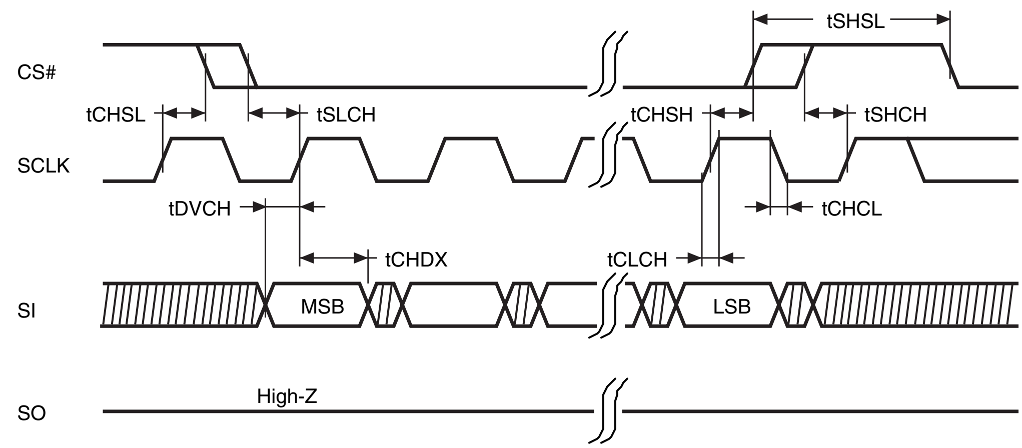


Figure 47. Output Timing

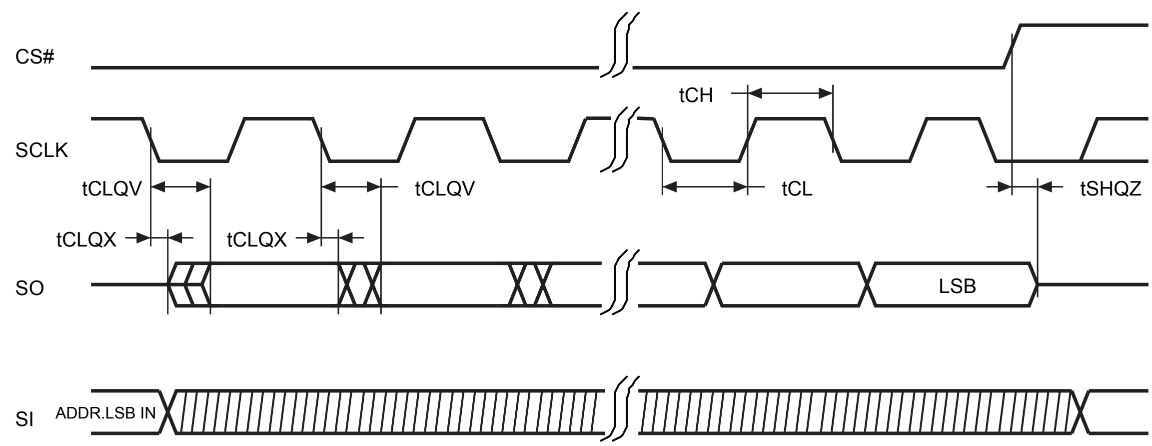
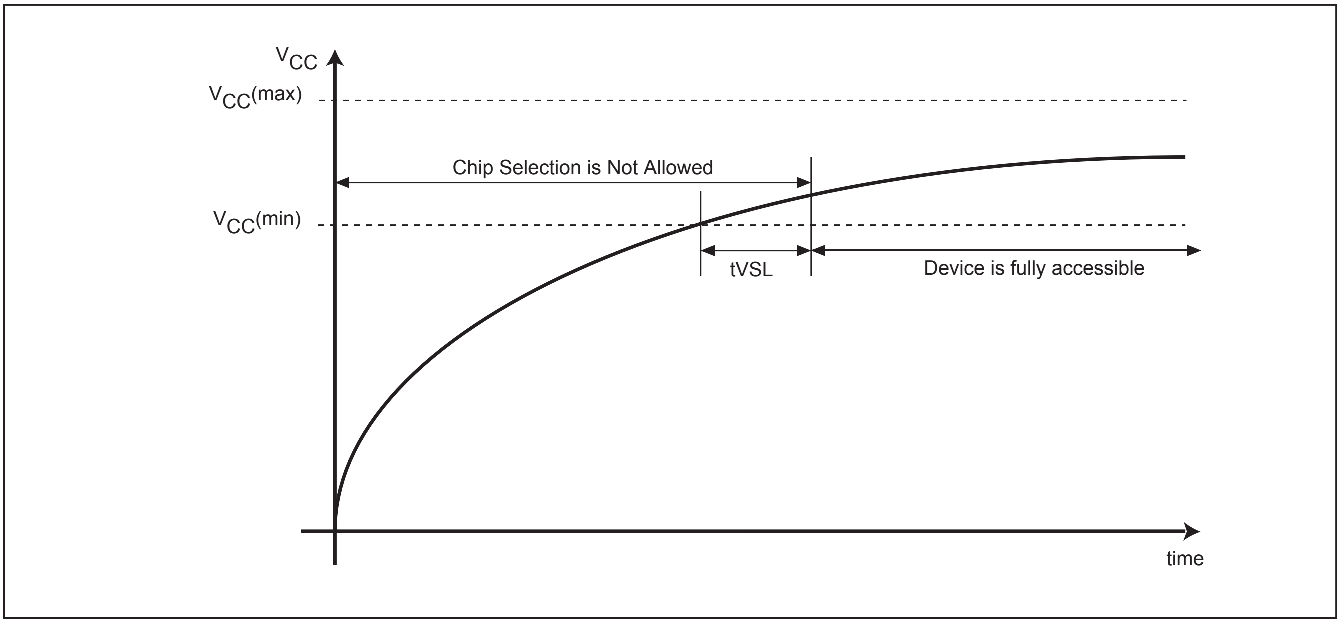


Figure 48. Power-Up Timing



Note: VCC (max.) is 3.6V and VCC (min.) is 2.7V.

Table 14. Power-Up Timing

Symbol	Parameter	Min.	Max.	Unit
tVSL(1)	VCC(min) to CS# low	300		us

Note: The parameter is characterized only.

12-1. Initial Delivery State

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0).

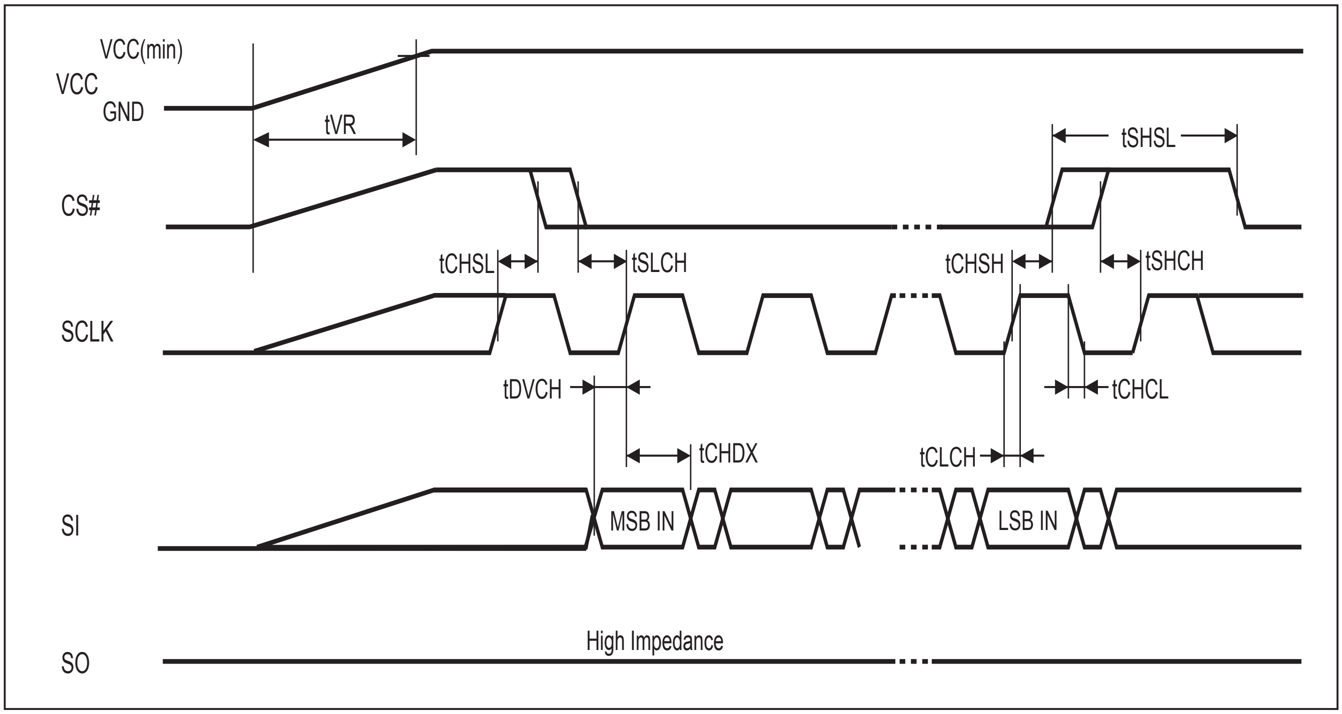
13. OPERATING CONDITIONS

At Device Power-Up and Power-Down

AC timing illustrated in *"Figure 49. AC Timing at Device Power-Up"* and *"Figure 50. Power-Down Sequence"* are for the supply voltages and the control signals at device power-up and power-down. If the timing in the figures is ignored, the device will not operate correctly.

During power-up and power-down, CS# needs to follow the voltage applied on VCC to keep the device not to be selected. The CS# can be driven low when VCC reach Vcc(min.) and wait a period of tVSL.

Figure 49. AC Timing at Device Power-Up

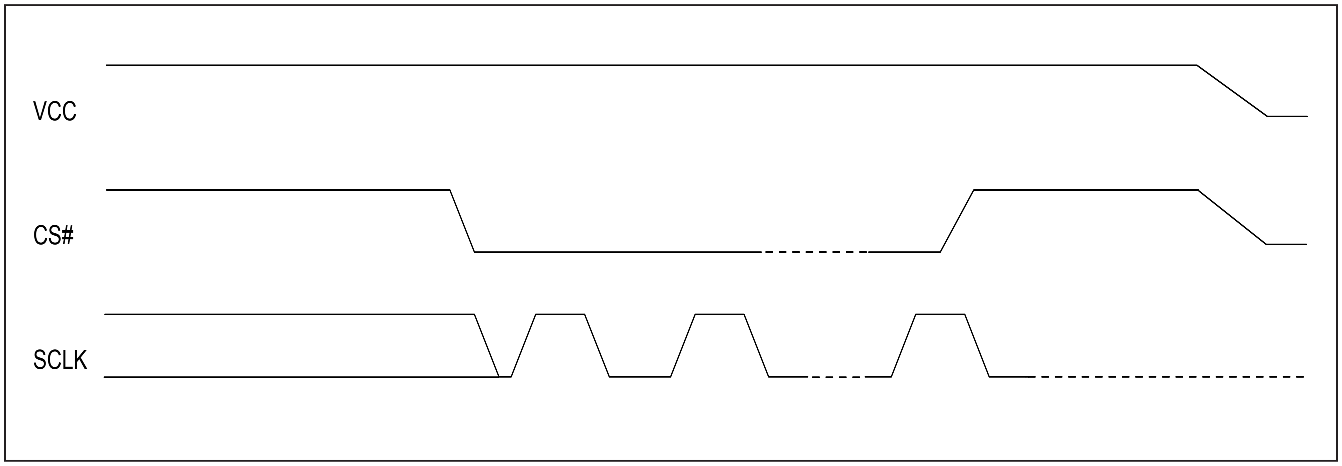


Symbol	Parameter	Notes	Min.	Max.	Unit
tVR	VCC Rise Time	1	20	500000	us/V

Notes :
1. Sampled, not 100% tested.
2. For AC spec tCHSL, tSLCH, tDVCH, tCHDX, tSHSL, tCHSH, tSHCH, tCHCL, tCLCH in the figure, please refer to *"Table 13. AC Characteristics"*.

Figure 50. Power-Down Sequence

During power-down, CS# needs to follow the voltage drop on VCC to avoid mis-operation.



14. ERASE AND PROGRAMMING PERFORMANCE

Parameter	Typ. (1)	Max. (2)	Unit
Write Status Register Cycle Time		40	ms
Sector Erase Time (4KB)	30	200	ms
Block Erase Time (32KB)	0.14	1.6	s
Block Erase Time (64KB)	0.25	2	s
Chip Erase Time	20	80	s
Byte Program Time (via page program command)	12	50	us
Page Program Time	0.7	3	ms
Erase/Program Cycle	100,000		cycles

Notes:
1. Typical program and erase time assumes the following conditions: 25°C, 3.3V, and checker board pattern.
2. Under worst conditions of 85°C and 2.7V.
3. System-level overhead is the time required to execute the first-bus-cycle sequence for the programming command.

15. DATA RETENTION

Parameter	Condition	Min.	Max.	Unit
Data retention	55˚C	20		years

16. LATCH-UP CHARACTERISTICS

	Min.	Max.
Input Voltage with respect to GND on all power pins, SI, CS#	-1.0V	2 VCCmax
Input Voltage with respect to GND on SO	-1.0V	VCC + 1.0V
Current	-100mA	+100mA
Includes all pins except VCC. Test conditions: VCC = 3.0V, one pin at a time.		

17. ORDERING INFORMATION

PART NO.	CLOCK (MHz)	TEMPERATURE	PACKAGE	Remark
MX25L6473EMI-10G *	104	-40°C~85°C	16-SOP (300mil)	
MX25L6473EM2I-10G	104	-40°C~85°C	8-SOP (200mil)	
MX25L6473EMBI-10G	104	-40°C~85°C	8-VSOP (200mil)	
MX25L6473EZNI-10G	104	-40°C~85°C	8-WSON (6x5mm)	

* Advanced Information.

18. PART NAME DESCRIPTION

MX 25 L 6473E M I - 10 G

OPTION:
G: RoHS Compliant and Halogen-free

SPEED:
10: 104MHz

TEMPERATURE RANGE:
I: Industrial (-40° C to 85° C)

PACKAGE:
M: 300mil 16-SOP
M2: 200mil 8-SOP
MB: 200mil 8-VSOP
ZN: 6x5mm 8-WSON

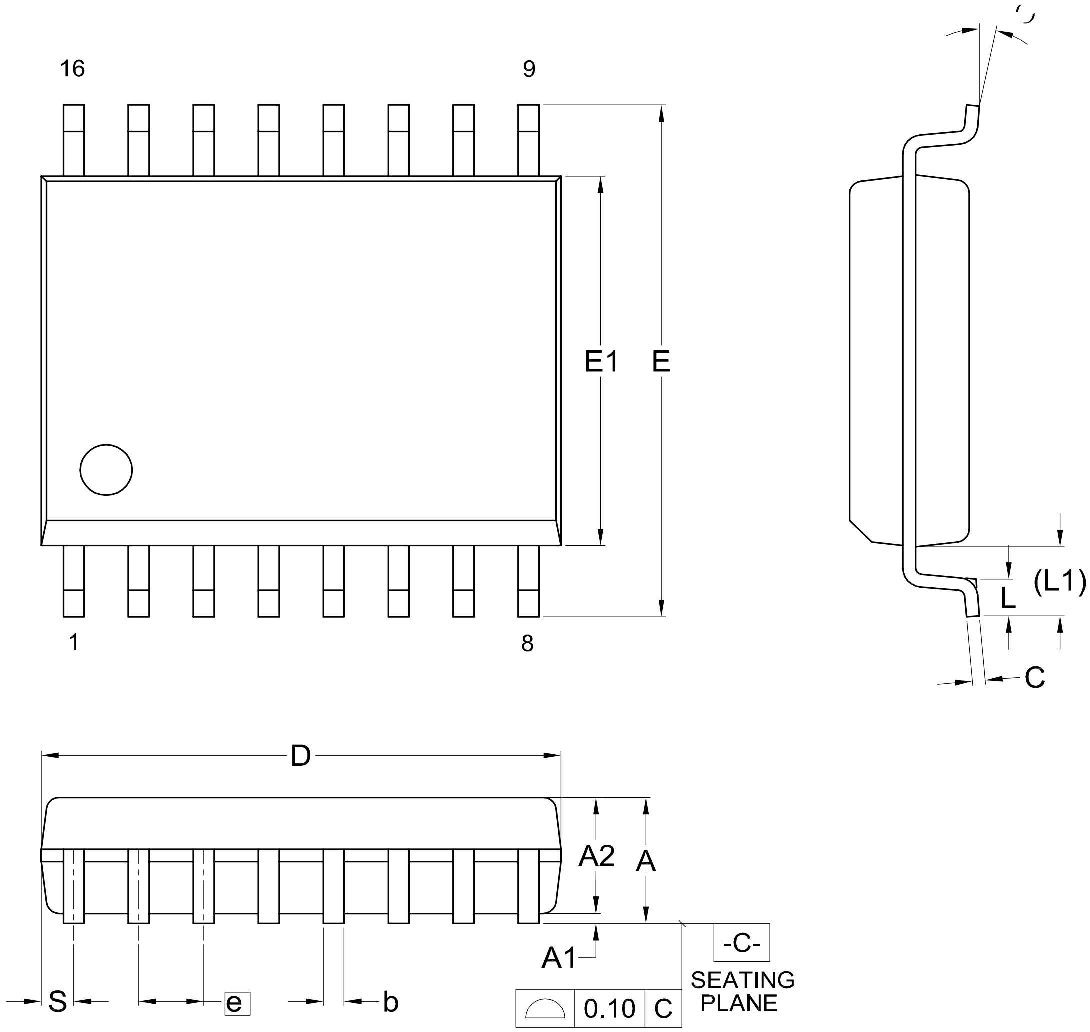
DENSITY & MODE:
6473E: 64Mb standard type

TYPE:
L: 3V

DEVICE:
25: Serial Flash

19. PACKAGE INFORMATION

Doc. Title: Package Outline for SOP 16L (300MIL)

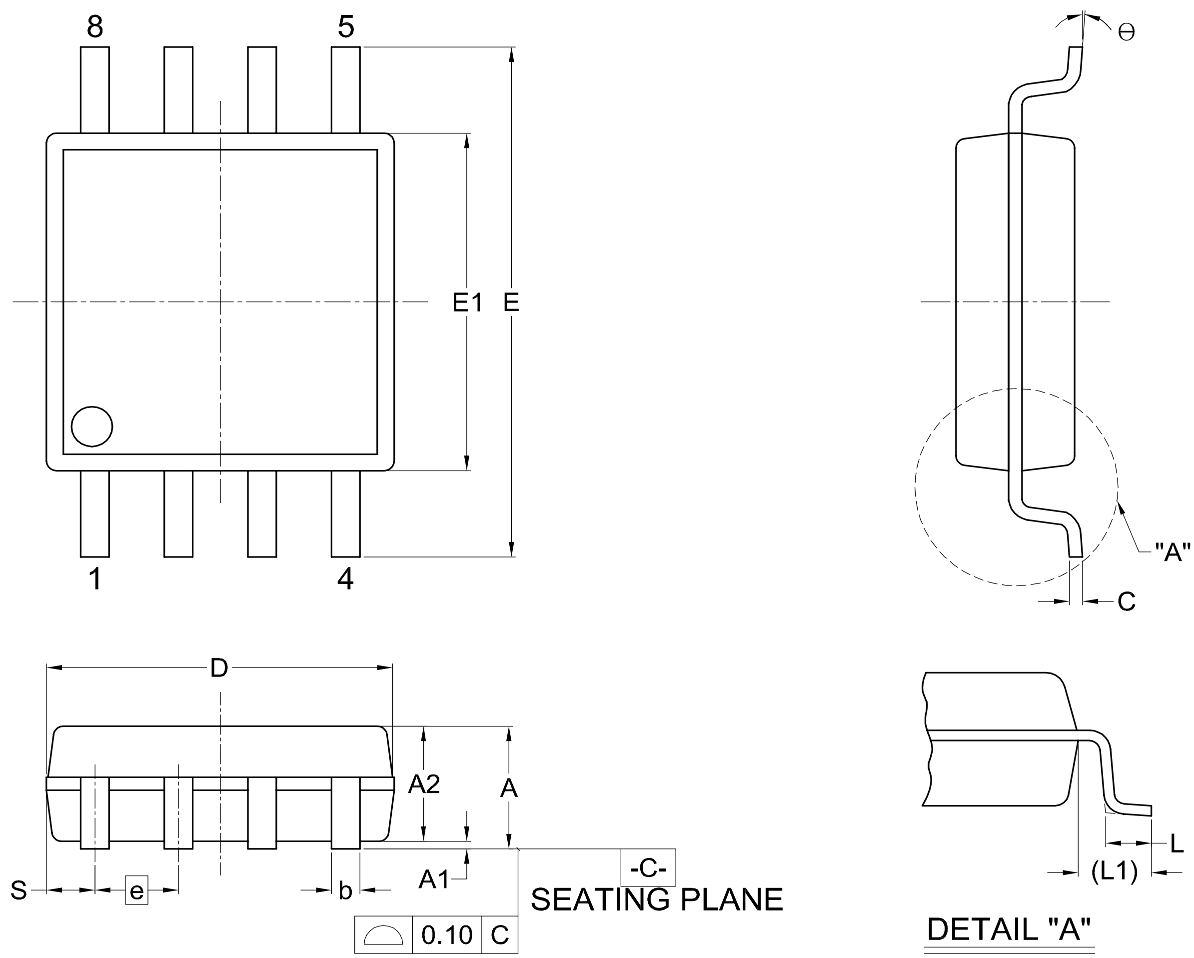


Dimensions (inch dimensions are derived from the original mm dimensions)

UNIT \ SYMBOL		A	A1	A2	b	C	D	E	E1	e	L	L1	S	Θ
mm	Min.	---	0.10	2.34	0.36	0.20	10.10	10.10	7.42	---	0.40	1.31	0.51	0
	Nom.	---	0.20	2.39	0.41	0.25	10.30	10.30	7.52	1.27	0.84	1.44	0.64	5
	Max.	2.65	0.30	2.44	0.51	0.30	10.50	10.50	7.60	---	1.27	1.57	0.77	8
Inch	Min.	---	0.004	0.092	0.014	0.008	0.397	0.397	0.292	---	0.016	0.052	0.020	0
	Nom.	---	0.008	0.094	0.016	0.010	0.405	0.405	0.296	0.050	0.033	0.057	0.025	5
	Max.	0.104	0.012	0.096	0.020	0.012	0.413	0.413	0.299	---	0.050	0.062	0.030	8

Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-1402	10	MS-013			

Doc. Title: Package Outline for SOP 8L 200MIL (official name - 209MIL)

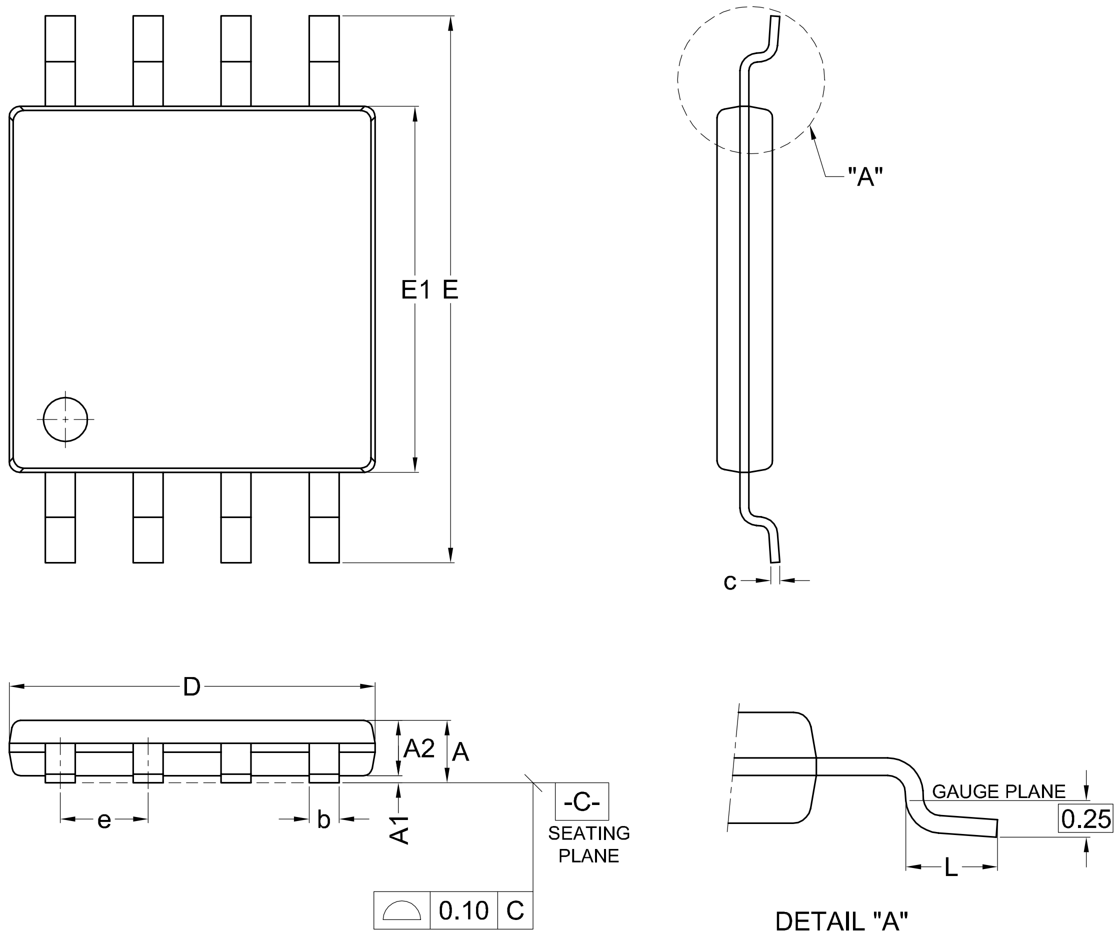


Dimensions (inch dimensions are derived from the original mm dimensions)

UNIT	SYMBOL	A	A1	A2	b	C	D	E	E1	e	L	L1	S	ϴ
mm	Min.	---	0.05	1.70	0.36	0.19	5.13	7.70	5.18	---	0.50	1.21	0.62	0
	Nom.	---	0.15	1.80	0.41	0.20	5.23	7.90	5.28	1.27	0.65	1.31	0.74	5
	Max.	2.16	0.20	1.91	0.51	0.25	5.33	8.10	5.38	---	0.80	1.41	0.88	8
Inch	Min.	---	0.002	0.067	0.014	0.007	0.202	0.303	0.204	---	0.020	0.048	0.024	0
	Nom.	---	0.006	0.071	0.016	0.008	0.206	0.311	0.208	0.050	0.026	0.052	0.029	5
	Max.	0.085	0.008	0.075	0.020	0.010	0.210	0.319	0.212	---	0.031	0.056	0.035	8

Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-1406	3				

Doc. Title: Package Outline for VSOP 8L 200MIL (official name - 209MIL)

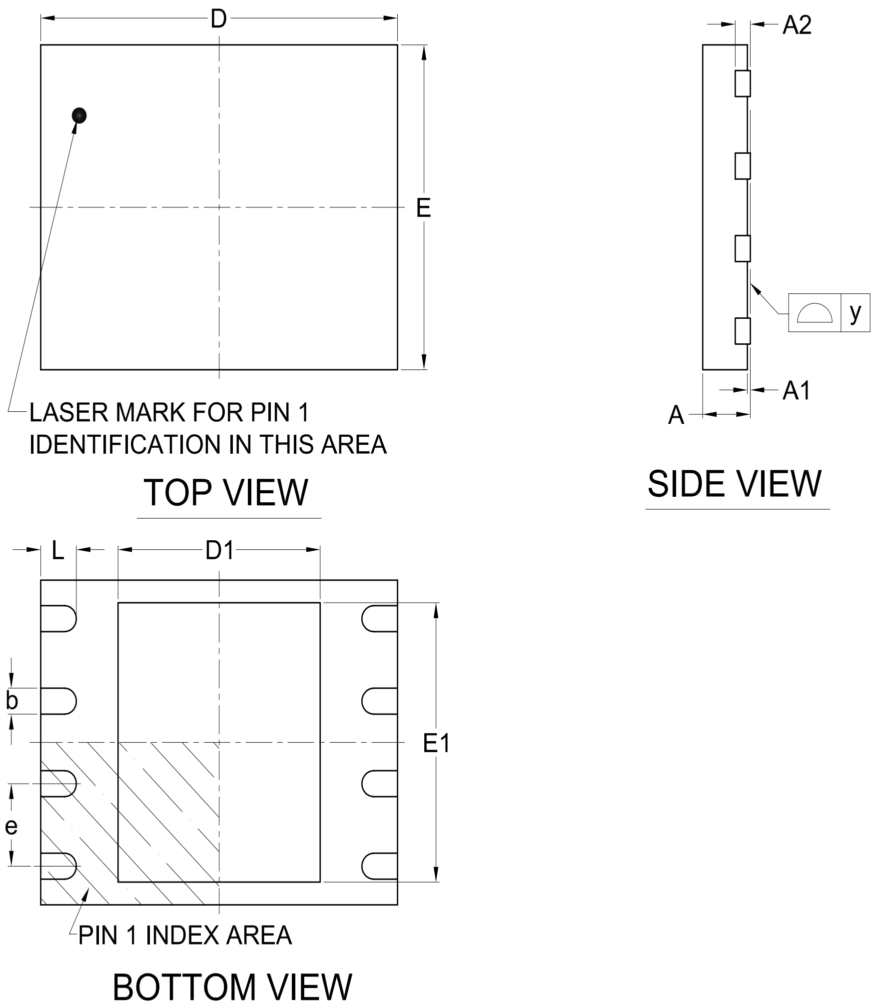


Dimensions (inch dimensions are derived from the original mm dimensions)

Unit \ Symbol		A	A1	A2	b	C	D	E	E1	e	L	Θ
mm	Min.	---	0.05	0.75	0.35	---	5.18	7.70	5.18	---	0.50	0°
	Nom.	---	0.10	0.80	0.42	0.127	5.28	7.90	5.28	1.27	0.65	---
	Max.	1.00	0.15	0.85	0.48	---	5.38	8.10	5.38	---	0.80	8°
Inch	Min.	---	0.002	0.030	0.014	---	0.204	0.303	0.204	---	0.020	0°
	Nom.	---	0.004	0.031	0.017	0.005	0.208	0.311	0.208	0.050	0.026	---
	Max.	0.039	0.006	0.033	0.019	---	0.212	0.319	0.212	---	0.031	8°

Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-1551	0				

Doc. Title: Package Outline for WSON 8L (6x5x0.8MM, LEAD PITCH 1.27MM)



Note:

This package has an exposed metal pad underneath the package. It is recommended to leave the metal pad floating or to connect it to the same ground as the GND pin of the package. Do not connect the metal pad to any other voltage or signal line on the PCB. Avoid placing vias or traces underneath the metal pad. Connection of this metal pad to any other voltage or signal line can result in shorts and/or electrical malfunction of the device.

Dimensions (inch dimensions are derived from the original mm dimensions)

UNIT \ SYMBOL		A	A1	A2	b	D	D1	E	E1	L	e	y
mm	Min.	0.70	---	---	0.35	5.90	3.30	4.90	3.90	0.50	---	0.00
	Nom.	---	---	0.20	0.40	6.00	3.40	5.00	4.00	0.60	1.27	---
	Max.	0.80	0.05	---	0.48	6.10	3.50	5.10	4.10	0.75	---	0.08
Inch	Min.	0.028	---	---	0.014	0.232	0.129	0.193	0.154	0.020	---	0.00
	Nom.	---	---	0.008	0.016	0.236	0.134	0.197	0.157	0.024	0.05	---
	Max.	0.032	0.002	---	0.019	0.240	0.138	0.201	0.161	0.030	---	0.003

Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-3401	6	MO-220			

20. REVISION HISTORY

Revision No.	Description	Page	Date
0.00	1. Initial released	All	NOV/02/2012
1.0	1. Removed Advanced Information state	P4	DEC/25/2012
	2. Kept MX25L6473EMI-10G as Advanced Information	P79	
1.1	1. Updated parameters for DC/AC Characteristics	P4,71,73	NOV/06/2013
	2. Updated Erase and Programming Performance	P4,78	
	3. Modified VCC to Ground Potential & Capacitance table	P69	

Except for customized products which have been expressly identified in the applicable agreement, Macronix's products are designed, developed, and/or manufactured for ordinary business, industrial, personal, and/or household applications only, and not for use in any applications which may, directly or indirectly, cause death, personal injury, or severe property damages. In the event Macronix products are used in contradicted to their target usage above, the buyer shall take any and all actions to ensure said Macronix's product qualified for its actual use in accordance with the applicable laws and regulations; and Macronix as well as it's suppliers and/or distributors shall be released from any and all liability arisen therefrom.

For the contact and order information, please visit Macronix's Web site at: http://www.macronix.com