

Features

- ESD Protection for 1 Line with Bi-directional
- Provide ESD protection for the protected line to IEC 61000-4-2 (ESD) $\pm 15\text{kV}$ (air), $\pm 8\text{kV}$ (contact)
- **Ultra low capacitance: 0.8pF typical**
- For low operating voltage applications: **5V and below**
- **0402 small DFN package** saves board space
- Protect one I/O line
- Fast turn-on and Low clamping voltage
- Solid-state silicon-avalanche and active circuit triggering technology
- **Green Part**

Applications

- Antenna applications
- Hand Held Portable Applications
- High Definition Multi-media Interface (HDMI)
- Digital Visual Interface (DVI)
- Display Port
- Serial ATA
- Desktop and Notebooks PCs
- Consumer Applications

Description

AZ5425-01F is a design which includes a bi-directional ESD rated clamping cell to protect high speed data interfaces in an electronic systems. The AZ5425-01F has been specifically designed to protect sensitive components which are connected to data and transmission lines from over-voltage caused by Electrostatic

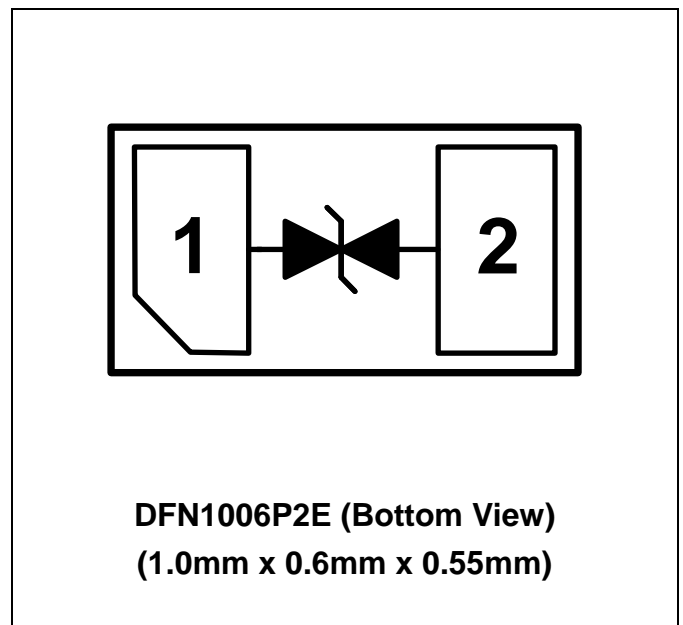
Discharging (ESD).

AZ5425-01F is a unique design which includes proprietary clamping cells with ultra low capacitance in a small package. During transient conditions, the proprietary clamping cells prevent over-voltage on the control/data lines, protecting any downstream components.

AZ5425-01F is bi-directional and may be used on lines where the signal swings above and below ground.

AZ5425-01F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 ($\pm 15\text{kV}$ air, $\pm 8\text{kV}$ contact discharge).

Circuit Diagram / Pin Configuration





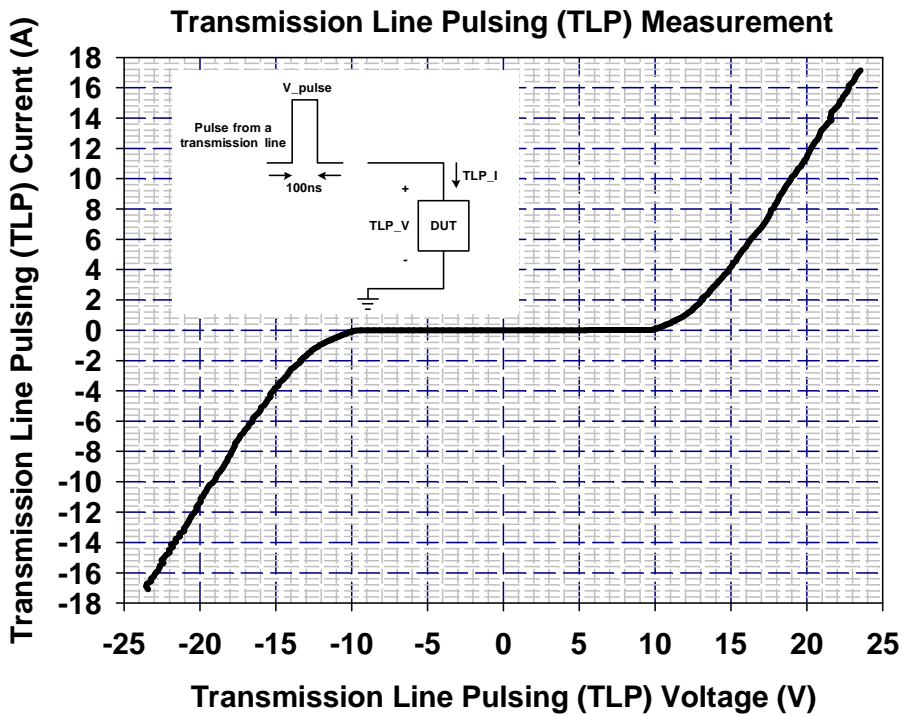
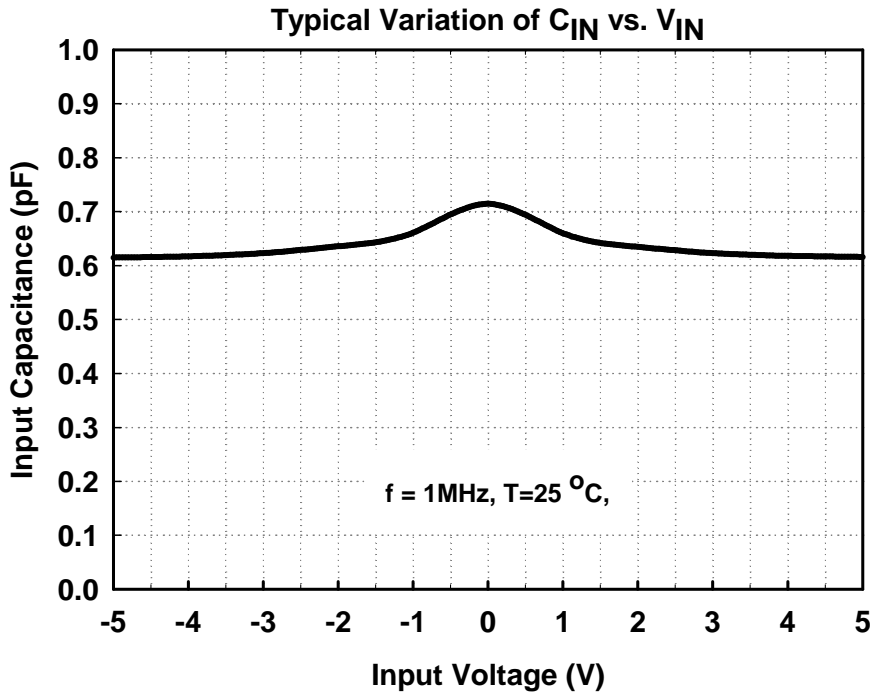
SPECIFICATIONS

| ABSOLUTE MAXIMUM RATINGS | | | |
|-----------------------------------|-----------|---------------|-------------|
| PARAMETER | PARAMETER | RATING | UNITS |
| Operating DC Voltage (I/O to GND) | V_{DC} | ± 6 | V |
| ESD per IEC 61000-4-2 (Air) | V_{ESD} | ± 15 | kV |
| ESD per IEC 61000-4-2 (Contact) | | ± 8 | kV |
| Lead Soldering Temperature | T_{SOL} | 260 (10 sec.) | $^{\circ}C$ |
| Operating Temperature | T_{OP} | -40 to +85 | $^{\circ}C$ |
| Storage Temperature | T_{STO} | -55 to +150 | $^{\circ}C$ |

| ELECTRICAL CHARACTERISTICS | | | | | | |
|--------------------------------|---------------|--|------|-----|-----|----------|
| PARAMETER | SYMBOL | CONDITIONS | MINI | TYP | MAX | UNITS |
| Stand-Off Voltage | V_{RWM} | $T=25^{\circ}C$, I/O to GND, or GND to I/O. | | | 5 | V |
| Leakage Current | I_{Leak} | $V_{RWM} = 5V$, $T=25^{\circ}C$, I/O to GND, or GND to I/O. | | | 1 | μA |
| Breakdown Voltage | V_{BV} | $I_{BV} = 1mA$, $T=25^{\circ}C$, I/O to GND, or GND to I/O. | 7 | | | V |
| ESD Clamping Voltage | V_{clamp} | IEC 61000-4-2, 6kV Contact mode, $T=25^{\circ}C$, I/O to GND, or GND to I/O. | | 24 | | V |
| ESD Dynamic Turn-on Resistance | $R_{dynamic}$ | IEC 61000-4-2, 0~6kV, Contact mode, $T=25^{\circ}C$, I/O to GND, or GND to I/O. | | 0.7 | | Ω |
| Input Capacitance | C_{IN} | $V_R = 0V$, $f = 1MHz$, $T=25^{\circ}C$, I/O to GND. | | 0.8 | 1.0 | pF |



Typical Characteristics





Applications Information

The AZ5425-01F is designed to protect one line against System ESD pulse by clamping it to an acceptable reference. It provides bi-directional protection.

The usage of the AZ5425-01F is shown in Fig. 1. Protected line, such as data line, control line, or power line, is connected at pin 1. The pin 2 is connected to a ground plane on the board. In order to minimize parasitic inductance in the board traces, all path lengths connected to the pins of AZ5425-01F should be kept as short as possible.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ5425-01F.
- Place the AZ5425-01F near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

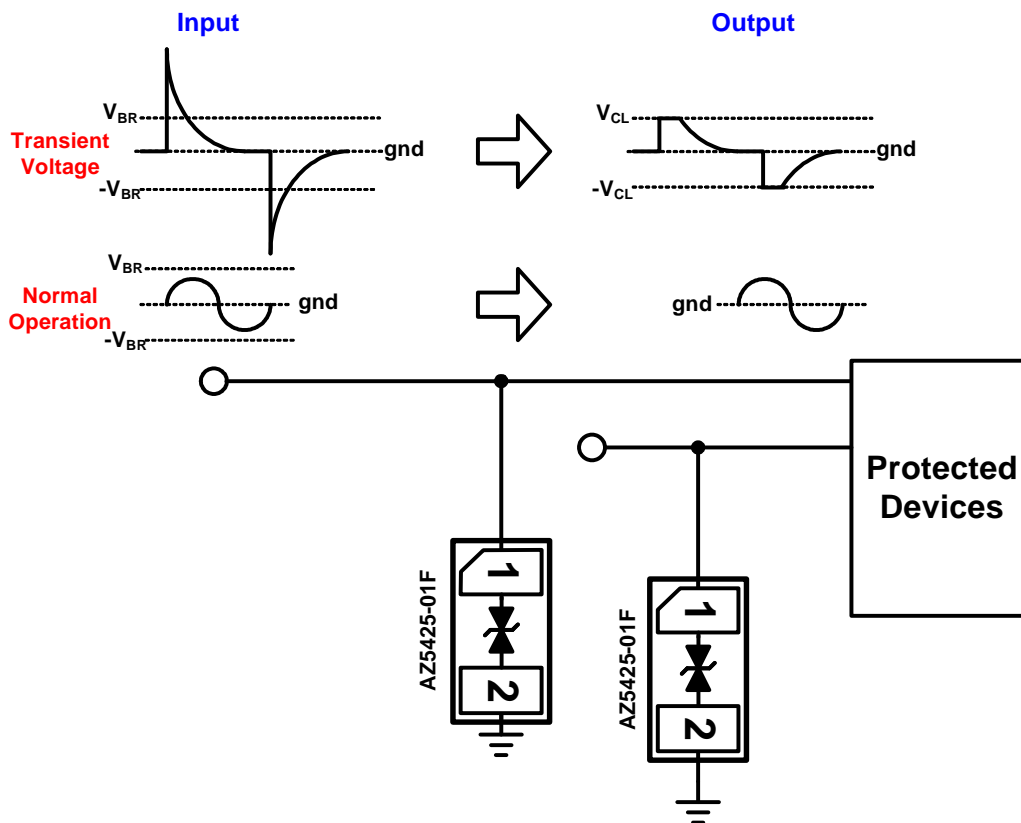


Fig. 1



Fig. 2 shows another simplified example of using AZ5425-01F to protect the control line, high speed data line, and power line from ESD transient stress.

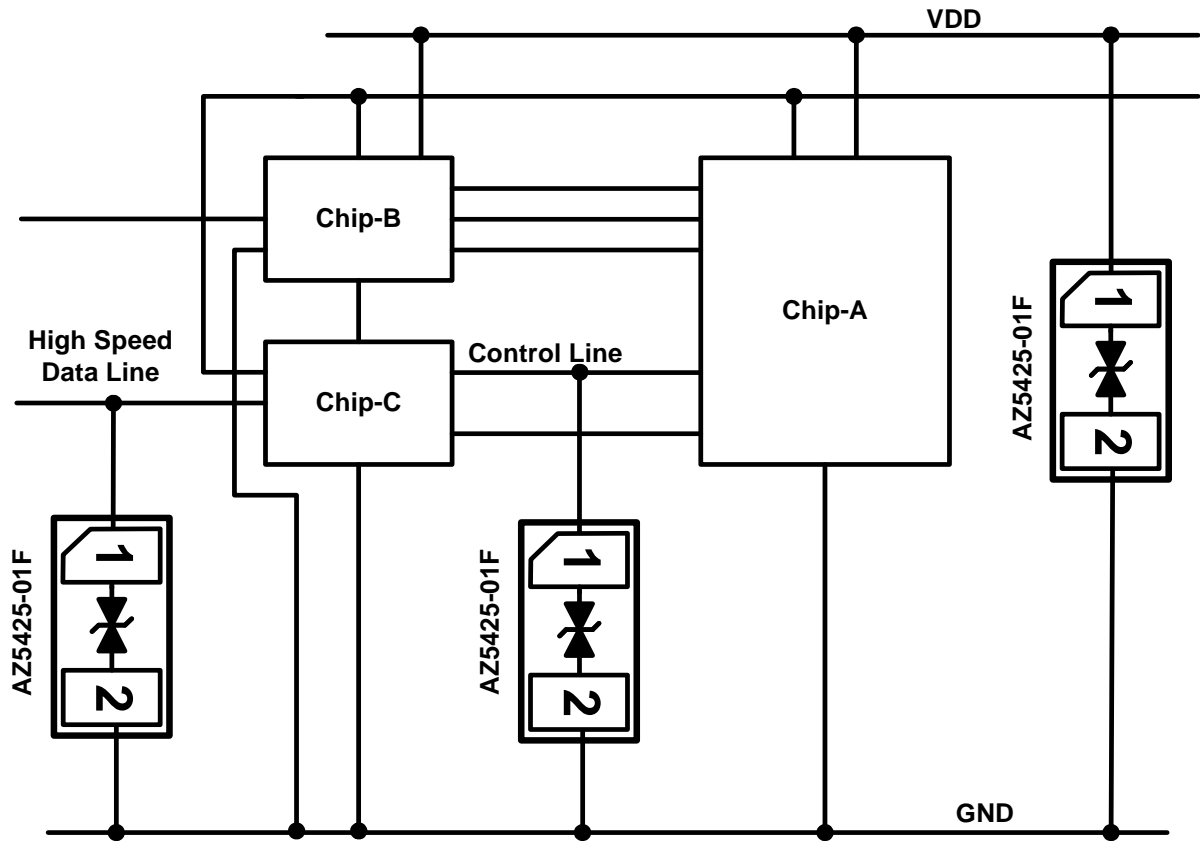
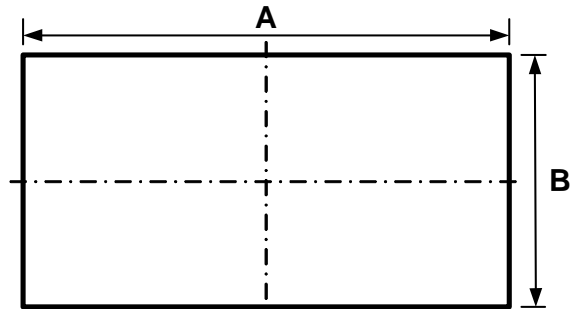


Fig. 2

Mechanical Details

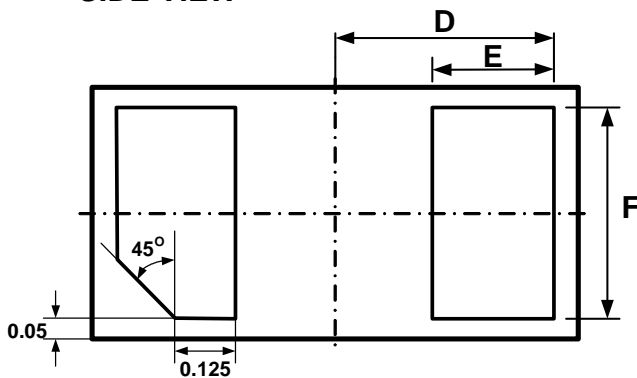
DFN1006P2E PACKAGE DIAGRAMS



TOP VIEW



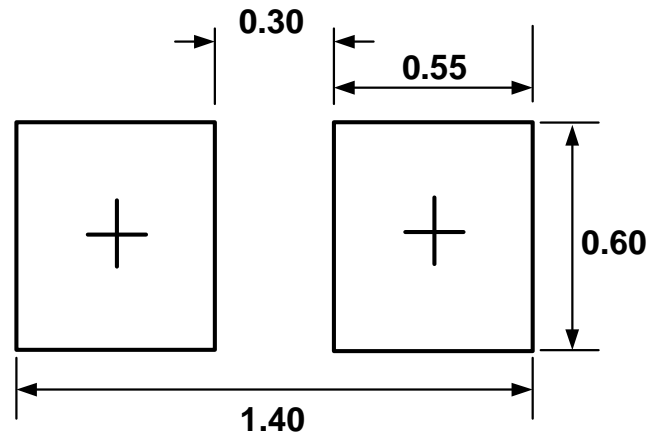
SIDE VIEW



BOTTOM VIEW

| SYMBOL | Millimeters | | |
|--------|-------------|------|------|
| | MIN. | NOM. | MAX. |
| A | 0.95 | 1.00 | 1.05 |
| B | 0.55 | 0.60 | 0.65 |
| C | 0.50 | 0.55 | 0.60 |
| D | 0.45 | | |
| E | 0.20 | 0.25 | 0.30 |
| F | 0.45 | 0.50 | 0.55 |

LAND LAYOUT

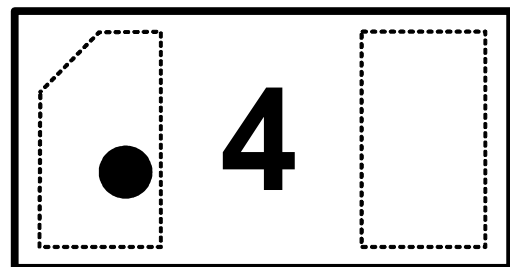


(Unit: mm)

Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

MARKING CODE



Top View

| Part Number | Marking Code |
|-----------------------------|--------------|
| AZ5425-01F.R7G | 4 |
| AZ5425-01F (Engineering) | 1 |



Ordering Information

| PN# | Material | Type | Reel size | MOQ/internal box | MOQ/carton |
|---------------|----------|------|-----------|--------------------|----------------------|
| AZ5425-01FR7G | Green | T/R | 7 inch | 4 reel= 12,000/box | 6 box =72,000/carton |

Revision History

| Revision | Modification Description |
|---------------------|--|
| Revision 2009/05/19 | Formal Release. |
| Revision 2010/07/07 | 1. Update the dimension tolerances of E, F, in the Package Diagrams. 2. Eliminate the C1 dimension. |
| Revision 2010/07/13 | In Package Diagrams, add the tolerant values for "A" and "B". |
| Revision 2011/05/24 | 1. Update the Company Logo. 2. Add the Ordering Information. |
| Revision 2011/06/20 | Mark the part number at Marking code with AZ5425-01F.R7G instead of AZ5425-01F. |
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