REALTEK

RTL8111C-GR

INTEGRATED GIGABIT ETHERNET CONTROLLER FOR PCI EXPRESS™ APPLICATIONS

DATASHEET

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2006/12/12	First release.
1.1	2007/02/09	Changed Figure 1, Pin Assignments, page 3. Changed Table 8, Power & Ground, page 7. Removed SMBus table. Added Table 9, GPIO Pins, page 7. Changed Table 10, NC (Not Connected) Pins, page 4. Renamed VDD12 to DVDD12.

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1. General Description

The Realtek RTL8111C-GR Gigabit Ethernet controller combines a triple-speed IEEE 802.3 compliant Media Access Controller (MAC) with a triple-speed Ethernet transceiver, PCI Express bus controller, and embedded memory. With state-of-the-art DSP technology and mixed-mode signal technology, the RTL8111C-GR offers high-speed transmission over CAT 5 UTP cable or CAT 3 UTP (10Mbps only) cable. Functions such as Crossover Detection & Auto-Correction, polarity correction, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery, and error correction are implemented to provide robust transmission and reception capability at high speeds.

The RTL8111C-GR is compliant with the IEEE 802.3u specification for 10/100Mbps Ethernet and the IEEE 802.3ab specification for 1000Mbps Ethernet. It also supports an auxiliary power auto-detect function, and will auto-configure related bits of the PCI power management registers in PCI configuration space.

Advanced Configuration Power management Interface (ACPI)—power management for modern operating systems that are capable of Operating System-directed Power Management (OSPM)—is supported to achieve the most efficient power management possible. PCI MSI (Message Signaled Interrupt) and MSI-X are also supported.

In addition to the ACPI feature, remote wake-up (including AMD Magic Packet™ and Microsoft® Wake-up frame) is supported in both ACPI and APM (Advanced Power Management) environments. To support WOL from a deep power down state (e.g., D3cold, i.e. main power is off and only auxiliary exists), the auxiliary power source must be able to provide the needed power for the RTL8111C-GR.

The RTL8111C-GR is fully compliant with Microsoft® NDIS5, NDIS6(IPv4, IPv6, TCP, UDP) Checksum and Segmentation Task-offload(Large send and Giant send) features, and supports IEEE 802 IP Layer 2 priority encoding and IEEE 802.1Q Virtual bridged Local Area Network (VLAN). The above features contribute to lowering CPU utilization, especially benefiting performance when in operation on a network server.

The RTL8111C-GR supports Receive Side Scaling (RSS) to hash incoming TCP connections and load-balance received data processing across multiple CPUs. RSS improves the number of transactions per second and number of connections per second, for increased network throughput.

The device also features inter-connect PCI Express technology. PCI Express is a high-bandwidth, low pin count, serial, interconnect technology that offers significant improvements in performance over conventional PCI and also maintains software compatibility with existing PCI infrastructure. The device embeds an adaptive equalizer in the PCIe PHY for ease of system integration and excellent link quality. The equalizer enables the length of the PCB traces to reach 40 inches.

The RTL8111C-GR is suitable for multiple market segments and emerging applications, such as desktop, mobile, workstation, server, communications platforms, and embedded applications.

2. Features

- Integrated 10/100/1000 transceiver
- Auto-Negotiation with Next Page capability
- Supports PCI Express™ 1.1
- Supports pair swap/polarity/skew correction
- Crossover Detection & Auto-Correction
- Wake-on-LAN and remote wake-up support
- Microsoft® NDIS5, NDIS6 Checksum Offload (IPv4, IPv6, TCP, UDP) and Segmentation Task-offload (Large send and Giant send) support
- Supports Full Duplex flow control (IEEE 802.3x)
- Fully compliant with IEEE 802.3, IEEE 802.3u, IEEE 802.3ab

- Supports IEEE 802.1P Layer 2 Priority Encoding
- Supports IEEE 802.1Q VLAN tagging
- Serial EEPROM
- Transmit/Receive on-chip buffer support
- Supports power down/link down power saving
- Supports PCI MSI (Message Signaled Interrupt) and MSI-X
- Supports Receive-Side Scaling (RSS)
- 64-pin QFN package (Green package)
- Embeds an adaptive equalizer in PCI express PHY (PCB traces to reach 40 inches)

3. System Applications

- PCI Express™ Gigabit Ethernet on Motherboard, Notebook, or Embedded system

4. Pin Assignments
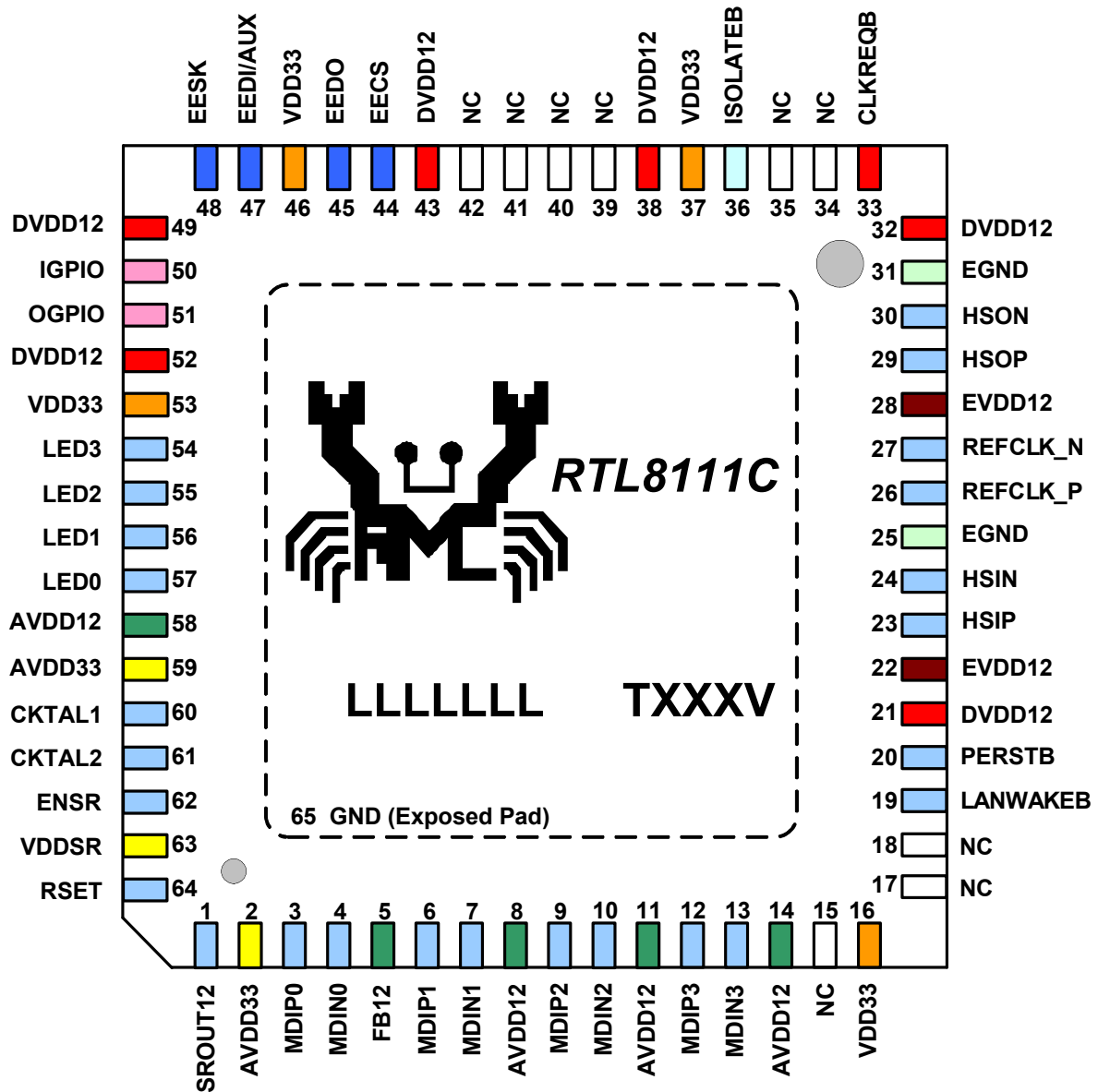
Figure 1. Pin Assignments

4.1. Package Identification

'Green' package is indicated by a 'G' in the location marked 'T' in Figure 1.

5.   Pin Descriptions

The signal type codes below are used in the following tables:

I: Input
O: Output
T/S: Tri-State bi-directional input/output pin

S/T/S: Sustained Tri-State
O/D: Open Drain

5.1.   Power Management/Isolation

Table 1.   Power Management/Isolation

Symbol	Type	Pin No	Description
LANWAKEB	O/D	19	Power Management Event: Open drain, active low. Used to reactivate the PCI Express slot's main power rails and reference clocks.
ISOLATEB	I	36	Isolate Pin: Active low. Used to isolate the RTL8111C-GR from the PCI Express bus. The RTL8111C-GR will not drive its PCI Express outputs (excluding LANWAKEB) and will not sample its PCI Express input as long as the Isolate pin is asserted.

5.2.   PCI Express Interface

Table 2.   PCI Express Interface

Symbol	Type	Pin No	Description
REFCLK_P	I	26	PCI Express Differential Reference Clock Source: 100MHz ± 300ppm.
REFCLK_N	I	27	
HSOP	O	29	PCI Express Transmit Differential Pair.
HSON	O	30	
HSIP	I	23	PCI Express Receive Differential Pair.
HSIN	I	24	
PERSTB	I	20	PCI Express Reset Signal: Active low. When the PERSTB is asserted at power-on state, the RTL8111C-GR returns to a pre-defined reset state and is ready for initialization and configuration after the de-assertion of the PERSTB.
CLKREQB	O/D	33	Reference clock request signal. This signal is used by the RTL8111C-GR to request starting of the PCI Express reference clock.

5.3. EEPROM

Table 3.   EEPROM

Symbol	Type	Pin No	Description
EESK	O	48	Serial data clock.
EEDI/AUX	O/I	47	EEDI: Output to serial data input pin of EEPROM. AUX: Input pin to detect if Aux. Power exists or not on initial power-on. This pin should be connected to EEPROM. To support wakeup from ACPI D3cold or APM power-down, this pin must be pulled high to Aux. Power via a resistor. If this pin is not pulled high to Aux. Power, the RTL8111C-GR assumes that no Aux. Power exists.
EEDO	I	45	Input from serial data output pin of EEPROM.
EECS	O	44	EECS: EEPROM chip select.

5.4. Transceiver Interface

Table 4.   Transceiver Interface

Symbol	Type	Pin No	Description
MDIP0	I/O	3	In MDI mode, this is the first pair in 1000Base-T, i.e. the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
MDIN0	I/O	4	
MDIP1	I/O	6	In MDI mode, this is the second pair in 1000Base-T, i.e. the BI_DB+/- pair, and is the transmit pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
MDIN1	I/O	7	
MDIP2	I/O	9	In MDI mode, this is the third pair in 1000Base-T, i.e. the BI_DC+/- pair.
MDIN2	I/O	10	In MDI crossover mode, this pair acts as the BI_DD+/- pair.
MDIP3	I/O	12	In MDI mode, this is the fourth pair in 1000Base-T, i.e. the BI_DD+/- pair.
MDIN3	I/O	13	In MDI crossover mode, this pair acts as the BI_DC+/- pair.

5.5. Clock

Table 5.   Clock

Symbol	Type	Pin No	Description
CKTAL1	I	60	Input of 25MHz clock reference.
CKTAL2	O	61	Output of 25MHz clock reference.

5.6. Regulator & Reference

Table 6.   Regulator & Reference

Symbol	Type	Pin No	Description
SROUT12	O	1	Switching regulator 1.2V output. Connect to 5uH inductor.
FB12	I	5	Feedback pin for switching regulator.
ENSR	I	62	3.3V: Enable switching regulator. 0 V: disable switching regulator.
VDDSR	Power	63	Digital 3.3V power supply for switching regulator.
RSET	I	64	Reference. External resistor reference.

5.7. LEDs

Table 7.   LEDs

Symbol	Type	Pin No	Description				
LED0	O	57	LEDS1-0	00	01	10	11
LED1	O	56	LED0	Tx/Rx	Tx/Rx	Tx	LINK10/ACT
LED2	O	55	LED1	LINK100	LINK10/100/1000	LINK	LINK100/ACT
LED3	O	54	LED2	LINK10	LINK10/100	Rx	FULL
			LED3	LINK1000	LINK1000	FULL	LINK1000/ACT

Note 1: During power down mode, the LED signals are logic high.

Note 2: LEDS1-0's initial value comes from the 93C46. If there is no 93C46, the
*   default value of the (LEDS1, LEDS0) = (1, 1).*

5.8. Power & Ground

Table 8. Power & Ground

Symbol	Type	Pin No	Description
VDD33	Power	16, 37, 46, 53	Digital 3.3V power supply.
DVDD12	Power	21, 32, 38, 43, 49, 52	Digital 1.2V power supply.
AVDD12	Power	8, 11, 14, 58	Analog 1.2V power supply.
EVDD12	Power	22, 28	Analog 1.2V power supply.
AVDD33	Power	2, 59	Analog 3.3V power supply.
EGND	Power	25, 31	Analog Ground.
GND	Power	65	Ground (Exposed Pad).

Note: Refer to the most updated schematic circuit for correct configuration.

5.9. GPIO

Table 9. GPIO Pins

Symbol	Type	Pin No	Description
IGPIO	I	50	Input GPIO Pin.
OGPIO	O	51	Output GPIO Pin. This pin reflects the link up or link down state. High: Link up Low: Link down.

5.10. NC (Not Connected) Pins

Table 10. NC (Not Connected) Pins

Symbol	Type	Pin No	Description
NC	-	15, 17, 18, 34, 35, 39, 40, 41, 42	Not Connected.

6. Functional Description

6.1. PCI Express Bus Interface

The RTL8111C-GR is compliant with PCI Express Base Specification Revision 1.1, and runs at a 2.5GHz signaling rate with X1 link width, i.e., one transmit and one receive differential pair. The RTL8111C-GR supports four types of PCI Express messages: interrupt messages, error messages, power management messages, and hot-plug messages. To ease PCB layout constraints, PCI Express lane polarity reversal and link reversal are also supported.

6.1.1. PCI Express Transmitter

The RTL8111C-GR's PCI Express block receives digital data from the Ethernet interface and performs data scrambling with Linear Feedback Shift Register (LFSR) and 8B/10B coding technology into 10-bit code groups. Data scrambling is used to reduce the possibility of electrical resonance on the link, and 8B/10B coding technology is used to benefit embedded clocking, error detection, and DC balance by adding an overhead to the system through the addition of 2 extra bits. The data code groups are passed through its serializer for packet framing. The generated 2.5Gbps serial data is transmitted onto the PCB trace to its upstream device via a differential driver.

6.1.2. PCI Express Receiver

The RTL8111C-GR's PCI Express block receives 2.5Gbps serial data from its upstream device to generate parallel data. The receiver's PLL circuits are re-synchronized to maintain bit and symbol lock. Through 8B/10B decoding technology and data de-scrambling, the original digital data is recovered and passed to the RTL8111C-GR's internal Ethernet MAC to be transmitted onto the Ethernet media.

6.2. LED Functions

The RTL8111C-GR supports four LED signals in four different configurable operation modes. The following sections describe the various LED actions.

6.2.1. Link Monitor

The Link Monitor senses link integrity, such as LINK10, LINK100, LINK1000, LINK10/100/1000, LINK10/ACT, LINK100/ACT, or LINK1000/ACT. Whenever link status is established, the specific link LED pin is driven low. Once a cable is disconnected, the link LED pin is driven high, indicating that no network connection exists.

6.2.2. Rx LED

In 10/100/1000Mbps mode, blinking of the Rx LED indicates that receive activity is occurring.
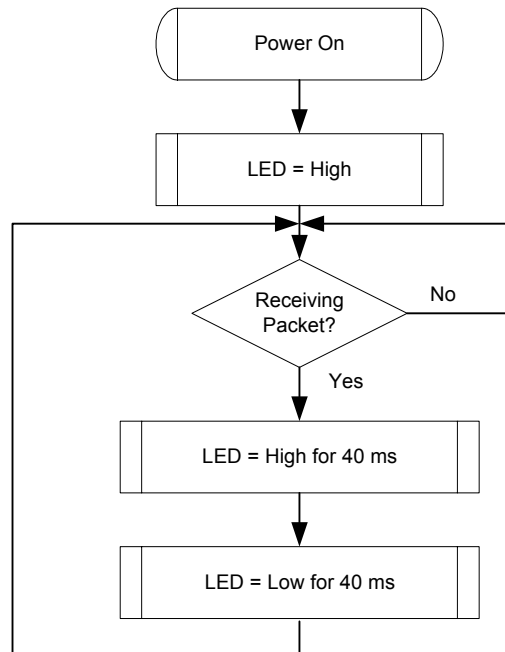
Figure 2.   Rx LED

6.2.3. Tx LED

In 10/100/1000Mbps mode, blinking of the Tx LED indicates that transmit activity is occurring.
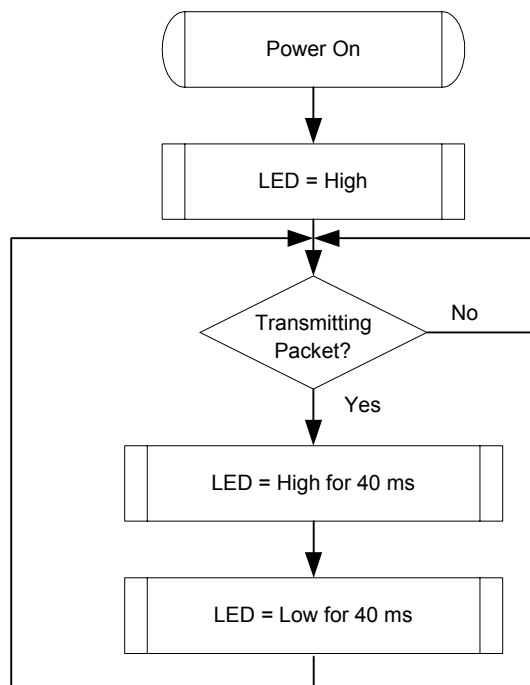
Figure 3.   Tx LED

6.2.4. Tx/Rx LED

In 10/100/1000Mbps mode, blinking of the Tx/Rx LED indicates that both transmit and receive activity is occurring.

```
                    ╭─────────────────╮
                    │    Power On      │
                    ╰─────────────────╯
                             │
                             ▼
                   ┌─────────────────┐
                   │   LED = High     │
                   └─────────────────┘
                             │
         ┌───────────────────┼──────────────────┐
         │                   ▼                  │
         │              ◇─────────◇       No    │
         │             Tx/Rx Packet? ───────────┘
         │              ◇─────────◇
         │                   │ Yes
         │                   ▼
         │        ┌─────────────────────┐
         │        │ LED = High for 40 ms │
         │        └─────────────────────┘
         │                   │
         │                   ▼
         │        ┌─────────────────────┐
         │        │ LED = Low for 40 ms  │
         │        └─────────────────────┘
         │                   │
         └───────────────────┘
```
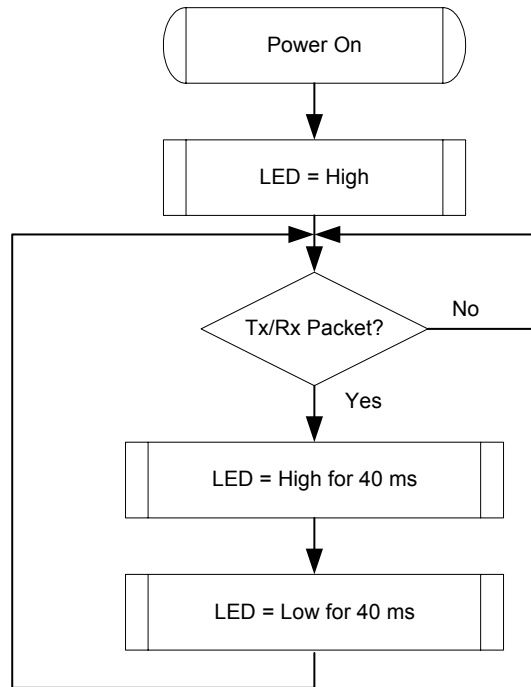
Figure 4.   Tx/Rx LED

6.2.5. LINK/ACT LED

In 10/100/1000Mbps mode, blinking of the LINK/ACT LED indicates that the RTL8111C-GR is linked and operating properly. When this LED is high for extended periods, it indicates that a link problem exists.

```
                    ┌──────────────┐
                    │   Power On   │
                    └──────┬───────┘
                           │
                           ▼
                    ┌──────────────┐
                    │  LED = High  │◄──────────┐
                    └──────┬───────┘           │
                           │                   │
                           ▼                   │
                        ◇ Link? ◇ ── No ───────┘
                           │
                          Yes
                           ▼
                    ┌──────────────┐
          ┌─────────│  LED = Low   │
          │         └──────┬───────┘
          │                │
          │                ▼
          │            ◇ Tx/Rx ◇ ── No ──►
          │             Packet?
          │                │
          │               Yes
          │                ▼
          │       ┌──────────────────────┐
          │       │ LED = High for 40 ms │
          │       └──────────┬───────────┘
          │                  │
          │                  ▼
          │       ┌──────────────────────┐
          │       │ LED = Low for 40 ms  │
          │       └──────────┬───────────┘
          │                  │
          └──────────────────┘
```
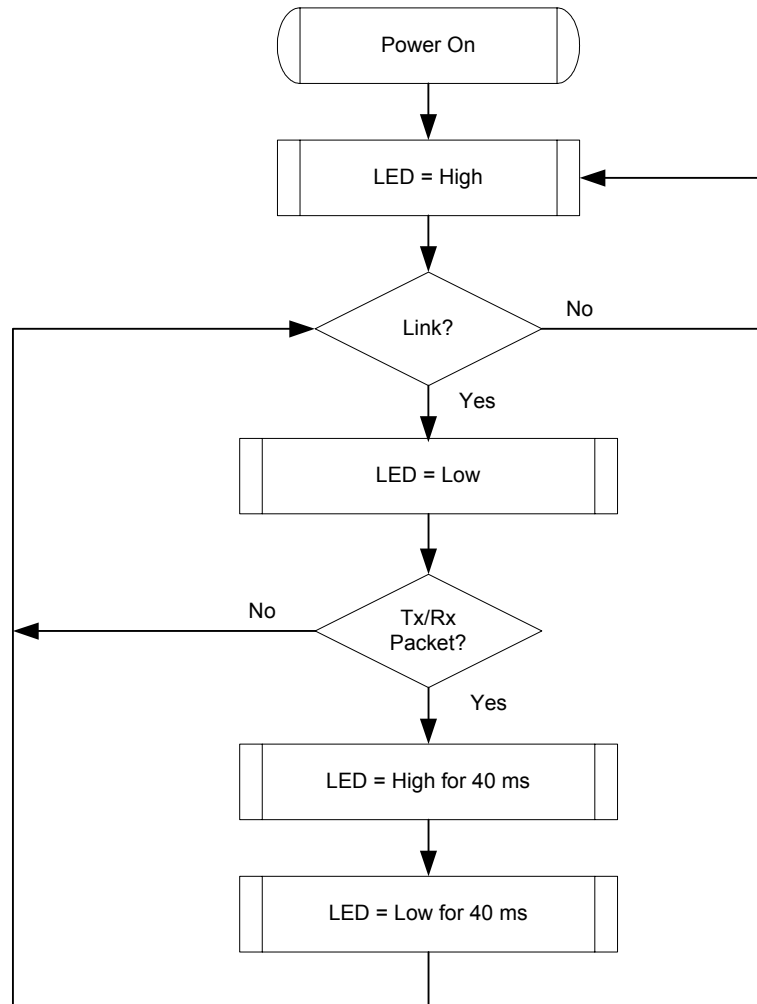
Figure 5.   LINK/ACT LED

6.3. *PHY Transceiver*

6.3.1. PHY Transmitter

Based on state-of-the-art DSP technology and mixed-mode signal processing technology, the RTL8111C-GR operates at 10/100/1000Mbps over standard CAT.5 UTP cable (100/1000Mbps), and CAT.3 UTP cable (10Mbps).

GMII (1000Mbps) Mode

The RTL8111C-GR's PCS layer receives data bytes from the MAC through the GMII interface and performs the generation of continuous code-groups through 4D-PAM5 coding technology. These code groups are passed through a waveform-shaping filter to minimize EMI effect, and are transmitted onto the 4-pair CAT5 cable at 125MBaud/s through a D/A converter.

MII (100Mbps) Mode

The transmitted 4-bit nibbles (TXD[3:0]) from the MAC, clocked at 25MHz (TXC), are converted into 5B symbol code through 4B/5B coding technology, then through scrambling and serializing, are converted to 125Mhz NRZ and NRZI signals. After that, the NRZI signals are passed to the MLT3 encoder, then to the D/A converter and transmitted onto the media.

MII (10Mbps) Mode

The transmitted 4-bit nibbles (TXD[3:0]) from the MAC, clocked at 2.5MHz (TXC), are serialized into 10Mbps serial data. The 10Mbps serial data is converted into a Manchester-encoded data stream and is transmitted onto the media by the D/A converter.

6.3.2. PHY Receiver

GMII (1000Mbps) Mode

Input signals from the media pass through the sophisticated on-chip hybrid circuit to separate the transmitted signal from the input signal for effective reduction of near-end echo. Afterwards, the received signal is processed with state-of-the-art technology, e.g., adaptive equalization, BLW (Baseline Wander) correction, cross-talk cancellation, echo cancellation, timing recovery, error correction, and 4D-PAM5 decoding. Then, the 8-bit-wide data is recovered and is sent to the GMII interface at a clock speed of 125MHz. The Rx MAC retrieves the packet data from the receive MII/GMII interface and sends it to the Rx Buffer Manager.

MII (100Mbps) Mode

The MLT3 signal is processed with an ADC, equalizer, BLW (Baseline Wander) correction, timing recovery, MLT3 and NRZI decoder, descrambler, 4B/5B decoder, and is then presented to the MII interface in 4-bit-wide nibbles at a clock speed of 25MHz.

MII (10Mbps) Mode

The received differential signal is converted into a Manchester-encoded stream first. Next, the stream is processed with a Manchester decoder and is de-serialized into 4-bit-wide nibbles. The 4-bit nibbles are presented to the MII interface at a clock speed of 2.5MHz.

6.4. Next Page

If 1000Base-T mode is advertised, three additional Next Pages are automatically exchanged between the two link partners. Users can set PHY Reg4.15 to 1 to manually exchange extra Next Pages via Reg7 and Reg8 as defined in IEEE 802.3ab.

6.5. EEPROM Interface

The RTL8111C-GR requires the attachment of an external EEPROM. The 93C46/93C56 is a 1K-bit/2K-bit EEPROM. The EEPROM interface permits the RTL8111C-GR to read from, and write data to, an external serial EEPROM device.

Values in the external EEPROM allow default fields in PCI configuration space and I/O space to be overridden following a power-on or software EEPROM auto-load command. The RTL8111C-GR will auto-load values from the EEPROM. If the EEPROM is not present, the RTL8111C-GR initialization uses default values for the appropriate Configuration and Operational Registers. Software can read and write to the EEPROM using bit-bang accesses via the 9346CR Register, or using PCI VPD (Vital Product Data). The interface consists of EESK, EECS, EEDO, and EEDI.

The correct EEPROM (i.e. 93C46/93C56) must be used in order to ensure proper LAN function.

Table 11.   EEPROM Interface

EEPROM	Description
EECS	93C46/93C56 chip select.
EESK	EEPROM serial data clock.
EEDI/Aux	Input data bus/Input pin to detect whether Aux. Power exists on initial power-on. This pin should be connected to EEPROM. To support wakeup from ACPI D3cold or APM power-down, this pin must be pulled high to Aux. Power via a resistor. If this pin is not pulled high to Aux. Power, the RTL8111C-GR assumes that no Aux. Power exists.
EEDO	Output data bus.

6.6. Power Management

The RTL8111C-GR is compliant with ACPI (Rev 1.0, 1.0b, 2.0), PCI Power Management (Rev 1.1), PCI Express Active State Power Management (ASPM), and Network Device Class Power Management Reference Specification (V1.0a), such as to support an Operating System-directed Power Management (OSPM) environment.

The RTL8111C-GR can monitor the network for a Wakeup Frame, a Magic Packet, and notify the system via a PCI Express Power Management Event (PME) Message, Beacon, or LANWAKEB pin when such a packet or event occurs. Then the system can be restored to a normal state to process incoming jobs.

When the RTL8111C-GR is in power down mode (D1 ~ D3):

- The Rx state machine is stopped. The RTL8111C-GR monitors the network for wakeup events such as a Magic Packet and Wakeup Frame in order to wake up the system. When in power down mode, the RTL8111C-GR will not reflect the status of any incoming packets in the ISR register and will not receive any packets into the Rx on-chip buffer.

- The on-chip buffer status and packets that have already been received into the Rx on-chip buffer before entering power down mode are held by the RTL8111C-GR.

- Transmission is stopped. PCI Express transactions are stopped. The Tx on-chip buffer is held.

- After being restored to D0 state, the RTL8111C-GR transmits data that was not moved into the Tx on-chip buffer during power down mode. Packets that were not transmitted completely last time are re-transmitted.

The D3cold_support_PME bit (bit15, PMC register) and the Aux_I_b2:0 bits (bit8:6, PMC register) in PCI configuration space depend on the existence of Aux power. If aux. power is absent, the above 4 bits are all 0 in binary.

Example:

If EEPROM D3c_support_PME = 1:

- If aux. power exists, then PMC in PCI config space is the same as EEPROM PMC
  (if EEPROM PMC = C3 F7, then PCI PMC = C3 F7)

- If aux. power is absent, then PMC in PCI config space is the same as EEPROM PMC except the above 4 bits are all 0's (if EEPROM PMC = C3 F7, then PCI PMC = 03 76)

In the above case, if wakeup support is desired when main power is off, it is suggested that the EEPROM PMC be set to C3 F7 (Realtek EEPROM default value).

If EEPROM D3c_support_PME = 0:

- If aux. power exists, then PMC in PCI config space is the same as EEPROM PMC
  (if EEPROM PMC = C3 77, then PCI PMC = C3 77)

- If aux. power is absent, then PMC in PCI config space is the same as EEPROM PMC except the above 4 bits are all 0's (if EEPROM PMC = C3 77, then PCI PMC = 03 76)

In the above case, if wakeup support is not desired when main power is off, it is suggested that the EEPROM PMC be set to 03 76.

Magic Packet Wakeup occurs only when the following conditions are met:

- The destination address of the received Magic Packet is acceptable to the RTL8111C-GR, e.g., a broadcast, multicast, or unicast packet addressed to the current RTL8111C-GR adapter.
- The received Magic Packet does not contain a CRC error.
- The Magic bit (CONFIG3#5) is set to 1, the PMEn bit (CONFIG1#0) is set to 1, and the corresponding wake-up method (message, beacon, or LANWAKEB) can be asserted in the current power state.
- The Magic Packet pattern matches, i.e. 6 * FFh + MISC (can be none) + 16 * DID (Destination ID) in any part of a valid Ethernet packet.

A Wakeup Frame event occurs only when the following conditions are met:

- The destination address of the received Wakeup Frame is acceptable to the RTL8111C-GR, e.g., a broadcast, multicast, or unicast address to the current RTL8111C-GR adapter.
- The received Wakeup Frame does not contain a CRC error.
- The PMEn bit (CONFIG1#0) is set to 1.
- The 16-bit CRC[A] of the received Wakeup Frame matches the 16-bit CRC of the sample Wakeup Frame pattern given by the local machine's OS. Or, the RTL8111C-GR is configured to allow direct packet wakeup, e.g., a broadcast, multicast, or unicast network packet.

Note: 16-bit CRC: The RTL8111C-GR supports eight long wakeup frames (covering 128 mask bytes from offset 0 to 127 of any incoming network packet).

The corresponding wake-up method (message, beacon, or LANWAKEB) is asserted only when the following conditions are met:

- The PMEn bit (bit0, CONFIG1) is set to 1.
- The PME_En bit (bit8, PMCSR) in PCI Configuration Space is set to 1.
- The RTL8111C-GR may assert the corresponding wake-up method (message, beacon, or LANWAKEB) in the current power state or in isolation state, depending on the PME_Support (bit15-11) setting of the PMC register in PCI Configuration Space.
- A Magic Packet, LinkUp, or Wakeup Frame has been received.
- Writing a 1 to the PME_Status (bit15) of the PMCSR register in the PCI Configuration Space clears this bit and causes the RTL8111C-GR to stop asserting the corresponding wake-up method (message, beacon, or LANWAKEB) (if enabled).

When the RTL8111C-GR is in power down mode, e.g., D1-D3, the IO and MEM accesses to the RTL8111C-GR are disabled. After a PERSTB assertion, the device's power state is restored to D0 automatically if the original power state was $D3_{cold}$. There is almost no hardware delay at the device's power state transition. When in ACPI mode, the device does not support PME (Power Management Enable) from D0 (this is the Realtek default setting of the PMC register auto-loaded from EEPROM). The setting may be changed from the EEPROM, if required.

6.7. *Vital Product Data (VPD)*

Bit 31 of the Vital Product Data (VPD) capability structure in the RTL8111C-GR's PCI Configuration Space is used to issue VPD read/write commands and is also a flag used to indicate whether the transfer of data between the VPD data register and the 93C46/93C56/93C66 has completed or not.

Write VPD register: (write data to the 93C46/93C56/93C66)
Set the flag bit to 1 at the same time the VPD address is written to write VPD data to EEPROM. When the flag bit is reset to 0 by the RTL8111C-GR, the VPD data (4 bytes per VPD access) has been transferred from the VPD data register to EEPROM.

Read VPD register: (read data from the 93C46/93C56/93C66)
Reset the flag bit to 0 at the same time the VPD address is written to retrieve VPD data from EEPROM. When the flag bit is set to 1 by the RTL8111C-GR, the VPD data (4 bytes per VPD access) has been transferred from EEPROM to the VPD data register.

Note1: Refer to the PCI 2.3 Specifications for further information.
Note2: The VPD address must be a DWORD-aligned address as defined in the PCI 2.3 Specifications.
VPD data is always consecutive 4-byte data starting from the VPD address specified.
Note3: Realtek reserves offset 60h to 7Fh in EEPROM mainly for VPD data to be stored.
Note4: The VPD function of the RTL8111C-GR is designed to be able to access the full range of the 93C46/93C56/93C66 EEPROM.

6.8. Message Signaled Interrupt (MSI)

6.8.1. MSI Capability Structure in PCI Configuration Space

Capability Structure for 32-bit Message Address

			Address
Message Control	Next Pointer	Capability ID	Capability Pointer
Message Address			Capability Pointer + 04h
Message Data			Capability Pointer + 08h

Bit positions: 31, 16, 15, 8, 7, 0
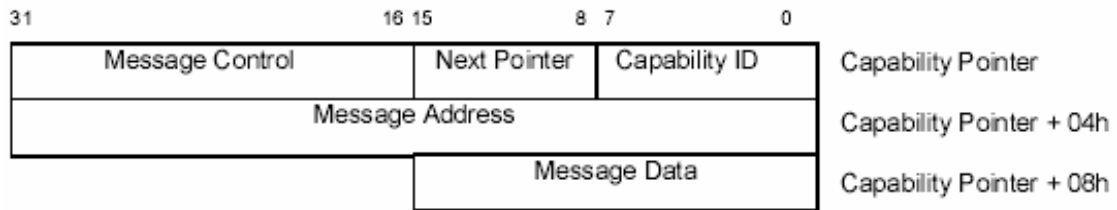
Capability Structure for 64-bit Message Address

			Address
Message Control	Next Pointer	Capability ID	Capability Pointer
Message Address			Capability Pointer + 04h
Message Upper Address			Capability Pointer + 08h
Message Data			Capability Pointer + 0Ch

Bit positions: 31, 16, 15, 8, 7, 0
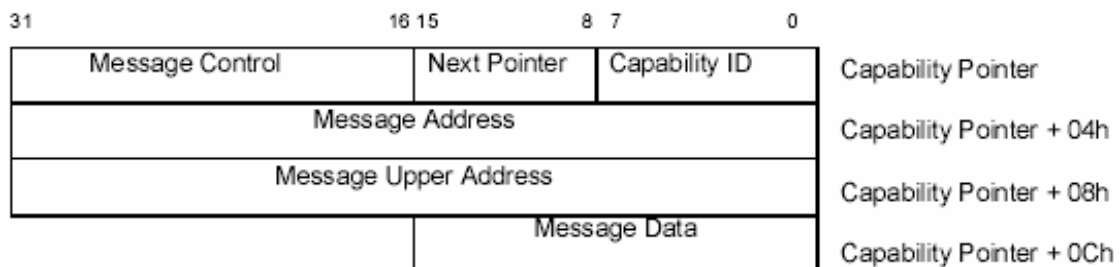
Figure 6. Message Capability Structure

6.8.2. Message Control

Table 12.   Message Control

Bits	RW	Field	Description
15:8	RO	Reserved	Reserved. Always return 0
7	RO	64-bit address capable	1: The RTL8111C is capable of generating a 64-bit message address. 0: The RTL8111C is NOT capable of generating a 64-bit message address. This bit is read only and the RTL8111C is set to 1.
6:4	RW	Multiple Message Enable	System software (e.g., BIOS, OS) indicates to the RTL8111C-GR the number of allocated messages/vectors (equal to or less than the number of requested messages/vectors). This field after PCI reset is '000'. Encoding / Number of Messages/Vectors table below
3:1	RO	Multiple Message Capable	Indication to system software (e.g., BIOS, OS) of the number of RTL8111C-GR requested vectors. The RTL8111C-GR supports only one vector messages/vectors.
0	RW	MSI Enable	1: Enable MSI (Also the INTx pin is disabled automatically, MSI and INTx are mutually exclusive), this bit is set by system software. 0: Disable MSI (Default value after power-on or PCI reset)

Multiple Message Enable encoding table:

Encoding	Number of Messages/Vectors
000	1
001	2
010	4
011	8
100	16
101	32
110	Reserved
111	Reserved

Multiple Message Capable encoding table:

Encoding	Number of Messages/Vectors
000	1
Others	Reserved

6.8.3. Message Address

Table 13.   Message Address

Bits	RW	Field	Description
31:02	RW	Message Address	System-specified message/vector address. Low DWORD aligned address for MSI memory write transaction.
01:00	RO	Reserved	Always return '00'. This bit is read only.

6.8.4. Message Upper Address

<p align="center">**Table 14. Message Upper Address**</p>

Bits	RW	Field	Description
31:00	RW	Message Upper Address	System-specified message/vector upper address. Upper 32 bits of a 64-bit message/vector address. This register is effective only when the DAC function is enabled, i.e., 64-bit addressing is enabled; bit7 in Message Control register is set. If the contents of this register are 0, the RTL8111C-GR only performs 32-bit addressing for the memory write of the messages/vectors. This bit is read/write.

6.8.5. Message Data

<p align="center">**Table 15. Message Data**</p>

Bits	RW	Field	Description
15:00	RW	Message Data	If the Message Enable bit is set, the message/vector data is driven onto the lower word of the memory write transaction's data phase. This bit is read/write.

6.9.   MSI-X

6.9.1.   MSI-X Capability Structure in PCI Configuration Space

31	16	15	8	7	3	2	0	
Message Control		Next Pointer		Capability ID				CP + 00h
Table Offset						Table BIR		CP + 04h
PBA Offset						PBA BIR		CP + 08h
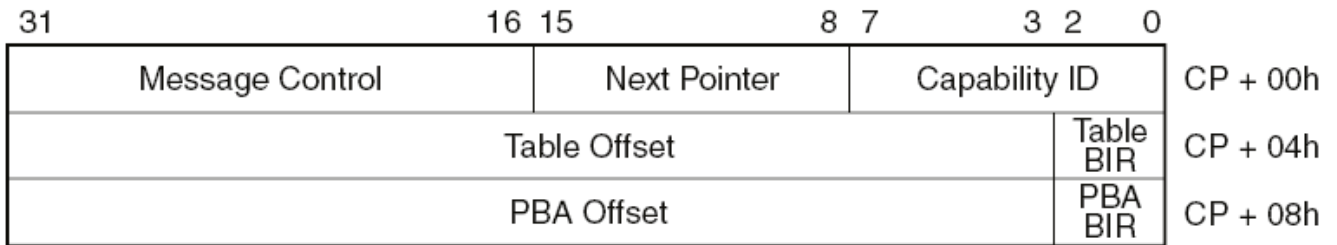
Figure 7.   MSI-X Capability Structure

DWORD 3	DWORD 2	DWORD 1	DWORD 0		
Vector Control	Msg Data	Msg Upper Addr	Msg Addr	entry 0	Base
Vector Control	Msg Data	Msg Upper Addr	Msg Addr	entry 1	Base + 1*16
Vector Control	Msg Data	Msg Upper Addr	Msg Addr	entry 2	Base + 2*16
•••	•••	•••	•••	•••	•••
Vector Control	Msg Data	Msg Upper Addr	Msg Addr	entry (N-1)	Base + (N-1)*16
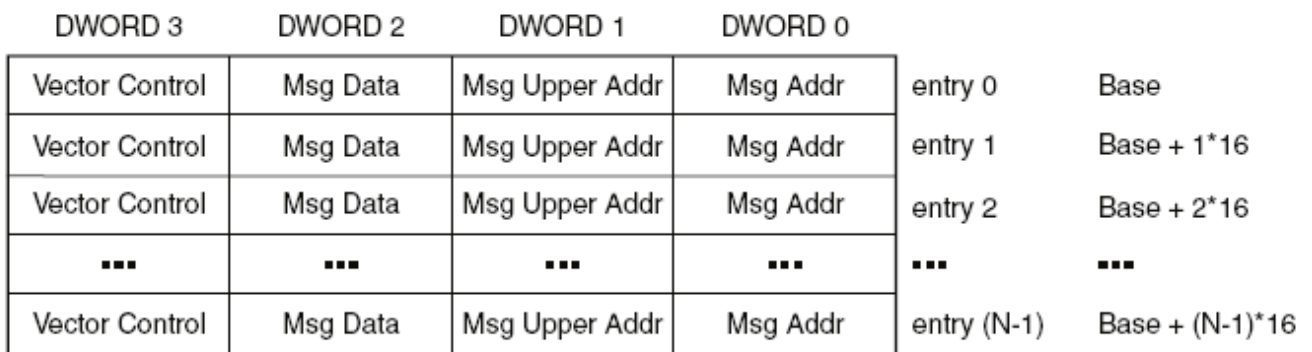
Figure 8.   MSI-X Table Structure

63	0		
Pending Bits 0 through 63		QWORD 0	Base
Pending Bits 64 through 127		QWORD 1	Base + 1*8
•••		•••	•••
Pending Bits ((N-1) div 64)*64 through N-1		QWORD ((N-1) div 64)	Base + ((N-1) div 64)*8
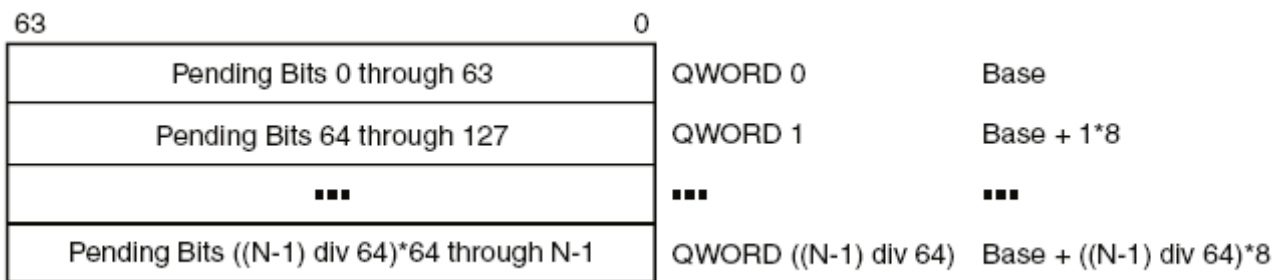
Figure 9.   MSI-X PBA Structure

6.9.2. Message Control

Table 16.　Message Control

Bits	RW	Field	Description
15	RW	MSI-X Enable	If 1 and the MSI Enable bit in the MSI Message Control register is 0, the function is permitted to use MSI-X to request service and is prohibited from using its INTx# pin. System configuration software sets this bit to enable MSI-X. A device driver is prohibited from writing this bit to mask a function's service request. If 0, the function is prohibited from using MSI-X to request service. This bit's state after reset is 0 (MSI-X is disabled). This bit is read/write.
14	RW	Function Mask	If 1, all of the vectors associated with the function are masked, regardless of their per-vector Mask bit states. If 0, each vector's Mask bit determines whether the vector is masked or not. Setting or clearing the MSI-X Function Mask bit has no effect on the state of the per-vector Mask bits. This bit's state after reset is 0 (unmasked). This bit is read/write.
13:11	RO	Reserved	Always returns 0 on a read. A write operation has no effect.
10:00	RO	Table Size	System software reads this field to determine the MSI-X Table Size N, which is encoded as N-1. The RTL8111C-GR value is '00000000001', indicating a table size of 2.

6.9.3. Table Offset/BIR

Table 17.　Table Offset/BIR

Bits	RW	Field	Description
31:03	RW	Table Offset	Used as an offset from the address contained by one of the function's Base Address registers to point to the base of the MSI-X Table. The lower 3 BIR bits are masked off (set to zero) by software to form a 32bit QWORD-aligned offset. This field is read only.

Bits	RW	Field	Description
02:00	RO	BIR	Indicates which one of a function's Base Address registers, located beginning at 10h in Configuration Space, is used to map the function's MSI-X Table into Memory Space.
			<table><tr><td>**BIR Value**</td><td>**Base Address register**</td></tr><tr><td>0</td><td>10h</td></tr><tr><td>1</td><td>14h</td></tr><tr><td>2</td><td>18h</td></tr><tr><td>3</td><td>1Ch</td></tr><tr><td>4</td><td>20h</td></tr><tr><td>5</td><td>24h</td></tr><tr><td>6</td><td>Reserved</td></tr><tr><td>7</td><td>Reserved</td></tr></table> For a 64-bit Base Address register, the BIR indicates the lower DWORD. With PCI-to-PCI bridges, BIR values 2 through 5 are also reserved. The function's Base Address registers of RTL8111C-GR located beginning at 20h. This field is read only.

6.9.4. PBA Offset/PBA BIR

Table 18. PBA Offset/PBA BIR

Bits	RW	Field	Description
31:03	RO	PBA Offset	Used as an offset from the address contained by one of the function's Base Address registers to point to the base of the MSI-X PBA. The lower 3 PBA BIR bits are masked off (set to zero) by software to form a 32-bit QWORD-aligned offset. This field is read only.
02:00	RO	PBA BIR	Indicates which one of a function's Base Address registers, located beginning at 10h in Configuration Space, is used to map the function's MSI-X PBA into Memory Space. The PBA BIR value definitions are identical to those for the MSI-X Table BIR. This field is read only.

6.9.5. Message Address for MSI-X Table Entries

Table 19. Message Address for MSI-X Table Entries

Bits	RW	Field	Description
31:02	RW	Message Address	System-specified message lower address. For MSI-X messages, the contents of this field from an MSI-X Table entry specifies the lower portion of the DWORD aligned address for the memory write transaction. This field is read/write.
01:00	RW	Message Address	For proper DWORD alignment, software must always write zeroes to these two bits; otherwise the result is undefined. The state of these bits after reset must be 0. These bits are permitted to be read only or read/write.

6.9.6.   Message Upper Address for MSI-X Table Entries

Table 20.   Message Upper Address for MSI-X Table Entries

Bits	RW	Field	Description
31:00	RW	Message Upper Address	System-specified message upper address bits. This field is read/write.

6.9.7.   Message Data for MSI-X Table Entries

Table 21.   Message Data

Bits	RW	Field	Description
31:00	RW	Message Data	System-specified message data. For MSI-X messages, the contents of this field are taken from an MSI-X Table entry. In contrast to message data used for MSI messages, the low-order message data bits in MSI-X messages are not modified by the function. This field is read/write.

6.9.8.   Vector Control for MSI-X Table Entries

Table 22.   Vector Control for MSI-X Table Entries

Bits	RW	Field	Description
31:01	RW	Reserved	After reset, the state of these bits must be 0. However, for potential future use, software must preserve the value of these reserved bits when modifying the value of other Vector Control bits. If software modifies the value of these reserved bits, the result is undefined.
00	RW	Mask Bit	When this bit is set, the function is prohibited from sending a message using this MSI-X Table entry. However, any other MSI-X Table entries programmed with the same vector will still be capable of sending an equivalent message unless they are also masked. This bit's state after reset is 1 (entry is masked). This bit is read/write.

6.9.9.   Pending Bits for MSI-X PBA Entries

Table 23.   Pending Bits for MSI-X PBA Entries

Bits	RW	Field	Description
63:00	RW	Pending Bits	For each Pending Bit that is set, the function has a pending message for the associated MSI-X Table entry. Pending bits that have no associated MSI-X Table entry are reserved. After reset, the state of reserved Pending bits must be 0. Software should never write, and should only read Pending Bits. If software writes to Pending Bits, the result is undefined. Each Pending Bit's state after reset is 0 (no message pending). These bits are permitted to be read only or read/write.

6.10. *Receive-Side Scaling (RSS)*

The RTL8111C-GR is compliant with the new Network Driver Interface Specification (NDIS) 6.0 Receive-Side Scaling (RSS) technology for the Microsoft Windows family of operating systems. RSS allows packet receive-processing from a network adapter to be balanced across the number of available computer processors, increasing perfromance on multi CPU platforms.

6.10.1. Receive-Side Scaling (RSS) Initialization

During RSS initialization, the Windows operating system will inform the RTL8111C-GR to store the following parameters: hash function, hash type, hash bits, indirection table, BaseCPUNumber, and the secret hash key.

Hash Function

The default hash function is the Toeplitz hash function.

Hash Type

The hash types indicate which field of the packet needs to be hashed to get the hash result. There are several combinations of these fields, mainly, TCP/IPv4, IPv4, TCP/IPv6, IPv6, and IPv6 extension headers.

- TCP/IPv4 requires hash calculations over the IPv4 source address, the IPv4 destination address, the source TCP port and the destination TCP port.
- IPv4 requires hash calculations over the IPv4 source address and the IPv4 destination address.
- TCP/IPv6 requires hash calculations over the IPv6 source address, the IPv6 destination address, the source TCP port and the destination TCP port.
- IPv6 requires hash calculations over the IPv6 source address and the IPv6 destination address (*Note: The RTL8111C-GR does not support the IPv6 extension header hash type in RSS*).

Hash Bits

Hash bits are used to index the hash result into the indirection table

Indirection Table

The Indirection Table stores values that are added to the BaseCPUNumber to enable RSS interrupts to be restricted from some CPUs. The OS will update the Indirection Table to rebalance the load.

BaseCPUNumber

The lowest number CPU to use for RSS. BaseCPUNumber is added to the result of the indirection table lookup.

Secret hash key

The key used in the Toeplitz function. For different hash types, the key size is different.

6.10.2. RSS Operation

After the parameters are set, the RTL8111C-GR will start hash calculation on each incoming packet and forward each packet to its correct queue according to the hash result. If the incoming packet is not in the hash type, it will be forwarded to the primary queue. The hash result plus the BaseCPUNumber will be indexed into the indirection table to get the correct CPU number. The RTL8111C-GR uses three methods to inform the system of incoming packets: inline interrupt, MSI, and MSIX. Periodically the OS will update the indirection table to rebalance the load across the CPUs.

7. Characteristics

7.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table 24.   Absolute Maximum Ratings

Symbol	Description	Minimum	Maximum	Unit
VDD33, AVDD33	Supply Voltage 3.3V	-0.3	+0.5	V
AVDD12, DVDD12	Supply Voltage 1.2V	-0.3	+0.4	V
EVDD12	Supply Voltage 1.2V	TBD	TBD	-
DCinput	Input Voltage	-0.3	Corresponding Supply Voltage + 0.5	V
DCoutput	Output Voltage	-0.3	Corresponding Supply Voltage + 0.5	V
	Storage Temperature	-55	+125	°C

* Refer to the most updated schematic circuit for correct configuration.

7.2. Recommended Operating Conditions

Table 25.   Recommended Operating Conditions

Description	Pins	Minimum	Typical	Maximum	Unit
Supply Voltage VDD	VDD33, AVDD33	2.97	3.3	3.63	V
	AVDD12, DVDD12	1.1	1.2	1.32	V
	EVDD12	1.14	1.2	1.26	V
Ambient Operating Temperature T_A	-	0	-	70	°C
Maximum Junction Temperature	-	-	-	125	°C

* Refer to the most updated schematic circuit for correct configuration.

7.3. Crystal Requirements

Table 26.   Crystal Requirements

Symbol	Description/Condition	Minimum	Typical	Maximum	Unit
F_{ref}	Parallel resonant crystal reference frequency, fundamental mode, AT-cut type.	-	25	-	MHz
F_{ref} Stability	Parallel resonant crystal frequency stability, fundamental mode, AT-cut type. T_a=25°C.	-50	-	+50	ppm
F_{ref} Tolerance	Parallel resonant crystal frequency tolerance, fundamental mode, AT-cut type. T_a=-20°C ~+70°C.	-30	-	+30	ppm
F_{ref} Duty Cycle	Reference clock input duty cycle.	40	-	60	%
C_L	Load Capacitance.	-	TBD	-	pF
ESR	Equivalent Series Resistance.	-	TBD	-	Ω
DL	Drive Level.	-	TBD	0.5	mW

7.4. *Thermal Characteristics*

Table 27.   Thermal Characteristics

Parameter	Minimum	Maximum	Units
Storage Temperature	-55	+125	°C
Ambient Operating Temperature	0	70	°C

7.5. *DC Characteristics*

Table 28.   DC Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
VDD33, AVDD33	3.3V Supply Voltage	-	2.97	3.3	3.63	V
EVDD12, AVDD12	1.2V Supply Voltage	-	1.1	1.2	1.32	V
DVDD12	1.2V Supply Voltage	-	1.1	1.2	1.32	V
Voh	Minimum High Level Output Voltage	I_{oh} = -4mA	0.9 * VDD33	-	VDD33	V
Vol	Maximum Low Level Output Voltage	I_{ol}= 4mA	0	-	0.1 * VDD33	V
Vih	Minimum High Level Input Voltage	-	1.8	-	-	V
Vil	Maximum Low Level Input Voltage	-	-	-	0.8	V
Iin	Input Current	V_{in} = VDD33 or GND	0	-	0.5	µA
Icc33	Average Operating Supply Current from 3.3V	At 1Gbps with heavy network traffic	-	TBD	-	mA
Icc12	Average Operating Supply Current from 1.8V	At 1Gbps with heavy network traffic	-	TBD	-	mA

* Refer to the most updated schematic circuit for correct configuration.

7.6. AC Characteristics

7.6.1. Serial EEPROM Interface Timing

93C46(64*16)/93C56(128*16)
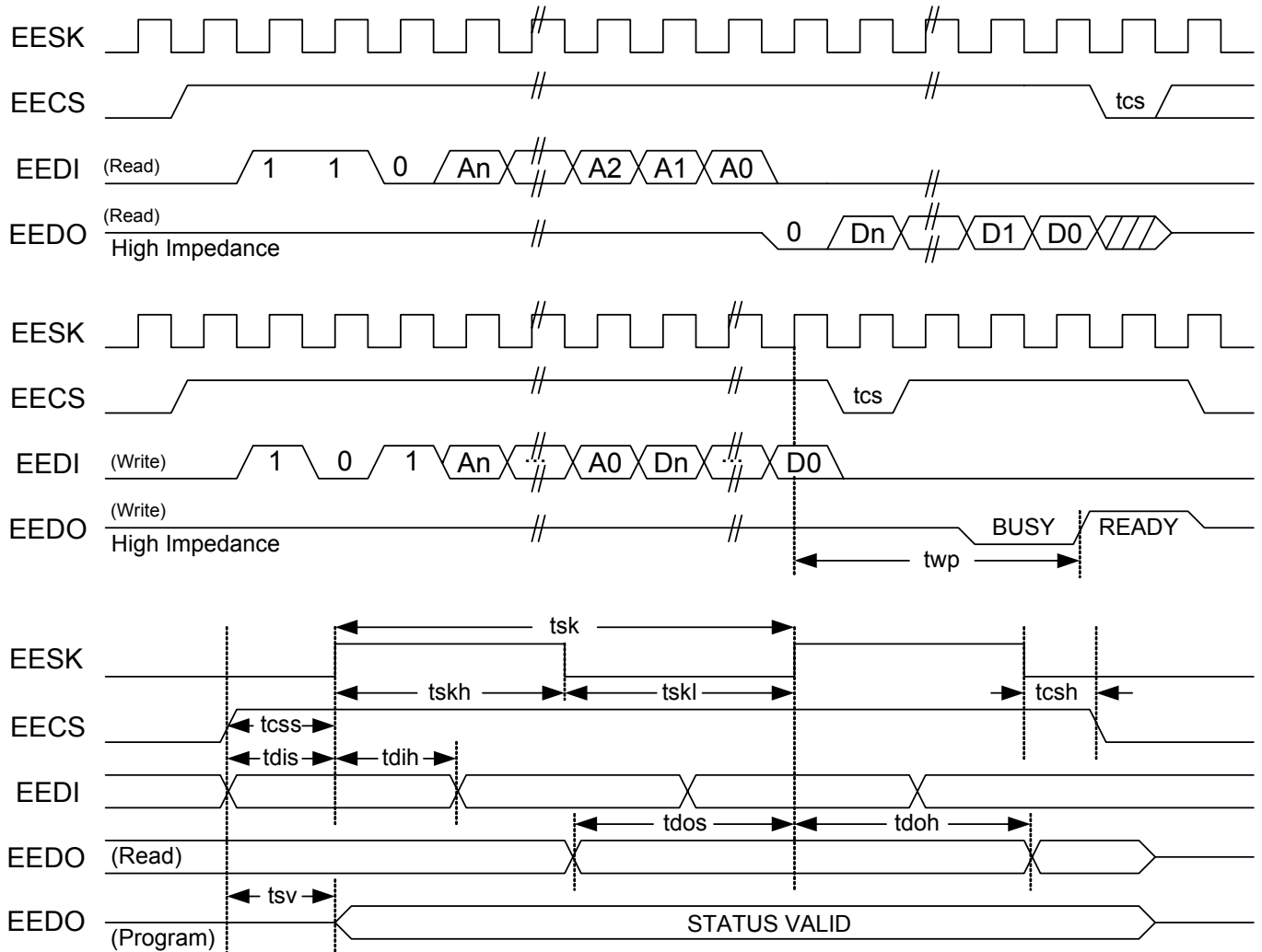
Figure 10. Serial EEPROM Interface Timing

Table 29.   EEPROM Access Timing Parameters

Symbol	Parameter	EEPROM Type	Min.	Max.	Unit
tcs	Minimum CS Low Time	9346	1000	-	ns
twp	Write Cycle Time	9346	-	10	ms
tsk	SK Clock Cycle Time	9346	4	-	μs
tskh	SK High Time	9346	1000	-	ns
tskl	SK Low Time	9346	1000	-	ns
tcss	CS Setup Time	9346	200	-	ns
tcsh	CS Hold Time	9346	0	-	ns
tdis	DI Setup Time	9346	400	-	ns
tdih	DI Hold Time	9346	400	-	ns
tdos	DO Setup Time	9346	2000	-	ns
tdoh	DO Hold Time	9346	-	2000	ns
tsv	CS to Status Valid	9346	-	1000	ns

7.7. PCI Express Bus Parameters

7.7.1. Differential Transmitter Parameters

Table 30. Differential Transmitter Parameters

Symbol	Parameter	Min	Typical	Max	Units
UI	Unit Interval[2]	399.88	400	400.12	ps
$V_{TX-DIFFp-p}$	Differential Peak to Peak Output Voltage	0.800	-	1.2	V
$V_{TX-DE-RATIO}$	De-Emphasized Differential Output Voltage (Ratio)	-3.0	-3.5	-4.0	dB
T_{TX-EYE}	Minimum Tx Eye Width	0.75	-	-	UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median	-	-	0.125	UI
$T_{TX-RISE}$, $T_{TX-FALL}$	D+/D- Tx Output Rise/Fall Time	0.125	-	-	UI
$V_{TX-CM-ACp}$	RMS AC Peak Common Mode Output Voltage	-	-	20	mV
$V_{TX-CM-DCACTIVE-IDLEDELTA}$	Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle	0	-	100	mV
$V_{TX-CM-DCLINE-DELTA}$	Absolute Delta of DC Common Mode Voltage between D+ and D-	0	-	25	mV
$V_{TX-IDLE-DIFFp}$	Electrical Idle Differential Peak Output Voltage	0	-	20	mV
$V_{TX-RCV-DETECT}$	The amount of voltage change allowed during Receiver Detection	-	-	600	mV
$V_{TX-DC-CM}$	The TX DC Common Mode Voltage	0	-	3.6	V
$I_{TX-SHORT}$	TX Short Circuit Current Limit	-	-	90	mA
$T_{TX-IDLE-MIN}$	Minimum time spent in Electrical Idle	50	-	-	UI
$T_{TX-IDLE-SETTO-IDLE}$	Maximum time to transition to a valid Electrical Idle after sending an Electrical Idle ordered set	-	-	20	UI
$T_{TX-IDLE-TOTO-DIFF-DATA}$	Maximum time to transition to valid TX specifications after leaving an Electrical Idle condition	-	-	20	UI
$RL_{TX-DIFF}$	Differential Return Loss	10	-	-	dB
RL_{TX-CM}	Common Mode Return Loss	6	-	-	dB
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance	80	100	120	Ω
$L_{TX-SKEW}$	Lane-to-Lane Output Skew	-	-	500+2 UI	ps
C_{TX}	AC Coupling Capacitor	75	-	200	nF
$T_{crosslink}$	Crosslink Random Timeout	0	-	1	ms

Note1: Refer to PCI Express Base Specification, rev.1.1, for correct measurement environment setting of each parameter.

Note2: The data rate can be modulated with an SSC (Spread Spectrum Clock) from +0 to -0.5% of the nominal data rate frequency, at a modulation rate in the range not exceeding 30 kHz – 33 kHz. The +/- 300 ppm requirement still holds, which requires the two communicating ports be modulated such that they never exceed a total of 600 ppm difference.

7.7.2. Differential Receiver Parameters

Table 31.   Differential Receiver Parameters

Symbol	Parameter	Min.	Typical	Max.	Units
UI	Unit Interval	399.88	400	400.12	ps
$V_{RX-DIFFp-p}$	Differential Input Peak to Peak Voltage	0.175	-	1.200	V
T_{RX-EYE}	Minimum Receiver Eye Width	0.4	-	-	UI
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median	-	-	0.3	UI
$V_{RX-CM-ACp}$	AC Peak Common Mode Input Voltage	-	-	150	mV
$RL_{RX-DIFF}$	Differential Return Loss	10	-	-	dB
RL_{RX-CM}	Common Mode Return Loss	6	-	-	dB
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance	80	100	120	Ω
Z_{RX--DC}	DC Input Impedance	40	50	60	Ω
$Z_{RX-HIGH-IMP-DC}$	Powered Down DC Input Impedance	200 k	-	-	Ω
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical Idle Detect Threshold	65	-	175	mV
$T_{RX-IDLE-DET-DIFFENTERTIME}$	Unexpected Electrical Idle Enter Detect Threshold Integration Time	-	-	10	ms
$L_{RX-SKEW}$	Total Skew	-	-	20	ns

Note: Refer to PCI Express Base Specification, rev.1.1, for correct measurement environment setting of each parameter.

7.7.3. REFCLK Parameters

Table 32.   REFCLK Parameters

Symbol	Parameter	100MHz Input		Units	Note
		Min	Max		
Rise Edge Rate	Rising Edge Rate	0.6	4.0	V/ns	2,3
Fall Edge Rate	Falling Edge Rate	0.6	4.0	V/ns	2,3
V_{IH}	Differential Input High Voltage	+150	-	mV	2
V_{IL}	Differential Input Low Voltage	-	-150	mV	2
V_{CROSS}	Absolute crossing point voltage	+250	+550	mV	1,4,5
$V_{CROSS\ DELTA}$	Variation of V_{CROSS} over all rising clock edges	-	+140	mV	1,4,9
V_{RB}	Ring-back Voltage Margin	-100	+100	mV	2,12
T_{STABLE}	Time before V_{RB} is allowed	500	-	ps	2,12
$T_{PERIOD\ AVG}$	Average Clock Period Accuracy	-300	+2800	ppm	2,10,13
$T_{PERIOD\ ABS}$	Absolute Period (including Jitter and Spread Spectrum)	9.847	10.203	ns	2,6
$T_{CCJITTER}$	Cycle to Cycle jitter	-	150	ps	2
V_{MAX}	Absolute Max input voltage	-	+1.15	V	1,7
V_{MIN}	Absolute Min input voltage	-	-0.3	V	1,8

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Symbol	Parameter	100MHz Input		Units	Note
		Min	Max		
Duty Cycle	Duty Cycle	40	60	%	2
Rise-Fall Matching	Rising edge rate (REFCLK+) to falling edge rate (REFCLK-) matching	-	20	%	1,14
$Z_{C\text{-}DC}$	Clock source DC impedance	40	60	Ω	1,11

Note1: Measurement taken from single ended waveform.

Note2: Measurement taken from differential waveform.

Note3: Measured from -150 mV to +150 mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing. See Figure 14, page 34.

Note4: Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-. See Figure 10, page 28.

Note5: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Figure 10, page 28.

Note6: Defines as the absolute minimum or maximum instantaneous period. This includes cycle to cycle jitter, relative PPM tolerance, and spread spectrum modulation. See Figure 13, page 33.

Note7: Defined as the maximum instantaneous voltage including overshoot. See Figure 10, page 28.

Note8: Defined as the minimum instantaneous voltage including undershoot. See Figure 10, page 28.

Note9: Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in VCROSS for any particular system. See Figure 11, page 33.

Note10: Refer to Section 4.3.2.1 of the PCI Express Base Specification, Revision 1.1 for information regarding PPM considerations.

Note11: System board compliance measurements must use the test load card described in Figure16. REFCLK+ and REFCLK- are to be measured at the load capacitors CL. Single ended probes must be used for measurements requiring single ended measurements. Either single ended probes with math or differential probe can be used for differential measurements. Test load C_L = 2 pF.

Note12: T_{STABLE} is the time the differential clock must maintain a minimum ±150 mV differential voltage after rising/falling edges before it is allowed to droop back into the V_{RB} ±100 mV differential range. See Figure 15.

Note13: PPM refers to parts per million and is a DC absolute period accuracy specification. 1 PPM is 1/1,000,000th of 100.000000 MHz exactly or 100 Hz. For 300 PPM then we have a error budget of 100 Hz/PPM * 300 PPM = 30 kHz. The period is to be measured with a frequency counter with measurement window set to 100 ms or greater. The ±300 PPM applies to systems that do not employ Spread Spectrum or that use common clock source. For systems employing Spread Spectrum there is an additional 2500 PPM nominal shift in maximum period resulting from the 0.5% down spread resulting in a maximum average period specification of +2800 PPM

Note14: Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75 mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 12, page 33.

Note15: Refer to PCI Express Card Electromechanical Specification, rev.1.1, for correct measurement environment setting of each parameter.
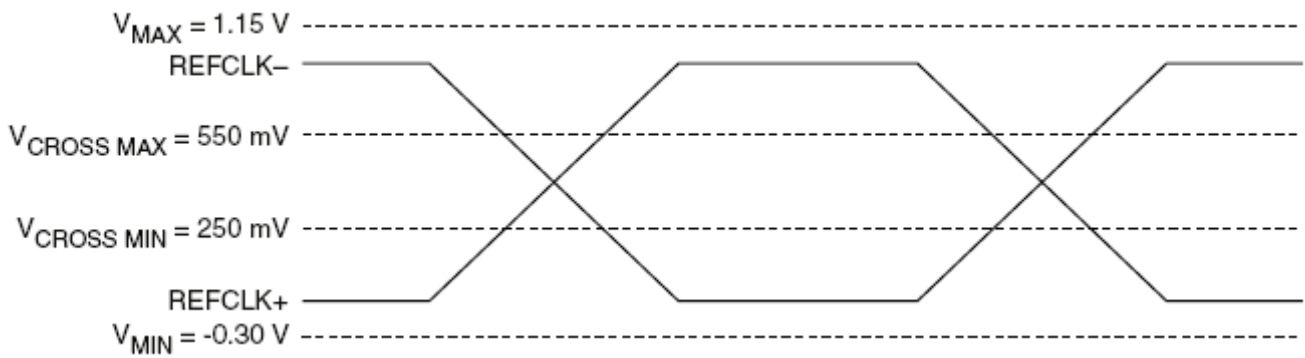
Figure 11.   Single-Ended Measurement Points for Absolute Cross Point and Swing
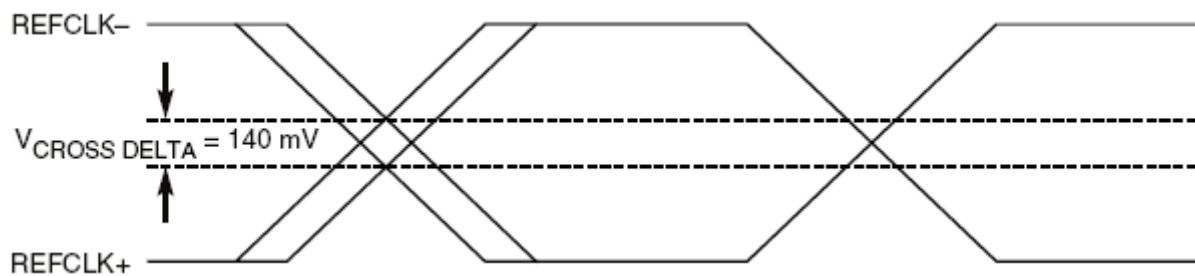
Figure 12.   Single-Ended Measurement Points for Delta Cross Point
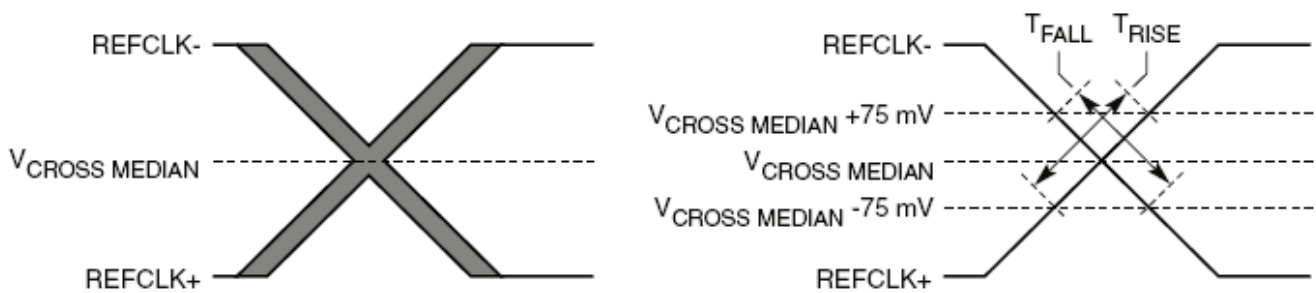
Figure 13.   Single-Ended Measurement Points for Rise and Fall Time Matching

Figure 14.   Differential Measurement Points for Duty Cycle and Period
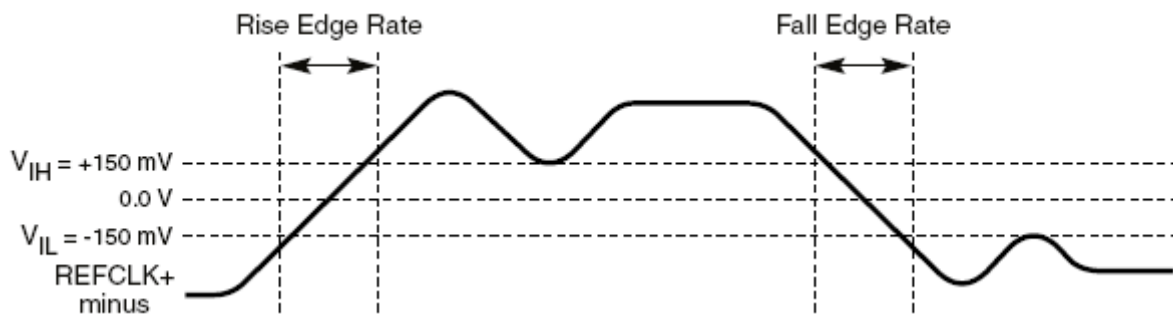
Figure 15.   Differential Measurement Points for Rise and Fall Time
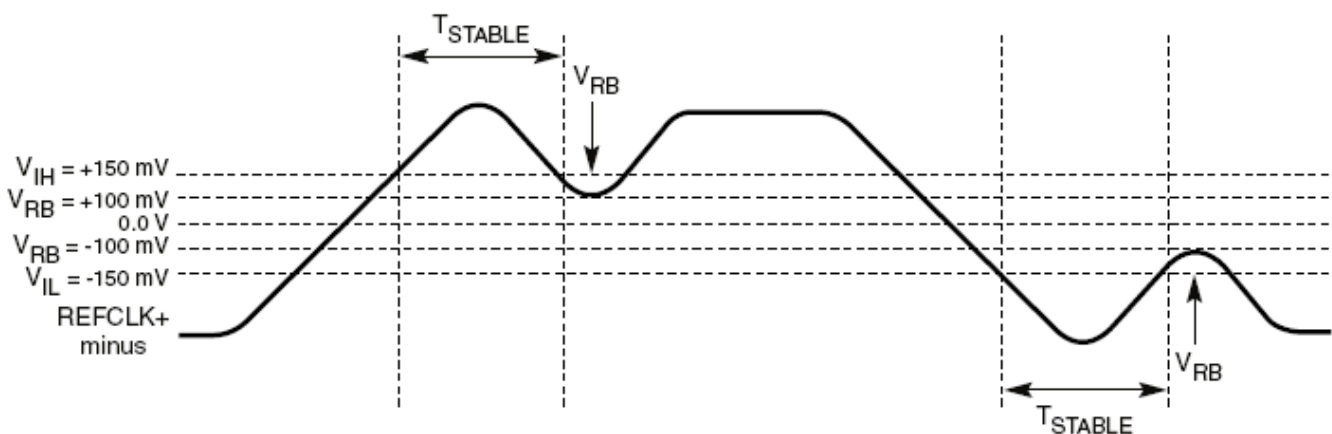
Figure 16.   Differential Measurement Points for Ringback
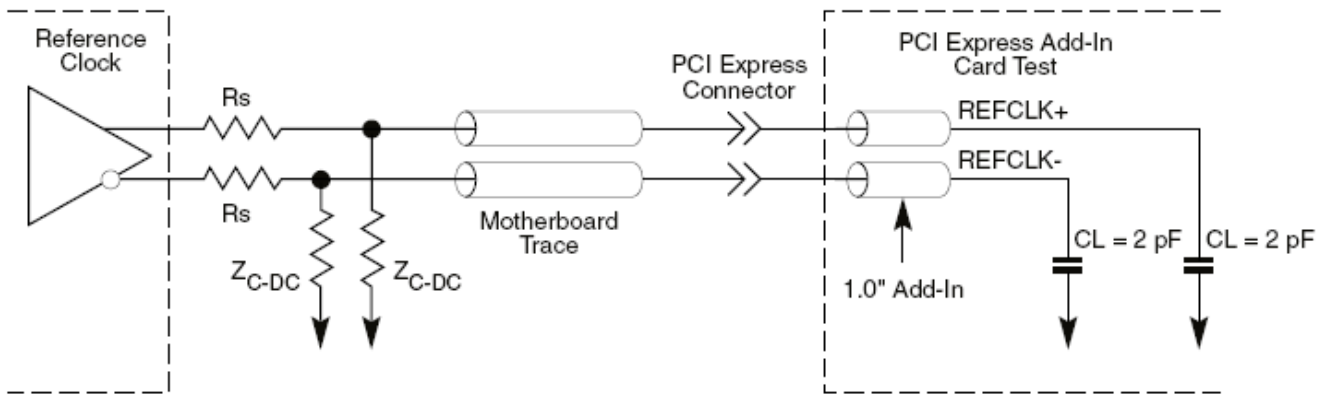
Figure 17.   Reference Clock System Measurement Point and Loading

7.7.4.   Auxiliary Signal Timing Parameters

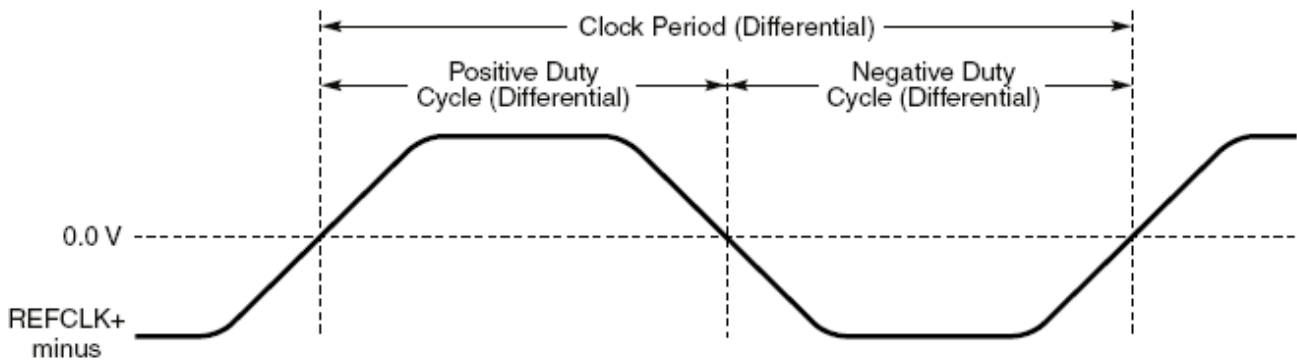**Table 33.   Auxiliary Signal Timing Parameters**

Symbol	Parameter	Min	Max	Units
T_{PVPERL}	Power stable to PERSTB inactive	100	-	ms
$T_{PERST-CLK}$	REFCLK stable before PERSTB inactive	100	-	μs
T_{PERST}	PERSTB active time	100	-	μs
T_{FAIL}	Power level invalid to PWRGD inactive	-	500	ns
T_{WKRF}	LANWAKEB rise – fall time	-	100	ns
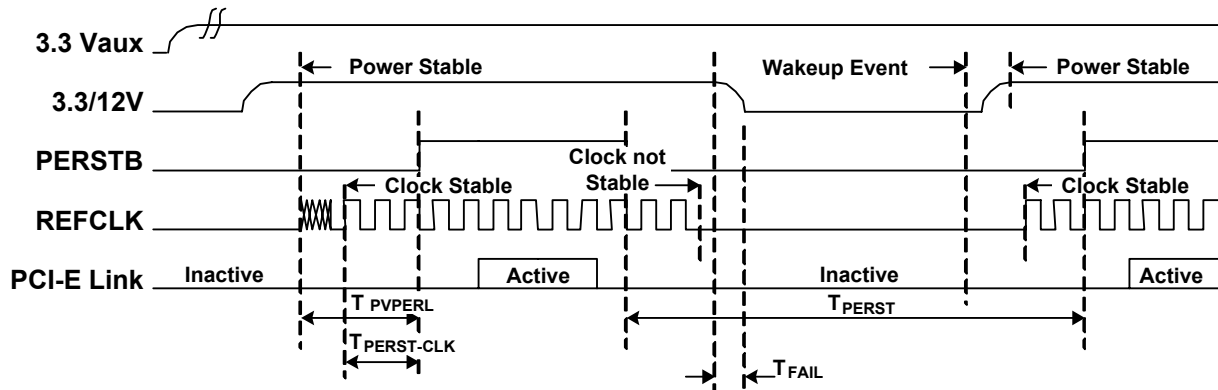
Figure 18.   Auxiliary Signal Timing

8. Mechanical Dimensions

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	1.00	0.031	0.033	0.039
A1	0.00	0.02	0.05	0.000	0.0008	0.002
A2	----	0.65	1.00	----	0.026	0.039
A3		0.20 REF			0.008 REF	
b	0.18	0.23	0.30	0.007	0.009	0.012
D		9.00 BSC			0.354 BSC	
D1		8.75 BSC			0.344 BSC	
E		9.00 BSC			0.354 BSC	
E1		8.75 BSC			0.344 BSC	
e		0.50 BSC			0.020 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020
θ	0°	----	12°	0°	----	12°
aaa	----	----	0.25	----	----	0.010
bbb	----	----	0.10	----	----	0.004
chamfer	----	----	0.60	----	----	0.024

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER

2. REFERENGE DOCUMENT: PROPSED JEDEC MO-220.

Exposed Pad Size & Support bar table

L/F	D2 (mm)			E2 (mm)			✳
①	6.90	7.05	7.20	6.90	7.05	7.20	YES / NO
②	6.70	6.85	7.00	6.70	6.85	7.00	NO
③	5.54	5.69	5.84	5.54	5.69	5.84	NO
④	3.64	3.79	3.94	3.64	3.79	3.94	NO

NOTE: RTL8111C's exposed pad size is L/F 3

TITLE : 64LD QFN (9X9 mm) PACKAGE OUTLINE			
L/F MATERIAL : A194 FH(PPF)			
APPR.	Holman Chan	DWG NO.	CE064-SW1
ENG.	C.Y.Horng	REV NO.	c
QM.	S.T.Liao	PRODUCT CODE	CE0641A
CHK.	Y.Y.Lai	DATE	06/18/'02
DWG.	R.K.Wang	SHT No.	1/1

COPY CONTROLLED

REV NO	DESCRIPTION	DATE
C	Add Exposed Pad Size & Support bar table	06/17/02

SILICONWARE PRECISION INDUSTRIES CO., LTD.

9. Ordering Information

Table 34. Ordering Information

Part Number	Package	Status
RTL8111C-GR	64-Pin QFN 'Green' package	Production

Note: See page 3 for package ID information.

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