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AN-6077

SG6742 — Highly Integrated Green-Mode PWM Controller

Abstract

This application note describes a detailed design strategy for a high-efficiency, compact flyback converter. Design considerations, mathematical equations, and guidelines for a Printed-Circuit-Board (PCB) layout are presented.

Features

- High-Voltage Startup
- Low Operating Current: 2.7mA
- Linearly Decreasing PWM Frequency to 22KHz
- Frequency Hopping to Reduce EMI Emission
- Fixed PWM Frequency:
  ML and MR are 65KHz.
  HL and HR are 100KHz.
- Peak-Current-Mode Control
- Cycle-by-Cycle Current Limiting
- Leading-Edge Blanking (LEB)
- Synchronized Slope Compensation
- Internal Open-Loop Protection
- Gate Output Maximum Voltage Clamp: 18V
- V_{DD} Under-Voltage Lockout (UVLO)
- V_{DD} Over-Voltage Protection (OVP)
- Programmable Over-Temperature Protection (OTP)
- Internal Latch Circuit (OVP, OTP)
- Internal Sense Short-Circuit Protection
- Built-In Soft-Start Function
  ML and MR are 5ms.
  HL and HR are 6ms.
- Constant Power Limit (Full AC Input Range)
- Internal OTP Sensor with Hysteresis

Applications

General-purpose, switch-mode power supplies and flyback power converters, including:

- Power Adapters
- Open-Frame Switch-Mode Power Supply (SMPS)

Introduction

The highly integrated SG6742 series of PWM controllers provides several features to enhance the performance of flyback converters.

To minimize standby power consumption, a proprietary green-mode function provides off-time modulation to linearly decrease the switching frequency at light-load conditions. To avoid acoustic-noise problems, the minimum PWM frequency is set above 22KHz. This green-mode function enables the power supply to meet international power conservation requirements. With the internal high-voltage startup circuitry, the power loss due to bleeding resistors is also eliminated. To further reduce power consumption, SG6742 is manufactured using the BiCMOS process, which allows an operating current of only 2.7mA.

Built-in synchronized slope compensation achieves stable peak-current-mode control. The proprietary external line compensation ensures a constant output-power limit over a wide AC input voltage range, from $90V_{AC}$ to $264V_{AC}$.

SG6742 provides many protection functions. In addition to cycle-by-cycle current limiting, the internal open-loop protection circuit ensures safety should an open-loop or output short-circuit failure occur.

	OVP (VDD)	OLP (FB)	OTP (RT)	SCP (SENSE)	Frequency
SG6742ML	Latch	Latch	Latch	Auto Restart	65KHz
SG6742MR	Latch	Auto Restart	Latch	Auto Restart	65KHz
SG6742HL	Latch	Latch	Latch	Auto Restart	100KHz
SG6742HR	Latch	Auto Restart	Latch	Auto Restart	100KHz

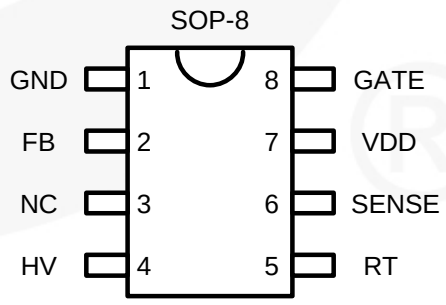

Figure 1. Pin Configuration (Top View)

Typical Application

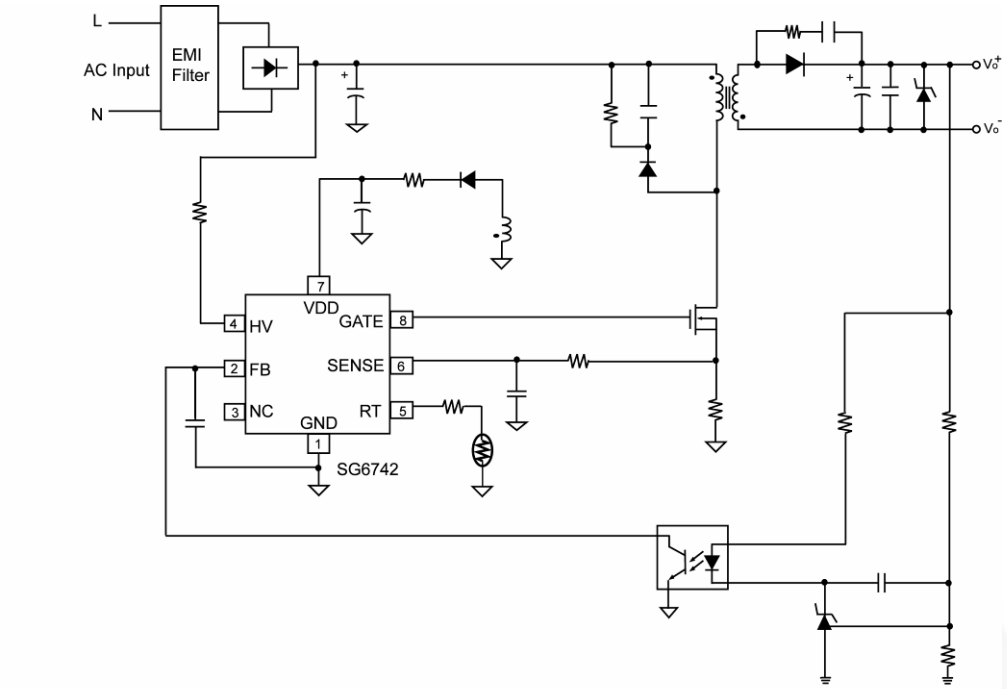

Figure 2. Typical Application

Block Diagram

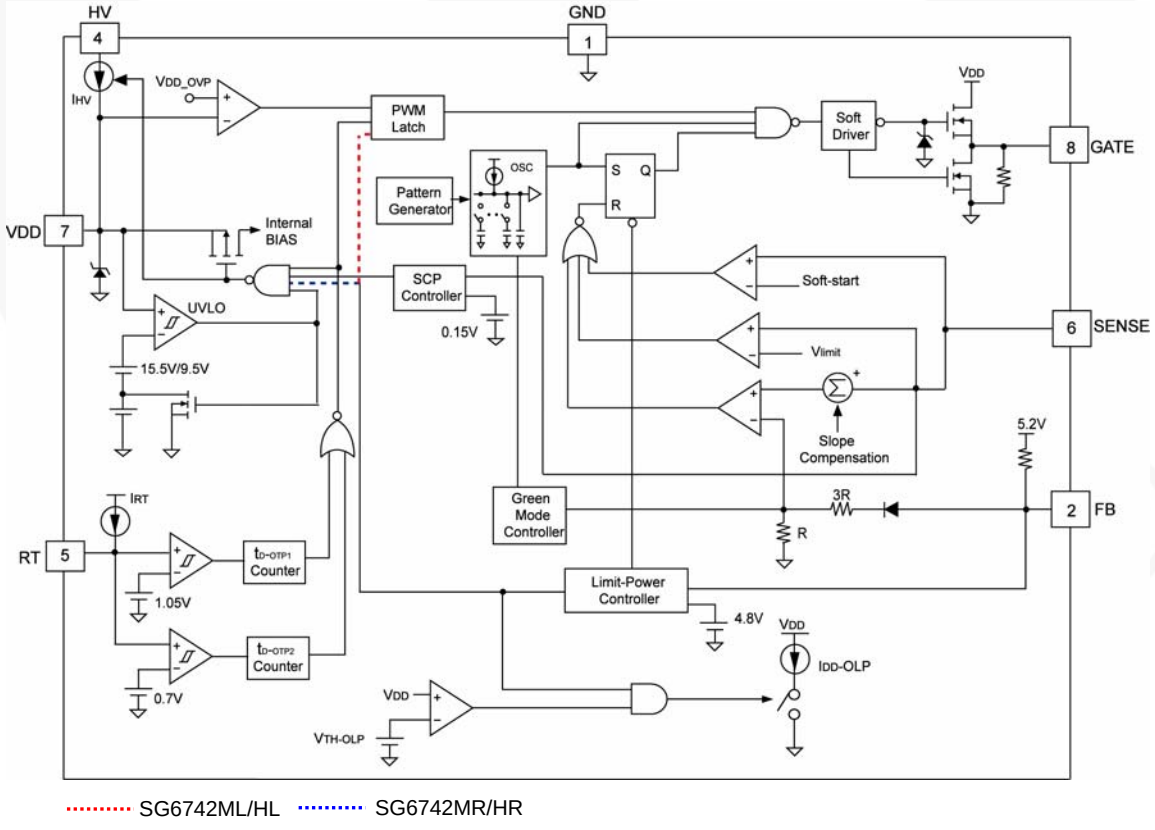

Figure 3. Functional Block Diagram

Internal Block Operation

Startup Circuitry

When the power is turned on, the internal current source (typically 2mA) charges the hold-up capacitor C_1 through a startup resistor R_{HV}. During the startup sequence, the V_{BULK} provides a startup current of about 2.3mA and charges the V_{DD} capacitor C_1. R_{HV} and D2 are series connections and can be directly connected by V_{AC} to the HV pin. As the VDD pin reaches the start threshold voltage V_{DD-ON}, the SG6742 activates and signals the MOSFET. The high-voltage source current is switched off and the supply current is drawn from the auxiliary winding of the main transformer, as shown in Figure 4.

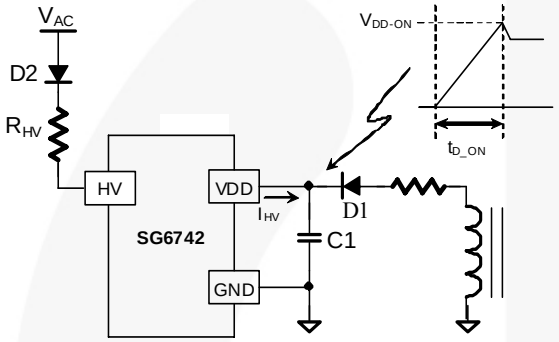

Figure 4. Startup Circuit for Power Transfer

When the supply current is drawn from the transformer, it draws a leakage current of about 1µA from the HV pin. The maximum power dissipation of the R_{HV} is:

$$P_{R_{HV}} = I_{HV-LC(Typ.)}{}^2 \times R_{HV} \quad (1)$$

where I_{HV-LC} is the supply current drawn from HV pin.

$$P_{R_{HV}} = 1\mu A^2 \times 100K\Omega \cong 0.1\mu W \quad (2)$$

Soft-Start

For many applications, it is necessary to minimize the inrush current during the startup period. The built-in 5ms/6ms soft-start circuit significantly reduces the startup current spike and output-voltage overshoot.

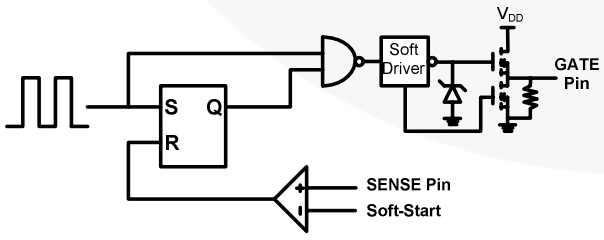

Figure 5. Soft-Start Circuit

Under-Voltage Lockout (UVLO)

The SG6742 has a voltage detector on the VDD pin to ensure that the chip has enough power to drive the MOSFET. Figure 6 shows a hysteresis of the turn-on and turn-off threshold levels and an open-loop-release voltage.

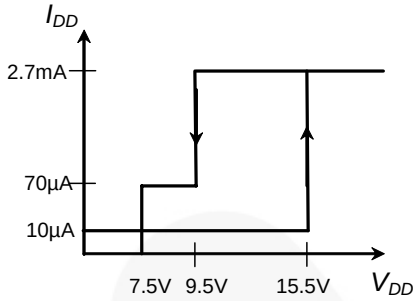

Figure 6. UVLO Specification

The turn-on and turn-off thresholds are internally fixed at 15.5V and 9.5V. During startup, the V_{DD} capacitor must be charged to 15.5V to enable the IC. The capacitor continues to supply the V_{DD} until the energy can be delivered from the auxiliary winding of the main transformer. The V_{DD} must not drop below 9.5V during startup.

If the secondary output short circuits or the feedback loop is open, the FB pin voltage rises rapidly toward the open-loop voltage, $V_{FB-OPEN}$. If the FB voltage remains above V_{FB-OLP} and lasts for t_{D-OLP}, the SG6742 stops emitting output pulses and enters latched-up mode until V_{DD} drops below 5V. To further limit the input power under a short-circuit or open-loop condition, a special two-step UVLO mechanism prolongs the discharge time of the V_{DD} capacitor. Figure 7 shows the traditional UVLO method, along with the special two-step UVLO method. In the two-step UVLO mechanism, an internal sinking current, I_{DD-OLP}, pulls the V_{DD} voltage toward the V_{DD-OLP}. This sinking current is disabled after the V_{DD} drops below V_{DD-OLP}; after which, the V_{DD} voltage is again charged towards V_{DD-ON}. With the two-step UVLO mechanism, the average input power during a short-circuit or open-loop condition is greatly reduced. As a result, over-heating does not occur.

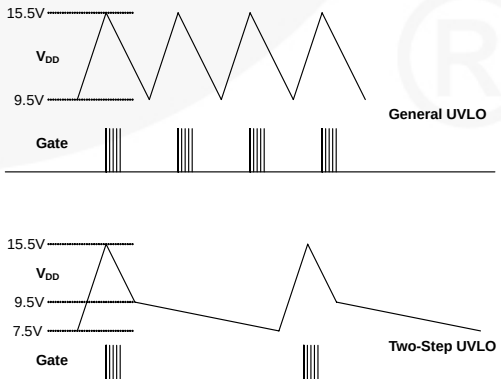

Figure 7. UVLO Effect

FB Input

The SG6742 is designed for peak-current-mode control. A current-to-voltage conversion is accomplished externally with current-sense resistor R_S. Under normal operation, the FB level controls the peak inductor current:

$$I_{PEAK} = \frac{V_{FB} - 0.6}{4 \times R_S} \quad (3)$$

where V_{FB} is the voltage on the FB pin and 4 is an internal divider ratio.

When V_{FB} is less than 0.6V, the SG6742 terminates the output pulses.

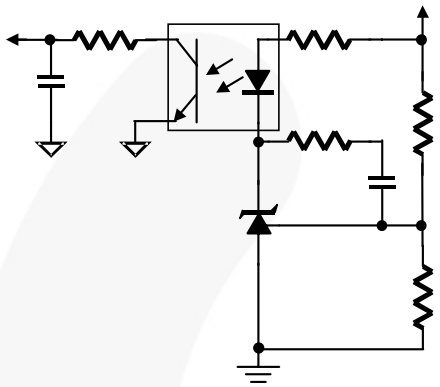

Figure 8. Feedback Circuit

Figure 8 is a typical feedback circuit consisting mainly of a shunt regulator and an opto-coupler. R_1 and R_2 form a voltage divider for the output-voltage regulation. R_3 and C_1 are adjusted for control-loop compensation. A small-value RC filter (e.g. R_{FB}= 47Ω, C_{FB}= 1nF) placed on the FB pin to the GND can further increase the stability. The maximum sourcing current of the FB pin is 1.5mA. The phototransistor must be capable of sinking this current to pull the FB level down at no load. The value of the biasing resistor R_b is determined as follows:

$$\frac{V_{OUT} - V_D - V_Z}{R_b} \cdot K \geq 1.5mA \quad (4)$$

where:

V_D is the drop voltage of photodiode, approximately 1.2V;

V_Z is the minimum operating voltage, 2.5V of the shunt regulator; and

K is the current transfer rate (CTR) of the opto-coupler.

For an output voltage V_{OUT}=5V, with CTR=100%, the maximum value of R_b is 860Ω.

Built-In Slope Compensation

A flyback converter can be operated in either Discontinuous-Current Mode (DCM) or Continuous-Current Mode (CCM). There are many advantages when operating the converter in CCM. With the same output power, a converter in CCM exhibits a smaller peak inductor current than one in DCM. Therefore, a small-sized transformer and a low-rated MOSFET can be applied. On the secondary side of the transformer, the RMS output current of DCM can be twice that of CCM. Larger wire gauge and output capacitors with larger ripple-current ratings are required. DCM operation also results in a higher output voltage spike. A large LC filter is added. Therefore, a flyback converter in CCM achieves better performance with lower component cost.

Despite the above advantages of CCM operation, there is one concern—stability. In CCM operation, the output power is proportional to the average inductor current, while the peak current remains controlled. This causes sub-harmonic oscillation when the PWM duty cycle exceeds 50%. Adding slope compensation (reducing the current-loop gain) is an effective way to prevent oscillation. The SG6742 introduces a synchronized positive-going ramp (V_{SLOPE}) in every switching cycle to stabilize the current loop. Therefore, SG6742 helps design a cost-effective, highly efficient, compact, flyback power supply that operates in CCM without additional external components.

The positive ramp added is:

$$V_{SLOPE} = V_{SL} \bullet D \quad (5)$$

where V_{SL} = 0.33V and D = duty cycle.

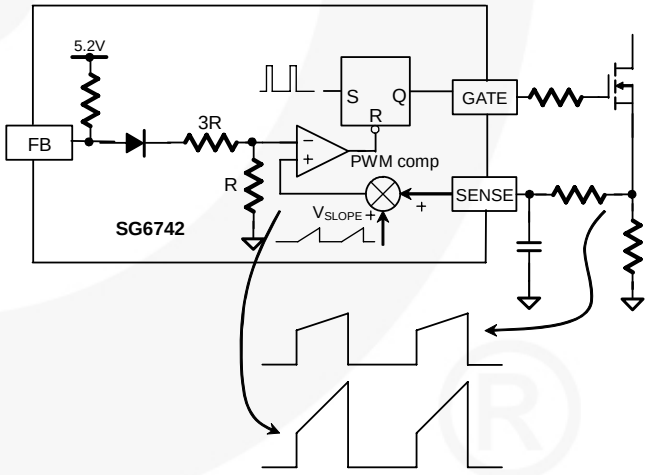

Figure 9. Synchronized Slope Compensation

Constant Output-Power Limit

The maximum output power of a flyback converter can generally be determined from the current-sense resistor R_S. When the load increases, the peak inductor current increases accordingly. When the output current arrives at the protection value, the Output-Current-Protection (OCP) comparator dominates the current-control loop. OCP occurs when the current-sense voltage reaches the threshold value. The output GATE driver is turned off after a small propagation delay t_{PD}. The delay time results in unequal power-limit levels under universal input. A sawtooth power limiter (saw limiter) is designed to solve the unequal power limit problem. As shown in Figure 10, the saw limiter is designed as a positive ramp signal (V_{limit_ramp}) and is fed into the inverting input of the OCP comparator. This results in a lower current limit at high-line inputs than at low-line inputs. However, with the fixed propagation delay t_{PD}, the peak primary current would be the same for various line-input voltages. Therefore, the maximum output power can remain a constant value within a wide input voltage range without adding any external circuitry.

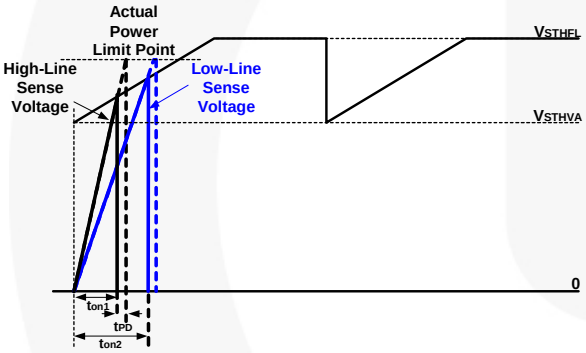

Figure 10. Constant Power-Limit Compensation

Leading-Edge Blanking (LEB)

A voltage signal proportional to the MOSFET current develops on the current-sense resistor R_S. Each time the MOSFET is turned on, a spike induced by the diode reverse recovery and the output capacitances of the MOSFET and diode, appears on the sensed signal. A leading-edge blanking time of about 140ns is introduced to avoid premature termination of the MOSFET by the spike. Therefore, only a small-value RC filter (e.g. 100Ω + 470pF) is required between the SENSE pin and R_S. Still, a non-inductive resistor for the R_S is recommended.

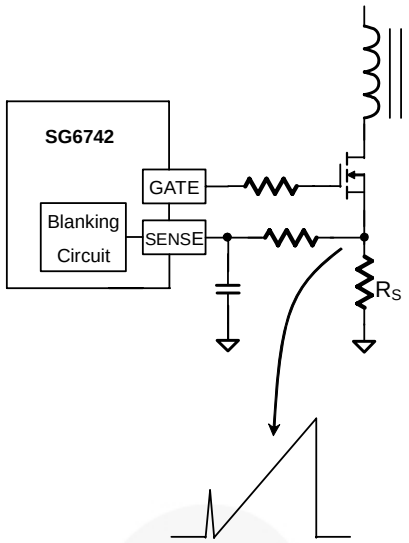

Figure 11. Circuit for Brownout

Sense-Pin Short-Circuit Protection

The SG6742 provides safety protection for power supply production. When the sense resistor is shorted by soldering during production, the pulse-by-pulse current limiting loses efficiency for the purpose of providing over-power protection for the unit. The unit may be damaged when the loading is larger than the original maximum load. To protect against a short circuit across the current-sense resistor, the controller is designed to immediately shut down if a continuously low voltage (around 0.15V/150μs) on the Sense pin is detected.

Open-Loop Protection (OLP)

The SG6742 contains the open loop protection function. If the output load is higher than the maximum output current, the output voltage will drop and the feedback error amplifier will be saturated. Once the FB voltage trips the OLP threshold 4.8V and keeps longer than 56ms, the protection will be activated to turns off the gate output to stop the switching of power circuit. As shown in Figure 12, the FB voltage is compared with 4.8V reference voltage. If the FB voltage is higher than 4.8V, the OLP timer starts counting. If the OLP condition persists for 56ms, the timer generates the OLP signal and acts as auto restart for SG6742MR/HR, latch off for SG6742ML/HL. Moreover, this protection will be reset after IC's UVLO.

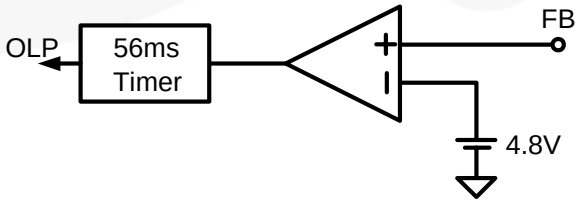

Figure 12. Open-Loop Protection Circuit

Output Driver / Soft Driving

The output stage is a fast totem-pole gate driver capable of directly driving an external MOSFET. An internal Zener diode clamps the driver voltage under 18V to protect the MOSFET against over-voltage. By integrating special circuits to control the slew rate of switch-on rising time, the external resistor R_G may not be necessary to reduce switching noise, improving Electromagnetic Interference (EMI) performance.

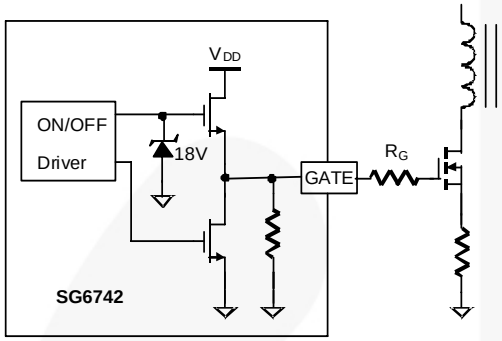

Figure 13. Gate Driver

Thermal Protection

A constant current I_{RT} (I_{RT} = 100μA) is provided from the RT pin. For over-temperature protection, an NTC thermistor R_T in series with a resistor R_a can be connected between the RT pin and ground. When V_{RT}, the voltage level of the RT pin, is less than 1.05V; PWM output is latched off after a debounce time of $t_{D\text{-}OTP1}$, which is added to prevent false triggering. If V_{RT} is less than 0.7V, PWM output latches off after a very short debounce time of $t_{D\text{-}OTP2}$.

If the thermal protection is not used, connect a small capacitor (around 0.47nF is recommended) from the RT pin to the GND pin to prevent noise interference. This RT capacitor cannot be larger than 1nF or the thermal protection is triggered before a successful startup of output voltage.

Over-Temperature Protection (OTP)

The built-in temperature-sensing circuit shuts down PWM output once the junction temperature exceeds 135°C. While PWM output is shut down, V_{DD} gradually drops to the UVLO voltage (around 7.5V). Then V_{DD} charges up to the startup threshold voltage of 15.5V through the startup resistor until PWM output is restarted. This hiccup-mode protection occurs repeatedly as long as the temperature remains above 130°C. The temperature hysteresis window for the OTP circuit is 25°C.

Printed Circuit Board Layout

Current, voltage, and switching frequency make PCB layout and design very important. Good PCB layout minimizes excessive EMI and prevents the power supply from being disrupted during surge/ESD tests. The following are some general guidelines:

- For better EMI performance and to reduce line frequency ripples, the output of the bridge rectifier should be connected to capacitor C_{bulk} first, then to switching circuits.
- The high-frequency current loop is found in the loop **C_{bulk} – Transformer – MOSFET – R_S – C_{bulk}** in Figure 14. The area enclosed by this current loop should be as small as possible. Keep the traces (especially 4→1) short, direct, and wide. High-voltage drain traces related to the MOSFET and RCD snubber should be kept far from control circuits to prevent unnecessary interference. If a heatsink is used for the MOSFET, grounding the heatsink is recommended.
- As indicated by 3 in Figure 14, the control circuits' ground should be connected first, then to other circuitry.
- As indicated by 2 in Figure 14, the area enclosed by the **transformer auxiliary winding, D_1, and C_1** should also be kept small. Place C_1 close to the SG6742 for good decoupling.

Two suggestions with pros and cons for ground connections are recommended.

- GND3→2→4→1: Possible method for circumventing the sense signals and common impedance interference.
- GND3→2→1→4: Potentially better for ESD testing where a ground is not available for the power supply. The charges for ESD discharge path go from secondary through the transformer stray capacitance to the GND2 first. Then, the charges go from GND2 to GND1 and back to the mains. It should be noted that control circuits should not be placed on the discharge path. Point discharge for common choke can decrease high-frequency impedance and help increase ESD immunity.
- Should a Y-cap between primary and secondary be required, the Y-cap should be connected to the **positive terminal of the C_{bulk} (V_{DC})**. If this Y-cap is connected to the primary GND, it should be connected to the **negative terminal of the C_{bulk} (GND1)** directly. Point discharge of the Y-cap also helps with ESD. However, according to safety requirements, the creepage between the two pointed ends should be at least 5mm.

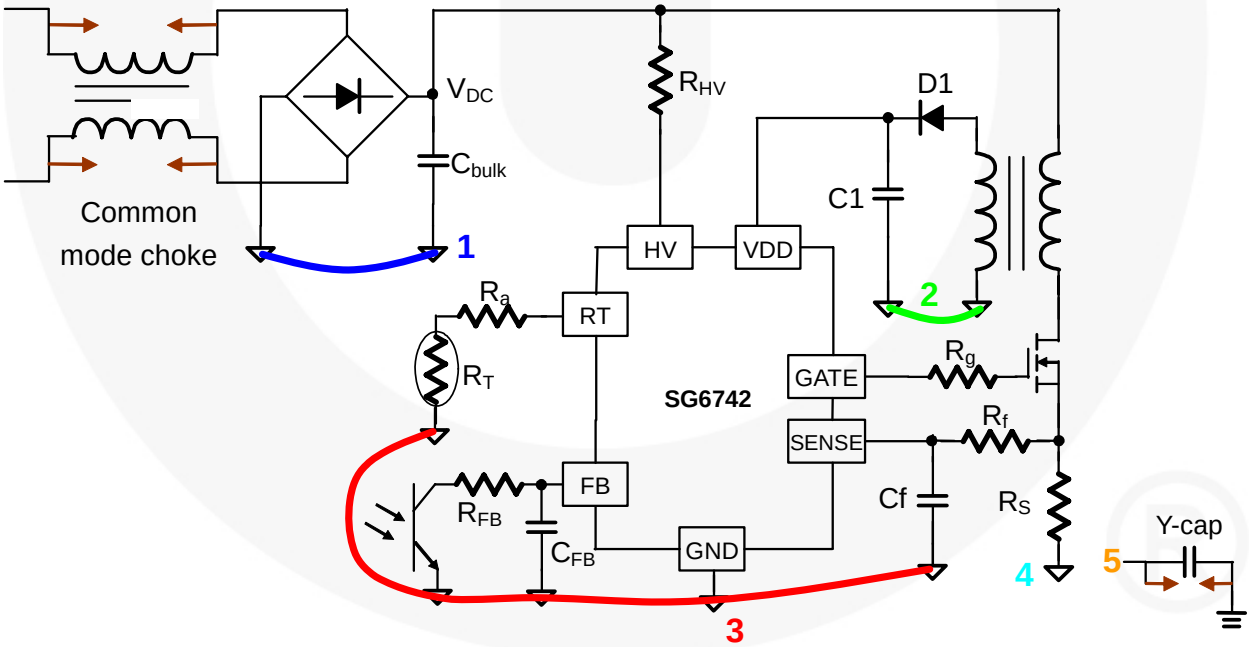

Figure 14. Layout Considerations

Related Datasheets

SG6742ML/MR — Highly Integrated Green-Mode PWM Controller

SG6742HL/HR — Highly Integrated Green-Mode PWM Controller

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