4-Channel LED Backlight Controller

## Features

- **4 Channels**
- **5.5V to 30V Input Voltage Supply**
- **Drive up to 68 (17x4) White LEDs (3.5V/160mA Each)**
- **Current Match (Balance) ±1% (Typ.)**
- **Current Accuracy ±1% (Typ.)**
- **External PWM Input from 100Hz to 50kHz Dimming Frequency**
- **Time Shift PWM Dimming Control**
- **Random Channel Selection for Dynamic Operations**
- **Adjustable Switching Frequency**
- **Protections**
  - **String Open Circuit Detection**
  - **String Short Circuit Detection**
  - **Over-Temperature Protection**
  - **Over-Voltage Protection**
- **Available in TSSOP-16P, SOP-16, DIP-16 and QFN4x4-16A Packages**
- **Lead Free and Green Devices Available (RoHS Compliant)**

## General Description

The APW7228B is a high efficiency driver for 4 channels of LEDs. It contains an adjustable-frequency current-mode PWM step-up controller, a 5V linear regulator, dimming control circuit and eight regulated current source circuit.

The APW7228B is capable of driving typically 68 (4x17) pieces of 3.5V/160mA LEDs. It contains 4 channels of voltage controlled current sources with typical currents matching of ±1%, which compensate for the non-uniformity effect of forward voltages variance in the LED stacks. To minimize the voltage headroom and power loss in the typical multi-strings operation, the APW7228B features a dynamic headroom control that monitors the highest LED forward voltage string and uses its feedback signal for output regulation.

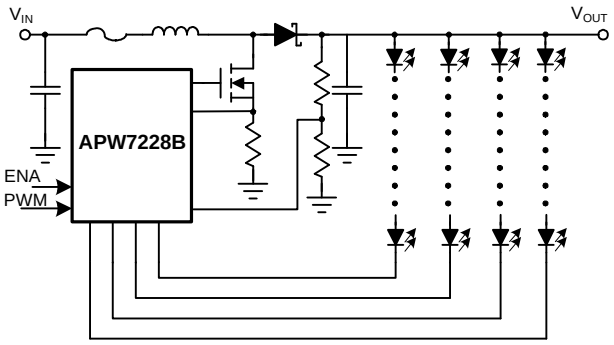
The APW7228B features extensive protection functions that include LED strings open and short circuit detections, Output Over-Voltage Protection (OVP) and Over-Temperature Protection (OTP).

The APW7228B is available in TSSOP-16P, SOP-16, DIP-16 and QFN4x4-16A package.

## Applications

- **NB LED Backlight**
- **LCD Monitor Backlight**
- **LCD TV LED Backlight**

## Simplified Application Circuit

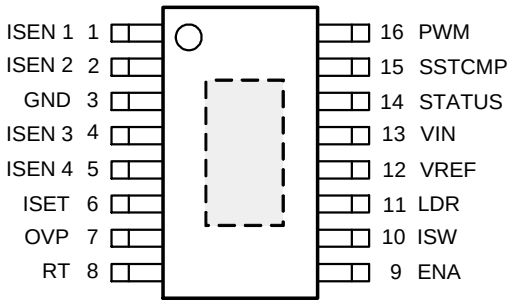


## Ordering and Marking Information

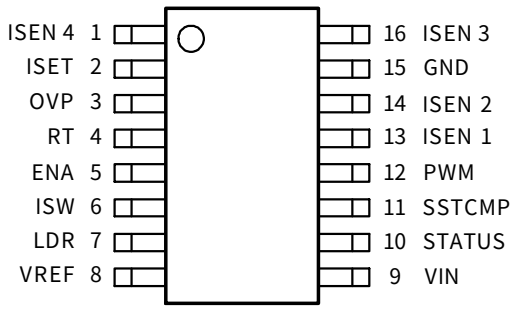
| | |
|---|---|
| APW7228B □□□-□□□<br>Assembly Material<br>Handling Code<br>Temperature Range<br>Package Code | Package Code<br>R : TSSOP-16P K : SOP-16 J: DIP-16 QA : QFN4x4-16A<br>Operating Ambient Temperature Range<br>I : -40 to 85 °C<br>Handling Code<br>TR : Tape & Reel<br>Assembly Material<br>G : Halogen and Lead Free Device |
| APW7228B R : W7228B XXXXX | XXXXX - Date Code |
| APW7228B K : W7228B XXXXX | XXXXX - Date Code |
| APW7228B J : W7228B XXXXX | XXXXX - Date Code |
| APW7228B QA : W7228B XXXXX | XXXXX - Date Code |

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

## Pin Configuration

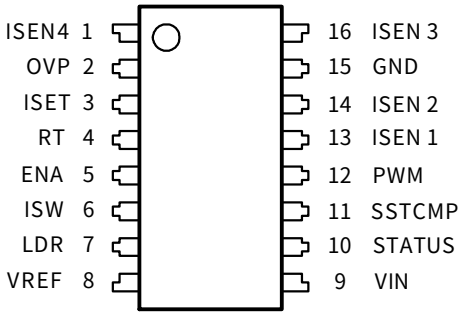



TSSOP -16P

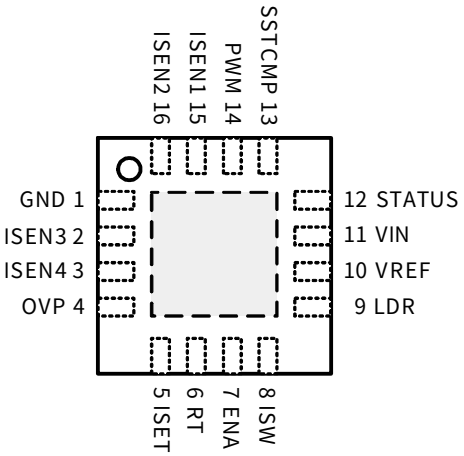



SOP - 16

## Pin Configuration(Cont.)




DIP-16




QFN 4x4-16A

## Absolute Maximum Ratings (Note 1)

| Symbol | Parameter | Rating | Unit |
|---|---|---|---|
| $V_{IN}$ | VIN Input Voltage (VIN to GND) | -0.3 to 40 | V |
| $V_{ISW}$ | ISW to GND Voltage | -0.3 to 65 | V |
| $V_{ISEN1} - V_{ISEN4}$ | ISEN1 – ISEN4 to GND Voltage | -0.3 to 65 | V |
| $I_{ISEN1\sim4}$ | ISEN1 – ISEN4 LED Current | ~ 180 | mA |
| $V_{I/O}$ | VREF, OVP, ENA, PWM, STATUS to GND Voltage | -0.3 to 7 | V |
| | RT, ISET, SSTCMP, LDR to GND Voltage | -0.3 to VREF+0.3 | V |
| $T_J$ | Maximum Junction Temperature | 150 | °C |
| $T_{STG}$ | Storage Temperature | -65 to 150 | °C |
| $T_{SDR}$ | Maximum Lead Soldering Temperature (10 Seconds) | 260 | °C |

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

## Thermal Characteristics

| Symbol | Parameter | Typical Value | Unit |
|---|---|---|---|
| $\theta_{JA}$ | Junction-to-Ambient Resistance in Free Air (Note 2) | | °C/W |
| | TSSOP-16P | 38 | |
| | SOP-16 | 80 | |
| | DIP-16 | 45 | |
| | QFN4x4-16A | 40 | |
| $\theta_{JC}$ | Junction-to-Case Resistance in Free Air (Note 2) | | °C/W |
| | TSSOP-16P | 15 | |
| | SOP-16 | 10 | |
| | DIP-16 | 8 | |
| | QFN4x4-16A | 6 | |

Note 2: $\theta_{JA}$ and $\theta_{JC}$ are measured with the component mounted on a high effective thermal conductivity test board in free air. The thermal pad of TSSOP-16P and QFN4x4-24A is soldered directly on the PCB.

## Recommended Operating Conditions (Note 3)

| Symbol | Parameter | Range | Unit |
|---|---|---|---|
| $V_{IN}$ | VIN Input Voltage (VIN to GND) | 5.5 to 30 | V |
| $V_{OUT}$ | Converter Output Voltage | ~60 | V |
| $I_{LED}$ | Output LED Current Per String | 20~160 | mA |
| $V_{ENA}$ | ENA Enable Voltage | 5 | V |
| $F_{PWM}$ | PWM Dimming Frequency | 100 to 50k | Hz |
| $T_A$ | Ambient Temperature | -40 to 85 | °C |
| $T_J$ | Junction Temperature | -40 to 125 | °C |

Note 3: Please refer to the typical application circuit.

## Electrical Characteristics

Unless otherwise specified, these specifications apply over $V_{IN}$=12V, $V_{ENA}$=5V and $T_A$=-40 to 85°C. Typical values are at $T_A$=25°C.

| Symbol | Parameter | Test Conditions | APW7228B | | | |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Unit |
| $I_{VIN}$ | VIN Operating Current | ENA=2V, PWM=5V | - | - | 12 | mA |
| | VIN Shutdown Current | ENA=0V, PWM=5V | - | 1 | 5 | uA |
| | VIN Standby Current | ENA=2V, PWM=0V | - | 100 | 150 | uA |
| **Enable and PWM Dimming** | | | | | | |
| | ENA and PWM Logic | High | 2.4 | - | - | V |
| | | Low | - | - | 0.8 | V |
| | PWM Dimming maximum frequency | | - | 70 | - | kHz |
| **Under Voltage Lockout** | | | | | | |
| | Lockout Logic Threshold | VREF Lockout | 4.1 | 4.2 | 4.3 | V |
| | Resume Logic Hysteresis | VREF Resume | - | 200 | - | mV |
| **Reference** | | | | | | |
| | Reference Voltage | | 5.35 | 5.5 | 5.65 | V |
| | | Thermal Coefficient | - | 50 | - | ppm/°C |
| | VREF Output Current Capability | IVREF | - | 30 | - | mA |

## Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over $V_{IN}$=12V, $V_{ENA}$=5V and $T_A$=-40 to 85°C. Typical values are at $T_A$=25°C.

| Symbol | Parameter | Test Conditions | APW7228B | | | |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Unit |
| **DRIVE CAPABILITY** | | | | | | |
| | LDR Sink Resistance | | 1 | 4 | 8 | Ω |
| | LDR Source Resistance | | 1 | 5 | 9 | Ω |
| | Minimum MOSFET ON Time | | - | 200 | - | ns |
| | Minimum MOSFET OFF Time | | - | 100 | - | ns |
| **REGULATION** | | | | | | |
| | Regulation LED Current Per Channel | ISET=12kΩ | 97 | 100 | 103 | mA |
| | LED Current Balance Rate | Δ | -3 | - | 3 | % |
| **PROTECTION** | | | | | | |
| | Output Over-Voltage Protection Threshold | OVP | 1.9 | 2 | 2.1 | V |
| | LED Open Circuit Protection Threshold | Internal MOSFET gate voltage (Note 4) | - | $V_{REF}$-0.5 | - | V |
| | LED Short Circuit Protection Threshold | ISEN1 -4 | 7.8 | 8.5 | 9.2 | V |
| **OCILLATOR** | | | | | | |
| | Operation Frequency | $R_{RT}$=100kΩ | 440 | 500 | 560 | kHz |
| | | Temp. Coefficient | - | 500 | - | ppm/°C |
| | SSTCMP Clamp High Voltage | | - | 3.9 | - | V |
| | SSTCMP Clamp Low voltage | | - | 1.1 | - | V |
| **STATUS OUTPUT** | | | | | | |
| | Sink Resistance | Status | - | - | 60 | Ω |
| **MOSFET OVER-CURRENT PROTECTION** | | | | | | |
| | N-FET Over-Current Protection | ISW | 0.46 | 0.54 | 0.64 | V |
| **VREF** | | | | | | |
| | Load Regulation | | - | 5 | - | mV/mA |
| | SEL High Threshold | | - | 0.3 | - | mV/V |
| **THERMAL PROTECTION** | | | | | | |
| | Lockout Temp | | - | 150 | - | °C |
| | Resume Temp | | - | 120 | - | °C |

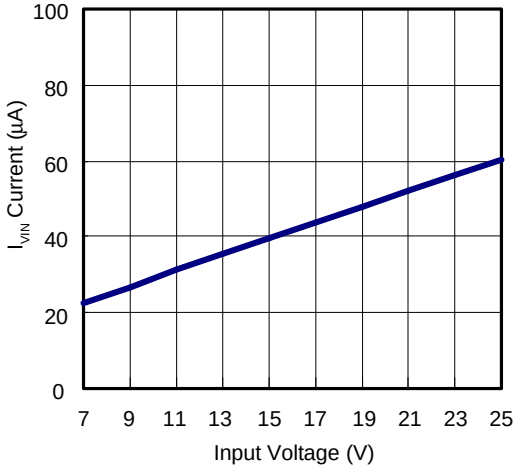
Note 4: Guaranteed by design, not production tested.

## Pin Description (I=Input, O=Output, S=Supply)

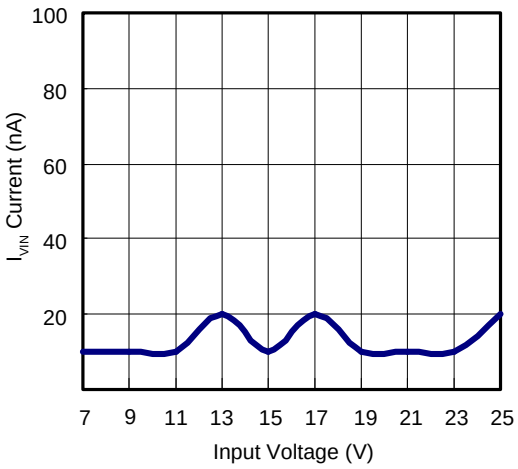
| NAME | PIN | | | | FUNCTION |
|---|---|---|---|---|---|
| | TSSOP-16P | SOP-16 | DIP-16 | QFN4x4-16A | |
| ISEN1 | 1 | 13 | 13 | 15 | Input 1 to WLED Current source. |
| ISEN2 | 2 | 14 | 14 | 16 | Input 2 to WLED Current source. |
| GND | 3 | 15 | 15 | 1 | Ground pin. |
| ISEN3 | 4 | 16 | 16 | 2 | Input 3 to WLED Current source. |
| ISEN4 | 5 | 1 | 1 | 3 | Input 4 to WLED Current source. |
| ISET | 6 | 2 | 3 | 5 | Resistor connection for setting maximum LED current. Do not short this pin to GND. |
| OVP | 7 | 3 | 2 | 4 | Over-Voltage Protection input pin. Calculate output over-voltage triggered point according to $V_{OUT} = (1+R_{UPPER}/R_{LOWER}) \times 2V$. |
| RT | 8 | 4 | 4 | 6 | This pin is allowed to adjust the switching frequency. Connect a resistor $R_{RT}$ from the RT pin to the GND pin. |
| ENA | 9 | 5 | 5 | 7 | Enable Control Input. Forcing this pin above 2.4V enables the device, or forcing this pin below 0.8V to shut it down. In shutdown, all functions are disabled to decrease the supply current below 1μA. Do not leave this pin floating. |
| ISW | 10 | 6 | 6 | 8 | Power MOSFET Current Sense Pin. |
| LDR | 11 | 7 | 7 | 9 | Low Side Power MOSFET gate driver. |
| VREF | 12 | 8 | 8 | 10 | 5V regulator supply for low voltage block. This pin provides bias supply for control circuitry and the Low-Side MOSFET LDR gate driver. |
| VIN | 13 | 9 | 9 | 11 | Main Supply Pin. Must be closely decoupled to the GND with a 4.7μF or greater ceramic capacitor. |
| STATUS | 14 | 10 | 10 | 12 | LED Operation Status Output. |
| SSTCMP | 15 | 11 | 11 | 13 | Soft Start and Control Loop Compensation. |
| PWM | 16 | 12 | 12 | 14 | PWM brightness control pin. Do not leave this pin floating. |

## Typical Operating Characteristics

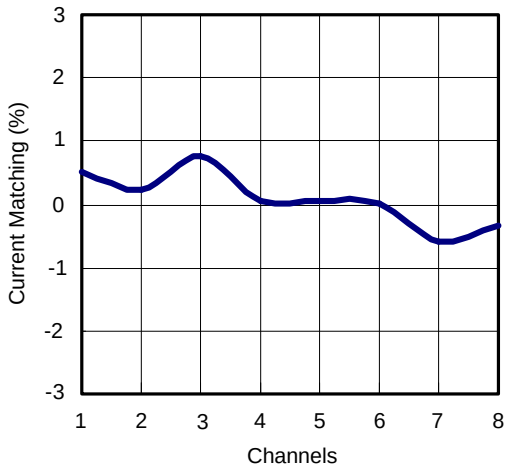
**Standby Current**
**ENA=5V, PWM=0V**



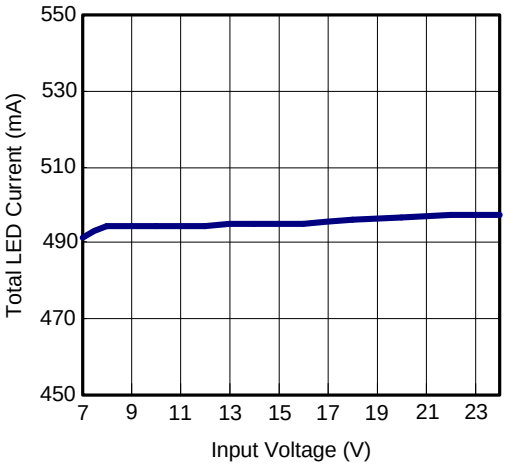

**Shutdown Current**
**ENA=0V, PWM=5V**



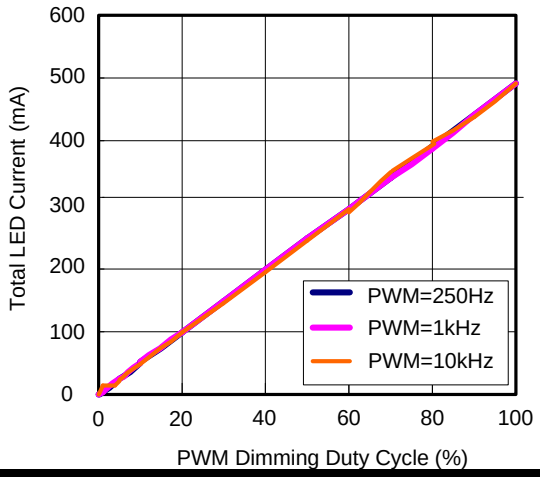

**Channel to Channel Current Matching**




**LED Current v.s. Input Voltage**

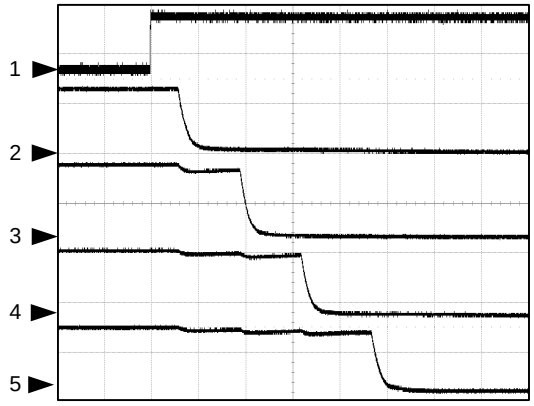



**LED Current v.s. Dimming Duty Cycle**



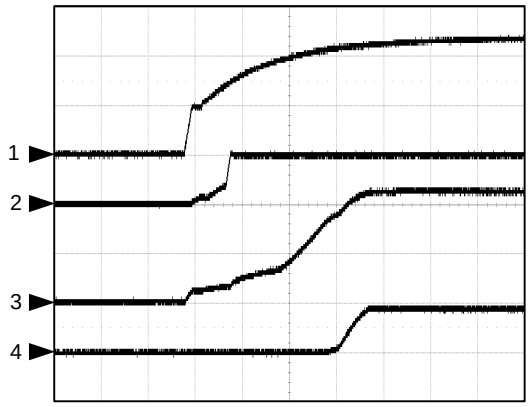
## Operating Waveforms

**PWM Goes High, ISEN Shift Behavior**



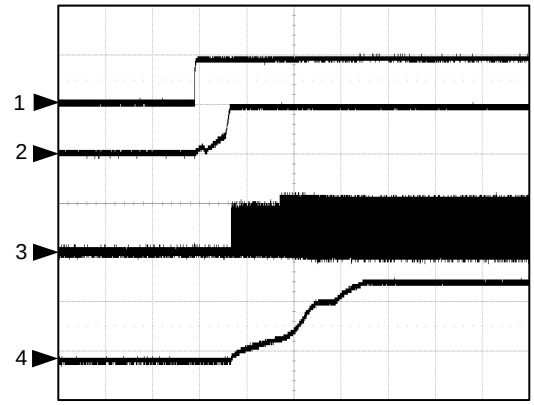

CH1: $V_{PWM}$ (5V/div)
CH2: $V_{ISEN1}$ (10V/div)
CH3: $V_{ISEN2}$(10V/div)
CH4: $V_{ISEN3}$ (10V/div)
CH5: $V_{ISEN4}$ (10V/div)
Time: 2μs/div

**$V_{IN}$ Power On , PWM=ENA=H**



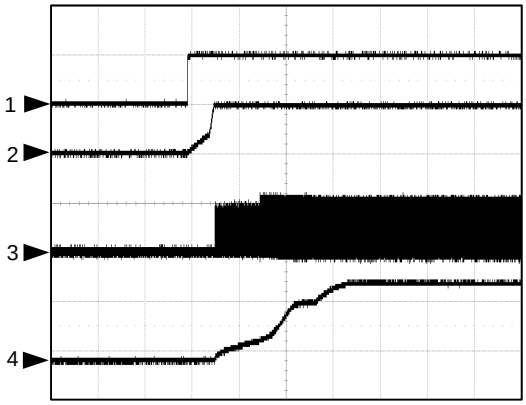

CH1: $V_{IN}$ (5V/div)
CH2: $V_{VREF}$ (5V/div)
CH3: $V_{OUT}$ (20V/div)
CH4: $I_{ILED}$ (500mA/div)
Time: 2ms/div

**Enable, Hot Plug-In ENA, PWM=H**




CH1: $V_{ENA}$ (5V/div)
CH2: $V_{VREF}$ (5V/div)
CH3: $V_{LDR}$ (5/div)
CH4: $V_{OUT}$ (20V/div)
Time: 2ms/div

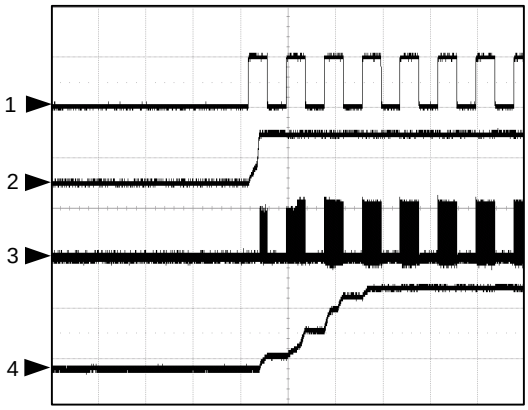
**Enable, Hot Plug-In PWM, ENA=H**




CH1: $V_{PWM}$ (5V/div)
CH2: $V_{VREF}$ (5V/div)
CH3: $V_{LDR}$ (5/div)
CH4: $V_{OUT}$ (20V/div)
Time: 2ms/div

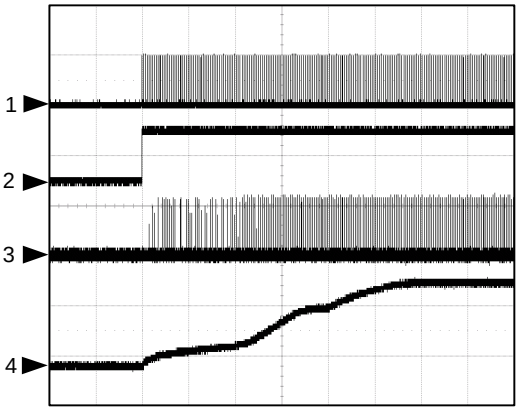
## Operating Waveforms (Cont.)

**PWM Dimming Enable, 250Hz, 50%**



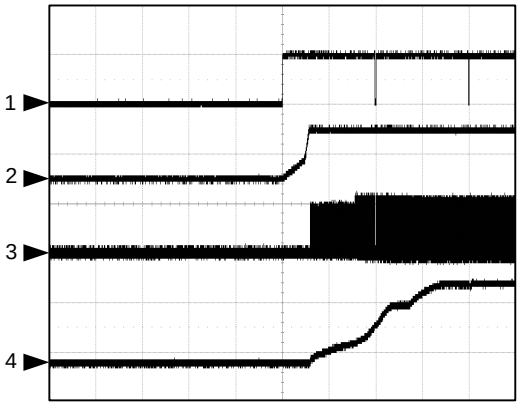

CH1: $V_{PWM}$ (5V/div)
CH2: $V_{VREF}$ (5V/div)
CH3: $V_{LDR}$ (5/div)
CH4: $V_{OUT}$ (20V/div)
Time: 5ms/div

**PWM Dimming Enable, 250Hz, 1%**



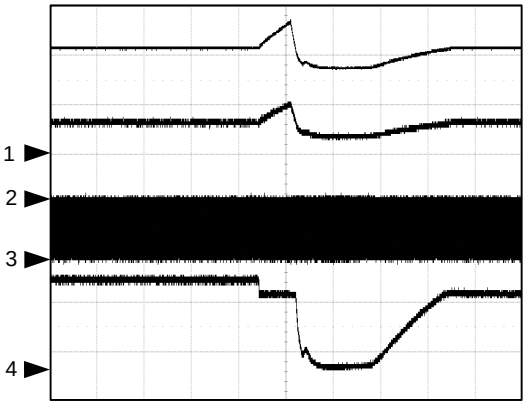

CH1: $V_{PWM}$ (5V/div)
CH2: $V_{VREF}$ (5V/div)
CH3: $V_{LDR}$ (5/div)
CH4: $V_{OUT}$ (20V/div)
Time: 100ms/div

**PWM Dimming Enable, 250Hz, 99%**




CH1: $V_{PWM}$ (5V/div)
CH2: $V_{VREF}$ (5V/div)
CH3: $V_{LDR}$ (5/div)
CH4: $V_{OUT}$ (20V/div)
Time: 2ms/div

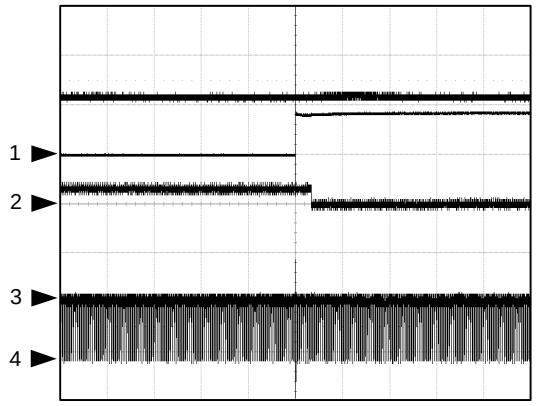
**One String Open**




CH1: $V_{OUT}$ (20V/div)
CH2: $V_{OVP}$ (1V/div)
CH3: $V_{LDR}$ (5/div)
CH4: $I_{ILED}$ (200mA/div)
Time: 1ms/div

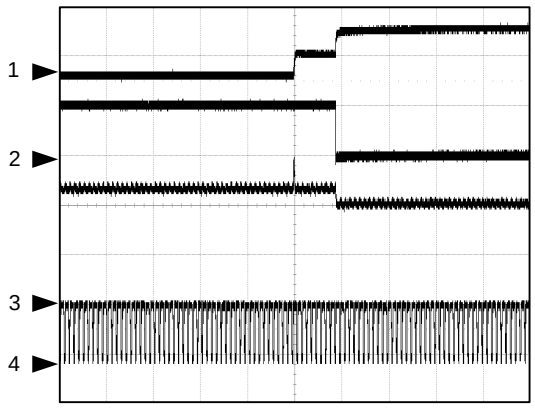
## Operating Waveforms (Cont.)

**One String ISEN Short to $V_{OUT}$**



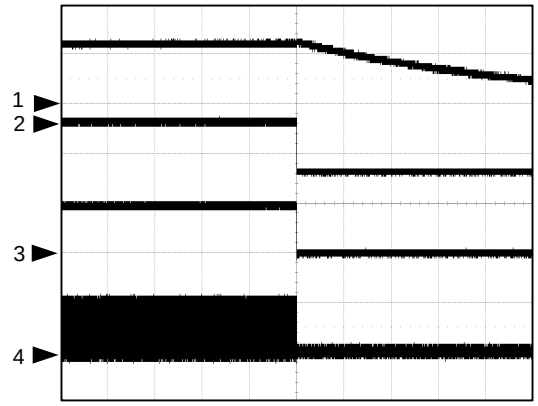

CH1: $V_{ISEN1}$ (50V/div)
CH2: $V_{OUT}$ (20V/div)
CH3: $I_{ILED}$ (200mA/div)
CH4: $V_{LDR}$ (5V/div)
Time: 50µs/div

**Three LEDs Short in One String**



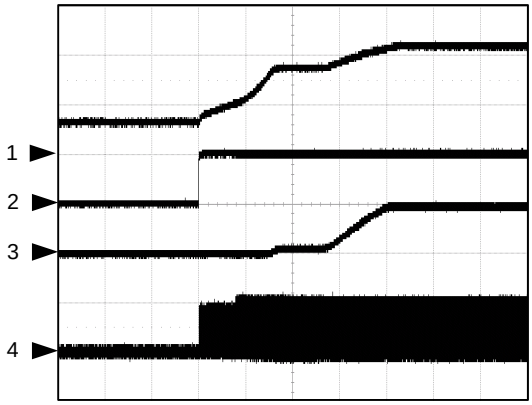

CH1: $V_{ISEN1}$ (20V/div)
CH2: $V_{STATUS}$ (5V/div)
CH3: $I_{ILED}$ (200mA/div)
CH4: $V_{LDR}$ (5V/div)
Time: 20µs/div

**Over-Temperature Protection**




CH1: $V_{OUT}$ (20V/div)
CH2: $V_{STATUS}$ (5V/div)
CH3: $I_{ILED}$ (500mA/div)
CH4: $V_{LDR}$ (5V/div)
Time: 50ms/div

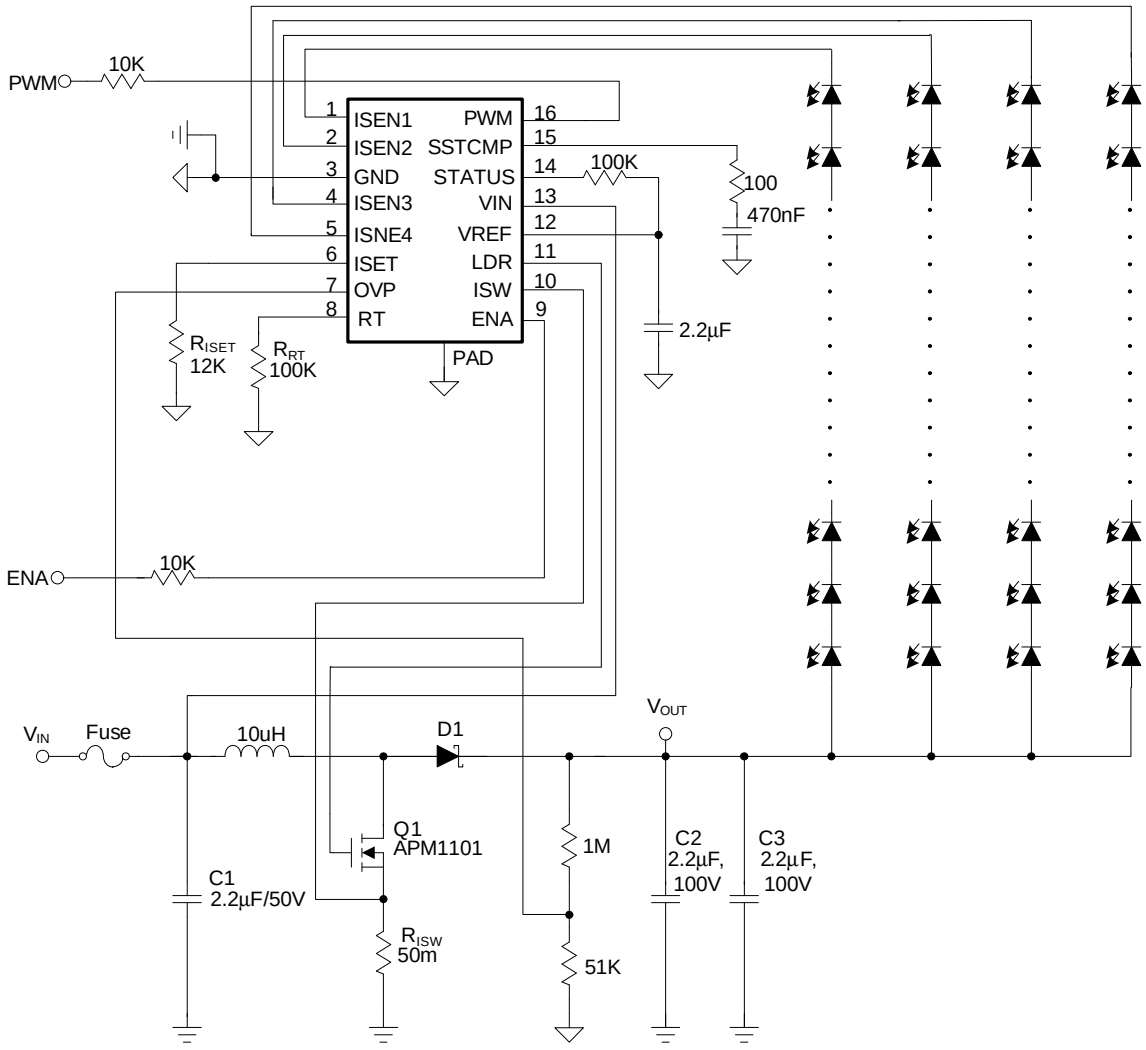
**Released Over-Temperature Protection**



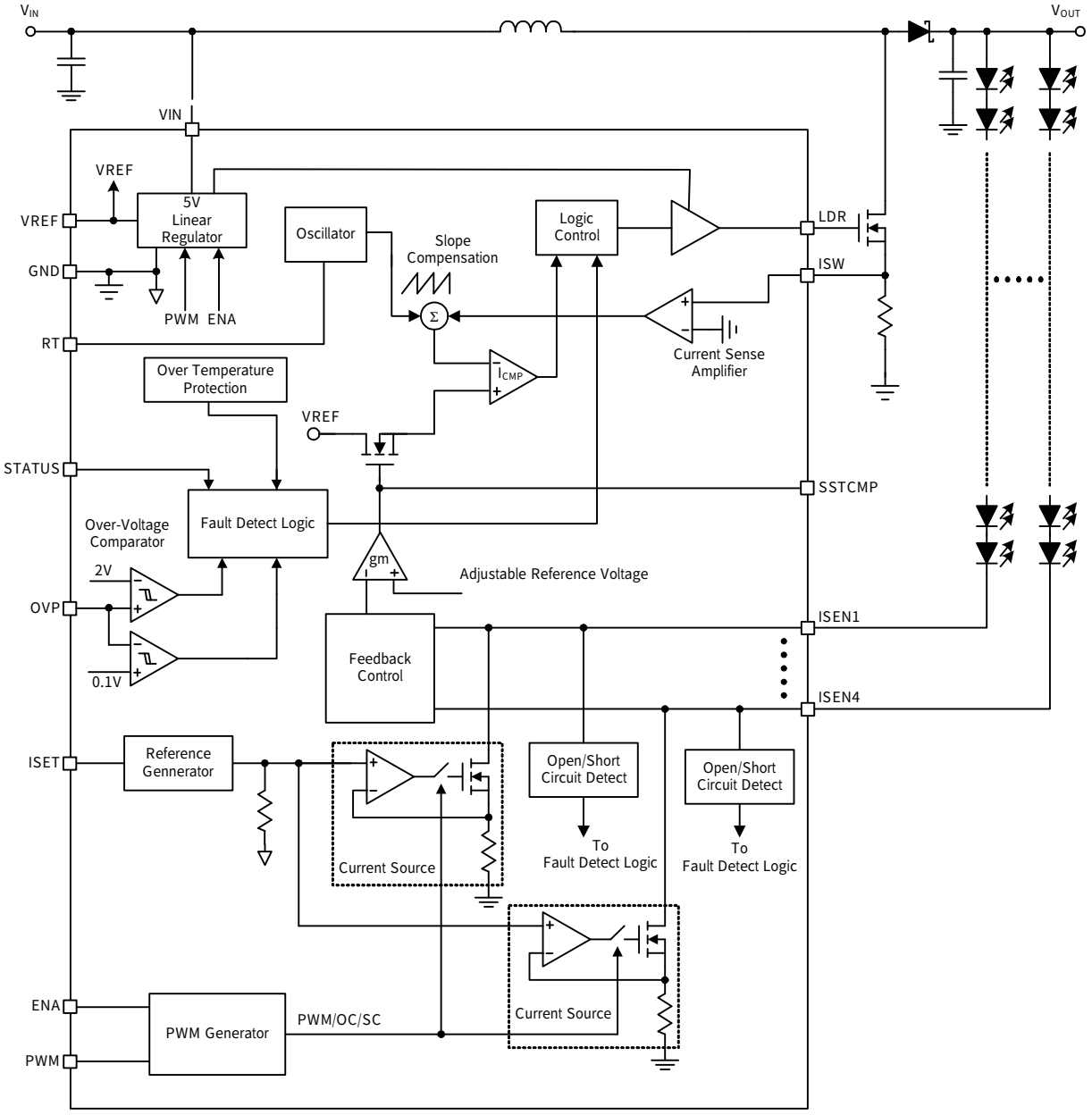

CH1: $V_{OUT}$ (20V/div)
CH2: $V_{STATUS}$ (5V/div)
CH3: $I_{ILED}$ (500mA/div)
CH4: $V_{LDR}$ (5V/div)
Time: 2ms/div

## Typical Application Circuit

**(Using TSSOP-16P)**



## Block Diagram



## Function Description

The APW7228B is a high efficiency driver for 4 channels of LEDs. It contains an adjustable-frequency current-mode PWM step-up controller, a 5V linear regulator, dimming control circuit and eight regulated current source.
The APW7228B contains 4 channels of voltage controlled current sources with typical currents matching of ±1%, which compensate for the non-uniformity effect of forward voltages variance in the LED stacks. To minimize the voltage headroom and power loss in the typical multi-strings operation, the APW7228B features a dynamic headroom control that monitors the highest LED forward voltage string and uses its feedback signal for output regulation.

### Enable and PWM

Driving ENA to the ground places the APW7228B in shutdown mode. When in shutdown, the internal gate driver turns off. The PWM can be used for PWM input for dimming. If the dimming function is not used, connect PWM and EN together. The EN and PWMI pins cannot be floating, thus a pull-low resistance may needs to be added.

### Current Source

The APW7228B integrated 4 matched current sources to maintain uniform LED brightness for LCD backlight application. The maximum LED current is set by $R_{ISET}$ pin with a scaling factor $1200/R_{ISET}$. The minimum voltage drop across each current source is 0.35V when the LED is 20mA. The low drop-voltage reduces power loss to improve efficiency.
The APW7228B detect the voltage from any of ISEN pins. When the lowest current source voltage is lower than the short circuit threshold, $V_{SC}$, such will be use as the feedback signal of the error amplifier input. The converter boosts the output voltage to the corresponding level using the lowest current source voltage. Since all LED strings connect to the same output voltage, the other pins will have a higher voltage, but the current sources could regulate the same current on all channel within 1%. The lowest current source voltage is related to $R_{ISET}$ resistance setting. When the $R_{ISET}$ is bigger, the lowest current source voltage level is lower.

### Programming the BOOST switching Frequency

The resistor $R_{RT}$ that is connected from the RT pin to the GNDA pin programs the boost converter switching frequency $F_{SW}$. The approximate PWM switching frequency is written as:

$$F_{SW} = \frac{1}{K \cdot R_{RT}}$$

Where:
- $F_{SW}$ is the PWM switching frequency
- $R_{RT}$ is the $F_{SW}$ programming resistor

$K = 2 \times 10^{-11}$

### PWM Dimming Controls

The APW7228B uses PWM signal to control LED current, and therefore brightness.

**- Maximum LED Current Setting**

Placing a resistor from ISET pin to GND sets the maximum LED current.

$$I_{LEDMAX} = 1200/R_{RSET}$$

**- PWM Signal Input**

The brightness could be adjusted by a PWM signal from PWM pin. The average LED current is proportion to duty cycle of PWM signal.

$$I_{LEDAVG} = I_{LEDMAX} \times D_{PWM}$$

where $D_{PWM}$ = duty cycle of PWM input signal. The PWM signal operation suggestion can follow the formula as below,
Minimum PWM Signal On Time:

$$\text{Duty}(\%) \geq 1500 \times 10^{-6} \times F_{PWM\_Signal}(\text{Hz})$$

Minimum PWM Signal Off Time:

$$(1-\text{Duty})(\%) \geq 50 \times 10^{-6} \times F_{PWM\_Signal}(\text{Hz})$$

Thus, the PWM dimming frequency could up to 40kHz with duty cycle range from 60% to 98%. If the dimming frequency is below 200Hz, the duty cycle range can be 0.3% to 99.99%.

## Function Description (Cont.)

**PWM Dimming Controls (Cont.)**

**- Phase Shift**

APW7228B provides a phase-shifted feature to reduce audible noise and ripple stresses. Referring to Figure 1, every two ISEN rising and falling edges are phase-shifted 2µs. ISEN1 follow external PWM signal and its delay time is about 1µs.

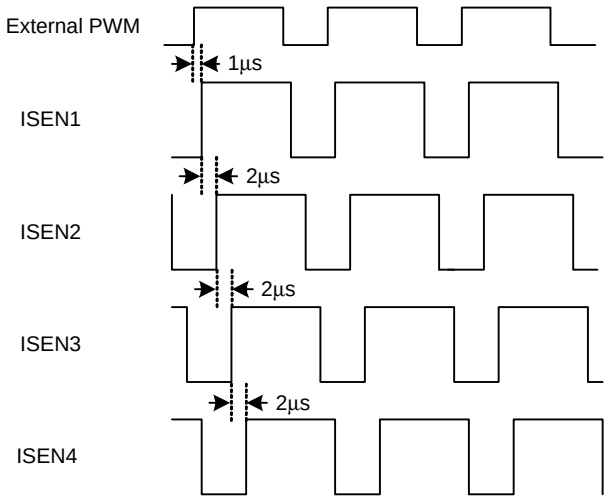



Figure 1. Phase-Shifted

**5V Low Dropout Regulator**

A 5V linear regulator is integrated to supply internal circuit and driver. Because VREF is the LDO output pin, it requires a bypass capacitor of 1µF or more for the regulation. The VREF pin can be used as a coarse reference with 25mA sourcing capability.

**Inrush Current Control and Soft-Start**

The APW7228B integrates independent inrush current control and soft-start functions. When the rising VREF voltage reaches the rising POR voltage threshold, the POR signal goes high and the chip initiates soft-start ope-rations.

During the soft-start, the step-up regulator directly limits the peak inductor current. The current-limit level is increased through the soft-start period from zero up to the full current-limit value in eight equal current steps ($I_{LIM}$/8).

**- Short-Circuit Protection (SCP)**

The APW7228B integrates the LED strings short-circuit protection (SCP) circuit. Such circuit monitors the voltage on each channel. When any channels exceed short-circuit threshold (8.5V typical), the device disable current channels. All the other good channels work normally.

**- Open Circuit Protection (OCP)**

The output voltage of APW7228B is regulated according to the minimum current source voltage on all strings in use. If one or more strings are opened, the respective ISEN are pulled to the GND. If any ISEN is below target current, the corresponding current source is disabled. The unaffected LED strings still operate normally. If all strings are opened, the APW7228B boosts the output voltage of converter high to the OVP threshold.

**- Over-Voltage Protection (OVP)**

When the load is opened, the converter unceasingly boosts the output voltage high. Therefore, an over-voltage protection, monitoring the output voltage via feedback input pin (OVP), is integrated into the chip to prevent the output voltage from exceeding their maximum voltage ratings. When the voltage on the OVP pin exceeds 2V, the converter stops switching and prevents the output voltage from rising. The converter can work again when the falling OVP voltage falls below the OVP voltage threshold. The desired OVP threshold on output voltage can be set as below:

$$OVP=2V \times (1+R_{UPPER}/R_{LOWER})$$

**- Over-Temperature Protection (OTP)**

The over-temperature circuit limits the junction temperature of the APW7228B. When the junction temperature exceeds 150°C, a thermal sensor turns off the power MOSFET, allowing the devices to cool. The thermal sensor allows the converters to start a soft-start process and to regulate the output voltage again after the junction temperature cools by 30°C. The OTP is designed with a 30°C hysteresis to lower the average Junction Temperature ($T_J$) during continuous thermal overload conditions, increasing the lifetime of the device.

## Function Description (Cont.)

**Inrush Current Control and Soft-Start (Cont.)**

**- Output Short-Circuit Protection**

Connecting a fuse component between the VIN and inductor terminals prevents the huge current by the output short to ground. Besides, the APW7228B monitors the voltage on OVP pin to sense output short to ground condition. During start-up, the current injects into output capacitor and then pull $V_{OUT}$ voltage high. If the output is shortened to the ground, and then the OVP pin voltage does not exceed 0.1V after soft-start is completed, the low-side MOSFET is switched off.

**Under-Voltage Lockout**

The Under-Voltage Lockout (UVLO) circuit compares the input voltage at VREF with the UVLO threshold (4.2V, typical) to ensure the input voltage is high enough for reliable operation. The 0.2V (typical) hysteresis prevents supply transients from causing a restart. Once the VREF voltage exceeds the UVLO rising threshold, start-up begins. When the VREF voltage falls below the UVLO falling threshold, the controller turns off the converter.

## Application Information

### Input Capacitor Selection

The input capacitor ($C_{IN}$) reduces the current peaks drawn from the input supply and reduces noise injection into the IC. The reflected ripple voltage will be smaller with larger CIN. For reliable operation, it is recommended to select the capacitor voltage rating at least 1.2 times higher than the maximum input voltage. The capacitors should be placed close to the VIN and GND.

### Inductor Selection

For high efficiencies, the inductor should have a low dc resistance to minimize conduction losses. Especially at high-switching frequencies the core material has a higher impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. A reasonable starting point for setting ripple current, ΔIL, is 30% to 50% of the average inductor current. The recommended inductor value can be calculated as below:

$$L \geq \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \times \frac{V_{OUT} - V_{IN}}{F_{SW} \times I_{OUT(MAX)}} \times \frac{\eta}{\left(\frac{\Delta I_L}{I_{L(AVG)}}\right)}$$

where

$V_{IN}$ = input voltage

$V_{OUT}$ = output voltage

$F_{SW}$ = switching frequency in MHz

$I_{OUT}$ = maximum output current in amp.

$\eta$ = Efficiency

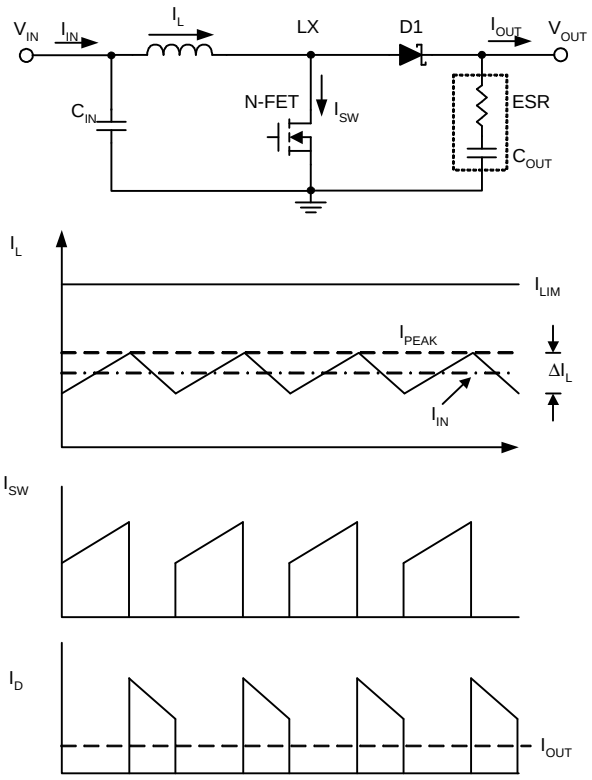
$\Delta I_L / I_{L(AVG)}$ = inductor ripple current/average current (0.3 to 0.5 typical)

To avoid saturation of the inductor, the inductor should be rated at least for the maximum input current of the converter plus the inductor ripple current. The maximum input current is calculated as below:

$$I_{IN(MAX)} = \frac{I_{OUT(MAX)} \times V_{OUT}}{V_{IN} \times \eta}$$

The peak inductor current is calculated as the following equation:

$$I_{PEAK} = I_{IN(MAX)} + \frac{1}{2} \cdot \frac{V_{IN} \cdot (V_{OUT} - V_{IN})}{V_{OUT} \cdot L \cdot F_{SW}}$$




### Output Capacitor Selection

The current-mode control scheme of the APW7228B allows the use of tiny ceramic capacitors. The higher capacitor value provides the good load transients response. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. If required, tantalum capacitors may be used as well. The output ripple is the sum of the voltages across the ESR and the ideal output capacitor.

$$\Delta V_{OUT} = \Delta V_{ESR} + \Delta V_{COUT}$$

$$\Delta V_{COUT} \approx \frac{I_{OUT}}{C_{OUT}} \times \left(\frac{V_{OUT} - V_{IN}}{V_{OUT} \times F_{SW}}\right)$$

$$\Delta V_{ESR} \approx I_{PEAK} \times R_{ESR}$$

where $I_{PEAK}$ is the peak inductor current.

## Application Information (Cont.)

### Output Capacitor Selection (Cont.)

For ceramic capacitor application, the output voltage ripple is dominated by the $\Delta V_{COUT}$. When choosing the input and output ceramic capacitors, the X5R or X7R with their good temperature and voltage characteristics are recommended.

### Diode Selection

To achieve high efficiency, a Schottky diode must be used. The current rating of the diode must meet the peak current rating of the converter.

**Recommended Capacitor Selection**

| Designator | Manufacturer | Part Number | Capacitance (µF) | TC Code | Rated Voltage (V) | Case size |
|---|---|---|---|---|---|---|
| C1 | Murata | GRM31CR71H225KA88K | 2.2 | X7R | 50 | 1206 T=1.6mm |
| C2 | Murata | GRM32ER72A225KA35K | 2.2 | X7R | 100 | 1206 T=1.6mm |
| C3 | Murata | GRM32ER72A225KA35K | 2.2 | X7R | 100 | 1206 T=1.6mm |

**Recommended Diode Selection**

| Designator | Manufacturer | Part Number | Maximum average forward rectified current (A) | Maximum repetitive peak reverse voltage (V) | Case size |
|---|---|---|---|---|---|
| D1 | Zowie | SSCD210SH | 2 | 100 | 1206-S T=3.4mm |

**Recommended MOSFET Selection**

| Designator | Manufacturer | Part Number | Drain-Source Breakdown Voltage (V) | Case size |
|---|---|---|---|---|
| Q1 | ANPEC | APM1101 | 100 | To-252-3 |

### Layout Considerations

For all switching power supplies, the layout is an important step in the design; especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show noise problems and duty cycle jitter.

1. The input capacitor should be placed close to the VIN and GND. Connecting the capacitor with VIN and GND pins by short and wide tracks for filtering and minimizing the input voltage ripple.

2. Place compensation network components closed to SSTCMP pin.

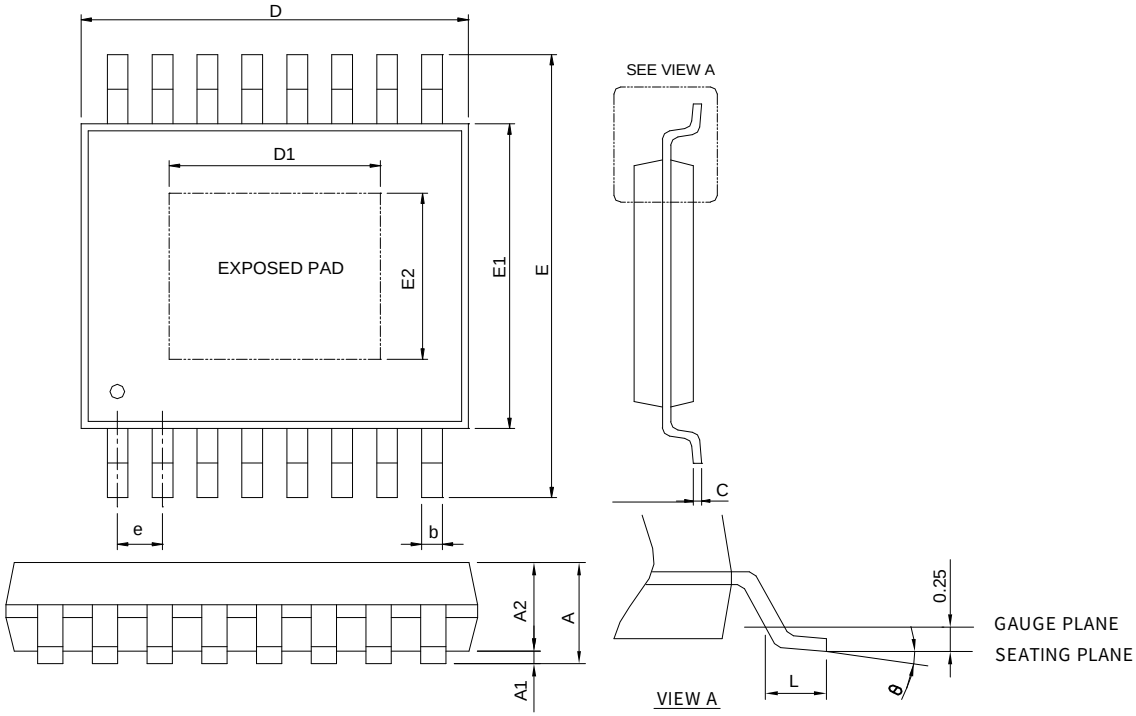
3. Frequency setting Resistor $R_{RT}$, ILED string current setting resistor $R_{ISET}$ and current sensing resistor $R_{ISW}$ should close to the RT, ISET and ISW pins respectively.

4. A star ground connection or ground plane minimizes ground shifts and noise is recommended.

5. Since the VREF voltage is generated for internally supply rail. A 2.2µF or greater ceramic capacitor must be connected as closed as possible to VREF pin for good filtering.

## Package Information

**TSSOP-16P**

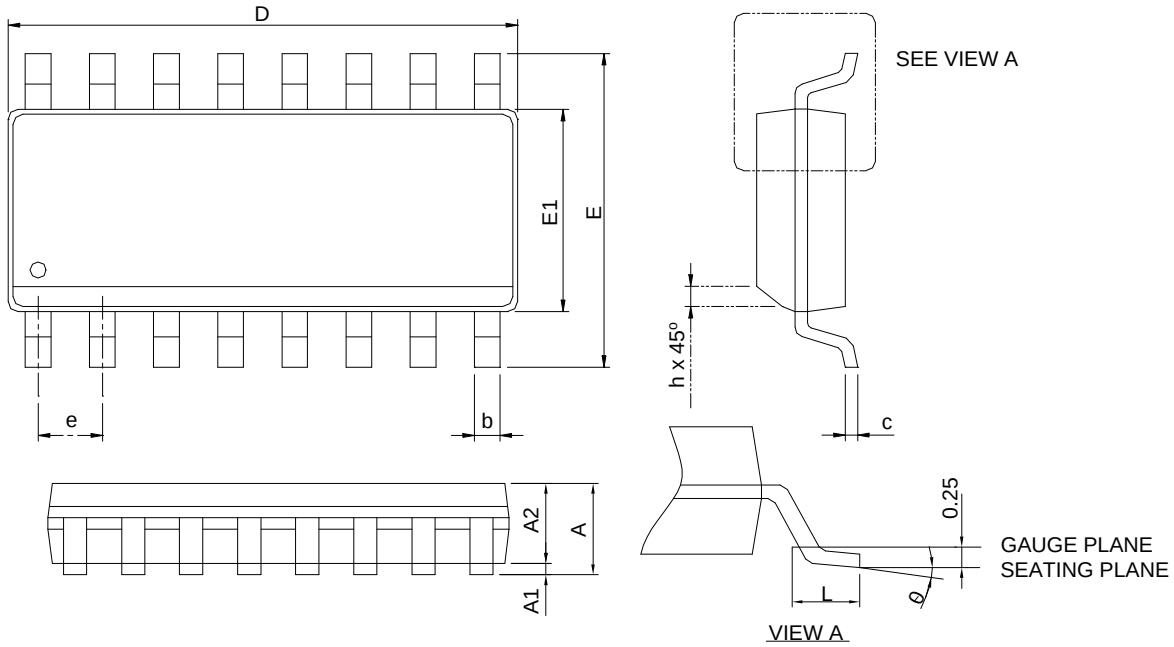



| SYMBOL | TSSOP-16P | | | |
|---|---|---|---|---|
| | MILLIMETERS | | INCHES | |
| | MIN. | MAX. | MIN. | MAX. |
| A | | 1.20 | | 0.047 |
| A1 | 0.05 | 0.15 | 0.002 | 0.006 |
| A2 | 0.80 | 1.05 | 0.031 | 0.041 |
| b | 0.19 | 0.30 | 0.007 | 0.012 |
| c | 0.09 | 0.20 | 0.004 | 0.008 |
| D | 4.90 | 5.10 | 0.193 | 0.201 |
| D1 | 2.00 | 3.50 | 0.079 | 0.138 |
| E | 6.20 | 6.60 | 0.244 | 0.260 |
| E1 | 4.30 | 4.50 | 0.169 | 0.177 |
| E2 | 2.50 | 3.50 | 0.098 | 0.138 |
| e | 0.65 BSC | | 0.026 BSC | |
| L | 0.45 | 0.75 | 0.018 | 0.030 |
| θ | $0^o$ | $8^o$ | $0^o$ | $8^o$ |

Note : 1. Follow from JEDEC MO-153 AB.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension "E1" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

## Package Information

**SOP-16**

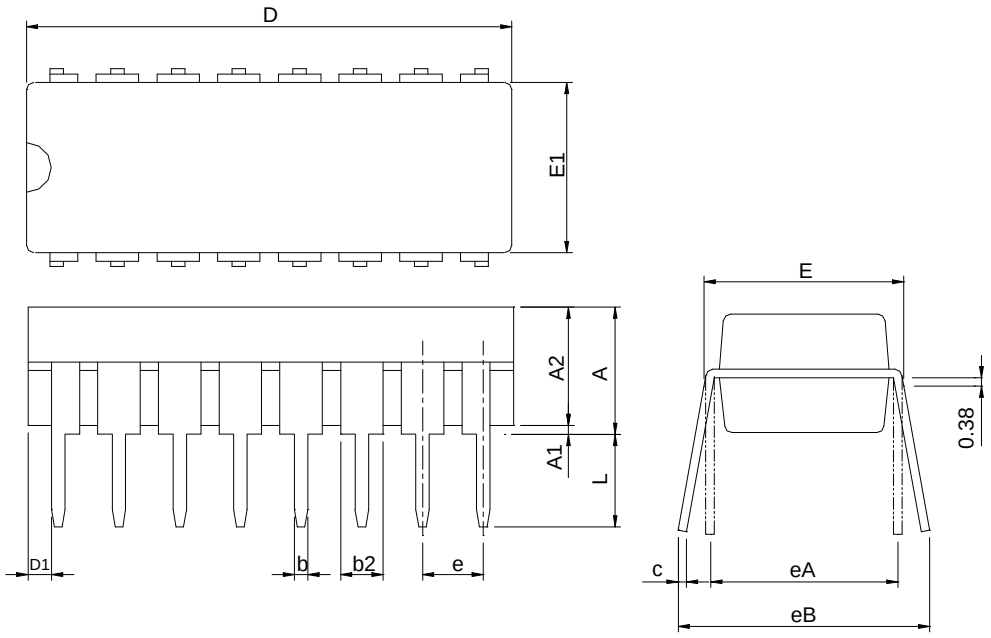



| SYMBOL | SOP-16 | | | |
|---|---|---|---|---|
| | MILLIMETERS | | INCHES | |
| | MIN. | MAX. | MIN. | MAX. |
| A | | 1.75 | | 0.069 |
| A1 | 0.00 | 0.15 | 0.000 | 0.006 |
| A2 | 1.25 | | 0.049 | |
| b | 0.31 | 0.51 | 0.012 | 0.020 |
| c | 0.17 | 0.25 | 0.007 | 0.010 |
| D | 9.80 | 10.00 | 0.386 | 0.394 |
| E | 5.80 | 6.20 | 0.228 | 0.244 |
| E1 | 3.80 | 4.00 | 0.150 | 0.157 |
| e | 1.27 BSC | | 0.050 BSC | |
| h | 0.25 | 0.50 | 0.010 | 0.020 |
| L | 0.40 | 1.27 | 0.016 | 0.050 |
| θ | 0° | 8° | 0° | 8° |

Note : 1. Follow from JEDEC MS-012 AC.
2. Dimension "D" does not include mold flash, protrusions or gate burrs.
Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension "E" does not include inter-lead flash or protrusions.
Inter-lead flash and protrusions shall not exceed 10 mil per side.

## Package Information

**DIP-16**

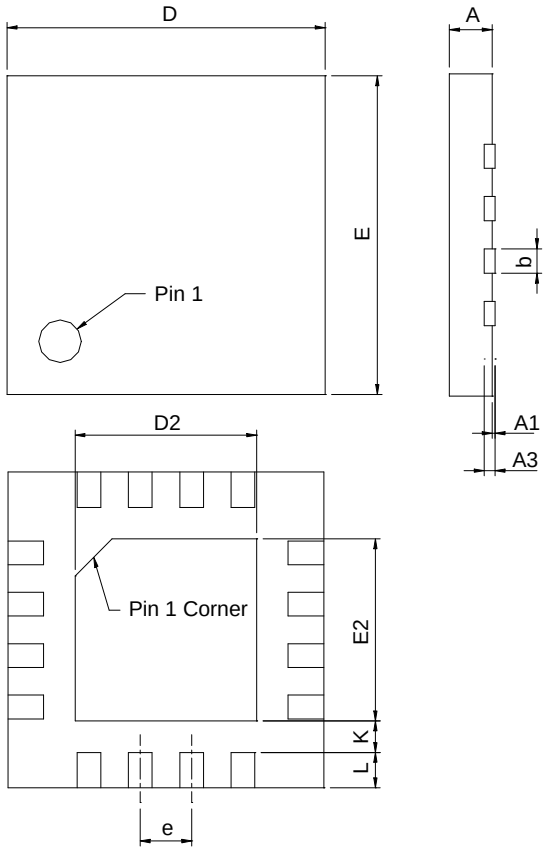



| SYMBOL | DIP-16 | | | |
|---|---|---|---|---|
| | MILLIMETERS | | INCHES | |
| | MIN. | MAX. | MIN. | MAX. |
| A | | 5.33 | | 0.210 |
| A1 | 0.38 | | 0.015 | |
| A2 | 2.92 | 4.95 | 0.115 | 0.195 |
| b | 0.36 | 0.56 | 0.014 | 0.022 |
| b2 | 1.14 | 1.78 | 0.045 | 0.070 |
| c | 0.20 | 0.35 | 0.008 | 0.014 |
| D | 18.6 | 20.31 | 0.732 | 0.800 |
| D1 | 0.13 | | 0.005 | |
| E | 7.62 | 8.26 | 0.300 | 0.325 |
| E1 | 6.10 | 7.11 | 0.240 | 0.280 |
| e | 2.54 BSC | | 0.100 BSC | |
| eA | 7.62 BSC | | 0.300 BSC | |
| eB | | 10.92 | | 0.430 |
| L | 2.92 | 3.81 | 0.115 | 0.150 |

Note : 1. Followed from JEDEC MS-001AB
2. Dimension D, D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 10 mil.

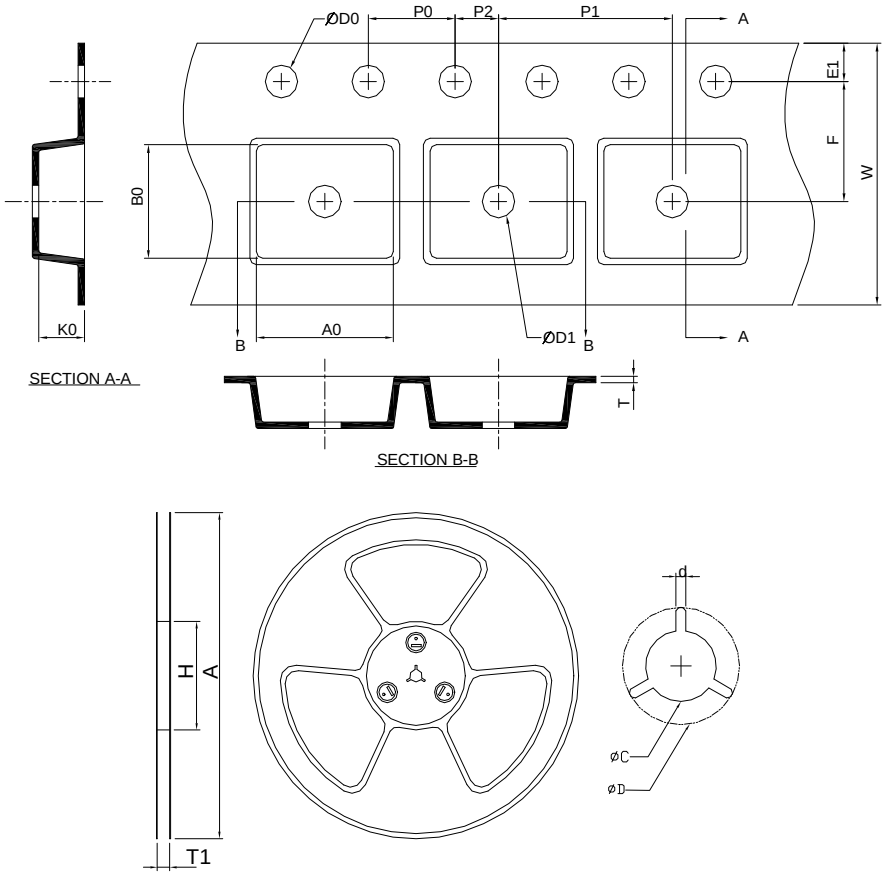
## Package Information

**QFN4x4-16A**




| SYMBOL | QFN4x4-16A | | | |
|---|---|---|---|---|
| | MILLIMETERS | | INCHES | |
| | MIN. | MAX. | MIN. | MAX. |
| A | 0.80 | 1.00 | 0.031 | 0.039 |
| A1 | 0.00 | 0.05 | 0.000 | 0.002 |
| A3 | 0.20 REF | | 0.008 REF | |
| b | 0.25 | 0.35 | 0.010 | 0.014 |
| D | 3.90 | 4.10 | 0.154 | 0.161 |
| D2 | 2.10 | 2.50 | 0.083 | 0.098 |
| E | 3.90 | 4.10 | 0.154 | 0.161 |
| E2 | 2.10 | 2.50 | 0.083 | 0.098 |
| e | 0.65 BSC | | 0.026 BSC | |
| L | 0.30 | 0.50 | 0.012 | 0.020 |
| K | 0.20 | | 0.008 | |

## Carrier Tape & Reel Dimensions




| Application | A | H | T1 | C | d | D | W | E1 | F |
|---|---|---|---|---|---|---|---|---|---|
| TSSOP-16P | 330.0±2.00 | 50 MIN. | 12.4+2.00 -0.00 | 13.0+0.50 -0.20 | 1.5 MIN. | 20.2 MIN. | 12.0±0.30 | 1.75±0.10 | 5.50±0.05 |
| | **P0** | **P1** | **P2** | **D0** | **D1** | **T** | **A0** | **B0** | **K0** |
| | 4.00±0.10 | 8.00±0.10 | 2.00±0.05 | 1.5+0.10 -0.00 | 1.5 MIN. | 0.6+0.00 -0.40 | 6.9±0.20 | 5.40.±0.20 | 1.60±0.20 |
| SOP-16 | **A** | **H** | **T1** | **C** | **d** | **D** | **W** | **E1** | **F** |
| | 330.0±2.00 | 50 MIN. | 16.4+2.00 -0.00 | 13.0+0.50 -0.20 | 1.5 MIN. | 20.2 MIN. | 16.0±0.30 | 1.75±0.10 | 7.5±0.10 |
| | **P0** | **P1** | **P2** | **D0** | **D1** | **T** | **A0** | **B0** | **K0** |
| | 4.0±0.10 | 8.0±0.10 | 2.0±0.10 | 1.5+0.10 -0.00 | 1.5 MIN. | 0.6+0.00 -0.40 | 6.40±0.20 | 10.30±0.20 | 2.10±0.20 |
| QFN4x4-16A | **A** | **H** | **T1** | **C** | **d** | **D** | **W** | **E1** | **F** |
| | 330.0±2.00 | 50 MIN. | 12.4+2.00 -0.00 | 13.0+0.50 -0.20 | 1.5 MIN. | 20.2 MIN. | 12.0±0.30 | 1.75±0.10 | 5.5±0.05 |
| | **P0** | **P1** | **P2** | **D0** | **D1** | **T** | **A0** | **B0** | **K0** |
| | 4.0±0.10 | 8.0±0.10 | 2.0±0.05 | 1.5+0.10 -0.00 | 1.5 MIN. | 0.6+0.00 -0.40 | 4.30±0.20 | 4.30±0.20 | 1.30±0.20 |

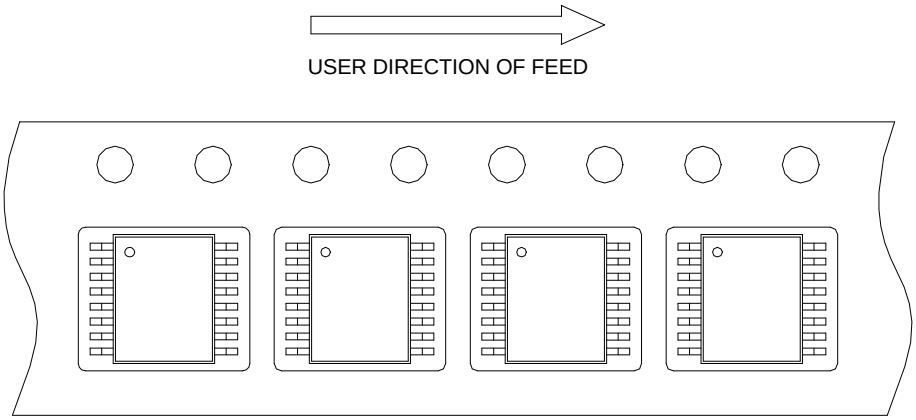
(mm)

## Devices Per Unit

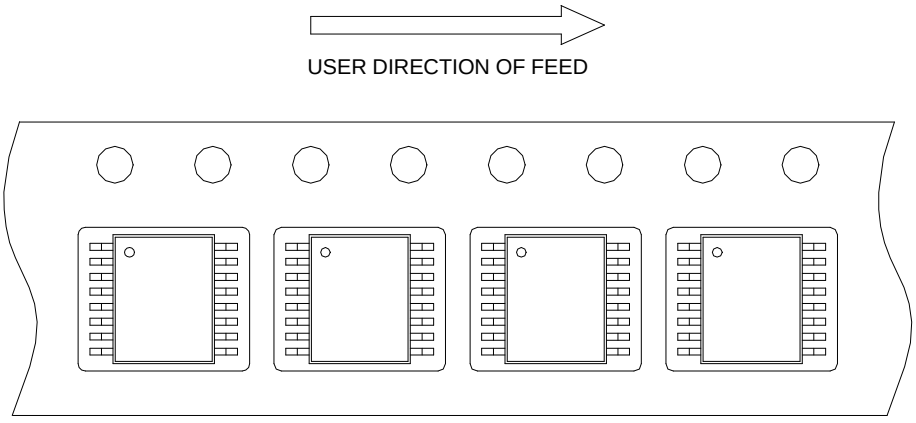
| Package Type | Unit | Quantity |
|---|---|---|
| **TSSOP-16P** | Tape & Reel | 2500 |
| **SOP-16** | Tape & Reel | 2500 |
| **QFN4x4-16A** | Tape & Reel | 3000 |

## Taping Direction Information

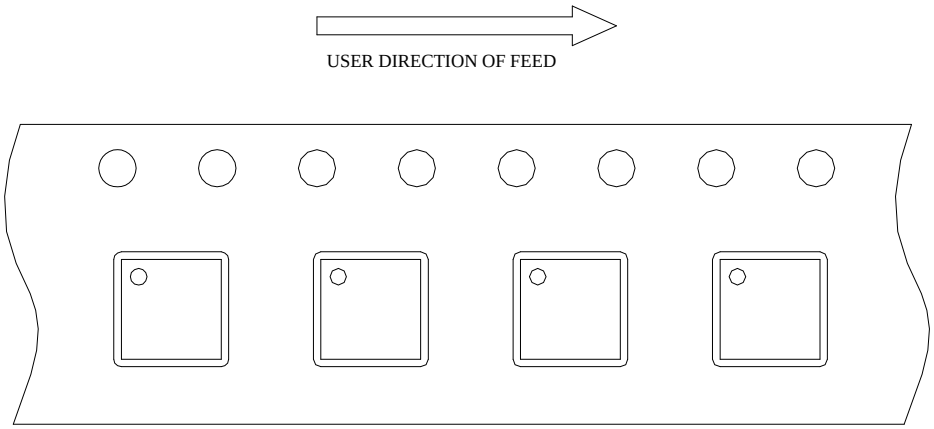
**TSSOP-16P**



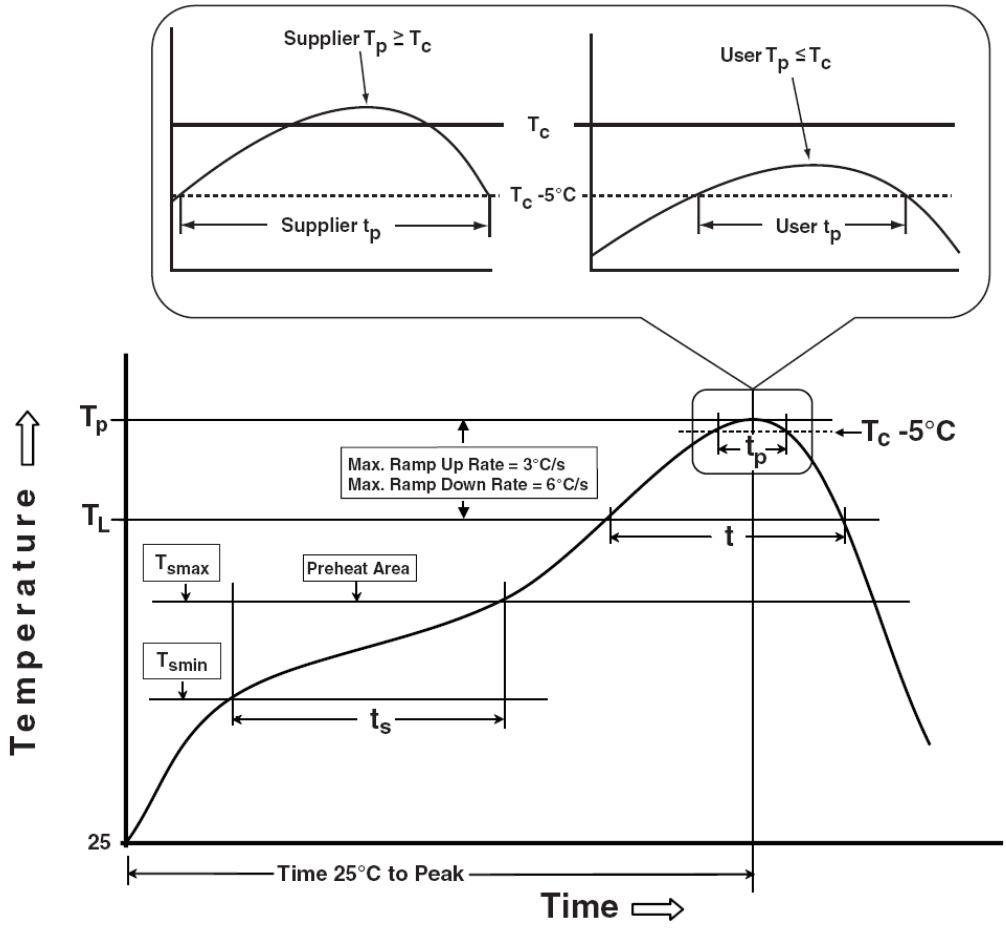

**SOP-16**



**QFN4x4-16A**




## Classification Profile



## Classification Reflow Profiles

| Profile Feature | Sn-Pb Eutectic Assembly | Pb-Free Assembly |
|---|---|---|
| **Preheat & Soak**<br>Temperature min ($T_{smin}$)<br>Temperature max ($T_{smax}$)<br>Time ($T_{smin}$ to $T_{smax}$) ($t_s$) | <br>100 °C<br>150 °C<br>60-120 seconds | <br>150 °C<br>200 °C<br>60-120 seconds |
| Average ramp-up rate ($T_{smax}$ to $T_P$) | 3 °C/second max. | 3°C/second max. |
| Liquidous temperature ($T_L$)<br>Time at liquidous ($t_L$) | 183 °C<br>60-150 seconds | 217 °C<br>60-150 seconds |
| Peak package body Temperature ($T_p$)* | See Classification Temp in table 1 | See Classification Temp in table 2 |
| Time ($t_P$)** within 5°C of the specified classification temperature ($T_c$) | 20** seconds | 30** seconds |
| Average ramp-down rate ($T_p$ to $T_{smax}$) | 6 °C/second max. | 6 °C/second max. |
| Time 25°C to peak temperature | 6 minutes max. | 8 minutes max. |
| * Tolerance for peak profile Temperature ($T_p$) is defined as a supplier minimum and a user maximum.<br>** Tolerance for time at peak profile temperature ($t_p$) is defined as a supplier minimum and a user maximum. | | |

## Classification Reflow Profiles (Cont.)

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

| Package Thickness | Volume $mm^3$ <350 | Volume $mm^3$ ≥350 |
|---|---|---|
| <2.5 mm | 235 °C | 220 °C |
| ≥2.5 mm | 220 °C | 220 °C |

Table 2. Pb-free Process – Classification Temperatures (Tc)

| Package Thickness | Volume $mm^3$ <350 | Volume $mm^3$ 350-2000 | Volume $mm^3$ >2000 |
|---|---|---|---|
| <1.6 mm | 260 °C | 260 °C | 260 °C |
| 1.6 mm – 2.5 mm | 260 °C | 250 °C | 245 °C |
| ≥2.5 mm | 250 °C | 245 °C | 245 °C |

## Reliability Test Program

| Test item | Method | Description |
|---|---|---|
| SOLDERABILITY | JESD-22, B102 | 5 Sec, 245°C |
| HOLT | JESD-22, A108 | 1000 Hrs, Bias @ $T_j$=125°C |
| PCT | JESD-22, A102 | 168 Hrs, 100%RH, 2atm, 121°C |
| TCT | JESD-22, A104 | 500 Cycles, -65°C~150°C |
| HBM | MIL-STD-883-3015.7 | VHBM≧2KV |
| MM | JESD-22, A115 | VMM≧200V |
| Latch-Up | JESD 78 | 10ms, $1_{tr}$≧100mA |

## Customer Service

**Anpec Electronics Corp.**
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