Data Sheet | March 2004 | FN9094.1

Dual Mobile-Friendly PWM Controller with DDR Option

The ISL6227 dual PWM controller delivers high efficiency precision voltage regulation from two synchronous buck DC/DC converters. It was designed especially to provide power regulation for DDR memory, chipsets, graphics and other system electronics in Notebook PCs. The ISL6227's wide input voltage range capability allows for voltage conversion directly from ac/dc adaptor or Li-Ion battery pack.

Automatic mode transition of constant-frequency synchronous rectification at heavy load, and hysteretic (HYS) diode-emulation at light load, assure high efficiency over a wide range of conditions. The HYS mode of operation can be disabled separately on each PWM converter if constant-frequency continuous-conduction operation is desired for all load levels. Efficiency is further enhanced by using the lower MOSFET $r_{DS(ON)}$ as the current sense element.

Voltage-feed-forward ramp modulation, current mode control, and internal feedback compensation provide fast response to input voltage and load transients. Input current ripple is minimized by channel-to-channel PWM phase shift of 0°, 90°, or 180° (determined by input voltage and status of the DDR pin).

The ISL6227 can control two independent output voltages adjustable from 0.9V to 5.5V, or by activating the DDR pin, transform into a complete DDR memory power supply solution. In DDR mode, CH2 output voltage VTT tracks CH1 output voltage VDDQ. CH2 output can both source and sink current, an essential power supply feature for DDR memory. The reference voltage VREF required by DDR memory is generated as well.

In dual power supply applications the ISL6227 monitors the output voltage of both CH1 and CH2. An independent PGOOD (power good) signal is asserted for each channel after the soft-start sequence has completed, and the output voltage is within PGOOD window. In DDR mode CH1 generates the only PGOOD signal.

Built-in overvoltage protection prevents the output from going above 115% of the set point by holding the lower MOSFET on and the upper MOSFET off. When the output voltage re-enters regulation, PGOOD will go HIGH and normal operation automatically resumes. Once the soft-start sequence has completed, undervoltage protection latches the offending channel off if the output drops below 75% of its set point value. Adjustable overcurrent protection (OCP) monitors the voltage drop across the $r_{DS(ON)}$ of the lower MOSFET. If more precise current-sensing is required, an external current sense resistor may be used.

Applications

- Notebook PCs and Desknotes
- Hand-held portable instruments
- Tablet PCs/Slates

Features

- Provides regulated output voltage in the range 0.9V–5.5V
- Operates from an input battery voltage range of 5V to 24V or from 3.3V/5V system rail
- Complete DDR1 and DDR2 memory power solution with VTT tracking VDDQ/2 and a VDDQ/2 buffered reference output
- Flexible PWM or HYS plus PWM mode selection with HYS diode emulation at light loads for higher system efficiency
- $r_{DS(ON)}$ current sensing
- Excellent dynamic response with voltage feed-forward and current mode control accommodating wide range LC filter selections
- Undervoltage lock-out on VCC pin
- Power-good, overcurrent, overvoltage, undervoltage protection for both channels
- Synchronized 300kHz PWM operation in PWM mode
- Pb-Free Available as an Option

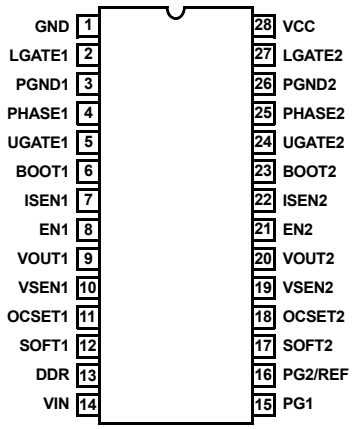
Ordering Information

PART #	TEMP. (°C)	PACKAGE	PKG. DWG. #
ISL6227CA	-10 to 100	28 Ld SSOP	M28.15
ISL6227CAZ (Note)	-10 to 100	28 Ld SSOP (Pb-Free)	M28.15
ISL6227CA-T	-10 to 100	28 Ld SSOP Tape and Reel	M28.15
ISL6227CAZ-T (Note)	-10 to 100	28 Ld SSOP Tape and Reel (Pb-Free)	M28.15

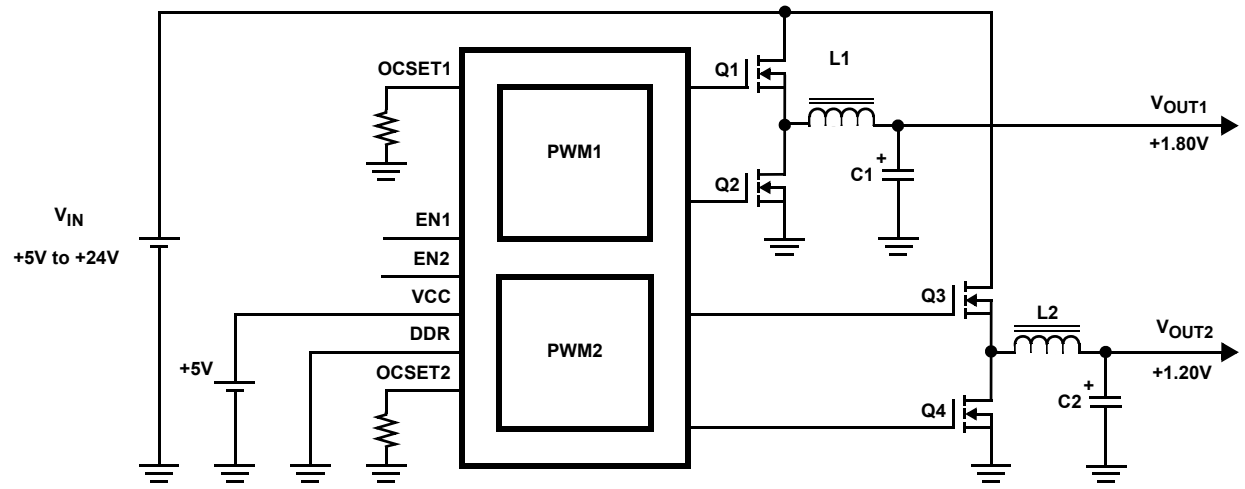
NOTE: Intersil Pb-Free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and Pb-free soldering operations. Intersil Pb-Free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J Std-020B.

Pinout

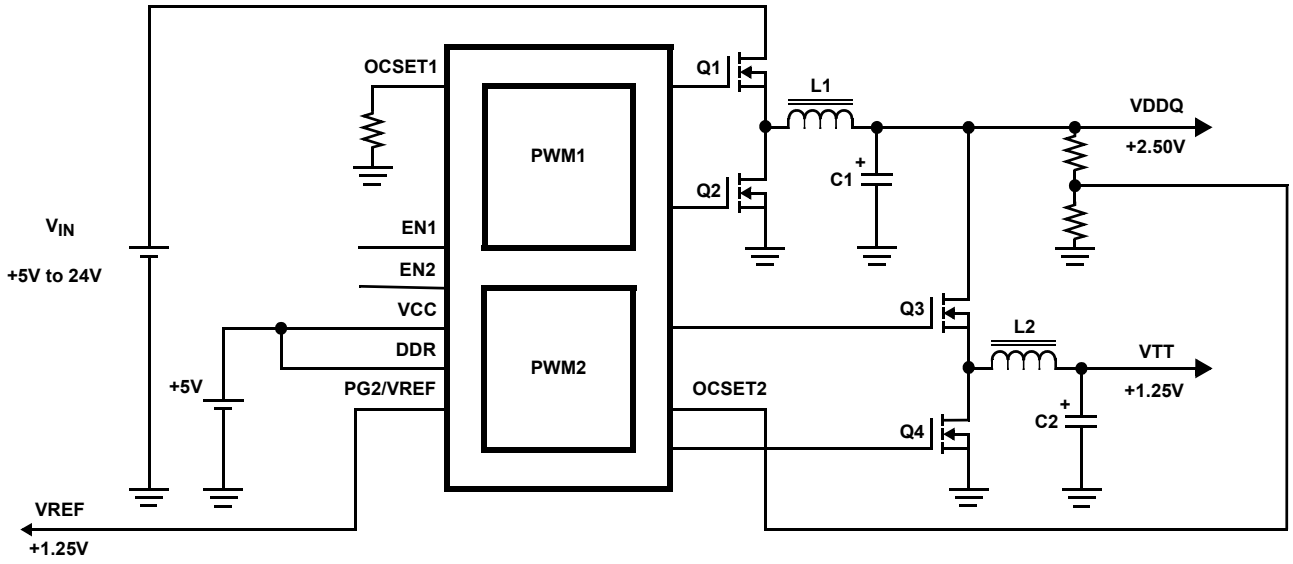
ISL6227 (28 LD SSOP) TOP VIEW



Generic Application Circuits



ISL6227 APPLICATION CIRCUIT FOR TWO CHANNEL POWER SUPPLY



ISL6227 APPLICATION CIRCUIT FOR COMPLETE DDR MEMORY POWER SUPPLY

Absolute Maximum Ratings

Bias Voltage, V_{CC} . . . . . +6.5V
Input Voltage, V_{IN} . . . . . +25.0V
PHASE, UGATE . . . . . GND -5V (Note 1) to 33.0V
BOOT, ISEN . . . . . GND -0.3V to +33.0V
BOOT with respect to PHASE . . . . . + 6.5V
All Other Pins . . . . . GND -0.3V to V_{CC} + 0.3V
ESD Classification . . . . . Class 2

Recommended Operating Conditions

Bias Voltage, V_{CC} . . . . . +5.0V $\pm$ 5%
Input Voltage, V_{IN} . . . . . +5.0V to +24.0V
Ambient Temperature Range . . . . . -10°C to 100°C
Junction Temperature Range . . . . . -10°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
SSOP Package	80

Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SSOP - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. 250ns transient. See Confining The Negative Phase Node Voltage Swing in Application Information Section
2. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY						
Bias Current	I_{CC}	LGATEx, UGATEx Open, VSENx forced above regulation point, V_{IN} > 5V	-	1.8	3.0	mA
Shut-down Current	I_{CCSN}		-	-	1	µA
VCC UVLO						
Rising VCC Threshold	V_{CCU}		4.3	4.45	4.5	V
Falling VCC Threshold	V_{CCD}		4	4.14	4.34	V
V_{IN}						
Input Voltage Pin Current (Sink)	I_{VIN}		-	-	35	µA
Shut-down Current	I_{VINS}		-	-	1	µA
OSCILLATOR						
PWM1 Oscillator Frequency	F_c		255	300	345	kHz
Ramp Amplitude, pk-pk	V_{R1}	V_{IN} = 16V, by design	-	2	-	V
Ramp Amplitude, pk-pk	V_{R2}	V_{IN} = 5V, by design	-	0.625	-	V
Ramp Offset	V_{ROFF}	By design	-	1	-	V
Ramp/V_{IN} Gain	G_{RB1}	$V_{IN} \geq$ 4.2V, by design	-	125	-	mV/V
Ramp/V_{IN} Gain	G_{RB2}	$V_{IN} \leq$ 4.1V by design	-	250	-	mV/V
REFERENCE AND SOFT-START						
Internal Reference Voltage	V_{REF}		-	0.9	-	V
Reference Voltage Accuracy			-1.0	-	+1.0	%
Soft-Start Current During Start-up	I_{SOFT}		-	-4.5	-	µA
Soft-Start Complete Threshold	V_{ST}	By design	-	1.5	-	V

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PWM CONVERTERS						
Load Regulation		0.0mA < I_{VOUT1} < 5.0A; 5.0V < V_{BATT} < 24.0V	-2.0	-	+2.0	%
VSEN pin bias current	I_{VSEN}	By design	-	80	-	nA
Minimum Duty Cycle	D_{min}		-	4	-	%
Maximum Duty Cycle	D_{max}		-	87	-	%
VOUT pin input impedance	I_{VOUT}	VOUT = 5V	-	134	-	kΩ
Undervoltage Shut-Down Level	V_{UVL}	Fraction of the set point; ~2µs noise filter	70	75	80	%
Overvoltage Protection	V_{OVP1}	Fraction of the set point; ~2µs noise filter	110	115	-	%
GATE DRIVERS						
Upper Drive Pull-Up Resistance	R_{2UGPUP}	V_{CC} = 5V	-	4	8	Ω
Upper Drive Pull-Down Resistance	R_{2UGPDN}	V_{CC} = 5V	-	2.3	4	Ω
Lower Drive Pull-Up Resistance	R_{2LGPUP}	V_{CC} = 5V	-	4	8	Ω
Lower Drive Pull-Down Resistance	R_{2LGPDN}	V_{CC} = 5V	-	1.1	3	Ω
POWER GOOD AND CONTROL FUNCTIONS						
Power Good Lower Threshold	V_{PG-}	Fraction of the set point; ~3µs noise filter	84	89	92	%
Power Good Higher Threshold	V_{PG+}	Fraction of the set point; ~3µs noise filter.	110	115	120	%
PGOODx Leakage Current	I_{PGLKG}	V_{PULLUP} = 5.5V	-	-	1	µA
PGOODx Voltage Low	V_{PGOOD}	I_{PGOOD} = -4mA	-	0.5	1	V
ISEN sourcing current		By design	-	-	260	µA
OCSET sourcing current range			2	-	20	µA
EN - Low (Off)			-	-	0.8	V
EN - High (On)			2.0	-	-	V
Continuous-Conduction-Mode(CCM) Enforced (HYS Operation Inhibited)		VOUTX pulled low	-	-	0.1	V
Automatic CCM/HYS Operation Enabled		VOUTX connected to the output	0.9	-	-	V
DDR - Low (Off)			-	-	0.8	V
DDR - High (On)			3	-	-	V
DDR REF Output Voltage	V_{DDREF}	DDR = 1, I_{REF} = 0...10mA	0.99* V_{OC2}	V_{OC2}	1.01* V_{OC2}	V
DDR REF Output Current	I_{DDREF}	DDR = 1. Guaranteed by design.	-	10	12	mA

Typical Operation Performance

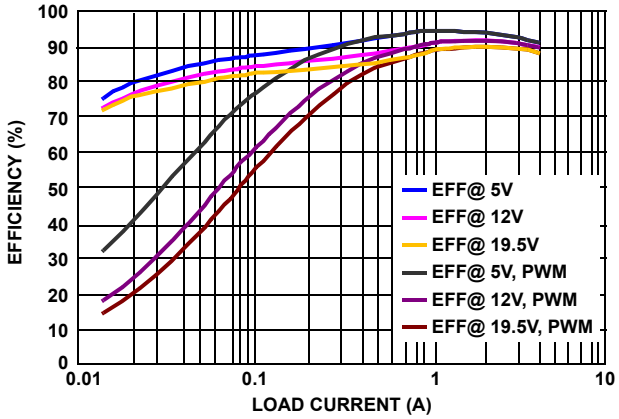


FIGURE 1. EFFICIENCY OF CHANNEL 1, 2.5V, HYS/PWM MODE

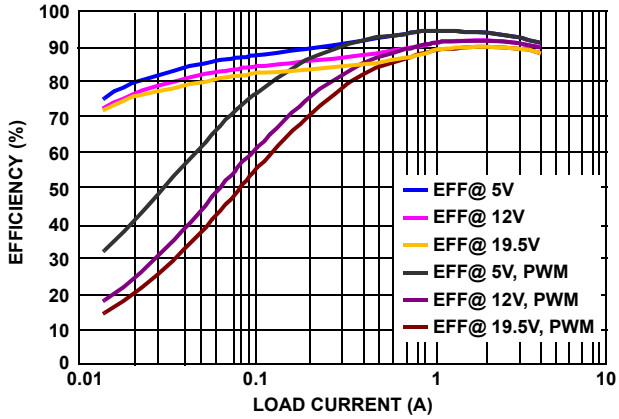


FIGURE 2. EFFICIENCY OF CHANNEL 2, 1.8V, HYS/PWM MODE

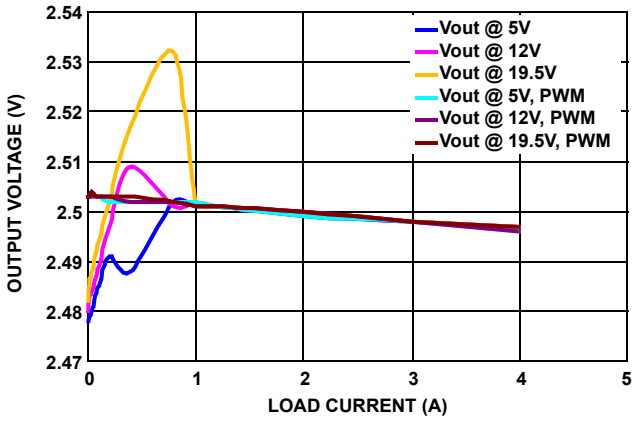


FIGURE 3. OUTPUT VOLTAGE OF CHANNEL 1 vs LOAD

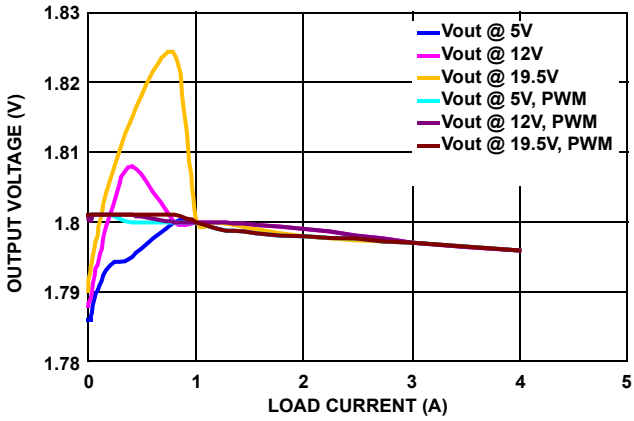


FIGURE 4. OUTPUT VOLTAGE OF CHANNEL 2 vs LOAD

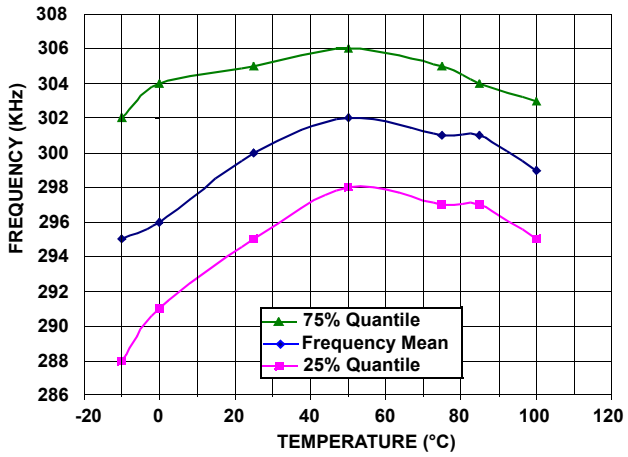


FIGURE 5. SWITCHING FREQUENCY OVER TEMPERATURE

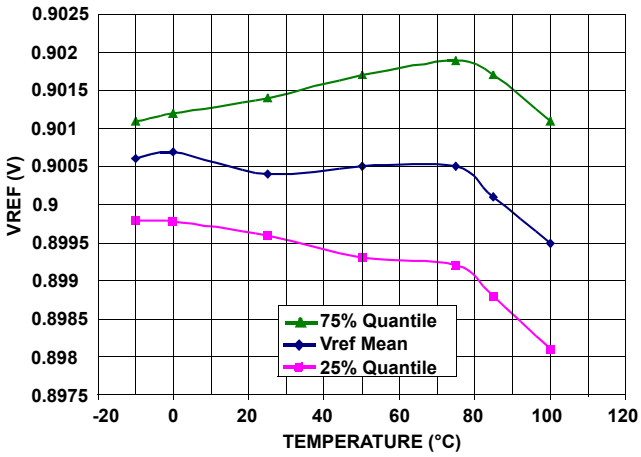


FIGURE 6. REFERENCE VOLTAGE ACCURACY OVER TEMPERATURE

Typical Operation Performance (Continued)

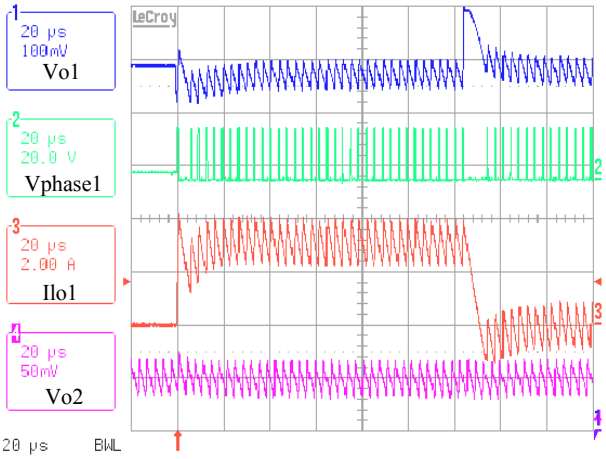


FIGURE 7. LOAD TRANSIENT (0 - 3A AT CHANNEL 1) (DIODE EMULATION MODE)

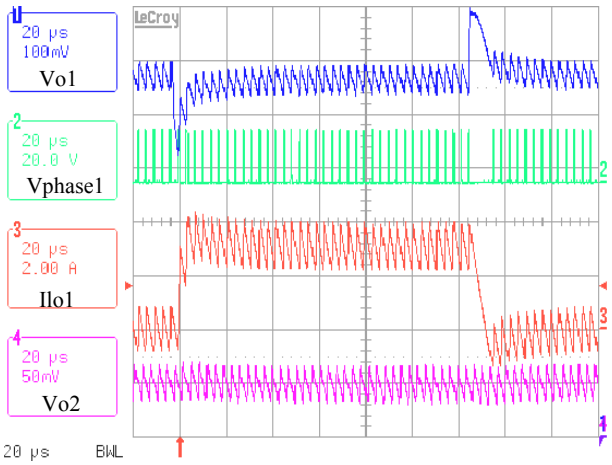


FIGURE 8. LOAD TRANSIENT (0 - 3A AT CHANNEL 1) (FORCED PWM MODE)

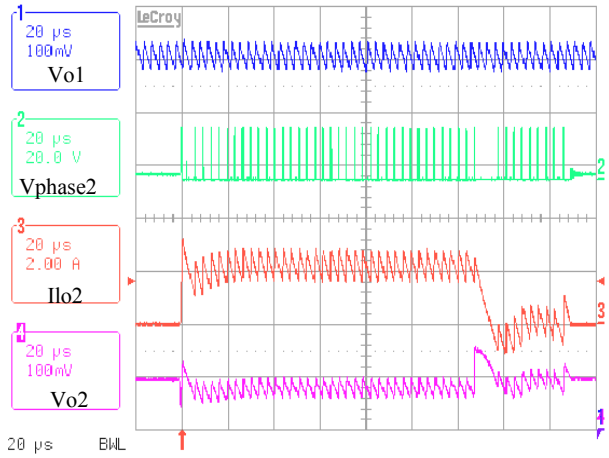


FIGURE 9. LOAD TRANSIENT (0 - 2A AT CHANNEL 2) (DIODE EMULATION MODE)

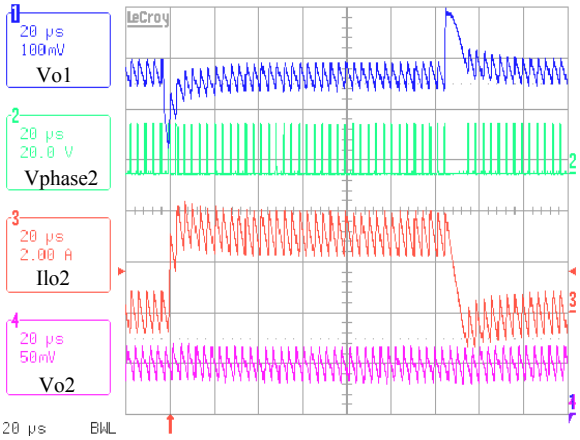


FIGURE 10. LOAD TRANSIENT (0 - 3A AT CHANNEL 2) (FORCED PWM MODE)

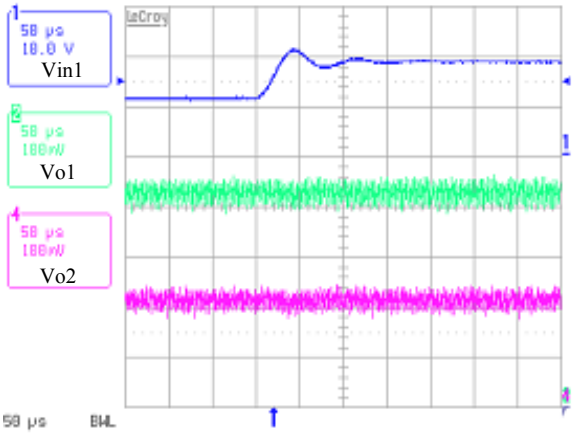


FIGURE 11. INPUT STEP-UP TRANSIENT AT PWM MODE

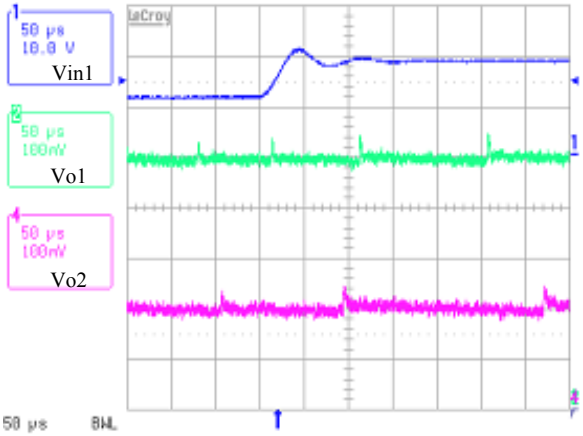


FIGURE 12. INPUT STEP-UP TRANSIENT AT HYS MODE

Typical Operation Performance (Continued)

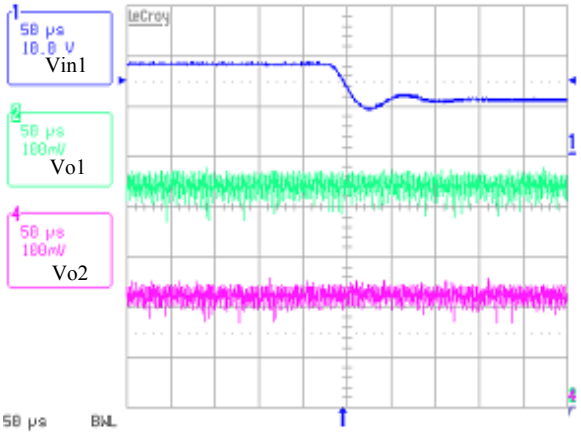


FIGURE 13. INPUT STEP-DOWN TRANSIENT AT PWM MODE

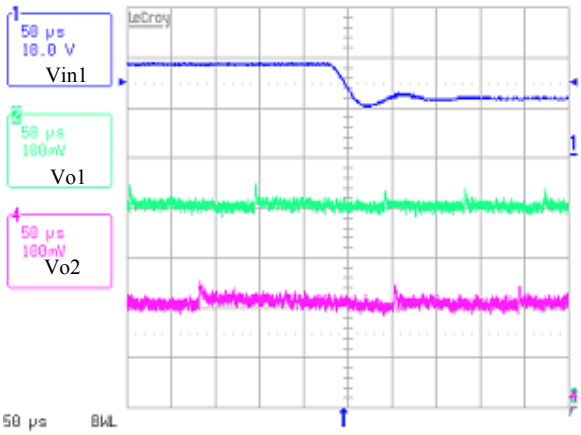


FIGURE 14. INPUT STEP-DOWN TRANSIENT AT HYS MODE

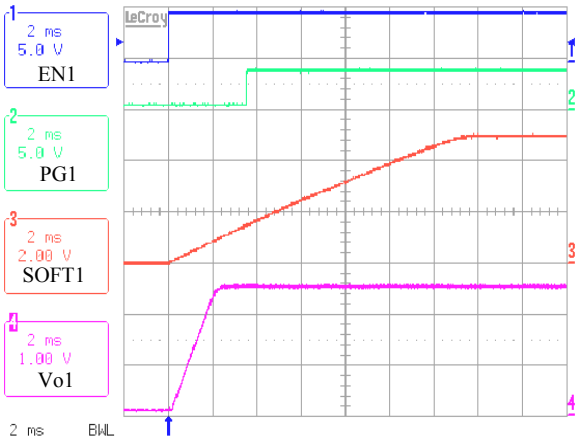


FIGURE 15. SOFT-START INTERVAL AT ZERO INITIAL VOLTAGE OF VO

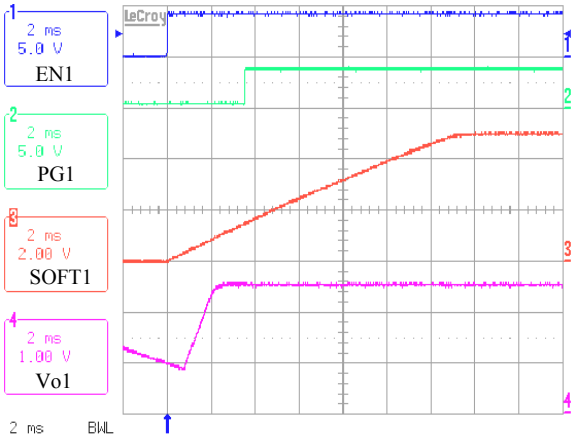


FIGURE 16. SOFT-START INTERVAL WITH NON-ZERO INITIAL VOLTAGE OF VO

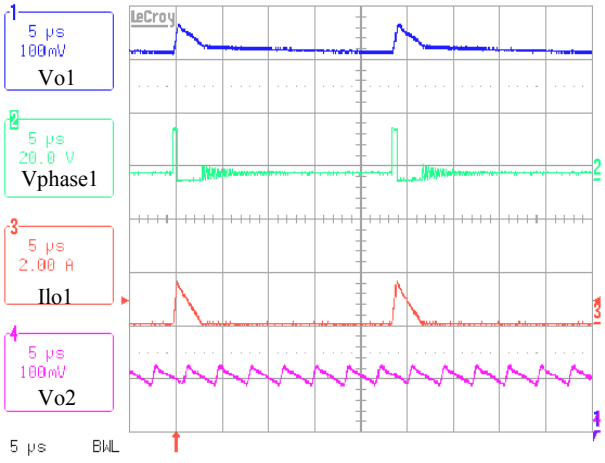


FIGURE 17. OPERATION AT LIGHT LOAD OF 100 MA, CHANNEL 1

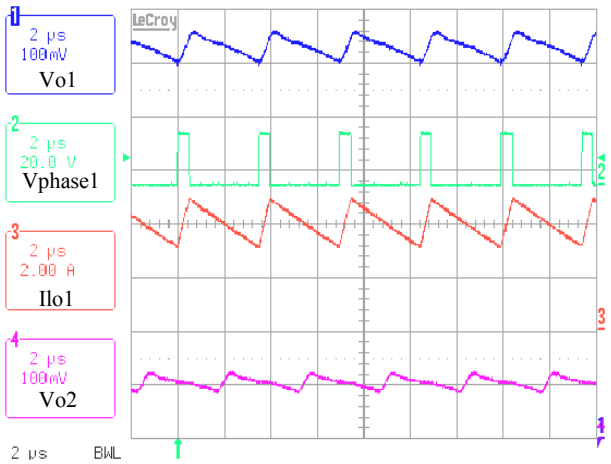


FIGURE 18. OPERATION AT HEAVY LOAD OF 4A, CHANNEL 1

Typical Operation Performance (Continued)

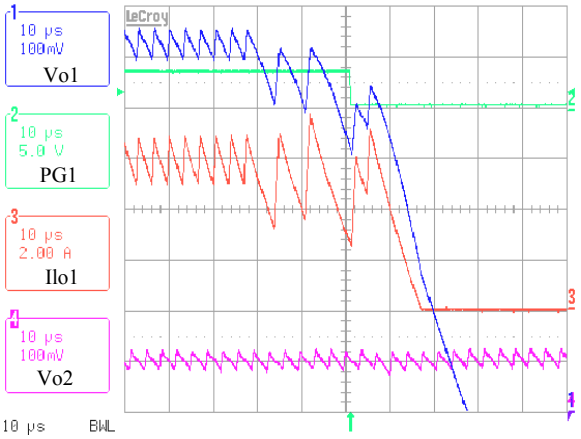


FIGURE 19. OVERCURRENT PROTECTION AT CHANNEL 1

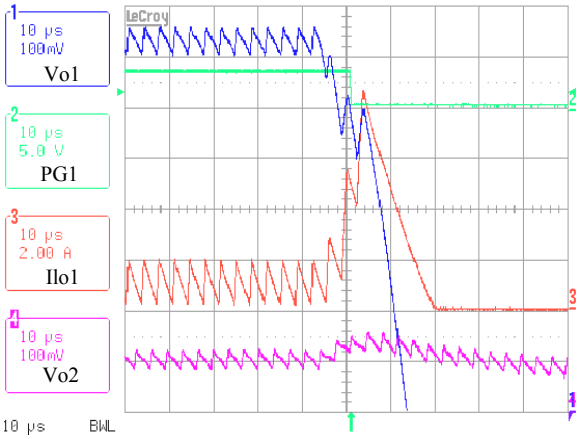


FIGURE 20. SHORT-CIRCUIT PROTECTION AT CHANNEL 1

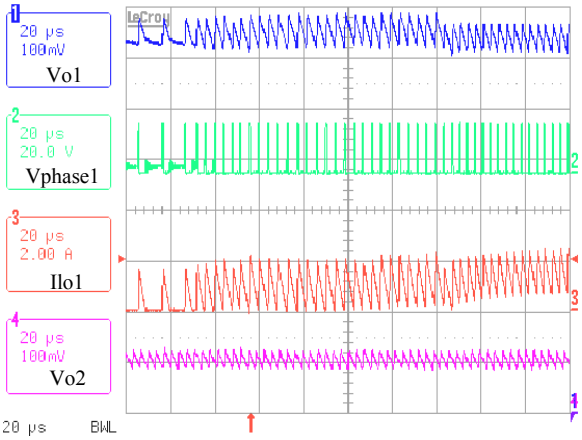


FIGURE 21. MODE TRANSITION OF HYS→ PWM

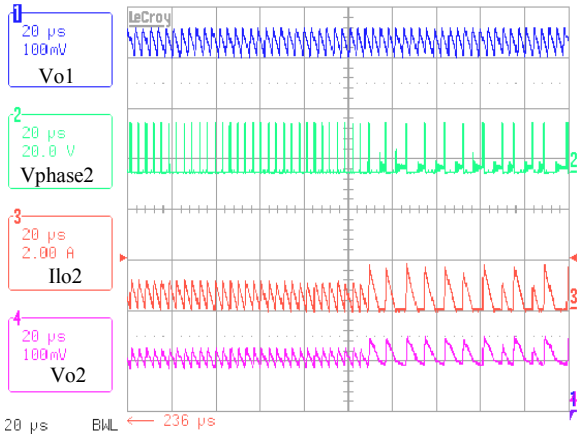


FIGURE 22. MODE TRANSITION OF PWM→ HYS

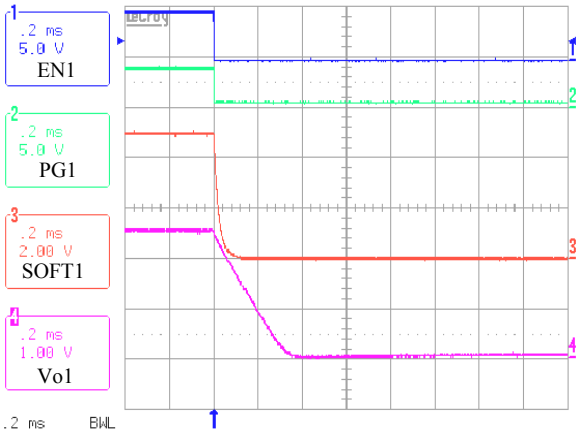


FIGURE 23. SOFT SHUTDOWN INTERVAL

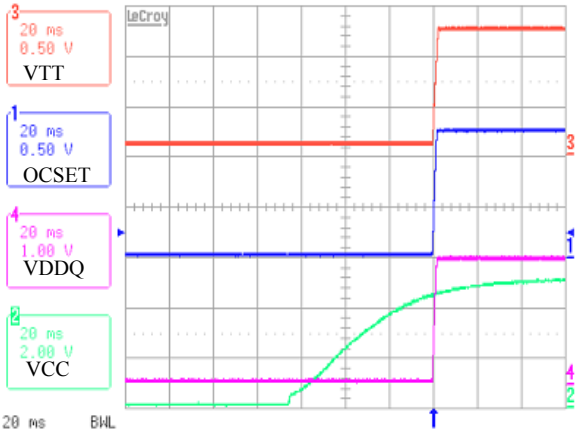


FIGURE 24. V_{CC} POWER UP IN DDR MODE

Typical Operation Performance (Continued)

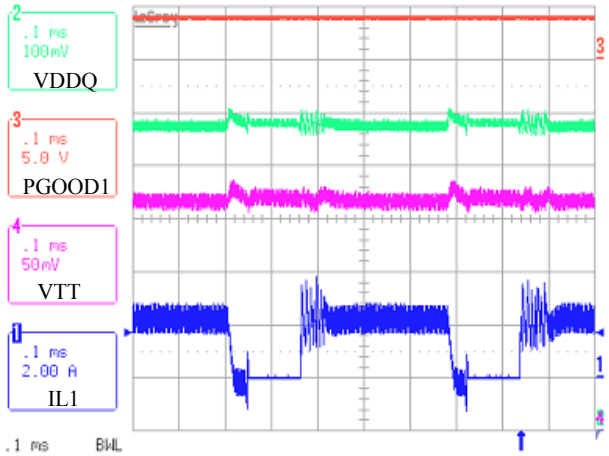


FIGURE 25. VIN = 19V, VDDQ 3A STEP LOAD, VTT 0A LOAD

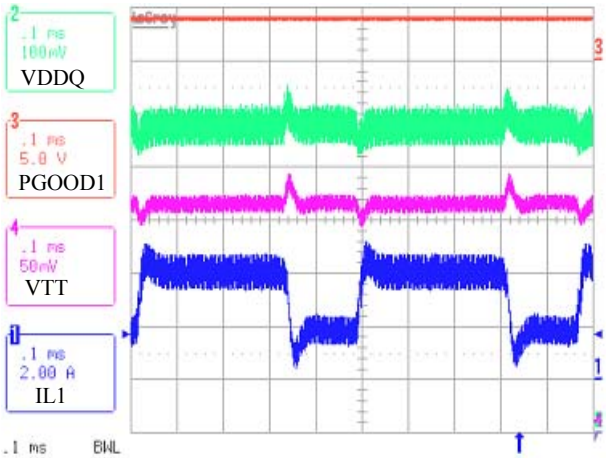


FIGURE 26. VIN = 19V, VDDQ 3A STEP LOAD, VTT 3A LOAD

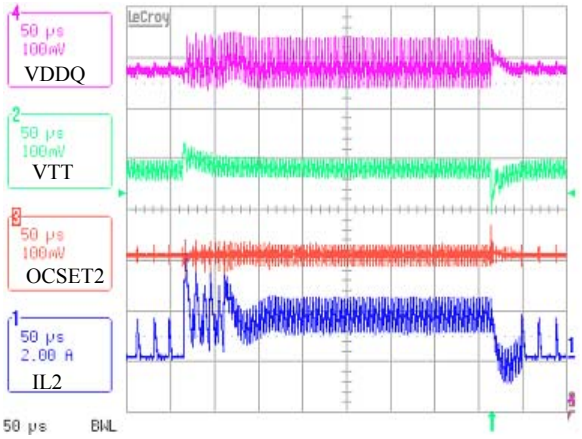


FIGURE 27. VIN = 19V, LOAD STEP ON VTT, VDDQ HYS MODE, 0.14A

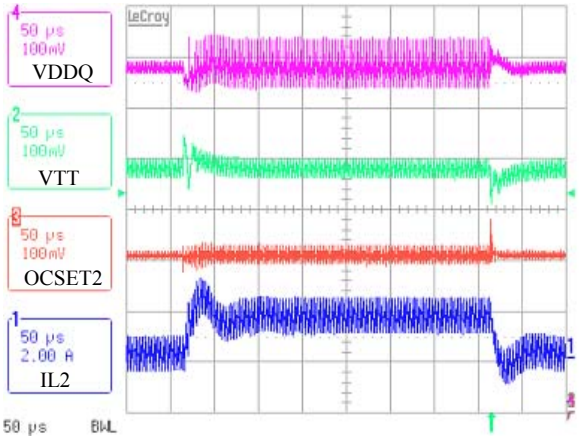


FIGURE 28. VIN = 19V, LOAD STEP ON VTT, VDDQ PWM MODE, 0.14A

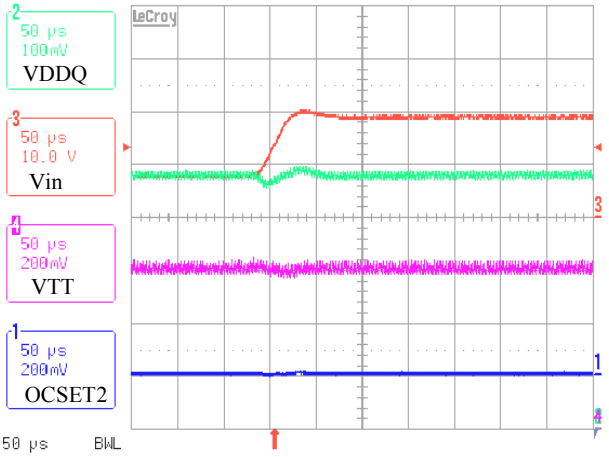


FIGURE 29. INPUT LINE TRANSIENT IN DDR MODE

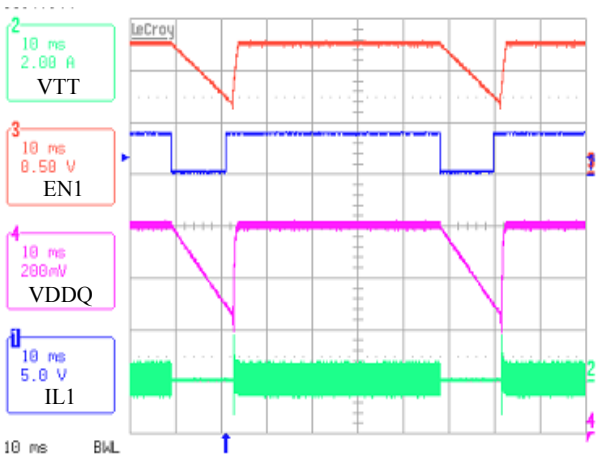


FIGURE 30. VTT FOLLOWS VDDQ, ENABLE 2 IS HIGH

Functional Pin Description

GND (Pin 1)

Signal ground for the IC.

LGATE1, LGATE2 (Pin 2, 27)

These are the outputs of the lower MOSFET drivers.

PGND1, PGND2 (Pin 3, 26)

These pins provide the return connection for lower gate drivers, and are connected to sources of the lower MOSFETs of their respective converters.

PHASE1, PHASE2 (Pin 4, 25)

The PHASE1 and PHASE2 points are the junction points of the upper MOSFET sources, output filter inductors, and lower MOSFET drains. Connect these pins to the respective converter's upper MOSFET source.

UGATE1, UGATE2 (Pin 5, 24)

These pins provide the gate drive for the upper MOSFETs.

BOOT1, BOOT2 (Pin 6, 23)

These pins power the upper MOSFET drivers of the PWM converter. Connect this pin to the junction of the bootstrap capacitor with the cathode of the bootstrap diode. The anode of the bootstrap diode is connected to the VCC voltage.

ISEN1, ISEN2 (Pin 7, 22)

These pins are used to monitor the voltage drop across the lower MOSFET for current feedback and Overcurrent protection. For precise current detection these inputs can be connected to the optional current sense resistors placed in series with the source of the lower MOSFETs.

EN1, EN2 (Pin 8, 21)

These pins enable operation of the respective converter when high. When both pins are low, the chip is disabled and only low leakage current is taken from VCC and VIN. EN1 and EN2 can be used independently to enable either channel 1 or channel 2.

VOUT1, VOUT2 (Pin 9, 20)

These pins, when connected to the converter's respective outputs, set the converter operating in a mixed hysteretic mode or PWM mode, depending on the load conditions. It also provides the voltage to the chip to clamp the PWM error amplifier in hysteretic mode to achieve smooth HYS/PWM transition. When connected to ground, these pins command forced continuous conduction mode (PWM) at all load levels.

VSEN1, VSEN2 (Pin 10, 19)

These pins are connected to the resistive dividers that set the desired output voltage. The PGOOD, UVP, and OVP circuits use this signal to report output voltage status.

OCSET1 (Pin 11)

This pin is a buffered 0.9V internal reference voltage. A resistor from this pin to ground sets the overcurrent threshold for the first controller.

SOFT1, SOFT2 (Pin 12, 17)

These pins provide soft-start function for their respective controllers. When the chip is enabled, the regulated 4.5µA pull-up current source charges the capacitor connected from the pin to ground. The output voltage of the converter follows the ramping voltage on the SOFT pin in the soft-start process with the SOFT pin voltage as reference. When the SOFT pin voltage is higher than 0.9V, the error amplifier will use the internal 0.9V reference to regulate output voltage.

In the event of undervoltage and overcurrent shutdown, the soft-start pin is pulled down though a 2K resistor to ground to discharge the soft-start capacitor.

DDR (Pin 13)

When the DDR pin is low, the chip can be used as a dual switcher controller. The output voltage of the two channels can be programmed independently by VSENx pin resistor dividers. The PWM signals of channel 1 and channel 2 will be synchronized 180 degrees out-of-phase. When the DDR pin is high, the chip transforms into a complete DDR memory solution. The OCSET2 pin becomes an input through a resistor divider tracking to VDDQ/2. The PG2/REF pin becomes the output of the VDDQ/2 buffered voltage. The VDDQ/2 voltage is also used as the reference to the error amplifier by the second channel. The channel phase-shift synchronization is determined by the VIN pin when DDR=1 as described in VIN (Pin 14) below.

VIN (Pin 14)

This pin has multiple functions. When connected to battery voltage, it provides battery voltage to the oscillator as a feed-forward for the rejection of input voltage variation. The ramp of the PWM comparator is proportional to the voltage on this pin (see Table 1 and Table 2 for details). While the DDR pin is high in the DDR application, and when the VIN pin voltage is greater than 4.2 volt when connecting to a battery, it commands 90° out-of-phase channel synchronization, with the second channel lagging the first channel, to reduce inter-channel interference. When the pin voltage is less than 4.2V, this pin commands in-phase channel synchronization.

PG1 (Pin 15)

PGOOD1 is an open drain output used to indicate the status of the output voltage. This pin is pulled low when the first channel output is out of -11% -- +15% of the set value.

PG2/REF (Pin 16)

This pin has a double function, depending on the mode of operation.

When the chip is used as a dual channel PWM controller (DDR = 0), the pin provides an open drain PGOOD2 function for the second channel the same way as PG1. The pin is pulled low when the second channel output is out of -11% -- +15% of the set value.

In DDR mode (DDR=1), this pin is the output of the buffer amplifier that takes VDDQ/2 voltage applied to OCSET2 pin from the resister divider. It can source a typical 10mA current.

OCSET2 (Pin 18)

In a dual channel application with DDR = 0, a resistor from this pin to ground sets the overcurrent threshold for the second channel controller. Its voltage is the buffered internal 0.9V reference.

In the DDR application with DDR=1, this pin connects to the center point of a resistor divider tracking the VDDQ/2. This voltage is then buffered by an amplifier voltage follower and sent to the PG2/REF pin. It sets the reference voltage of channel 2 for its regulation.

VCC (Pin 28)

This pin powers the controller.

Typical Application

Figures 31 and 32 show the application circuits of a dual channel DC/DC converter for a notebook PC.

The power supply in Figure 31 provides +2.5V and +1.8V voltages for memory and the graphics interface chipset from a +5.0-24VDC battery voltage.

Figure 32 illustrates the application circuit for a DDR memory power solution. The power supply shown in Figure 32 generates +2.5V VDDQ voltage from a battery. The +1.25V VTT termination voltage tracks VDDQ/2 and is derived from +2.5V VDDQ. To complete the DDR memory power requirements, the +1.25V reference voltage is provided through the PG2 pin.

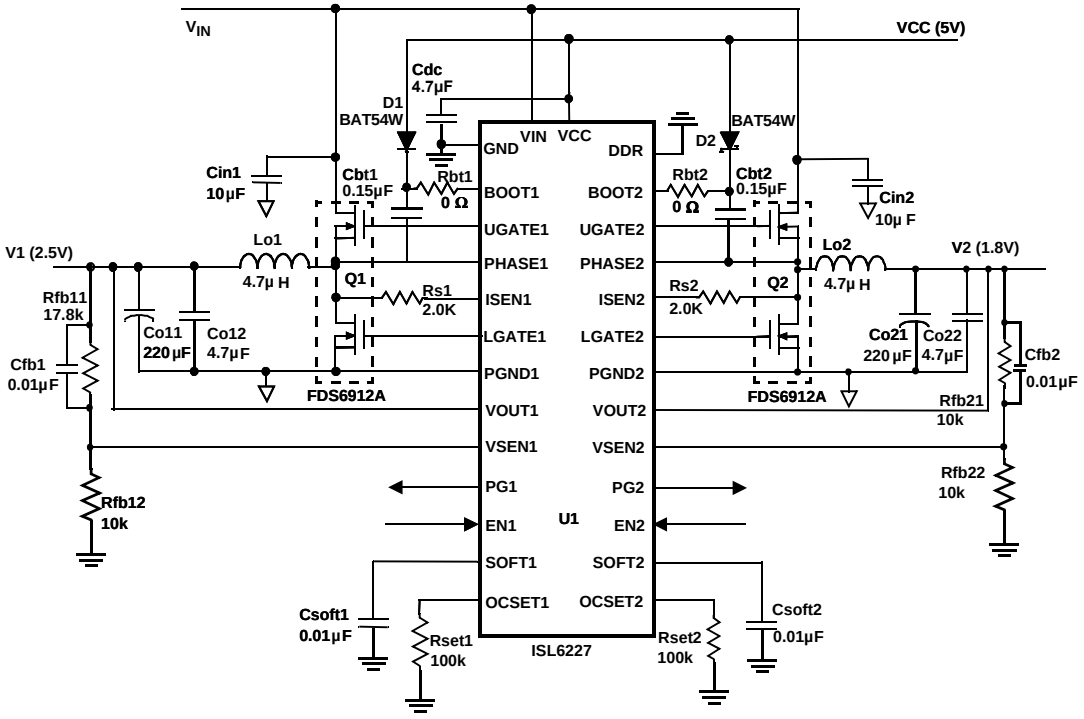


FIGURE 31. TYPICAL APPLICATION CIRCUIT AS DUAL SWITCHER, VOUT1=2.5V, VOUT2=1.8V

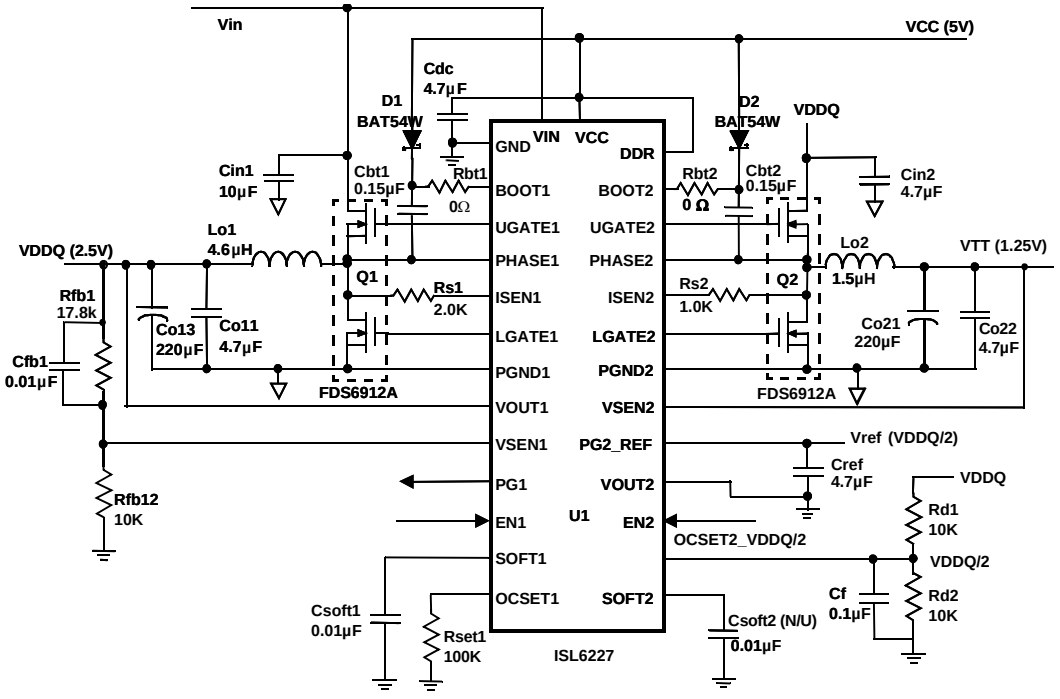
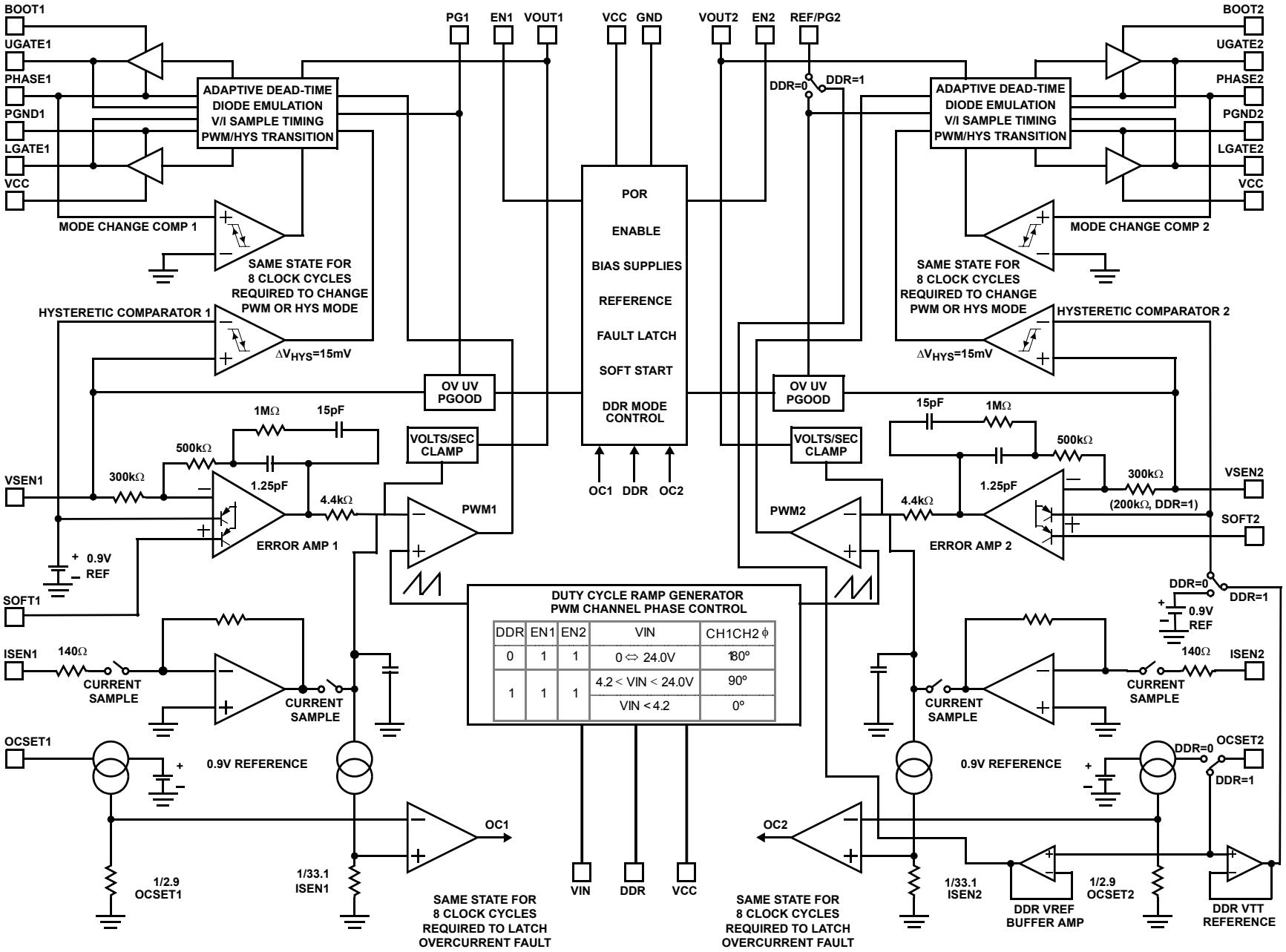


FIGURE 32. TYPICAL APPLICATION AS DDR MEMORY POWER SUPPLY, VDDQ=2.5V, VTT=1.25V

Block Diagram



Theory of Operation

Operation

The ISL6227 is a dual channel PWM controller intended for use in power supplies for graphic chipsets, SDRAM, DDR DRAM, or other low voltage power applications in modern notebook and sub-notebook PCs. The IC integrates two control circuits for two synchronous buck converters. The output voltage of each controller can be set in the range of 0.9V to 5.5V by an external resistive divider.

The synchronous buck converters can operate from either an unregulated DC source, such as a notebook battery, with a voltage ranging from 5.0V to 24V, or from a regulated system rail of 3.3V or 5V. In either operational mode the controller is biased from the +5V source.

The controllers operate in the current mode with input voltage feed-forward which simplifies feedback loop compensation and rejects input voltage variation. An integrated feedback loop compensation dramatically reduces the number of external components.

Depending on the load level, converters can operate either in a fixed 300kHz frequency mode or in a HYS mode. Switch-over to the HYS mode of operation at light loads improves converter efficiency and prolongs battery life. The HYS mode of operation can be inhibited independently for each channel if a variable frequency operation is not desired.

The ISL6227 has a special means to rearrange its internal architecture into a complete DDR solution. When the DDR pin is set high, the second channel can provide the capability to track the output voltage of the first channel. The buffered reference voltage required by DDR memory chips is also provided.

Initialization

The ISL6227 initializes if at least one of the enable pins is set high. The Power-On Reset (POR) function continually monitors the bias supply voltage on the VCC pin, and initiates soft-start operation when EN1 or EN2 is high after the input supply voltage exceeds 4.45V. Should this voltage drop lower than 4.14V, the POR disables the chip.

Soft-Start

When soft-start is initiated, the voltage on the SOFT pin of the enabled channel starts to ramp up gradually with the internal 4.5µA current charging the soft-start capacitor. The output voltage follows the soft-start voltage with the converter operating at 300kHz PWM switching frequency.

When the SOFT pin voltage reaches 0.9V, the output voltage comes into regulation, (see block diagram). When the SOFT voltage reaches 1.5V, the power good (PGOOD) and the mode control is enabled. The soft-start process is depicted in Figure 33.

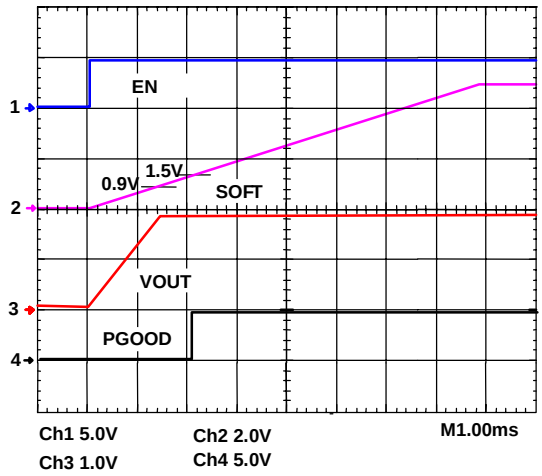


FIGURE 33. START UP

Even though the soft-start pin voltage continues to rise after reaching 1.5V, this voltage does not affect the output voltage. During the soft-start, the converter always operates in continuous conduction mode independent of the load level or VOUT pin connection.

The soft-start time (the time from the moment when EN becomes high to the moment when PGOOD is reported) is determined by the following equation:

$$T_{SOFT} = \frac{1.5V \times Csoft}{4.5\mu A} \quad \text{(EQ. 1)}$$

The time it takes the output voltage to come into regulation can be obtained from the following equation.

$$T_{RISE} = 0.6 \times T_{SOFT} \quad \text{(EQ. 2)}$$

During soft-start stage before the PGOOD pin is ready, the undervoltage protection is prohibited. The overvoltage and overcurrent protection functions are enabled.

If the output capacitor has residue voltage before startup, both lower and upper MOSFETs are in off-state until the soft-start capacitor charges equal the VSEN pin voltage. This will ensure the output voltage starts from its existing voltage level.

Output Voltage Program

The output voltage of either channel is set by a resistive divider from the output to ground. The center point of the divider is connected to the VSEN pin as shown in Figure 34. The output voltage value is determined by the following equation.

$$V_O = \frac{0.9V \bullet (R1 + R2)}{R2} \quad \text{(EQ. 3)}$$

where 0.9V is the value of the internal reference. The VSEN pin voltage is also used by the controller for the power good function and to detect undervoltage and overvoltage conditions.

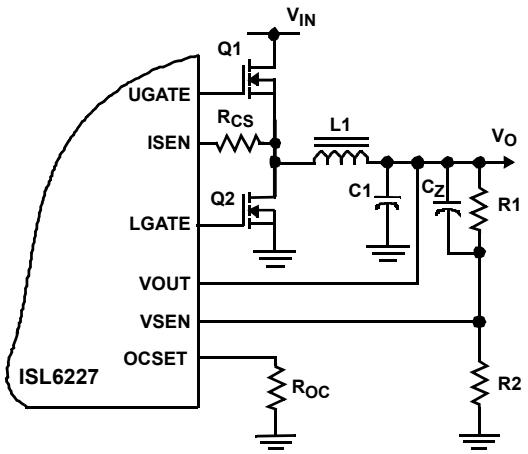


FIGURE 34. OUTPUT VOLTAGE PROGRAM

Operation Mode Control

VOUTx pin programs the two channels of ISL6227 in two different operational modes:

1. If VOUTx is connected to ground, the channel will be put into a fixed switching frequency of 300kHz CCM, also known as forced PWM mode regardless of load conditions.
2. If the VOUTx is connected to the output voltage, the channel will operate in either fixed 300kHz PWM mode or HYS mode, depending on the load conditions. It operates in the PWM mode when the load current exceeds the critical discontinuous conduction value, otherwise it will operate in a HYS mode, as shown in the following table.

VOUT PIN	INDUCTOR CURRENT	OPERATION MODE
GND	Any value	Forced PWM
Connects to output voltage	$\leq I_{HYS}$	HYS
Connects to output voltage	$>I_{HYS1}$	PWM

The two channels can be programmed to operate in different modes depending on the VOUTx connection and the load current. Once both channels operate in the PWM mode, however, they will be synchronized to the 300kHz switching clock. The 180° phase shift reduces the noise couplings between the two channels and reduces the input current ripple.

The critical discontinuous conduction current value for the PWM to HYS mode switch-over can be calculated by the following expression.

$$I_{HYS} = \frac{(V_{IN} - V_O) \bullet V_O}{2 \bullet F_{SW} \bullet L_O \bullet V_{IN}} \quad \text{(EQ. 4)}$$

The HYS mode to PWM switch-over current I_{HYS1} is determined by the activation time of the HYS mode controller. It is affected by the ESR, the inductor value, the input and output voltage.

The HYS mode control can improve converter efficiency with reduced switching frequency. The efficiency is further improved by the diode emulation scheme in discontinuous conduction mode. The diode emulation scheme does not allow the inductor sink current from the output capacitor, thereby reducing the circulating energy. It is achieved by sensing the free-wheeling current going through the synchronous MOSFET through Phase node voltage polarity change after the upper MOSFET is turned off. Before the current reverses direction, the lower MOSFET gate pulses are terminated.

The PWM-HYS and HYS-PWM switch-over is provided automatically by the mode control circuit, which constantly monitors the inductor current through phase voltage polarity, and alters the way the gate driver pulse signal is generated.

Mode Transition

For a buck regulator, if the load current is higher than critical value I_{HYS1}, the voltage drop on the synchronous MOSFET in the free-wheeling period is always negative, and vice versa. The mode control circuit monitors the phase node voltage in the off-period. The polarity of this voltage is used as the criteria for whether the load current is greater than the critical value, and thus determines whether the converter will operate in PWM or HYS mode.

To prevent chatter between operating modes, the circuit looks for eight sequentially matching polarity signals before it decides to perform a mode change. The algorithm is true for both CCM-HYS and HYS-CCM transitions.

In the HYS mode, the PWM comparator and the error amplifier, that provided control in the CCM mode, are put in a clamped stage and the hysteretic comparator is activated. A change is also made to the gate logic. The synchronous MOSFET is controlled in diode emulation fashion, hence the current in the synchronous MOSFET will be kept in one direction only. Figures 35 and 36 illustrate the mode change by counting eight switching cycles.

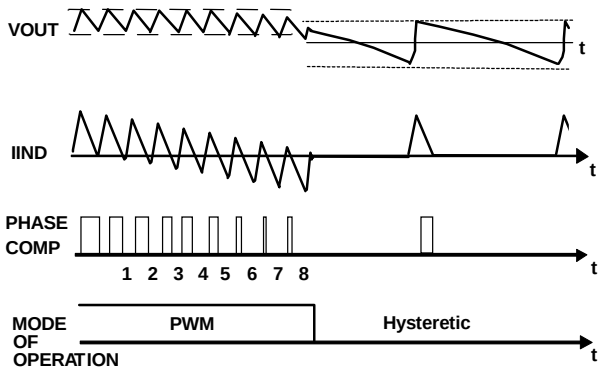


FIGURE 35. CCM—HYSTERETIC TRANSITION

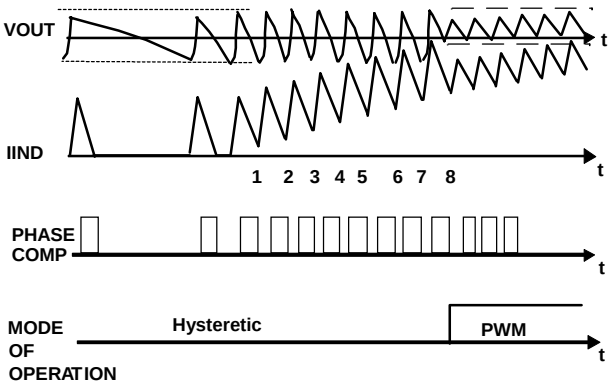


FIGURE 36. HYSTERETIC—CCM TRANSITION

If load current slowly increases or decreases, mode transition will occur naturally, as described above; however, if there is an instantaneous load current increase resulting in a large output voltage drop before the hysteretic mode controller responds, a comparator with threshold of 20mV below the reference voltage will be tripped, and the chip will jump into the forced PWM mode immediately. The PWM controller will process the load transient smoothly.

Once the PWM controller is engaged, 8 consecutive switching cycles of negative inductor current are required to transition back to the hysteretic mode. In this way, chattering between the two modes is prevented. Current sinking during the 8 PWM switching cycle dumps energy to input, smoothing output voltage load step-down.

As a side effect to this design, the comparator may be triggered consistently if the ESR of the capacitor is so big that the output ripple voltage exceeds the 20mV window, resulting in a pure PWM pulse.

The PWM error amplifier is put in clamped voltage during the hysteretic mode. The output voltage through the VOUT pin and the input voltage through the VIN pin are used to determine the error amplifier output voltage and the duty cycle. The error amplifier stays in an armed state while waiting for the transition to occur. The transition decision point is aligned with the PWM clock. When the need for transition is detected, there is a 500ns delay between the first/last pulse of the PWM controller from the last/first pulse of the hysteretic mode controller.

Current Sensing

The current on the lower MOSFET is sensed by measuring its voltage drop within its on-time. In order to activate the current sampling circuitry, two conditions need to be met. (1) the Lgate is high and (2) the phase pin sees a negative voltage for regular buck operation, which means the current is freewheeling through lower MOSFET. For the second channel of the DDR application, the phase pin voltage needs to be higher than 0.1V to activate the current sensing circuit for bidirectional current sensing. The current sampling finishes at about 400ns after the lower MOSFET has turned on. This current information is held for current mode control and overcurrent protection. The current sensing pin can source up to 260µA. The current sense resistor and OCSET resistor can be adjusted simultaneously for the same overcurrent protection level, however, the current sensing gain will be changed only according to the current sense resistor value, which will affect the current feedback loop gain. The middle point of the Isen current can be at 75µA, but it can be tuned up and down to fit application needs.

If another channel is switching at the moment the current sample is finishing, it could cause current sensing error and phase voltage jitter. In the design stage, the duty cycles and synchronization have to be analyzed for all the input voltage and load conditions to reduce the chance of current sensing error. The relationship between the sampled current and MOSFET current is given by:

$$I_{SEN}(R_{CS} + 140) = r_{DS(ON)}\ I_D \qquad \text{(EQ. 5)}$$

Which means the current sensing pin will source current to make the voltage drop on the MOSFET equal to the voltage generated on the sensing resistor, plus the internal resistor, along the ISEN pin current flowing path.

Feedback Loop Compensation

Both channel PWM controllers have internally compensated error amplifiers. To make internal compensation possible several design measures were taken.

- The ramp signal applied to the PWM comparator has been made proportional to the input voltage by the VIN pin. This keeps the product of the modulator gain and the input voltage constant even when the input voltage varies.
- The load current proportional signal is derived from the voltage drop across the lower MOSFET during the PWM off time interval, and is subtracted from the error amplifier output signal before the PWM comparator input. This effectively creates an internal current control loop.

The resistor connected to the ISEN pin sets the gain in the current sensing. The following expression estimates the required value of the current sense resistor, depending on the maximum continuous load current, and the value of the MOSFETs $r_{DS(ON)}$, assuming the ISEN pin sources 75µA current.

$$R_{CS} = \frac{I_{MAX} \bullet r_{DS(ON)}}{75\mu A} - 140\Omega \quad \text{(EQ. 6)}$$

Because the current sensing circuit is a sample-and-hold type, the information obtained at the last moment of the sampling is used. This current sensing circuit samples the inductor current very close to its peak value. The current feedback essentially injects a resistor R_i in series with the original LC filter as shown in Figure 37, where the sample-and-hold effect of the current loop has been ignored. Vc and Vo are small signal components extracted from its DC operation points.

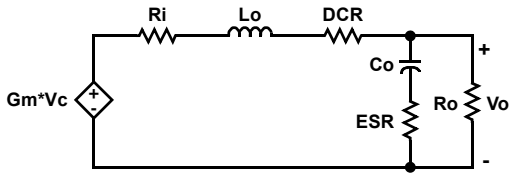


FIGURE 37. THE EQUIVALENT CIRCUIT OF THE POWER STAGE WITH CURRENT LOOP INCLUDED

The value of the injected resistor can be estimated by:

$$R_i = \frac{V_{IN}}{V_{ramp}} \frac{r_{DS(ON)}}{R_{CS} + 140} \bullet 4.4k\Omega \quad \text{(EQ. 7)}$$

R_i is in kΩ, and R_{DS} and R_{CS} are in Ω . V_{IN} divided by V_{ramp}, is defined as Gm, which is a constant 8 or 18 dB for both channels in dual switcher applications, when V_{IN} is above 3V. Refer to Table 1 for the ramp amplitude in different V_{IN} pin connections. The feed-forward effect of the V_{IN} is reflected in Gm. V_c is defined as the error amplifier output voltage.

TABLE 1. PWM COMPARATOR RAMP AMPLITUDE FOR DUAL SWITCHER APPLICATION

	VIN PIN CONNECTIONS		VRAMP AMPLITUDE
Ch1 and Ch2	Input Voltage	Input voltage >4.2V	Vin/8
		Input voltage <4.2V	1.25V
	GND		1.25V

TABLE 2. PWM COMPARATOR RAMP VOLTAGE AMPLITUDE FOR DDR APPLICATION

	VIN PIN CONNECTION		VRAMP AMPLITUDE
Ch1	Input Voltage	Input voltage >4.2V	Vin/8
		Input voltage <4.2V	1.25V
	GND		1.25V
Ch2	Input voltage >4.2V		0.625V
	GND		1.25V

The small signal transfer function from the error amplifier output voltage V_c to the output voltage V_o can be written in the following expression:

$$G(s) = G_m \frac{R_o}{R_i + DCR + R_o} \frac{\left(\frac{s}{Wz} + 1\right)}{\left(\frac{s}{Wp1} + 1\right)\left(\frac{s}{Wp2} + 1\right)} \quad \text{(EQ. 8)}$$

The dc gain is derived by shorting the inductor and opening the capacitor. There is one zero and two poles in this transfer function. The zero is related to ESR and the output capacitor.

The first pole is a low frequency pole associated with the output capacitor and its charging resistors. The inductor can be regarded as short. The second pole is the high frequency pole related to the inductor. At high frequency the output capacitor can be regarded as a short circuit. By approximation, the poles and zero are inversely proportional to the time constants, associated with inductor and capacitor, by the following expressions:

$$Wz = \frac{1}{ESR * C_o} \quad \text{(EQ. 9)}$$

$$Wp1 = \frac{1}{(ESR + (R_i + DCR) \| R_o) * C_o} \quad \text{(EQ.10)}$$

$$Wp2 = \frac{R_i + DCR + ESR \| R_o}{L_o} \quad \text{(EQ.11)}$$

Since the current loop separates the LC resonant poles into two distant poles, and ESR zero tends to cancel the high frequency pole, the second order system behaves like a first order system. This control method simplifies the design of the internal compensator and makes it possible to accommodate many applications having a wide range of parameters.

The schematics for the internal compensator is shown in Figure 38.

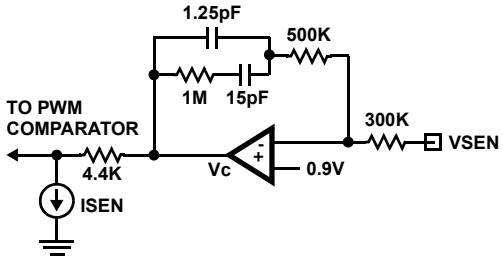


FIGURE 38. THE INTERNAL COMPENSATOR

Its transfer function can be written as the following:

$$Gcomp(s) = \frac{1.857 \bullet 10^5\left(\frac{s}{2\pi f_{z1}} + 1\right)\left(\frac{s}{2\pi f_{z2}} + 1\right)}{s\left(\frac{s}{2\pi f_{p1}} + 1\right)} \quad \text{(EQ.12)}$$

where

f_{z1}=6.98kHz, f_{z2}=380kHz, and f_{p1}=137kHz

Outside the ISL6227 chip, a capacitor C_z can be placed in parallel with the top resistor in the feedback resistor divider, as shown in Figure 34. In this case the transfer function from the output voltage to the middle point of the divider can be written as:

$$Gfd(s) = \frac{R_2}{R_1 + R_2}\frac{sR_1C_z + 1}{s(R_1 \parallel R_2)C_z + 1} \quad \text{(EQ.13)}$$

The ratio of R_1 and R_2 is determined by the output voltage set point; therefore, the position of the pole and zero frequency in the above equation may not be far apart; however, they can improve the loop gain and phase margin with the proper design.

The C_z can bring the high frequency transient output voltage variation directly to the VSEN pin to cause the PGOOD drop. Such an effect should be considered in the selection of C_z.

From the analysis above, the system loop gain can be written as:

$$Gloop(s) = G(s) \bullet Gcomp(s) \bullet Gfd(s) \quad \text{(EQ.14)}$$

Figure 39 shows the composition of the system loop gain. As shown in the graph, the power stage becomes a well damped second order system as compared to the LC filter characteristics. The ESR zero is so close to the high frequency pole that they cancel each other out. The power stage behaves like a first order system. With an internal compensator, the loop gain transfer function has a cross over frequency at about 30kHz. With a given set of parameters, including the MOSFET $r_{DS(ON)}$, current sense resistor R_{CS}, output LC filter, and voltage feedback network, the system loop gain can be accurately analyzed and modified by the system designers based on the application requirements.

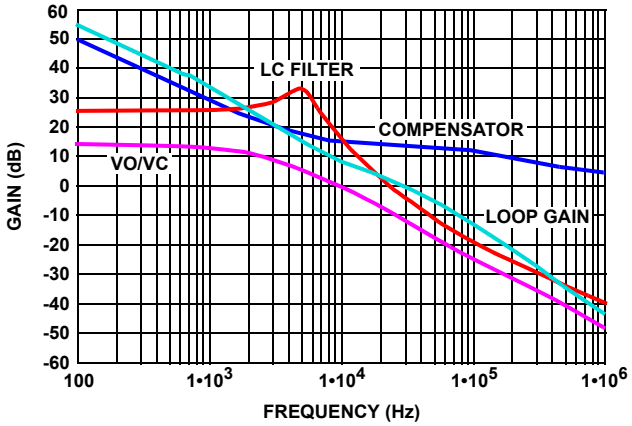


FIGURE 39. THE BODE PLOT OF THE LC FILTER, COMPENSATOR, CONTROL TO OUTPUT VOLTAGE TRANSFER FUNCTION, AND SYSTEM LOOP GAIN

Gate Control Logic

The gate control logic translates generated PWM signals into gate drive signals providing necessary amplification, level shift, and shoot-through protection. It bears some functions that help to optimize the IC performance over a wide range of the operational conditions. As MOSFET switching time can vary dramatically from type to type, and with the input voltage, the gate control logic provides adaptive dead time by monitoring real gate waveforms of both the upper and the lower MOSFETs.

Dual-Step Conversion

The ISL6227 dual channel controller can be used either in power systems with a single-stage power conversion, when the battery power is converted into the desired output voltage in one step, or in the systems where some intermediate voltages are initially established. The choice of the approach may be dictated by the overall system design criteria, or the approach may be a matter of voltages available to the system designer, as in the case of PCI card applications.

When the output voltage is regulated from low voltage such as 5V, the feed-forward ramp may become too shallow, creating the possibility of duty-factor jitter; this is particularly relevant in a noisy environment. Noise susceptibility, when operating from low level regulated power sources, can be improved by connecting the VIN pin to ground, by which the feed-forward ramp generator will be internally reconnected from the VIN pin to the VCC pin, and the ramp slew rate will be doubled.

Voltage Monitor and Protections

The converter output is monitored and protected against extreme overload, short circuit, overvoltage, and undervoltage conditions. A sustained overload on the output sets the PGOOD low and latches off the offending channel of the chip. The controller operation can be restored by cycling the VCC voltage or toggling both enable (EN) pins to low to clear the latch.

Power Good

In the soft-start process, the PGOOD is established after the soft pin voltage is at 1.5V. In normal operation, the PGOOD window is 100mV below the 0.9V and 135mV higher than 0.9V. The VSEN pin has to stay within this window for PGOOD to be high. Since the VSEN pin is used for both feedback and monitoring purposes, the output voltage deviation can be coupled directly to the VSEN pin by the capacitor in parallel with the voltage divider as shown in Figure 4. In order to prevent false PGOOD drop, capacitors need to parallel at the output to confine the voltage deviation with severe load step transient. The PGOOD comparator has a built-in 3µs filter. PGOOD is an open drain output.

Overcurrent Protection

In dual switcher application, both PWM controllers use the lower MOSFETs on-resistance $r_{DS(ON)}$, to monitor the current for protection against shorted outputs. The sensed current from the ISEN pin is compared with a current set by a resistor connected from the OCSET pin to ground:

$$R_{SET} = \frac{10.3V}{\frac{I_{OC} \bullet r_{DS(ON)}}{R_{CS} + 140\Omega} + 8\mu A} \quad \text{(EQ.15)}$$

where, I_{OC} is a desired overcurrent protection threshold and R_{CS} is the value of the current sense resistor connected to the ISEN pin. The 8µA is the offset current added on top of the sensed current from the ISEN pin for internal circuit biasing.

If the lower MOSFET current exceeds the overcurrent threshold, a pulse skipping circuit is activated. The upper MOSFET will not be turned on as long as the sensed current is higher than the threshold value, limiting the current supplied by the DC voltage source. The current in the lower MOSFET will be continuously monitored until it is lower than the OC threshold value, then the following UGATE pulse will be released and normal current sample resumes. This kind of operation remains for eight clock cycles after the overcurrent comparator was tripped for the first time. If after the first eight clock cycles the current exceeds the overcurrent threshold again, in a time interval of another eight clock cycles, the overcurrent protection latches and disables the offending channel. If the overcurrent condition goes away during the first eight clock cycles, normal operation is restored and the overcurrent circuit resets itself at the end of sixteenth clock cycles; see Figure 40.

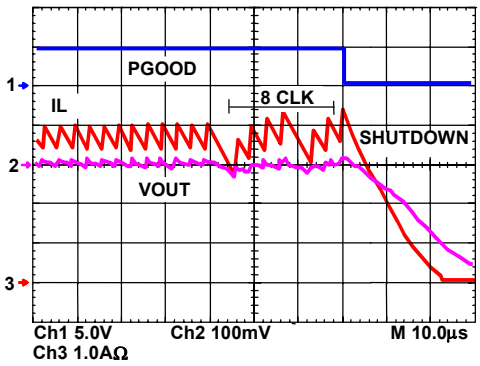


FIGURE 40. OVERCURRENT PROTECTION

Due to the nature of the used current sensing technique, and to accommodate a wide range of the $r_{DS(ON)}$ variation, the value of the overcurrent threshold should set at about 180% of the nominal load value. If more accurate current protection is desired, a current sense resistor placed in series with the lower MOSFET source may be used. The inductor current going through the lower MOSFET is sensed and held at 400ns after the upper MOSFET is turned off; therefore, the sensed current is very close to its peak value. The inductor peak current can be written as:

$$I_{peak} = \frac{(V_{IN} - V_o) \bullet V_o}{2L_o \bullet F_{SW} \bullet V_{IN}} + I_{load} \quad \text{(EQ.16)}$$

As seen from the equation above, the inductor peak current changes with the input voltage and the inductor value once an output voltage is selected.

After overcurrent protection is activated, there are two ways to bring the offending channel back: (1) Both EN1 and EN2 have to be held low to clear the latch, (2) To recycle the Vcc of the chip, the POR will clear the latch.

Undervoltage Protection

In the process of operation, if a short circuit occurs, the output voltage will drop quickly. Before the overcurrent protection circuit responds, the output voltage will fall out of the required regulation range. The chip comes with undervoltage protection. If a load step is strong enough to pull the output voltage lower than the undervoltage threshold, the offending channel latches off immediately. The undervoltage threshold is 75% of the nominal output voltage. Toggling both pins to low, or recycling Vcc, will clear the latch and bring the chip back to operation.

Overvoltage Protection

Should the output voltage increase over 115% of the normal value due to the upper MOSFET failure, or for other reasons, the overvoltage protection comparator will force the synchronous rectifier gate driver high. This action actively pulls down the output voltage and eventually attempts to blow the battery fuse. As soon as the output voltage is within regulation, the OVP comparator is disengaged. The MOSFET driver will restore its normal operation. When the OVP occurs, the PGOOD will drop to low as well.

This OVP scheme provides a 'soft' crowbar function, which helps clamp the voltage overshoot, and does not invert the output voltage when otherwise activated with a continuously high output from lower MOSFET driver - a common problem for OVP schemes with a latch.

DDR Application

High throughput Double Data Rate (DDR) memory ICs are replacing traditional memory ICs in the latest generation of Notebook PCs and in other computing devices. A novel feature associated with this type of memory are the referencing and data bus termination techniques. These techniques employ a reference voltage, VREF, that tracks the center point of VDDQ and VSS voltages, and an additional VTT power source where all terminating resistors are connected. Despite the additional power source, the overall memory power consumption is reduced compared to traditional termination.

The added power source has a cluster of requirements that should be observed and considered. Due to the reduced differential thresholds of DDR memory, the termination power supply voltage, VTT, closely tracks VDDQ/2 voltage.

Another very important feature of the termination power supply is the capability to operate at equal efficiency in sourcing and sinking modes. The VTT supply regulates the output voltage with the same degree of precision when current is flowing from the supply to the load, and when the current is diverted back from the load into the power supply.

The ISL6227 dual channel PWM controller possesses several important enhancements that allow re-configuration for DDR memory applications, and provides all three voltages required in a DDR memory compliant computer.

To reconfigure the ISL6227 for a complete DDR solution, the DDR pin should be set high permanently to the VCC rail. This activates some functions inside the chip that are specific to DDR memory power needs.

In the DDR application presented in Figure 32, the first controller regulates the VDDQ rail to 2.5V. The output voltage is set by external dividers Rfb1 and Rfb12. The second controller regulates the VTT rail to VDDQ/2. The OCSET2 pin function is now different, and serves as an input that brings VDDQ/2 voltage, created by the Rd1 and Rd2 divider, inside the chip, effectively providing a tracking function for the VTT voltage.

The PG2 pin function is also different in DDR mode. This pin becomes the output of the buffer, whose input is connected to the center point of the R/R divider from the VDDQ output by the OCSET2 pin. The buffer output voltage serves as a 1.25V reference for the DDR memory chips. Current capability of this pin is 10mA (12mA max).

For the VTT channel where output is derived from the VDDQ output, some control and protective functions have been significantly simplified. For example, the overcurrent, and overvoltage, and undervoltage protections for the second channel controller are disabled when the DDR pin is set high. The hysteretic mode of operation is also disabled on the VTT channel to allow sinking capability to be independent from the load level. As the VTT channel tracks the VDDQ/2 voltage, the soft-start function is not required, and the SOFT2 pin may be left open, in the event both channels are enabled simultaneously. However, if the VTT channel is enabled later than the VDDQ, the SOFT2 pin must have a capacitor in place to ensure soft-start. In case of overcurrent or undervoltage caused by short circuit on VTT, the fault current will propagate to the first channel and shut down the converter.

The VREF voltage will be present even if the VTT is disabled.

Channel Synchronization in DDR Applications

The presence of two PWM controllers on the same die requires channel synchronization, to reduce inter-channel interference that may cause the duty factor jitter and increased output ripple.

The PWM controller is at greatest noise susceptibility when an error signal on the input of the PWM comparator approaches the decision making point. False triggering may occur, causing jitter and affecting the output regulation.

A common approach used to synchronize dual channel converters is out-of-phase operation. Out-of-phase operation reduces input current ripple and provides a minimum interference for channels that control different voltage levels.

When the DDR pin is connected to GND for dual switcher applications, the channels operate 180° out-of-phase. When used in a DDR application with cascaded converters (VTT generated from VDDQ), several methods of synchronization are implemented in the ISL6227. In the DDR mode, when the DDR pin is connected to VCC, the channels operate either with 0° phase shift, when the VIN pin is connected to the GND, or with 90° phase shift if the VIN pin is connected to a voltage higher than 4.2V.

The following table lists the different synchronization schemes and their usage:

DDR PIN	VIN PIN	SYNCHRONIZATION
0	Vin pin >4.2V	180° out of phase
1	Vin pin voltage <4.2V	0° phase
1	Vin pin voltage >4.2V	90° phase shift

Application Information

Design Procedures

GENERAL

A ceramic decoupling capacitor should be used between the VCC and GND pin of the chip. There are three major currents drawn from the decoupling capacitor:

1. the quiescent current, supporting the internal logic and normal operation of the IC
2. the gate driver current for the lower MOSFETs
3. and the current going through the external diodes to the bootstrap capacitor for upper MOSFET.

In order to reduce the noisy effect of the bootstrap capacitor current to the IC, a small resistor, such as 10Ω, can be used with the decoupling cap to construct a low pass filter for the IC, as shown in Figure 41. The soft-start capacitor and the resistor divider setting the output voltage is easy to select as discussed in the “Block Diagram” on page 13.

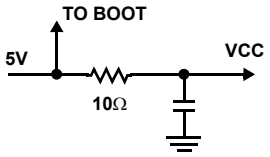


FIGURE 41. INPUT FILTERING FOR THE CHIP

Selection of the Current Sense Resistor

The value of the current sense resistor determines the gain of the current sensing circuit. It affects the current loop gain and the overcurrent protection setpoint. The voltage drop on the lower MOSFET is sensed within 400ns after the upper MOSFET is turned off. The current sense pin has a 140Ω resistor in series with the external current sensing resistor. The current sense pin can source up to a 260µA current while sensing current on the lower MOSFET, in such a way that the voltage drop on the current sensing path would be equal to the voltage on the MOSFET.

$$I_{SOURCING}(R_{CS} + 140\Omega) = I_D r_{DS(ON)} \quad \text{(EQ.17)}$$

I_D can be assumed to be the inductor peak current. In a worst case scenario, the high temperature $r_{DS(ON)}$ could increase to 150% of the room temperature level. During overload condition, the MOSFET drain current I_D could be 130% higher than the normal inductor peak. If the inductor has 30% peak-to-peak ripple, I_D would equal to 115% of the load current. The design should consider the above factors so that the maximum $I_{SOURCING}$ will not saturate to 260µA under worst case conditions. To be safe, $I_{SOURCING}$ should be less than 100µA in normal operation at room temperature. The formula in the earlier discussion assumes a 75µA sourcing current. Users can tune the sourcing current of the ISEN pin to meet the overcurrent protection and the change the current loop gain. The lower the current sensing resistor, the higher gain of the current loop, which can damp the output LC filter more.

A higher value current-sensing resistor will decrease the current sense gain. If the phase node of the converter is very noisy due to poor layout, the sensed current will be contaminated, resulting in duty cycle jittering by the current loop. In such a case, a bigger current sense resistor can be used to reduce both real and noise current levels. This can help damp the phase node wave form jittering.

Sometimes, if the phase node is very noisy, a resistor can be put on the ISEN pin to ground. This resistor together with the R_{CS} can divide the phase node voltage down, seen by the internal current sense amplifier, and reduce noise coupling.

Sizing the Overcurrent Setpoint Resistor

The internal 0.9V reference is buffered to the OCSET pin with a voltage follower (refer to the equivalent circuit in Figure 42). The current going through the external overcurrent set resistor is sensed from the OCSET pin. This current, divided by 2.9, sets up the overcurrent threshold and compares with the scaled ISEN pin current going through R_{CS} with an 8µA offset. Once the sensed current is higher than the threshold value, an OC signal is generated. The first OC signal starts a counter and activates a pulse skipping function. The inductor current will be continuously monitored through the phase node voltage after the first OC trip. As long as the sensed current exceeds the OC threshold value, the following PWM pulse will be skipped. This operation will be the same for 8 switching cycles. Another OC occurring between 8 to 16 switching cycles would result in a latch off with both upper and lower drives low. If there is no OC within 8 to 16 switching cycles, normal operation resumes.

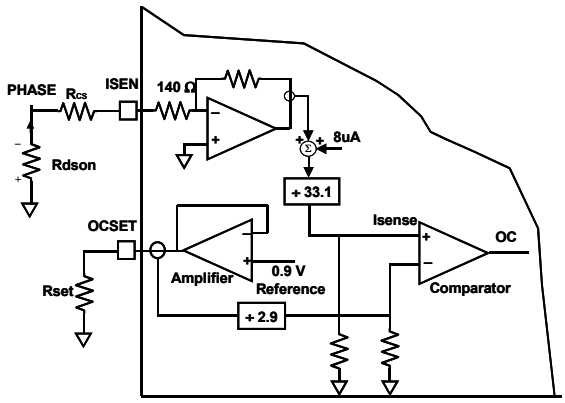


FIGURE 42. EQUIVALENT CIRCUIT FOR OC SIGNAL GENERATOR

Based on the above description and functional block diagram, the OC set resistor can be calculated as:

$$R_{set} = \frac{10.3V}{\frac{I_{OC} r_{DS(ON)}}{R_{CS} + 140} + 8\mu A} \quad \text{(EQ.18)}$$

I_{OC} is the inductor peak current and not the load current. Since inductor peak current changes with input voltage, it is better to use an oscilloscope when testing the overcurrent setting point to monitor the inductor current, and to determine when the OC occurs. To get consistent test results on different boards, it is best to keep the MOSFET at a fixed temperature.

The MOSFET will not heat-up when applying a very low frequency and short load pulses with an electronic load to the output.

As an example, assume the following:

- the maximum normal operation load current is 1,
- the inductor peak current is 1.15-1.3 times higher than the load current, depending on the inductor value and the input voltage,
- and the $r_{DS(ON)}$ has a 45% increase at higher temperature.

I_{OC} should set at least 1.8 to 2 times higher than the maximum load current to avoid nuisance overcurrent trip.

Selection of the LC Filter

The duty cycle of a buck converter is a function of the input voltage and output voltage. Once an output voltage is fixed, it can be written as:

$$D(V_{IN}) = \frac{V_o}{V_{IN}} \quad \text{(EQ.19)}$$

The switching frequency, F_{SW}, of ISL6227 is 300kHz. The peak-to-peak ripple current going through the inductor can be written as:

$$I_{pp} = \frac{V_o(1 - D(V_{IN}))}{F_{sw}L_o} \quad \text{(EQ.20)}$$

As higher ripple current will result in higher switching loss and higher output voltage ripple, the peak-to-peak current of the inductor is generally designed with a 20%-40% peak-to-peak ripple of the nominal operation current. Based on this assumption, the inductor value can be selected with the above equation. In addition to the mechanical dimension, a shielded ferrite core inductor with a very low DC resistance, DCR, is preferred for less core loss and copper loss. The DC copper loss of the inductor can be estimated by:

$$P_{copper} = I_{load}^2 DCR \quad \text{(EQ.21)}$$

The inductor copper loss can be significant in the total system power loss. Attention has to be given to the DCR selection. Another factor to consider when choosing the inductor is its saturation characteristics at elevated temperature. Saturated inductors could result in nuisance OC, or OV trip.

Output voltage ripple and the transient voltage deviation are factors that have to be taken into consideration when selecting an output capacitor. In addition to high frequency noise related MOSFET turn-on and turn-off, the output voltage ripple includes the capacitance voltage drop and ESR voltage drop caused by the AC peak-to-peak current. These two voltages can be represented by:

$$\Delta V_c = \frac{I_{pp}}{8C_oF_{sw}} \quad \text{(EQ.22)}$$

$$\Delta V_{esr} = I_{pp}ESR \quad \text{(EQ.23)}$$

These two components constitute a large portion of the total output voltage ripple. Several capacitors have to be paralleled in order to reduce the ESR and the voltage ripple. If the output of the converter has to support another load with high pulsating current, more capacitors are needed in order to reduce the equivalent ESR and suppress the voltage ripple to a tolerable level.

To support a load transient that is faster than the switching frequency, more capacitors have to be used to reduce the voltage excursion during load step change. Another aspect of the capacitor selection is that the total AC current going through the capacitors has to be less than the rated RMS current specified on the capacitors, to prevent the capacitor from over-heating.

Selection of the Input Capacitor

When the upper MOSFET is on, the current in the output inductor will be seen by the input capacitor. Even though this current has a triangular shape top, its RMS value can be fairly approximated by:

$$Iin_{rms}(V_{IN}) = \sqrt{D(V_{IN})} * I_{load} \quad \text{(EQ.24)}$$

This RMS current includes both DC and AC components. Since the DC component is the product of duty cycle and load current, the AC component can be approximated by:

$$Ii_{nac}(V_{IN}) = \sqrt{(D(V_{IN}) - D(V_{IN})^2)I_{load}} \quad \text{(EQ.25)}$$

AC components will be provided from the input capacitor. The input capacitor has to be able to handle this ripple current without overheating and with tolerable voltage ripple. In addition to the capacitance, a ceramic capacitor is generally used between the drain terminal of the upper MOSFET and the source terminal of the lower MOSFET, in order to clamp the parasitic voltage ringing at the phase node in switching.

Choosing MOSFETs

For a notebook battery with a maximum voltage of 24V, at least a minimum 30V MOSFETs should be used. The design has to trade off the gate charge with the $r_{DS(ON)}$ of the MOSFET:

- For the lower MOSFET, before it is turned on, the body diode has been conducting. The lower MOSFET driver will not charge the miller capacitor of this MOSFET.
- In the turning off process of the lower MOSFET, the load current will shift to the body diode first. The high dv/dt of the phase node voltage will charge the miller capacitor through the lower MOSFET driver sinking current path.

This results in much less switching loss of the lower MOSFETs.

The duty cycle is often very small in high battery voltage applications, and the lower MOSFET will conduct most of the switching cycle; therefore, the lower the $r_{DS(ON)}$ of the lower MOSFET, the less the power loss. The gate charge for this MOSFET is usually of secondary consideration.

The upper MOSFET does not have this zero voltage switching condition, and because it conducts for less time compared to the lower MOSFET, the switching loss tends to be dominant. Priority should be given to the MOSFETs with less gate charge, so that both the gate driver loss, and switching loss, will be minimized.

For the lower MOSFET, its power loss can be assumed to be the conduction loss only.

$$P_{lower}(V_{IN}) \approx (1 - D(V_{IN}))I_{load}^2 r_{DS(ON)Lower} \quad \text{(EQ.26)}$$

For the upper MOSFET, its conduction loss can be written as:

$$P_{uppercond}(V_{IN}) = D(V_{IN})I_{load}^2 R_{DS(ON)upper} \quad \text{(EQ.27)}$$

and its switching loss can be written as:

$$P_{uppersw}(V_{IN}) = \frac{V_{IN} I_{vally} T_{on} F_{sw}}{2} + \frac{V_{IN} I_{peak} T_{off} F_{sw}}{2} \quad \text{(EQ.28)}$$

The peak and valley current of the inductor can be obtained based on the inductor peak-to-peak current and the load current. The turn-on and turn-off time can be estimated with the given gate driver parameters in the Electrical Specification Table on page 3. For example, if the gate driver turn-on path of MOSFET has a typical on-resistance of 4Ω, its maximum turn-on current is 1.2A with 5V Vcc. This current would decay as the gate voltage increased. With the assumption of linear current decay, the turn-on time of the MOSFETs can be written with:

$$T_{on} = \frac{2Q_{gd}}{I_{driver}} \quad \text{(EQ.29)}$$

Q_{gd} is used because when the MOSFET drain-to-source voltage has fallen to zero, it gets charged. Similarly, the turn-off time can be estimated based on the gate charge and the gate drivers sinking current capability.

The total power loss of the upper MOSFET is the sum of the switching loss and the conduction loss. The temperature rise on the MOSFET can be calculated based on the thermal impedance given on the datasheet of the MOSFET. If the temperature rise is too much, a different MOSFET package size, layout copper size, and other options have to be considered to keep the MOSFET cool. The temperature rise can be calculated by:

$$T_{rise} = \theta_{ja} P_{totalpower\ loss} \quad \text{(EQ.30)}$$

The MOSFET gate driver loss can be calculated with the total gate charge and the driver voltage Vcc. The lower MOSFET only charges the miller capacitor at turn-off.

$$P_{driver} = V_{cc} Q_{gs} F_{sw} \quad \text{(EQ.31)}$$

Based on the above calculation, the system efficiency can be estimated by the designer.

Confining the Negative Phase Node Voltage Swing with Schottky Diode

At each switching cycle, the body diode of the lower MOSFET will conduct before the MOSFET is turned on, as the inductor current is flowing to the output capacitor. This will result in a negative voltage on the phase node. The higher the load current, the lower this negative voltage. This voltage will ring back less negative when the lower MOSFET is turned on.

A total 400ns period is given to the current sample-and-hold circuit on the ISEN pin to sense the current going through the lower MOSFET after the upper MOSFET turns off. An excessive negative voltage on the lower MOSFET will be treated as overcurrent. In order to confine this voltage, a schottky diode can be used in parallel with the lower MOSFET for high load current applications. PCB layout parasitics should be minimized in order to reduce the negative ringing of phase voltage.

The second concern for the phase node voltage going into negative is that the boot strap capacitor between the BOOT and PHASE pin could get be charged higher than VCC voltage, exceeding the 6.5V absolute maximum voltage between BOOT and PHASE when the phase node voltage became negative. A resistor can be placed between the cathode of the boot strap diode and BOOT pin to increase the charging time constant of the boot cap. This resistor will not affect the turn-on and off of the upper MOSFET.

Schottky diode can reduce the reverse recovery of the lower MOSFET when transition from freewheeling to blocking, therefore, it is generally good practice to have a schottky diode closely parallel with the lower MOSFET. B340LA, from Diodes, Inc.®, can be used as the external schottky diode.

Tuning the Turn-on of Upper MOSFET

The turn-on speed of the upper MOSFET can be adjusted by the resistor connecting the boot cap to the BOOT pin of the chip. This resistor can confine the voltage ringing on the boot capacitor from coupling to the boot pin. This resistor slows down only the turn-on of the upper MOSFET.

If the upper MOSFET is turned on very fast, it could result in a very high dv/dt on the phase node, which could couple into the lower MOSFET gate through the miller capacitor, causing momentous shoot-through. This phenomenon, together with the reverse recovery of the body diode of the lower MOSFET, can over-shoot the phase node voltage to beyond the voltage rating of the MOSFET. However, a bigger resistor will slow the turn-on of the MOSFET too much and lower the efficiency. Trade-offs need to be made in choosing a suitable resistor value.

System Loop Gain and Stability

The system loop gain is a product of three transfer functions:

1. the transfer function from the output voltage to the feedback point,
2. the transfer function of the internal compensation circuit from the feedback point to the error amplifier output voltage,
3. and the transfer function from the error amplifier output to the converter output voltage.

These transfer functions are written in a closed form in the Theory of Operation section on page 18. The external capacitor, in parallel with the upper resistor of the resistor divider, C_Z, can be used to tune the loop gain and phase margin. Other component parameters, such as the inductor value, can be changed for a wider cross-over frequency of the system loop gain. A body plot of the loop gain transfer function with a 45 degree phase margin (a 60 degree phase margin is better) is desirable to cover component parameter variations.

Testing the Overvoltage on Buck Converters

For synchronous buck converters, if an active source is used to raise the output voltage for the overvoltage protection test, the buck converter will behave like a boost converter and dump energy from the external source to the input. The overvoltage test can be done on ISL6227 by connecting the VSEN pin to an external voltage source or signal generator through a diode. When the external voltage, or signal generator voltage, is tuned to a higher level than the overvoltage threshold (the lower MOSFET will be on), it indicates the overvoltage protection works. This kind of overvoltage protection does not require an external schottky in parallel with the output capacitor.

Layout Considerations

Power and Signal Layer Placement on the PCB

As a general rule, power layers should be close together, either on the top or bottom of the board, with signal layers on the opposite side of the board. For example, prospective layer arrangement on a 4 layer board is shown below:

1. Top Layer: ISL6227 signal lines
2. Signal Ground
3. Power Layers: Power Ground
4. Bottom Layer: Power MOSFET, Inductors and other Power traces

It is a good engineering practice to separate the power voltage and current flowing path from the control and logic level signal path. The controller IC will stay on the signal layer, which is isolated by the signal ground to the power signal traces.

Component Placement

The control pins of the two-channel ISL6227 are located symmetrically on two sides of the IC; it is desirable to arrange the two channels symmetrically around the IC.

The power MOSFET should be close to the IC so that the gate drive signal, the LGATEx, UGATEx, PHASEx, BOOTx, and ISENx traces can be short.

Place the components in such a way that the area under the ISL6227 has fewer noise traces with high dv/dt and di/dt, such as gate signals and phase node signals.

Signal Ground and Power Ground Connection

At minimum, a reasonably large area of copper, which will shield other noise couplings through the IC, could be used as signal ground beneath the ISL6227. The best tie-point between the signal ground and the power ground is at the negative side of the output capacitor on each channel, where there is less noise. Noisy traces beneath the ISL6227 are not recommended.

Pin 1 and Pin 28, the GND and VCC

At least one high quality ceramic decoupling cap should be used across these two pins. A via can tie Pin 1 to signal ground. Since Pin1 and Pin 28 are close together, the decoupling cap can be put close to the IC.

Pin 2 and Pin 27, the LGATE1 and LGATE2

These are the gate drive signals for the bottom MOSFETs of the buck converter. The signal going through these traces have both high dv/dt and high di/dt, with high peak charging and discharging current. These two traces should be short, wide, and away from other traces. There should be no other weak signal traces in parallel with these traces on any layer.

Pin 3 and Pin 26, the PGND1 and PGND2

Each pin should be laid out to the negative side of the relevant output cap with separate traces.The negative side of the output capacitor must be close to the source node of the bottom MOSFET. These traces are the return path of LGATE1 and LGATE2.

Pin 4 and Pin 25, the PHASE1 and PHASE2 pin

These traces should be short, and positioned away from other weak signal traces. The phase node has a very high dv/dt with a voltage swing from the input voltage to ground. No trace should be in parallel with these traces. These traces are also the return path for UGATE1 and UGATE2. Connect these pins to the respective converter's upper MOSFET source.

Pin 5 and Pin 24, the UGATE1 and UGATE2

These pins have a square shape waveform with high dv/dt. It provides the gate drive current to charge and discharge the top MOSFET with high di/dt. This trace should wide, short, and away from other traces similar to the LGATEx.

Pin 6 and Pin 23, the BOOT1 and BOOT2

These pins di/dt are as high as that of the UGATEx; therefore, the traces should be as short as possible.

Pin 7 and Pin 22, the ISEN1 and ISEN2

The ISEN trace should be a separate trace, and independently go to the drain terminal of the lower MOSFET. The current sense resistor should be close to ISEN pin.

The loop formed by the bottom MOSFET, output inductor, and output capacitor, should be very small. The source of the bottom MOSFET should tie to the negative side of the output capacitor in order for the current sense pin to get the voltage drop on the R_{DSON}.

Pin 8 and Pin 21, the EN1 and EN2

These pins stay high in enable mode and low in idle mode and are relatively robust. Enable signals should refer to the signal ground.

Pin 9 and Pin 20, the VOUT1 and VOUT2

These pins connect either to the output voltage or to the signal ground. They are signal lines and should be kept away from noisy lines.

Pin 10 and Pin 19, the VSEN1 and VSEN2

There is usually a resistor divider connecting the output voltage to this pin. The input impedance of these two pins is high because they are the input to the amplifiers. The correct layout should bring the output voltage from the regulation point to the SEN pin with kelvin traces. Build the resistor divider close to the pin so that the high impedance trace is shorter.

Pin 11 and Pin 18, the OCSET1 and OCSET2

In dual switcher mode operation, the overcurrent set resistor should be put close to this pin. In DDR mode operation, the voltage divider, which divides the VDQQ voltage in half, should be put very close to this pin. The other side of the OC set resistor should connect to signal ground.

Pin 12 and Pin 17, the SOFT1 and SOFT2

The soft-start capacitors should be laid out close to this pin. The other side of the soft-start cap should tie to signal ground.

Pin 15 and Pin 16, the PG1 and PG2/REF

For dual switcher operations, these two lines are less noise sensitive. For DDR applications, a capacitor should be placed to the PG2/REF pin.

Pin 13, the DDR

This pin should connect to VCC in DDR applications, and to signal ground in dual switcher applications.

Pin 14, the VIN

This pin connects to battery voltage, and is less noise sensitive.

Copper Size for the Phase Node

Big coppers on both sides of the Phase node introduce parasitic capacitance. The capacitance of PHASE should be kept very low to minimize ringing. If ringing is excessive, it could easily affect current sample information. It would be best to limit the size of the PHASE node copper in strict accordance with the current and thermal management of the application.

Identify the Power and Signal Ground

The input and output capacitors of the converters, the source terminals of the bottom switching MOSFET PGND1, and PGND2, should be closely connected to the power ground. The other components should connect to signal ground. Signal and power ground are tied together at the negative terminal of the output capacitors.

Decoupling Capacitor for Switching MOSFET

It is recommended that ceramic caps be used closely connected to the drain side of the upper MOSFET, and the source of the lower MOSFET. This capacitor reduces the noise and the power loss of the MOSFET. Refer to Figure 43 for the power component placement.

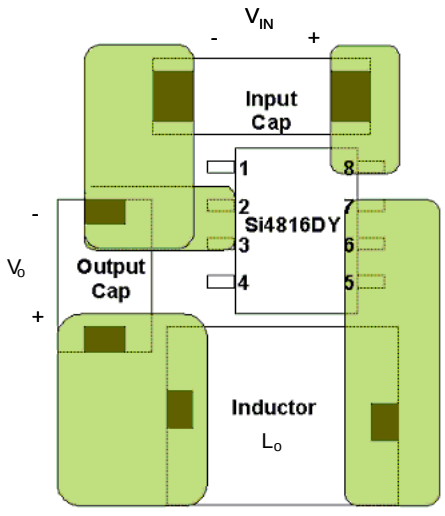
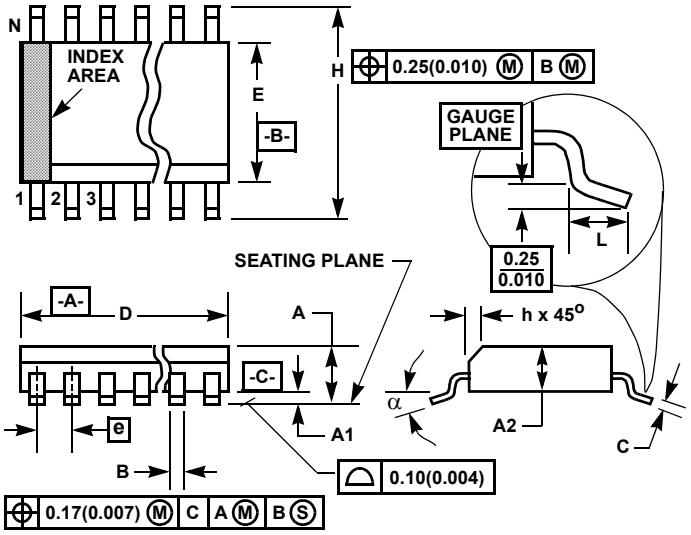


FIGURE 43. A GOOD EXAMPLE POWER COMPONENT REPLACEMENT. IT SHOWS THE NEGATIVE OF INPUT AND OUTPUT CAP AND THE SOURCE OF THE MOSFET ARE TIED AT ONE POINT.

Shrink Small Outline Plastic Packages (SSOP)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “B” does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm (0.004 inch) total in excess of “B” dimension at maximum material condition.
10. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

M28.15

28 LEAD SHRINK NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.053	0.069	1.35	1.75	-
A1	0.004	0.010	0.10	0.25	-
A2	-	0.061	-	1.54	-
B	0.008	0.012	0.20	0.30	9
C	0.007	0.010	0.18	0.25	-
D	0.386	0.394	9.81	10.00	3
E	0.150	0.157	3.81	3.98	4
e	0.025 BSC		0.635 BSC		-
H	0.228	0.244	5.80	6.19	-
h	0.0099	0.0196	0.26	0.49	5
L	0.016	0.050	0.41	1.27	6
N	28		28		7
α	0°	8°	0°	8°	-

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