Complete DDR3/ DDR4 Memory Power Solution Converter

General Description

The uP1740S is a high performance synchronous buck converter with 1.5A source/sink LDO for memory system power. It also provides a buffered low noise reference VTTREF. The uP1740S has wide operation range from 4.5V to 26V for input voltage and 0.75V to 3.3V for memory output voltage.

The synchronous buck of the uP1740S adopts uPI proprietary robust constant on-time (RCOT™) PWM scheme that features easy-to-use, low external component count, fast transient response and quasi-constant frequency operation over the operation range.

The 1.5A source/sink LDO for VTT has fast transient response, requiring only two 10uF of ceramic output capacitors. In addition, the LDO supply input is available externally to significantly reduce the total power losses. The uP1740S supports all the sleep state controls, in S3 state (suspend to RAM) VTT is disable and in S4/S5 (suspend to disk) VDDQ, VTT and VTTREF are soft off.

The uP1740S has complete functions including under voltage protection, over current protection, over voltage protection, power-up sequencing, power OK output, and thermal shutdown. The uP1740S is available in WQFN4x4 - 32L package.

Applications

- **Desktop PCs, Notebooks, and Workstations**
- **Microprocessor and Chipset Supplies**
- **DDR3/DDR3L/DDR4 Memory Power Supplies**
- **SSTL-2 SSTL-18 and HSTL Bus Termination**

Ordering Information

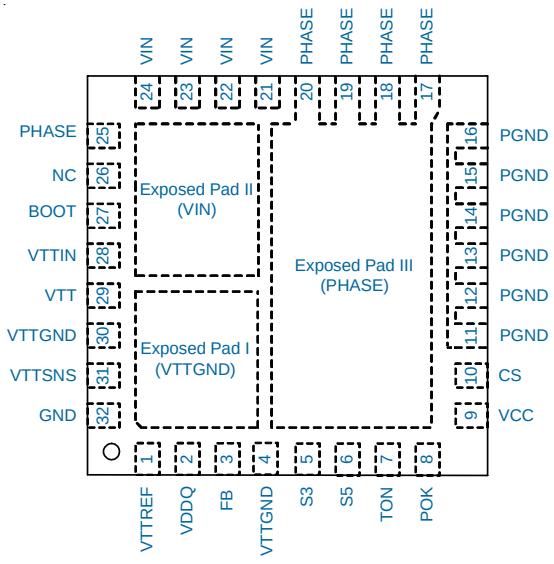
Order Number	Package Type	Remark
uP1740SQMI	WQFN4x4 - 32L	

Note:
(1) Please check the sample/production availability with uPI representatives.
(2) uPI products are compatible with the current IPC/ JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

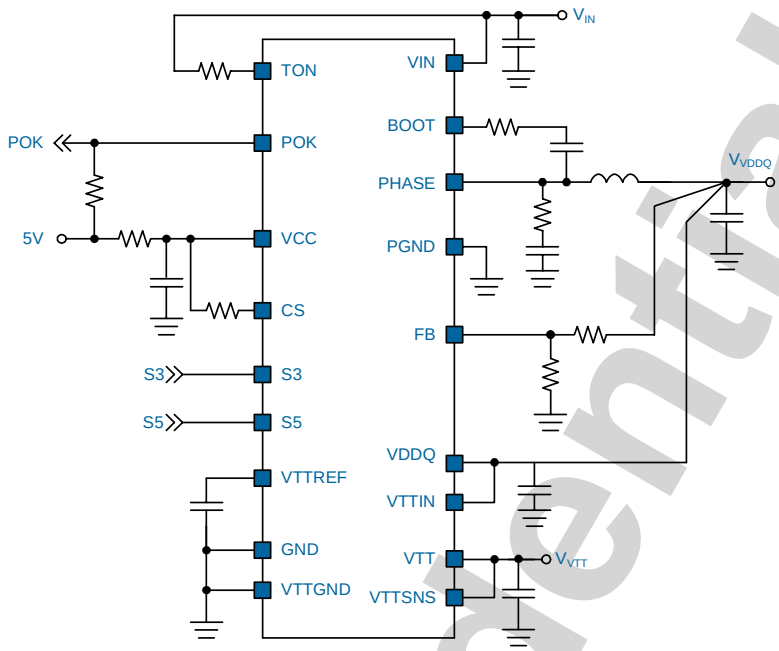
Features

- **Synchronous Buck Converter (VDDQ)**
  - **Wide Input Voltage Range from 4.5V to 26V**
  - **Fast Load Transient Response**
  - **Output Current up to 8A**
  - **RCOT™ Control Topology**
  - **Soft-Off in S4/S5 States**
  - **Output or Adjustable from 0.75V to 3.3V**
  - **POK, OVP, UVP and Thermal Shutdown**
- **LDO (VTT)**
  - **1.5A Source/Sink Capability**
  - **Requires Only Two 10uF Ceramic Output Capacitors**
  - **Disable in S3 and Soft-Off in S4/S5**
  - **Thermal Shutdown**
  - **± 20mV Accuracy**
- **Reference Voltage (VTTREF)**
  - **± 20mV Accuracy**
  - **Low Noise ± 10mA Output**
- **RoHS Compliant and Halogen Free**

Pin Configuration



Typical Application Circuit



Fixed Output Voltage Regulator for VDDQ

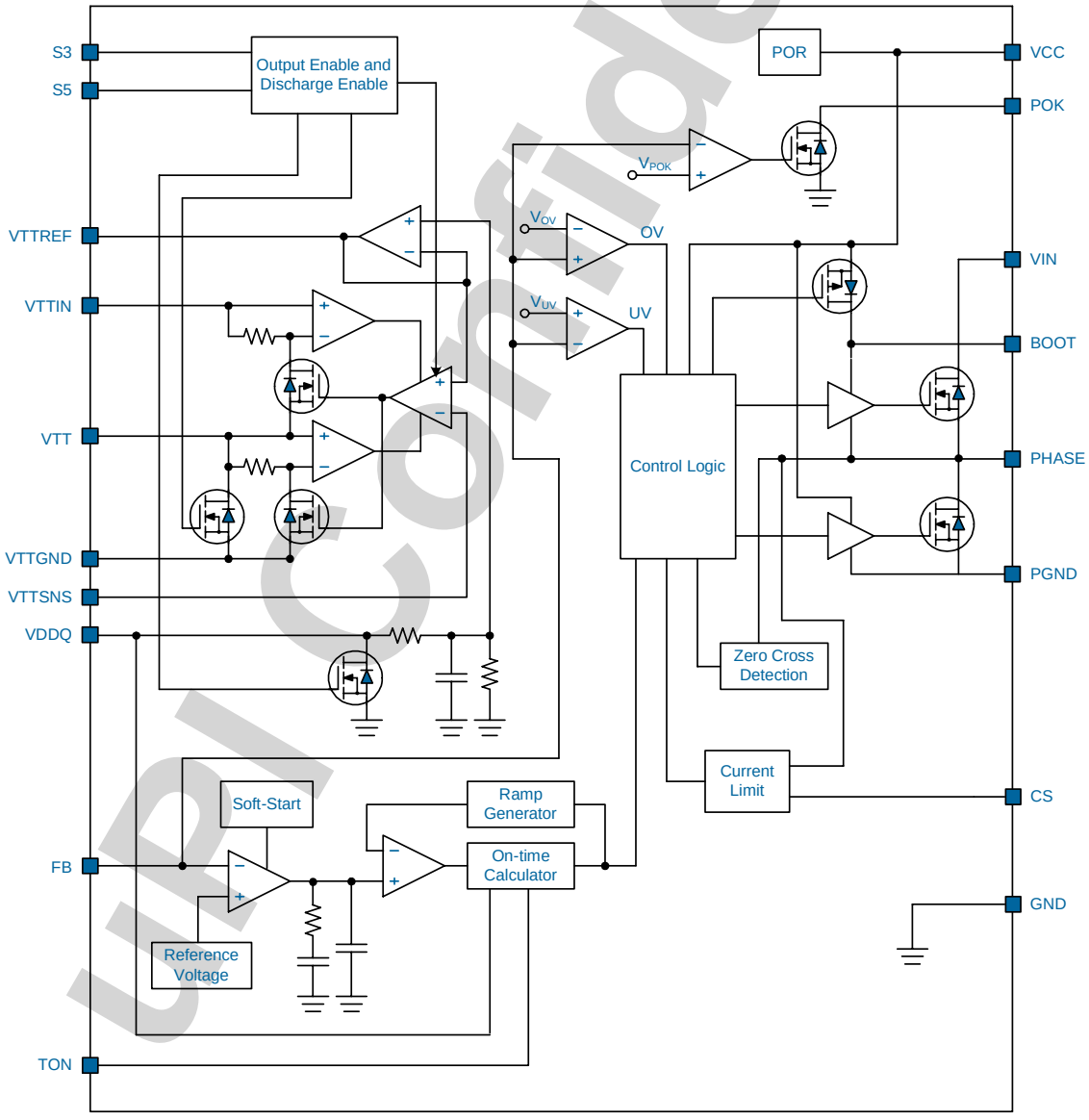
Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VTTREF	**Buffered Reference Output.** Bypass this pin with a 33nF ceramic capacitor to GND. This pin is capable of sourcing up to 10mA current for external loads.
2	VDDQ	**Reference Input for VTT and VTTREF.** Connect this pin to the VDDQ output. This pin is the discharge current sinking terminal of VDDQ output in S4/S5 states. When VDDQ regulator is in fixed output configuration (FB pin is tied to VCC or GND), this pin is the output voltage feedback input.
3	FB	**VDDQ Voltage Feedback Input.** This pin is the inverting input of the error amplifier. A resistor divider from output to GND is used to set the regulator output voltage. For fixed output voltage application, connect this pin to VCC for DDR2 power supply, or connect this pin to GND for DDR3 power supply.
4,30	VTTGND	**Power Ground for the VTT LDO.**
5	S3	**S3 Signal Input.** Connect this pin to the computer system's SLP_S3 signal. This pin companied with S5 switches the IC's operating state from active (S0, S1/S2) to S3 and S4/S5 sleep states.
6	S5	**S5 Signal Input.** Connect this pin to the computer system's SLP_S5 signal. This pin companied with S3 switches the IC's operating state from active (S0, S1/S2) to S3 and S4/S5 sleep states.
7	TON	**On-Time Setting Pin.** Connect a resistor from this pin to V_{IN} to set the on-time for the upper MOSFET.
8	POK	**Power OK Indication.** POK is the open-drain architecture that indicates the output voltage is ready or not. This pin is set to high impedance when the output voltage is within regulation and the soft-start ends. POK is pulled low immediately when either output is in soft-start, standby, shutdown or fault protection.
9	VCC	**5V Power Supply Input.** This pin provides power for internal circuit. Bypass this pin with a 1uF ceramic capacitor to GND.
10	CS	**Current Limit Threshold Setting.** Connect this pin through the setting resistor to VCC for inductor current limit threshold setting.
11~16	PGND	**Power Ground.** This pin is dedicated for lower MOSFET gate driver and should be directly connected to the source of the lower MOSFET with an isolated path.
17~20, 25	PHASE	**Switch Node.** This pin is used as the sink for the upper MOSFET gate driver. This pin is also monitored by the shoot-through protection circuitry to determine when the upper MOSFET has turned off. Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET.
21~24	VIN	**Supply Input.** Input voltage that supplies current to the output voltage.
26	NC	**Not Internally Connected.**
27	BOOT	**Bootstrap Supply for the Floating Upper MOSFET Gate Driver.** The bootstrap capacitor provides the charge to turn on the upper MOSFET. Connect this bootstrap capacitor between BOOT pin and the PHASE pin to form a bootstrap circuit.
28	VTTIN	**Input for the VTT LDO.** This is the drain input to the power device that supplies current to the VTT pin.
29	VTT	**Output for the VTT LDO.** This pin is the output of VTT. Typical value of two 10uF ceramic capacitors is recommended to reduce the effects of current transients on VOUT. A pull low resistance exists when the device is disabled.

Functional Pin Description

Pin No.	Pin Name	Pin Function
31	VTTSNS	**VTT LDO Output Voltage Sense.** Connect this pin to the VTT LDO output capacitors for VTT output voltage sensing.
32	GND	**Signal Ground for the IC.** All voltage levels are measured with respect to this pin.
Exposed Pad Ⅰ		**Power Ground for the VTT LDO.**
Exposed Pad Ⅱ		**Supply Input.** Input voltage that supplies current to the output voltage.
Exposed Pad Ⅲ		**Switch Node.** This pin is used as the sink for the upper MOSFET gate driver. This pin is also monitored by the shoot-through protection circuitry to determine when the upper MOSFET has turned off. Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET.

Functional Block Diagram



Functional Description

The uP1740S is a high performance synchronous buck converter with 1.5A source/sink VTT LDO for memory system power. It also provides the buffered low noise reference with 10mA capability.

The buck converter adopts RCOT™ PWM scheme that features easy-to-use, low external component count, fast transient response and quasi-constant frequency operation over the operation range.

The 1.5A source/sink VTT LDO has fast transient response that only requires two 10uF of ceramic output capacitors.

The reference voltage tracks VDDQ/2 within 1% of VDDQ. The VTT tracks VTTREF within 20mV at no load condition and within 40mV over all load conditions.

The uP1740S supports all the sleep state controls, and also has complete functions including over current protection, over voltage protection, thermal shutdown, power-up sequencing, power OK output, and thermal shutdown. The uP1740S is available in space-saving WQFN4x4-32L package.

Output Voltage Selection

uP1740S can support DDR2, DDR3, DDR3L, DDR4 power supply or adjustable output voltage by connecting resistor divider to the FB pin.

The uP1740S can adjust output voltage by connecting a resistive voltage divider between VDDQ and GND as shown in Figure 1. Choose R_{FB2} to be approximately 10kΩ and solve R_{FB1} using the equation as below:

$$V_{DDQ} = V_{REF} \times (1 + \frac{R_{FB1}}{R_{FB2}})$$

where V_{REF} is 0.75V (typ.).

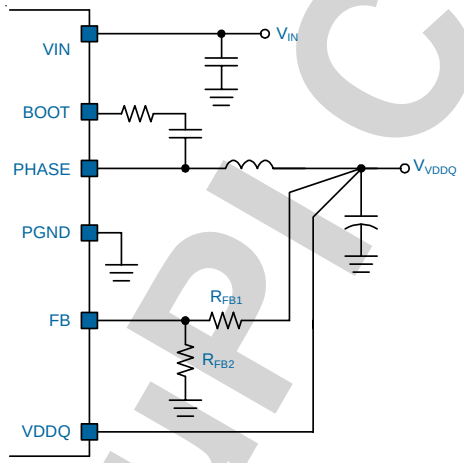


Figure 1. VDDQ Output Voltage Setting

On-Time Setting

The uP1740S adopts a compensated constant-on-time control scheme. A resistor R_{TON} connected to TON pin programs the constant on time according to equation:

$$T_{ON} = \frac{3.8 \times 10^{-12} \times VDDQ \times R_{TON}}{VIN - 0.5V}$$

where R_{TON} is in kΩ, VIN is the supply input voltage and VDDQ is the sensed output voltage.

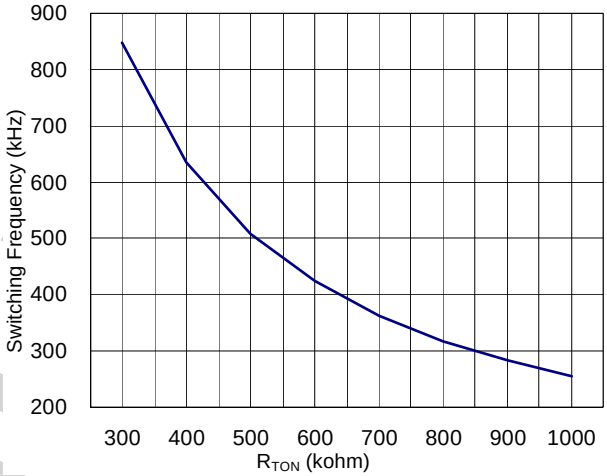


Figure 2. Switching Frequency vs. R_{TON}

Soft Start and POK

The power sequence of uP1740S is shown in Figure 3. After S5 is set high, VDDQ begins to ramp up after a period of delay time T1. Then the output voltage begins to soft start to 90% of the target voltage with time interval T2 as the end of soft start. The controller then checks the output voltage after a period of delay time T3. If the output voltage is in regulation, POK will be set to high impedance to complete the power on sequence. The typical value of T1, T2 and T3 is shown in Figure 3. The POK is an open-drain output. When fault protection (OVP/UVP/thermal shutdown) is triggered during operation, the POK will be pulled low.

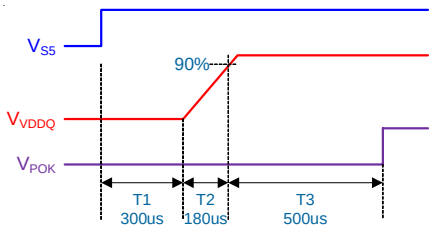


Figure 3. VDDQ Soft Start and POK Timing

Functional Description

VDDQ Light Load Operation

The uP1740S automatically reduces switching frequency at light load to maintain high efficiency. As the output current decreases from heavy-load condition, the inductor current will also be reduced, and eventually comes to the point that its valley touches zero current, which is the boundary between continuous conduction and discontinuous conduction modes. By emulating the behavior of diodes, the lower MOSFET allows only partial of negative current when the inductor freewheeling current reaches negative. As the load current is further decreased, it takes longer time to discharge the output capacitor to the level than requires the next ON cycle.

Outputs Control by S3, S5

The uP1740S provides the output management for the sleep-mode signals such as SLP_S3 and SLP_S5 in the notebook PC system by monitoring S3, S5 status, the output control table is as shown in Table 2 below.

Table 2. S0, S3 and S5 State

State	S3	S5	VDDQSNS	VTTREF	VTT
S0	High	High	On	On	On
S3	Low	High	On	On	Off (discharge)
S4 S5	Low	Low	Off (discharge)	Off (discharge)	Off (discharge)

Ouput Discharge Control

The uP1740S is in non-tracking discharge mode when it enters S4/S5 state. In this non-tracking discharge mode, the uP1740S discharges the VDDQ and VTT outputs through the internal MOSFETs with 15Ω $R_{DS(on)}$ which are connected from VDDQ to GND, and from VTT to VTTGND, respectively.

Output Current Limit

The synchronous buck VDDQ monitors the inductor valley current by lower MOSFET $R_{DS(ON)}$ when it turns on. The over current limit is triggered once the sensing current level is higher than V_{OCSET}. When triggered, the over current limit will keep upper MOSFET off even the voltage loop commands it to turn on.

The output voltage will decrease if the load continuously demands more current than current limit level. Further increase in load current higher than the current limit level will eventually let V_{VDDQ} decrease to trip UVP to shut down the uP1740S.

The current limit threshold is set by connecting a resistor from CS to VCC. The CS pin will sink a 10uA current source and create a voltage drop across R_{CS} as the V_{OCSET}.

V_{OCSET} = 10uA x R_{CS}.

When the voltage drop across the lower MOSFET equals the voltage across the setting resistor, the current limit will be activated.

The current limit level is calculated as:

$$I_{LIM} = \frac{V_{OCSET}}{R_{DS(ON)}} + \frac{I_{RIPPIE}}{2}$$

where I_{RIPPLE} is the peak-to-peak inductor ripple current at steady state.

Over Voltage/Under Voltage Protection

The uP1740S monitors FB voltage to detect overvoltage and undervoltage condition of VDDQ output.

When the FB voltage becomes higher than 115% of the target voltage, the OVP is triggered. Then, upper MOSFET is off and lower MOSFET is on. When the FB voltage is lower than 55% of the target voltage, the UVP is triggered after 10us fault detection. Then, upper MOSFET and lower MOSFET are latched off. This function is enabled 5ms after S5 go high to ensure startup.

VCC UVLO

The VCC has under voltage lockout protection (UVLO). When the VCC voltage is lower than UVLO threshold voltage, all functions are turned off. This is non-latch protection.

Thermal Protection

The uP1740S monitors the temperature of itself. If the temperature exceeds typical 150°C, the uP1740S will be turned off. This is non-latch protection.

Absolute Maximum Rating

(Note 1)

VCC to GND ---------- -0.3V to +6V

BOOT to PHASE ---------- -0.3V to +6V

PHASE to GND

DC ---------- -0.3V to +30V

<50ns ---------- -5V to +30V

Other Pins ---------- -0.3V to +6V

Storage Temperature Range ---------- -65°C to +150°C

Junction Temperature ---------- 150°C

Lead Temperature Range(Soldering 10sec) ---------- 260°C

ESD Rating (Note 2)

HBM(Human Body Mode) ---------- 2KV

MM(Mechine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)

WQFN4x4-32L $\theta_{JA,\ controller}$ ---------- 54°C/W

WQFN4x4-32L $\theta_{JA,\ HS}$ ---------- 42°C/W

WQFN4x4-32L $\theta_{JA,\ LS}$ ---------- 38°C/W

WQFN4x4-32L $\theta_{JC,\ controller}$ ---------- 21°C/W

WQFN4x4-32L $\theta_{JC,\ HS}$ ---------- 10°C/W

WQFN4x4-32L $\theta_{JC,\ LS}$ ---------- 6°C/W

Power Dissipation, P_D @ T_A = 25°C

WQFN4x4-32L $P_{D,\ controller}$ ---------- 1.85W

WQFN4x4-32L $P_{D,\ HS}$ ---------- 2.38W

WQFN4x4-32L $P_{D,\ LS}$ ---------- 2.63W

Recommended Operation Conditions

(Note 4)

Supply Input Voltage, V_{IN} ---------- 4.5V to 26V

Control Voltage, VCC ---------- 4.5V to 5.5V

Operating Junction Temperature Range ---------- -40°C to +125°C

Operating Ambient Temperature Range ---------- -40°C to +85°C

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective thermal conductivity test board of JEDEC 51-7 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Guarantee by design.

Electrical Characteristics

(V_{IN} = 12V, V_{VCC} = 5V, VTTIN is connected to VDDQ output, T_A = +25°C unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current						
VCC Current	I_{VCC}	Supply current, V_{S3} = 0V, V_{S5} = 5V, force FB above regulation level (no switching).	--	350	500	uA
		Shutdown current, V_{S3} = V_{S5} = 0V	--	1	10	
VTTIN Current	I_{VTTIN}	Standby current, V_{S3} = 0V, V_{S5} = 5V. No load at VTT pin	--	0.1	10	uA
		Shutdown current, V_{S3} = V_{S5} = 0V	--	0.1	1	
		Bias current, V_{S3} = V_{S5} = 5V, no load at VTT pin.	--	1	--	
TON Current	I_{TON}	Operating current, R_{TON} = 1MΩ	--	15	--	uA
		Shutdown current, V_{S3} = V_{S5} = 0V	--	0.1	3	
Reference Voltage						
FB Reference Voltage	V_{REF}	V_{VCC} = 4.5V to 5.5V	0.742	0.75	0.758	V
FB Input Bias Current	I_{FB}	V_{FB} = 0.75V.	-1	0.1	1	uA
VTTREF Output						
VTTREF Output Voltage	V_{VTTREF}	Connect FB pin to GND.	--	0.75	--	V
VTTREF Output Voltage Tolerance	$V_{VTTREFTO}$	V_{VDDQ} = V_{VTTIN} = 1.5V , $\lvert I_{VTTREF} \rvert$ <10mA	-15	--	15	mV
VTTREF Source Current Limit	$I_{VTTREFOCLSRC}$	V_{VTTREF} = 0V	10	--	--	mA
VTT Output						
VTT Output Voltage Tolerance	V_{VTTTO}	V_{VDDQ} = V_{VTTIN} = 1.2V/ 1.35V /1.5V/ 1.8V, I_{VTT} = 0A	-20	--	20	mV
		V_{VDDQ} = V_{VTTIN} = 1.2V/ 1.35V/ 1.5V /1.8V, $\lvert I_{VTT} \rvert$ < 1A	-30	--	30	
		V_{VDDQ} = V_{VTTIN} = 1.2V/ 1.35V, $\lvert I_{VTT} \rvert$ < 1.2A	-40	--	40	
		V_{VDDQ} = V_{VTTIN} = 1.5V/ 1.8V, $\lvert I_{VTT} \rvert$ < 1.5A	-40	--	40	
VTT Source Current Limit	$I_{VTTTOCLSRC}$	V_{VTT} = (V_{VDDQ}/ 2) x 0.95	1.5	--	--	A
		V_{VTT} = 0V	--	1.3	--	
VTT Sink Current Limit	$I_{VTTTOCLSNK}$	V_{VTT} = (V_{VDDQ}/ 2) x 1.05	1.5	--	--	A
		V_{VTT} = V_{VDDQ}	--	1.3	--	
VTTSNS Leakage Current	$I_{VTTSNSLK}$	Sink current = 1mA	- 1	--	1	uA
VTT Discharge Current	I_{VTTDis}	V_{S3} = V_{S5} = 0V, V_{VDDQ} = 0V, V_{VTT} = 0.5V	10	30	--	mA

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDDQ						
VDDQ Input Resistance	R_{VDDQ}		--	100	--	kΩ
VDDQ Discharge Resistance	$I_{VDDQDis}$	V_{S5} = 0V	--	15	--	Ω
On Time						
On-Time	T_{ON}	R_{TON} = 1MΩ, V_{VDDQ} = 1.25V	267	334	401	ns
Minimum On-Time	T_{ONMIN}		--	80	--	ns
Minimum Off-Time	T_{OFFMIN}		--	600	--	ns
Power OK						
POK Rising Threshold	V_{THPOKH}	Measured at FB, with respect to reference voltage.	87	90	93	%
		Hysteresis	--	6.7	--	
POK Propagation Delay	T_{POK}	From FB forced below POK falling threshold to POK go low.	--	2.5	--	us
POK Leakage Current	I_{LK_POK}	High state, POK = 5V	--	--	1	uA
POK Output Low Voltage	V_{POK_L}	Sink current = 1mA	--	--	0.4	V
Logic Input Threshold						
High Level Input Voltage	V_{IH}	S3, S5 High	2	--	--	V
Low Level Input Voltage	V_{IL}	S3, S5 Low	--	--	0.8	V
Logic Input Leakage Current	V_{INLEAK}	S3, S5 = 5V/0V	-1	--	1	uA
Internal Bootstrap Switch						
Internal Boost Charging Switch On-Resistance	R_{BOOT}	VCC to BOOT, I_{BOOT} = 10mA	--	80	--	Ω
Power Switches						
Upper Switch Resistance	$R_{UG,DSON}$		--	17.7	--	mΩ
Lower Switch Resistance	$R_{LG,DSON}$		4	5.5	7.8	mΩ
Protection: Current Limit						
CS Sink Current	I_{CS}	V_{CS} > 4.5V	9	10	11	uA
CS Current Temp. Coefficient	T_{CICS}	On the basis of 25°C (Note 5)	--	4700	--	ppm/°C
OCP Comparator Offset	V_{OCLoff}	GND - V_{PHASE}, R_{CS} = 5kΩ	-15	--	15	mV
Zero Current Threshold	V_{ZC}	GND - V_{PHASE}	-5	--	10	mV

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Protection: UVP & OVP						
OVP Trip Threshold	V_{OVP}	Measured at FB, with respect to reference voltage.	110	115	120	%
OVP Propagation Delay	T_{OVPDEL}	Force FB above OVP trip threshold.	--	20	--	us
UVP Trip Threshold	V_{UVP}	Measured at FB, with respect to reference voltage.	45	55	65	%
UVP Propagation Delay	T_{UVPDEL}	Force FB below UVP trip threshold.	--	10	--	us
UVP Enable Delay	T_{UVPEN}	From S5 signal go high	--	0.5	--	ms
Protection: UVLO						
VCC UVLO Threshold	V_{UVLO}	Rising edge	3.8	4.1	4.5	V
		Hysteresis	--	0.3	--	
Protection: Thermal Shutdown						
Thermal Shutdown Threshold	T_{SDN}	Shutdown temperature	--	150	--	°C
		Hysteresis	--	20	--	

Typical Operation Characteristics

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Application Information

PCB Layout Considerations

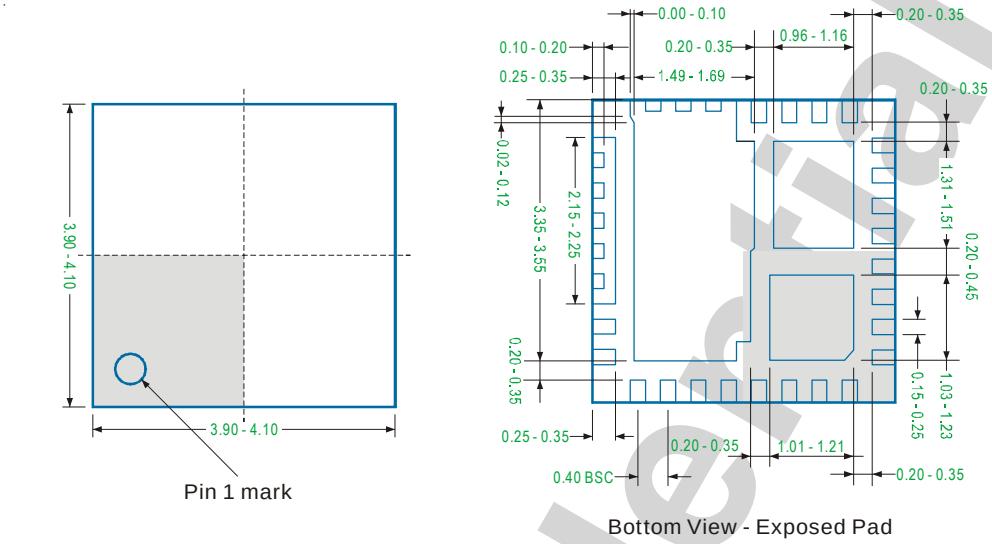
High speed switching and relatively large peak currents in a synchronous-rectified buck converter make the PCB layout a very important part of design. Fast current switching from one device to another in a synchronous-rectified buck converter causes voltage spikes across the interconnecting impedances and parasitic circuit elements. The voltage spikes can degrade efficiency and radiate noise that result in overvoltage stress on devices. Careful component placement layout and printed circuit board design minimizes the voltage spikes induced in the converter.

Follow the layout guidelines for optimal performance of uP1740S.

- Keep the PCB trace PHASE node as short and wide as possible.
- Add a sunbber circuit between PHASE and PGND to eliminate the high frequency voltage spike at PHASE node.
- Keep sensitive analog circuits such as VDDQ, VTTSNS and CS away from high voltage switching node such as PHASE.
- Connect VDDQ output to VTTIN with short and wide trace. If other power source is used as VTTIN, a bypass input capacitor should be placed as close to VTTIN as possible.
- Place the output capacitor for VTT should close to the pin with short and wide trace to avoid additional ESR and/or ESL of the trace.
- Connect VTT to the positive of VTT output capacitors with a separate trace.
- VDDQ can be connected separately from VTTIN. Remember that this sensing potential is the reference voltage of VTTREF. Avoid any noise generative lines.
- Negative node of VTT output capacitor(s) and VTTREF capacitor should be tied together by avoiding common impedance to the high current path of the VTT source/sink current.
- GND (Signal GND) pin node represents the reference potential for VTTREF and VTT outputs. Connect GND to negative nodes of VTT capacitor(s), VTTREF capacitor and VDDQ capacitor(s) with care to avoid additional ESR and/or ESL. GND and PGND (power ground) should be connected together at a single point.

Package Information

WQFN4x4-32L



Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

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