

Signal Phase PWM Controller with Integrated Driver for IMVP8 Mobile CPU Core Power Supply

General Description

The RT3601EA is an IMVP8 compliant CPU power controller with 1 embedded driver. The RT3601EA adopts G-NAVP™ (Green Native AVP) which is Richtek's proprietary topology derived from finite DC gain of EA amplifier with current mode control, making it easy to set the droop to meet all Intel CPU requirements of AVP (Adaptive Voltage Positioning). Based on the G-NAVP™ topology, the RT3601EA also features a quick response mechanism for optimized AVP performance during load transient. The RT3601EA supports mode transition function with various operating states. A serial VID (SVID) interface is built in the RT3601EA to communicate with Intel IMVP8 compliant CPU. The RT3601EA supports VID on-the-fly function with three different slew rates : Fast, Slow and Decay. By utilizing the G-NAVP™ topology, the operating frequency of the RT3601EA varies with VID, load and input voltage to further enhance the efficiency even in CCM. Moreover, the G-NAVP™ with CCRCOT (Constant Current Ripple COT) technology provides superior output voltage ripple over the entire input/output range. The built-in high accuracy DAC converts the SVID code ranging from 0.25V to 1.52V with 5mV per step. The RT3601EA integrates a high accuracy ADC for platform setting functions, such as quick response trigger level. Besides, the setting function also supposes this two rails address exchange. The RT3601EA provides VR ready output signals. It also features complete fault protection functions including over-voltage (OV), negative voltage (NV), over-current (OC) and under-voltage lockout (UVLO). The RT3601EA is available in the WQFN-28L 4x4 small foot print package.

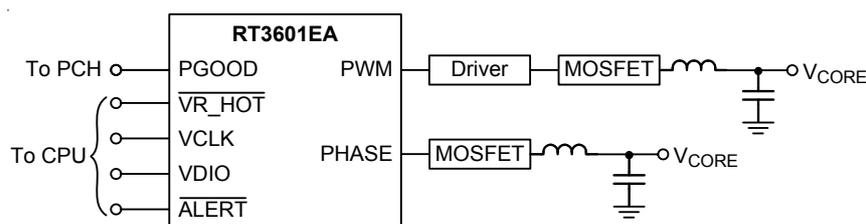
Features

- Intel IMVP8 Serial VID Interface Compatible Power Management States
- Single Phase with 1 Embedded MOSFET Driver PWM Controller
- G-NAVP™ (Green Native Adaptive Voltage Positioning) Topology
- 0.5% DAC Accuracy
- Differential Remote Voltage Sensing
- Built-in ADC for Platform Programming
- Accurate Current Balance
- System Thermal Compensated AVP
- Diode Emulation Mode at Light Load Condition for Multiple or Single Phase Operation
- Fast Transient Response
- VR Ready Indicator
- Thermal Throttling
- Current Monitor Output
- OVP, OCP, NVP, UVLO
- Slew Rate Setting/Address Flip Function
- Rail Address Flexibility
- DVID Enhancement

Applications

- IMVP8 Intel Core Supply
- Notebook/ Desktop Computer/ Servers Multi-phase CPU Core Supply
- AVP Step-Down Converter

Simplified Application Circuit



Ordering Information

RT3601EA □ □

- Package Type
QW : WQFN-28L 4x4 (W-Type)
- Lead Plating System
G : Green (Halogen Free and Pb Free)

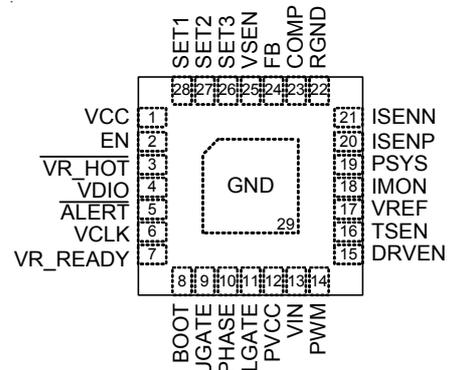
Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

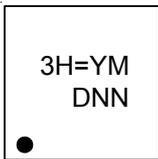
Pin Configuration

(TOP VIEW)



WQFN-28L 4x4

Marking Information



3H= : Product Code
YMDNN : Date Code

Functional Pin Description

| Pin No | Pin Name | Pin Function |
|--------|----------|--|
| 1 | VCC | Controller power supply. Connect this pin to 5V and place a decoupling capacitor 2.2μF at least. The decoupling capacitor is as close PWM controller as possible. |
| 2 | EN | VR enable control input. |
| 3 | VR_HOT | Thermal monitor output, this pin is active low. |
| 4 | VDIO | VR and CPU data transmission interface. |
| 5 | ALERT | SVID alert. (Active low) |
| 6 | VCLK | Synchronous clock from the CPU. |
| 7 | VR_READY | VR ready indicator. |
| 8 | BOOT | Bootstrap supply for high-side gate MOSFET driver. |
| 9 | UGATE | High-side driver output. Connect the pin to the gate of high-side MOSFET. |
| 10 | PHASE | Switch node of high-side driver. Connect the pin to high-side MOSFET source together with the low-side MOSFET drain and inductor. |
| 11 | LGATE | Low-side driver output. This pin drives the gate of low-side MOSFET. |
| 12 | PVCC | Driver power supply input. Connect this pin to GND by a minimum 2.2μF ceramic Capacitor. |
| 13 | VIN | VIN input pin. Connect a low pass filter to this pin to set on-time. |
| 14 | PWM | PWM outputs. |
| 15 | DRVEN | External driver enable control. Connecting to driver enable pin. |
| 16 | TSEN | Thermal sense input. Platform can use this to set BOOT voltage and DVID threshold. |
| 17 | VREF | Fixed 0.6V output reference voltage. This voltage is only used to offset the output voltage of IMON pin. Between this pin and GND must be placed a exact 0.47μF capacitor and 3.9Ω resistor. |

Operation

The RT3601EA adopts G-NAVP™ (Green Native AVP) which is Richtek's proprietary topology derived from finite DC gain of EA amplifier with current mode control, making it easy to set the droop to meet all Intel CPU requirements of AVP (Adaptive Voltage Positioning).

The G-NAVP™ controller is one type of current mode constant on-time control with DC offset cancellation. The approach can not only improve DC offset problem for increasing system accuracy but also provide fast transient response. When current feedback signal reaches COMP signal, the RT3601EA generates an on-time width to achieve PWM modulation.

TON GEN/Driver Interface PWMx

Generate the sequentially according to the phase control signal from the Loop Control/Protection Logic. Pulse width is determined by current balance result and pin setting. Once quick response mechanism is triggered, VR will allow all PWM to turn on at the same time. PWM status is also controlled by Protection Logic. Different protections may cause different PWM status (Both High-Z or LG turn-on).

SVID Interface/Configuration Registers/Control Logic

The interface receives the SVID signal from CPU and sends the relative signals to Loop Control/Protection Logic for loop control to execute the action by CPU. The registers save the pin setting data from ADC output. The Control Logic controls the ADC timing, generates the digital code of the VID for VSEN voltage.

Loop Control/Protection Logic

It controls the power on sequence, the protection behavior, and the operational phase number.

MUX and ADC

The MUX supports the inputs from SET1, SET2, SET3, IMON, TSEN. The ADC converts these analog signals to digital codes for reporting or performance adjustment.

Current Balance

Each phase current sense signal is sent to the current balance circuit which adjusts the on-time of each phase to optimize current sharing.

Offset Cancellation

Cancel the current/voltage ripple issue to get the accurate VSEN.

UVLO

Detect the DVD and VCC voltage and issue POR signal as they are high enough.

DAC

Generate an analog signal according to the digital code generated by Control Logic.

Soft-Start & Slew Rate Control

Control the Dynamic VID slew rate of VSET according to the SetVID fast or SetVID slow.

Error Amp

Error amplifier generates COMP signal by the difference between VSET and FB.

PWM CMP

The PWM comparator compares Ramp signal COMP signal and current feedback signal to generate a signal for TON trigger.

IMON Filter

IMON Filter is used for average sum current signal by analog RC filter.

Table 1. VR12.5 VID Code Table

| VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | HEX | Voltage (V) |
|------|------|------|------|------|------|------|------|-----|-------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01 | 0.25 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 02 | 0.255 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 03 | 0.26 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 04 | 0.265 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 05 | 0.27 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 06 | 0.275 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 07 | 0.28 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 08 | 0.285 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 09 | 0.29 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0A | 0.295 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0B | 0.3 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0C | 0.305 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0D | 0.31 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0E | 0.315 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0F | 0.32 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10 | 0.325 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 11 | 0.33 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 12 | 0.335 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 13 | 0.34 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 14 | 0.345 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 15 | 0.35 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 16 | 0.355 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 17 | 0.36 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 18 | 0.365 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 19 | 0.37 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1A | 0.375 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1B | 0.38 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1C | 0.385 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1D | 0.39 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1E | 0.395 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1F | 0.4 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 20 | 0.405 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 21 | 0.41 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 22 | 0.415 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 23 | 0.42 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 24 | 0.425 |

| VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | HEX | Voltage (V) |
|------|------|------|------|------|------|------|------|-----|-------------|
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 25 | 0.43 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 26 | 0.435 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 27 | 0.44 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 28 | 0.445 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 29 | 0.45 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 2A | 0.455 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 2B | 0.46 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 2C | 0.465 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 2D | 0.47 |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 2E | 0.475 |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 2F | 0.48 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 30 | 0.485 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 31 | 0.49 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 32 | 0.495 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 33 | 0.5 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 34 | 0.505 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 35 | 0.51 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 36 | 0.515 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 37 | 0.52 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 38 | 0.525 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 39 | 0.53 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 3A | 0.535 |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 3B | 0.54 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 3C | 0.545 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 3D | 0.55 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 3E | 0.555 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 3F | 0.56 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 40 | 0.565 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 41 | 0.57 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 42 | 0.575 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 43 | 0.58 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 44 | 0.585 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 45 | 0.59 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 46 | 0.595 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 47 | 0.6 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 48 | 0.605 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 49 | 0.61 |

| VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | HEX | Voltage (V) |
|------|------|------|------|------|------|------|------|-----|-------------|
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 4A | 0.615 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 4B | 0.62 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 4C | 0.625 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 4D | 0.63 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 4E | 0.635 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 4F | 0.64 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 50 | 0.645 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 51 | 0.65 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 52 | 0.655 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 53 | 0.66 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 54 | 0.665 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 55 | 0.67 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 56 | 0.675 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 57 | 0.68 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 58 | 0.685 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 59 | 0.69 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 5A | 0.695 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 5B | 0.7 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 5C | 0.705 |
| 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 5D | 0.71 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 5E | 0.715 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 5F | 0.72 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 60 | 0.725 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 61 | 0.73 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 62 | 0.735 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 63 | 0.74 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 64 | 0.745 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 65 | 0.75 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 66 | 0.755 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 67 | 0.76 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 68 | 0.765 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 69 | 0.77 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 6A | 0.775 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 6B | 0.78 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 6C | 0.785 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 6D | 0.79 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 6E | 0.795 |

| VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | HEX | Voltage (V) |
|------|------|------|------|------|------|------|------|-----|-------------|
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 6F | 0.8 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 70 | 0.805 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 71 | 0.81 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 72 | 0.815 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 73 | 0.82 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 74 | 0.825 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 75 | 0.83 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 76 | 0.835 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 77 | 0.84 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 78 | 0.845 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 79 | 0.85 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 7A | 0.855 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 7B | 0.86 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 7C | 0.865 |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 7D | 0.87 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 7E | 0.875 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 7F | 0.88 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 80 | 0.885 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 81 | 0.89 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 82 | 0.895 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 83 | 0.9 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 84 | 0.905 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 85 | 0.91 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 86 | 0.915 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 87 | 0.92 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 88 | 0.925 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 89 | 0.93 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 8A | 0.935 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 8B | 0.94 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 8C | 0.945 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 8D | 0.95 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 8E | 0.955 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 8F | 0.96 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 90 | 0.965 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 91 | 0.97 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 92 | 0.975 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 93 | 0.98 |

| VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | HEX | Voltage (V) |
|------|------|------|------|------|------|------|------|-----|-------------|
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 94 | 0.985 |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 95 | 0.99 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 96 | 0.995 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 97 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 98 | 1.005 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 99 | 1.01 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 9A | 1.015 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 9B | 1.02 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 9C | 1.025 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 9D | 1.03 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 9E | 1.035 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 9F | 1.04 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | A0 | 1.045 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | A1 | 1.05 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | A2 | 1.055 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | A3 | 1.06 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | A4 | 1.065 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | A5 | 1.07 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | A6 | 1.075 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | A7 | 1.08 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | A8 | 1.085 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | A9 | 1.09 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | AA | 1.095 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | AB | 1.1 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | AC | 1.105 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | AD | 1.11 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | AE | 1.115 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | AF | 1.12 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | B0 | 1.125 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | B1 | 1.13 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | B2 | 1.135 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | B3 | 1.14 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | B4 | 1.145 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | B5 | 1.15 |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | B6 | 1.155 |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | B7 | 1.16 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | B8 | 1.165 |

| VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | HEX | Voltage (V) |
|------|------|------|------|------|------|------|------|-----|-------------|
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | B9 | 1.17 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | BA | 1.175 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | BB | 1.18 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | BC | 1.185 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | BD | 1.19 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | BE | 1.195 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | BF | 1.2 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | C0 | 1.205 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | C1 | 1.21 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | C2 | 1.215 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | C3 | 1.22 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | C4 | 1.225 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | C5 | 1.23 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | C6 | 1.235 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | C7 | 1.24 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | C8 | 1.245 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | C9 | 1.25 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | CA | 1.255 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | CB | 1.26 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | CC | 1.265 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | CD | 1.27 |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | CE | 1.275 |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | CF | 1.28 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | D0 | 1.285 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | D1 | 1.29 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | D2 | 1.295 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | D3 | 1.3 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | D4 | 1.305 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | D5 | 1.31 |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | D6 | 1.315 |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | D7 | 1.32 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | D8 | 1.325 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | D9 | 1.33 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | DA | 1.335 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | DB | 1.34 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | DC | 1.345 |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | DD | 1.35 |

| VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 | HEX | Voltage (V) |
|------|------|------|------|------|------|------|------|-----|-------------|
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | DE | 1.355 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | DF | 1.36 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | E0 | 1.365 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | E1 | 1.37 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | E2 | 1.375 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | E3 | 1.38 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | E4 | 1.385 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | E5 | 1.39 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | E6 | 1.395 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | E7 | 1.4 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | E8 | 1.405 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | E9 | 1.41 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | EA | 1.415 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | EB | 1.42 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | EC | 1.425 |
| 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | ED | 1.43 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | EE | 1.435 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | EF | 1.44 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | F0 | 1.445 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | F1 | 1.45 |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | F2 | 1.455 |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | F3 | 1.46 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | F4 | 1.465 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | F5 | 1.47 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | F6 | 1.475 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | F7 | 1.48 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | F8 | 1.485 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | F9 | 1.49 |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | FA | 1.495 |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | FB | 1.5 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | FC | 1.505 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | FD | 1.51 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | FE | 1.515 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | FF | 1.52 |

Absolute Maximum Ratings (Note 1)

- VCC to GND ----- -0.3V to 6.5V
- RGND to GND ----- -0.3V to 0.3V
- VIN to GND ----- -0.3V to 28V
- PVCC to GND ----- -0.3V to 6.5V
- BOOT to PHASE ----- -0.3V to 6.5V
- PHASE to GND
 - DC ----- -0.3V to 30V
 - <20ns ----- -10V to 35V
- LGATE to GND
 - DC ----- -0.3V to (VCC+ 0.3V)
 - <20ns ----- -2V to (VCC+ 0.3V)
- UGATE to GND
 - DC ----- (V_{PHASE} - 0.3V) to (V_{BOOT} + 0.3V)
 - <20ns ----- (V_{PHASE} - 2V) to (V_{BOOT} + 0.3V)
- Other Pins ----- -0.3V to (V_{CC} + 0.3V)
- Power Dissipation, P_D @ T_A = 25°C
 - WQFN-28L 4x4 ----- 3.5W
- Package Thermal Resistance (Note 2)
 - WQFN-28L 4x4, θ_{JA} ----- 28.5°C/W
 - WQFN-28L 4x4, θ_{JC} ----- 7°C/W
- Junction Temperature ----- 150°C
- Lead Temperature (Soldering, 10 sec.) ----- 260°C
- Storage Temperature Range ----- -65°C to 150°C
- ESD Susceptibility (Note 3)
 - HBM (Human Body Model) ----- 2kV

Recommended Operating Conditions (Note 4)

- Supply Voltage, VIN ----- 4.5V to 24V
- Supply Voltage, VCC, PVCC ----- 4.5V to 5.5V
- Junction Temperature Range ----- -40°C to 125°C
- Ambient Temperature Range ----- -40°C to 85°C

Electrical Characteristics

(V_{CC} = 5V, T_A = 25°C, unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|-----------------------|----------------------|--------------------------|-----|-----|-----|------|
| Supply Input | | | | | | |
| Supply Voltage | V _{CC} | | 4.5 | 5 | 5.5 | V |
| Supply Current | I _{VCC} | EN = 1.05V, no switching | -- | 5 | -- | mA |
| Supply Current at PS4 | I _{VCC_PS4} | EN = 1.05V, no switching | -- | 0.1 | -- | |
| Shutdown Current | I _{SHDN} | V _{EN} = 0 | -- | -- | 5 | μA |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---------------------------------------|---------------------|--|------------------------|------------------------|------------------------|----------|
| Reference and DAC | | | | | | |
| DAC Accuracy | V _{FB} | V _{DAC} = 0.75V – 1.52V | -0.5% | 0 | 0.5% | % of VID |
| | | V _{DAC} = 0.5V – 0.745V | -8 | 0 | 8 | mV |
| | | V _{DAC} = 0.25V – 0.495V | -10 | 0 | 10 | |
| Slew Rate | | | | | | |
| Dynamic VID Slew Rate | SR | Set VID fast | 30 | 33.75 | 45 | mV/μs |
| | | Set VID slow, set slow = 1/2 fast | 15 | 16.875 | 22.5 | |
| EA Amplifier | | | | | | |
| DC Gain | ADC | R _L = 47kΩ (Note 5) | 70 | 80 | -- | dB |
| Gain-Bandwidth Product | GBW | C _{LOAD} = 5pF (Note 5) | -- | 5 | -- | MHz |
| Input Offset | V _{EAOFS} | | -3 | -- | 3 | mV |
| Slew Rate | SREA | C _{LOAD} = 10pF (Gain= -4, R _F = 47kΩ, V _{OUT} = 0.5V to -3V) | -- | 5 | -- | V/μs |
| Output Voltage Range | V _{COMP} | R _L = 47kΩ | 0.3 | -- | 3.6 | V |
| Max Source/Sink Current | I _{OUTEA} | V _{COMP} = 2V | -- | 5 | -- | mA |
| Current Sensing Amplifier | | | | | | |
| Input Offset Voltage | V _{OCS} | V _{DAC} = 1.1V, -40mV < I _{SENP} – I _{SENN} < 40mV | -0.4 | -- | 0.4 | mV |
| Impedance at Positive Input | R _{ISENxP} | | 1 | -- | -- | MΩ |
| Current Sensing Resistor | R _{CS} | V _{IENP} – V _{IENN} = 10mV | 2.085 | 2.15 | 2.215 | kΩ |
| Input Range | V _{IEN_IN} | V _{DAC} = 1.1V, I _{SENP} – I _{SENN} | -40 | -- | 40 | mV |
| TON Setting | | | | | | |
| On-Time Setting | t _{ON} | V _{IN} = 19V, V _{DAC} = 1.3V, T _{ON} = 160ns | -- | 160 | -- | ns |
| Minimum Off time | t _{OFF} | V _{DAC} = 1V | -- | 165 | -- | ns |
| Protections | | | | | | |
| Under-Voltage Lockout Threshold | V _{UVLO} | Falling edge | 3.86 | 4.06 | 4.26 | V |
| | ΔV _{UVLO} | Rising edge hysteresis | -- | 190 | -- | mV |
| Over-Voltage Protection Threshold | V _{OV} | Respect to V _{DAC} voltage | V _{DAC} + 300 | V _{DAC} + 350 | V _{DAC} + 400 | mV |
| | | V _{DAC} < 1V | 1300 | 1350 | 1400 | mV |
| Under-Voltage Protection Threshold | V _{UV} | Respect to V _{DAC} voltage | V _{DAC} - 400 | V _{DAC} - 350 | V _{DAC} - 300 | mV |
| | | | | | | mV |
| Negative Voltage Protection Threshold | V _{NV} | | -100 | -50 | -- | mV |
| EN and VR_REDAY | | | | | | |
| EN Threshold | V _{IH} | | 0.7 | -- | -- | V |
| | V _{IL} | | -- | -- | 0.3 | V |
| Leakage Current of EN | | | -1 | -- | 1 | μA |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|--|----------------------|--|-------|-------|-------|---------|
| PGOOD Pull Low Voltage | VPGOOD | IVR_Ready = 10mA | -- | -- | 0.13 | V |
| Serial VID and VR_HOT | | | | | | |
| VCLK, VDIO | V _{IH} | Respect to INTEL Spec. with 50mV hysteresis | 0.65 | -- | -- | V |
| | V _{IL} | | -- | -- | 0.45 | |
| Leakage Current of VCLK, VDIO, $\overline{\text{ALERT}}$ and $\overline{\text{VR_HOT}}$ | I _{LEAK_IN} | | -1 | -- | 1 | μA |
| VDIO, $\overline{\text{ALERT}}$ and $\overline{\text{VR_HOT}}$ Pull Low Voltage | | I _{VDIO} = 10mA | -- | -- | 0.13 | V |
| | | I _{ALERT} = 10mA | | | | |
| | | I _{VR_HOT} = 10mA | | | | |
| VREF | | | | | | |
| VREF | VREF | | 0.595 | 0.6 | 0.605 | V |
| ADC | | | | | | |
| Digital IMON Set | V _{IMON} | V _{IMON} – V _{IMON_INI} = 0.8V, Auxiliary rail | -- | 255 | -- | Decimal |
| | | V _{IMON} – V _{IMON_INI} = 0.4V, Main rail | -- | 255 | -- | |
| Update Period | t _{IMON} | (Note 5) | -- | 125 | -- | μs |
| TSEN Threshold for Tmp_Zone[7] Transition | V _{TSEN} | 100°C | -- | 1.092 | -- | V |
| TSEN Threshold for Tmp_Zone[6] Transition | | 97°C | -- | 1.132 | -- | |
| TSEN Threshold for Tmp_Zone[5] Transition | | 94°C | -- | 1.176 | -- | |
| TSEN Threshold for Tmp_Zone[4] Transition | | 91°C | -- | 1.226 | -- | |
| TSEN Threshold for Tmp_Zone[3] Transition | | 88°C | -- | 1.283 | -- | |
| TSEN Threshold for Tmp_Zone[2] Transition | | 85°C | -- | 1.346 | -- | |
| TSEN Threshold for Tmp_Zone[1] Transition | | 82°C | -- | 1.418 | -- | |
| TSEN Threshold for Tmp_Zone[0] Transition | | 75°C | -- | 1.624 | -- | |
| Update Period | t _{TSEN} | (Note 5) | -- | 100 | -- | μs |
| PWM Driving Capability | | | | | | |
| PWM_x | RPWMsr | | -- | 30 | -- | Ω |
| | RPWMsk | | -- | 10 | -- | |
| Driver On-Resistance | | | | | | |
| UGATE _x Drive Source | RUGATE _{sr} | V _{BOOT} – V _{PHASE} Forced to 5V | -- | 1.7 | -- | Ω |
| UGATE _x Drive Sink | RUGATE _{sk} | V _{BOOT} – V _{PHASE} Forced to 5V | -- | 1.4 | -- | Ω |
| LGATE _x Drive Source | RLGATE _{sr} | I _{Source} = 100mA | -- | 1.6 | -- | Ω |
| LGATE _x Drive Sink | RLGATE _{sk} | I _{Sink} = 100mA | -- | 1.1 | -- | Ω |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---------------------------------|-------------------|---|-----|-----|-----|------|
| Dead-Time | | From LGATE falling to UGATE rising | | 30 | | ns |
| | | From UGATE falling to LGATE rising | | 20 | | |
| Internal Boost Diode Resistance | R _{BOOT} | PVCC to BOOTx, I _{BOOT} = 10mA | -- | 40 | 80 | Ω |

Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at $T_A = 25^\circ\text{C}$ with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

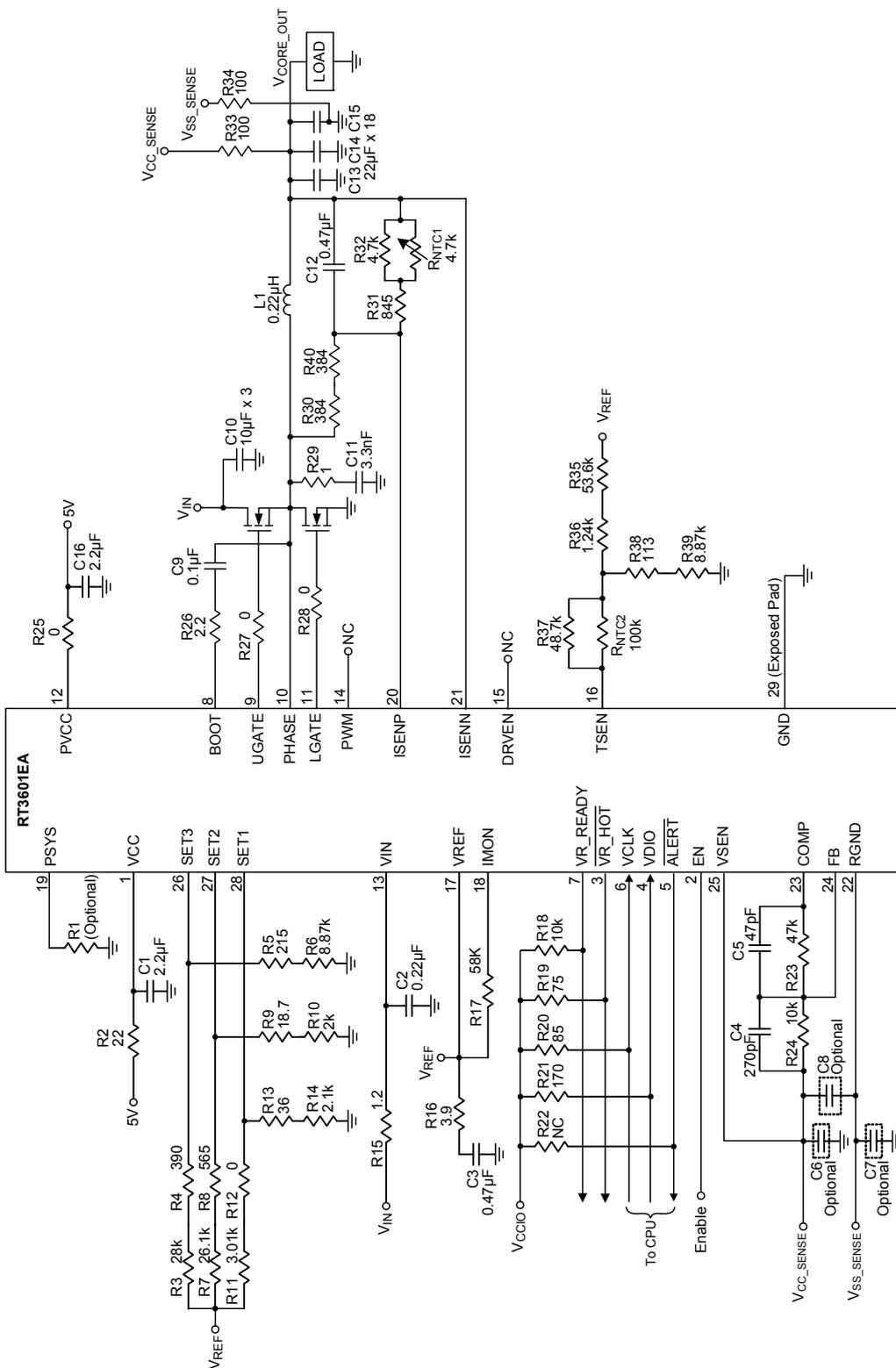
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

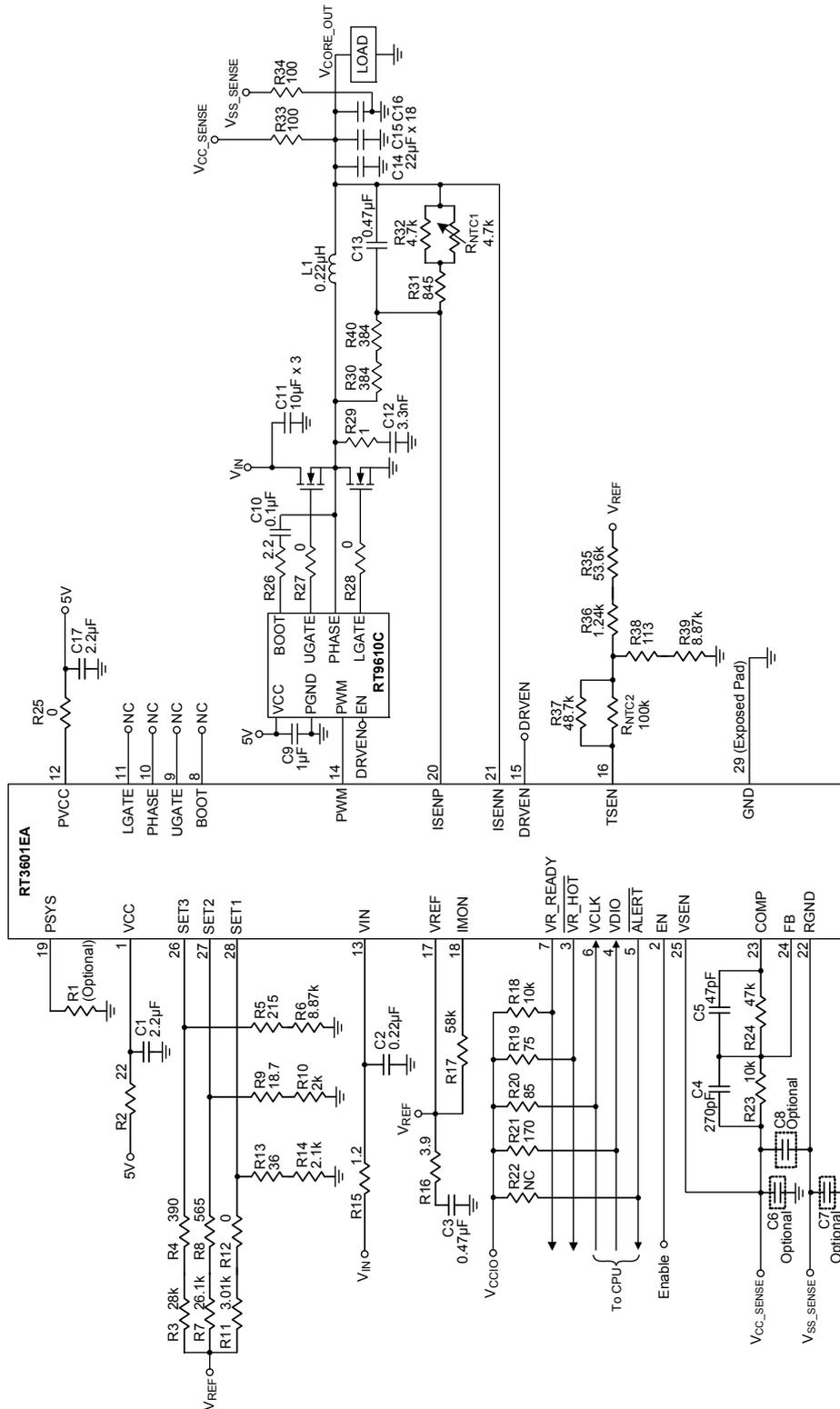
Note 5. Guarantee by design.

Typical Application Circuit

Using Embedded MOSFET Driver

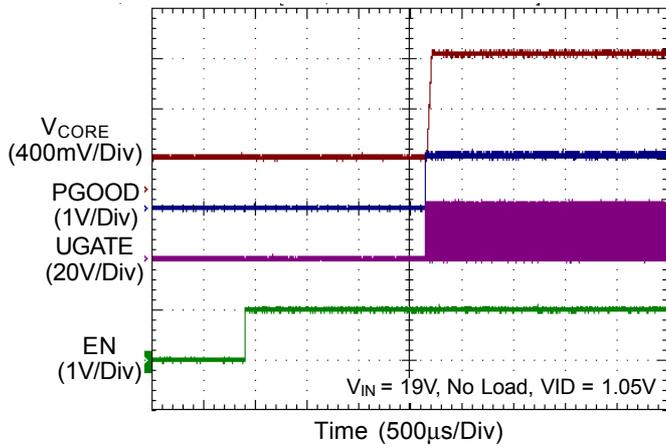


Using External MOSFET Driver

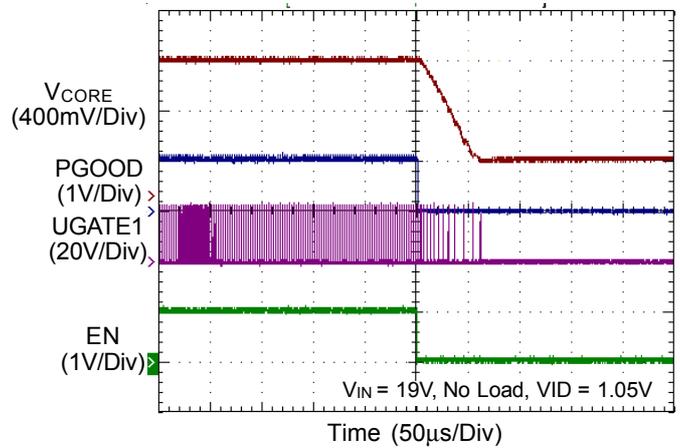


Typical Operating Characteristics

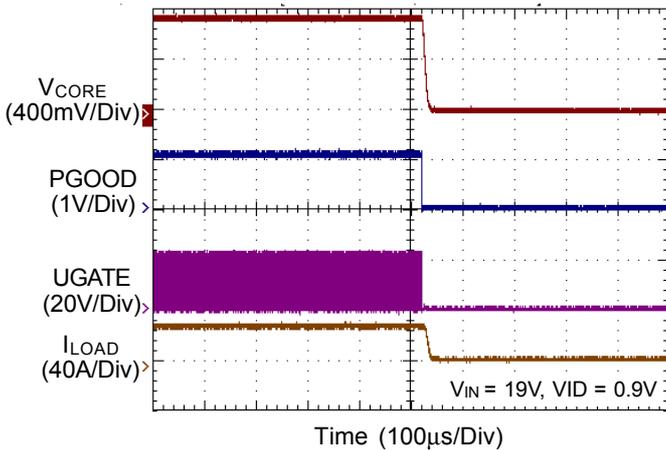
VR Power On from EN



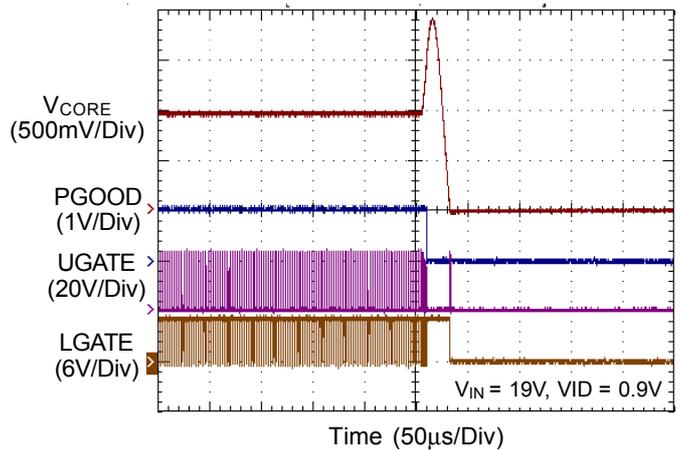
CORE VR Power Off from EN



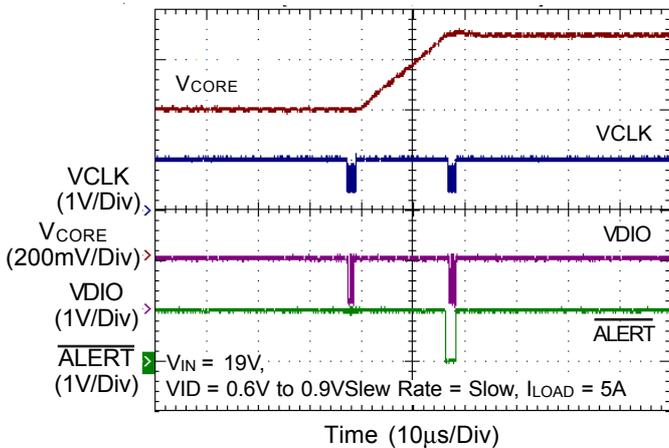
CORE VR OCP



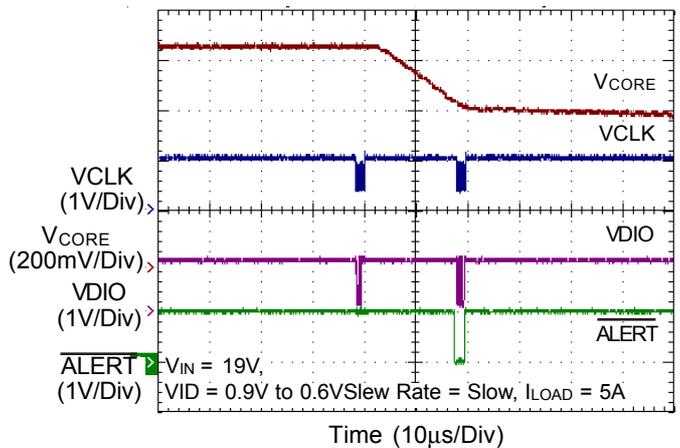
CORE VR OVP



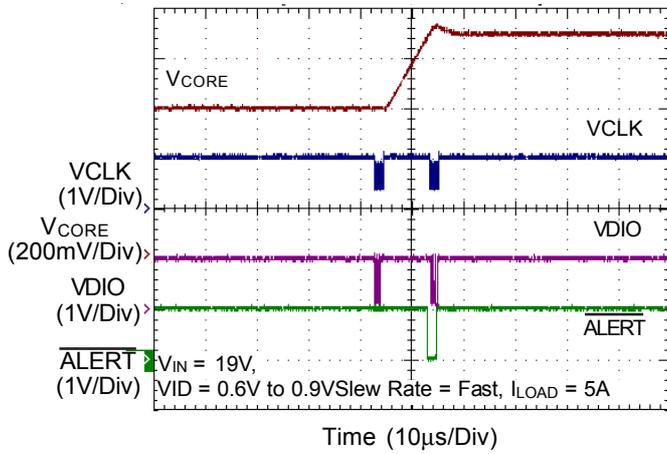
CORE VR Dynamic VID Up



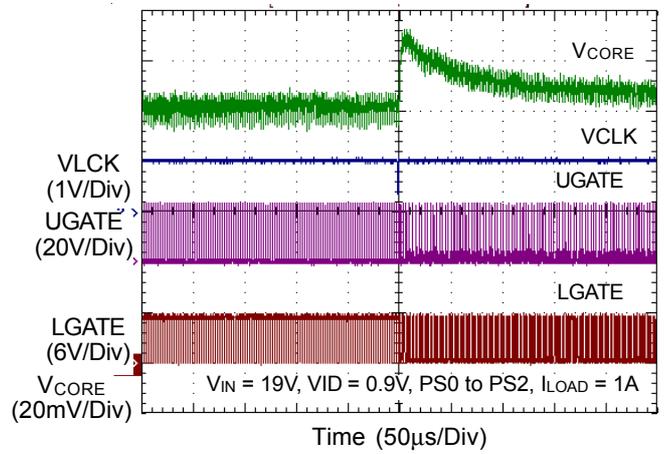
CORE VR Dynamic VID Down



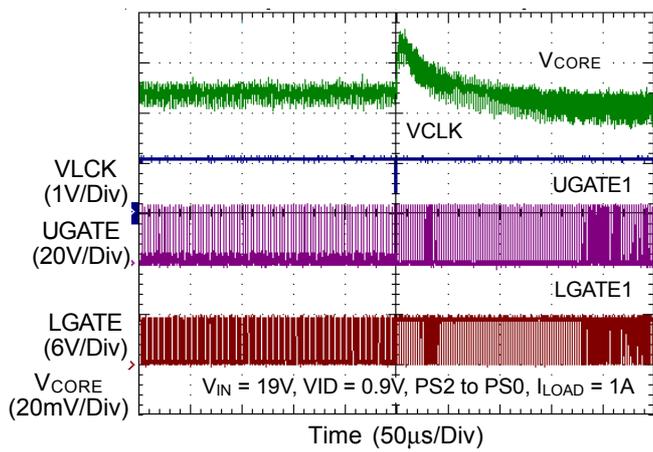
CORE VR Dynamic VID Up



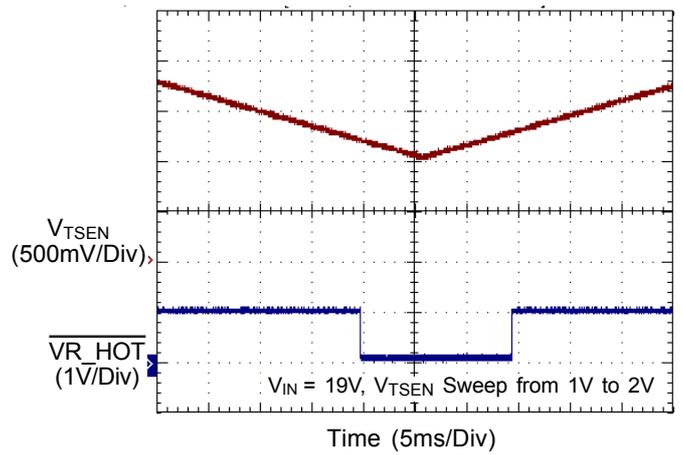
CORE VR Mode Transient



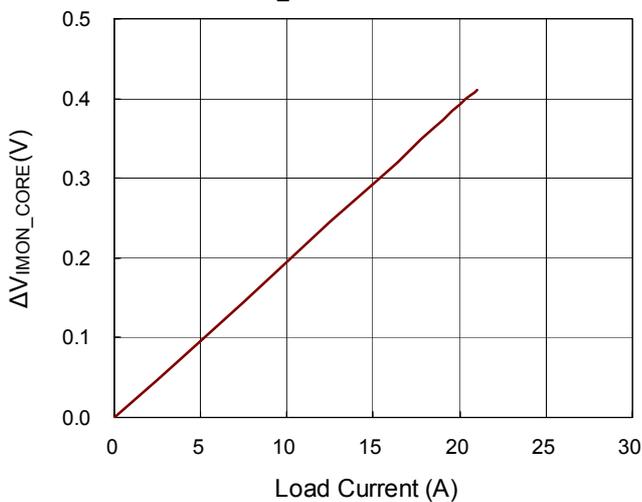
CORE VR Mode Transient



CORE VR Thermal Monitoring



ΔV_{IMON_CORE} vs. Load Current



Applications Information

The RT3601EA is a single phase synchronous Buck controller, designed to meet Intel IMVP8 compatible CPUs specification with a serial SVID control interface. The controller uses an ADC to implement all kinds of settings to save total pin number for easy use and increasing PCB space utilization. The RT3601EA is used in notebooks, desktop computers and servers.

General loop Function

G-NAVP™ Control Mode

The RT3601EA adopts the G-NAVP™ controller, which is a current mode constant on-time control with DC offset cancellation. The approach can not only improve DC offset problem for increasing system accuracy but also provide fast transient response. When current feedback signal reaches comp signal, the RT3601EA generates an on-time width to achieve PWM modulation. Figure 1 shows the basic G-NAVP™ behavior waveforms in continuous conduct mode (CCM).

Diode Emulation Mode (DEM)

As well-known, the dominate power loss is switching related loss during light load, hence VR needs to be operated in asynchronous mode (or called discontinuous conduct mode, DCM) to reduce switching related loss since switching frequency is dependent on loading in the asynchronous mode. The RT3601EA can operate in diode emulation mode (DEM) to improve light load efficiency. In DEM operation, the behavior of low-side MOSFET(s) needs to work like a diode, that is, the low-side MOSFET(s) will be turned on when the phase voltage is a negative value, i.e. the inductor current follows from Source to Drain of low-side MOSFET(s). And the low-side MOSFET(s) will be turned off when phase voltage is a positive value, i.e. reversed current is not allowed. Figure 2 shows the control behavior in DEM. Figure 3 shows the G-NAVP™ operation in DEM to illustrate the control behaviors. When the load decreases, the discharge time of output capacitors increases during UGATE and LGATE are turned off. Hence, the switching frequency and switching loss will be reduced to improve efficiency in light load condition.

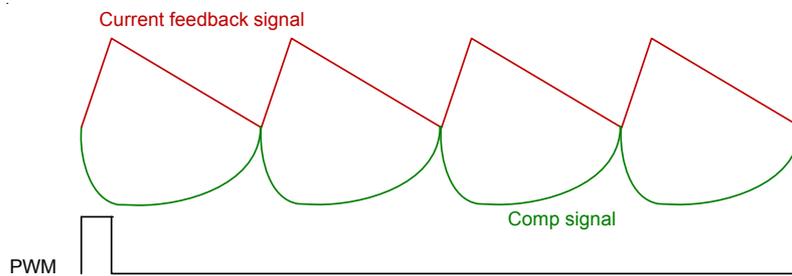


Figure 1 (a). G-NAVP™ Behavior Waveforms in CCM in Steady State

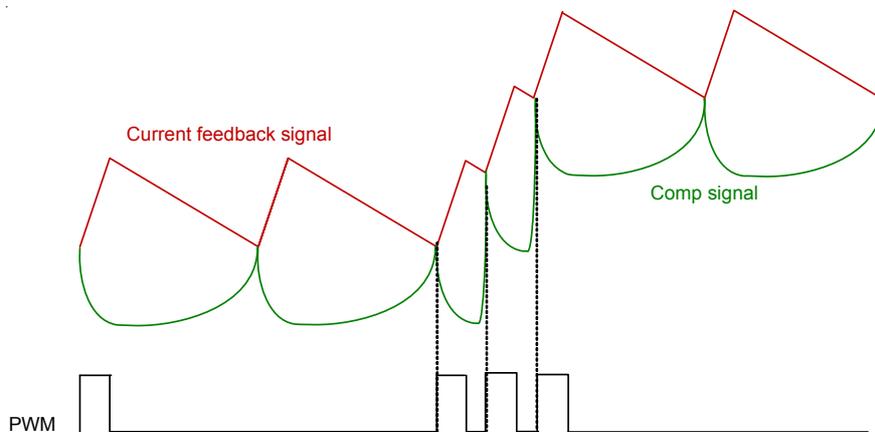


Figure 1 (b). G-NAVP™ Behavior Waveforms in CCM in Load Transient.

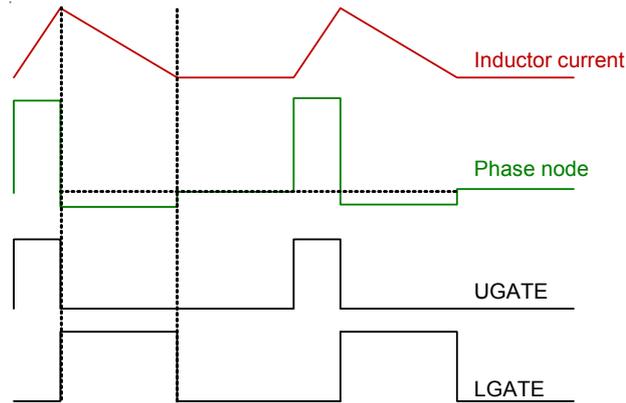


Figure 2. Diode Emulation Mode (DEM) in Steady State

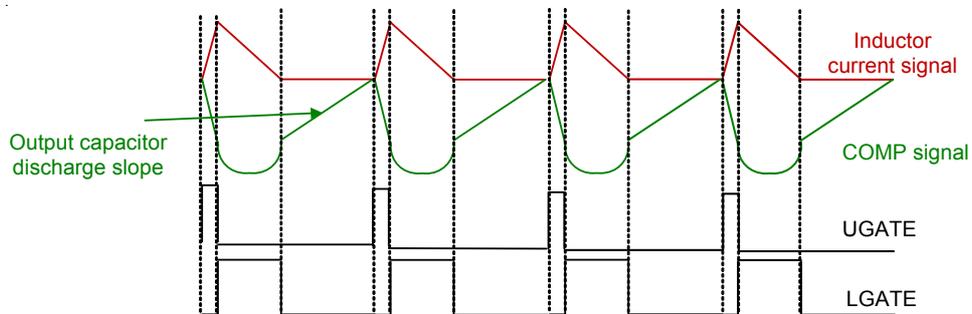
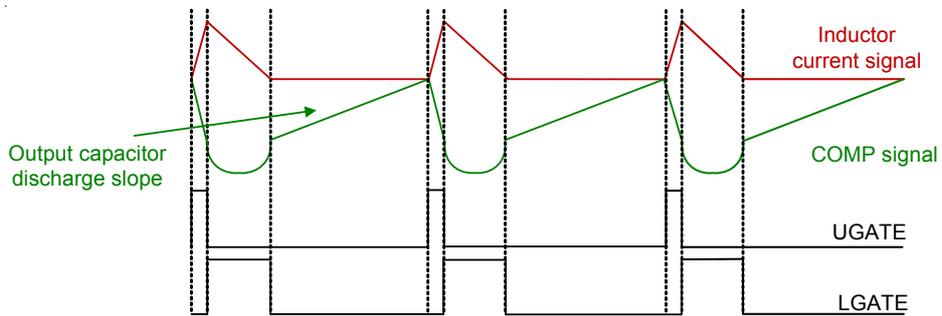


Figure 3. G-NAVP™ Operation in DEM. (a) : The load is lighter, output capacitor discharge slope is smaller and the switching frequency is lower. (b) : The load is increasing, output capacitor discharge slope is increased and switching frequency is increased, too.

Multi-Function Pin Setting Mechanism

For reducing total pin number of package, SET [1:3] pins adopt the multi-function pin setting mechanism in the RT3601EA. Figure 4 illustrates this operating mechanism for SET [1:3]. The voltage at VREF pin will be pulled up to 3.2V after power ready (POR). First, external voltage divider is used to set the Function1, and then internal current source 80μA is used to set the Function2. The setting voltage of Function1 and Function2 can be represented as

$$V_{Function1} = \frac{R2}{R1+R2} \times 3.2V$$

$$V_{Function2} = 80\mu A \times \frac{R1 \times R2}{R1+R2}$$

All function setting will be done within 500μs after power ready (POR), and the voltage at VREF pin will be fixed to 0.6V after all function setting over.

If $V_{Function1}$ and $V_{Function2}$ are determined, R1 and R2 can be calculated as follows :

$$R1 = \frac{3.2V \times V_{Function2}}{80\mu A \times V_{Function1}}$$

$$R2 = \frac{R1 \times V_{Function1}}{3.2V - V_{Function1}}$$

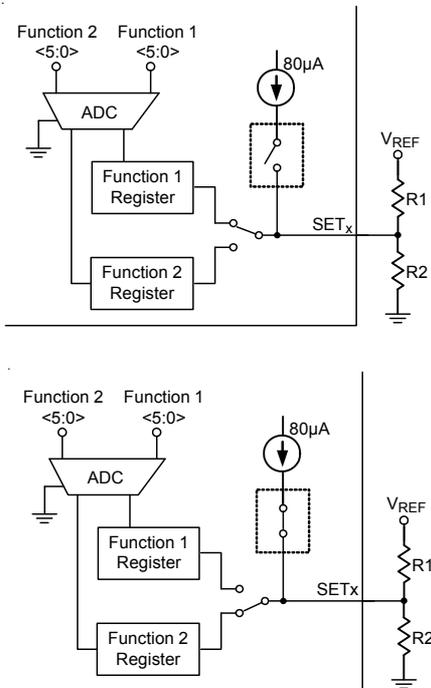


Figure 4. Multi-Function Pin Setting Mechanism for SET [1:3]

Connecting a R3 resistor from the SET[1:3] pin to the middle node of voltage divider can help to fine tune the set voltage of Function 2, which does not affect the set voltage of Function1. The Figure 5 shows the setting method and the set voltage of Function 1 and Function2 can be represented as :

$$V_{Function1} = \frac{R2}{R1+R2} \times 3.2V$$

$$V_{Function2} = 80\mu A \times \left(R3 + \frac{R1 \times R2}{R1+R2} \right)$$

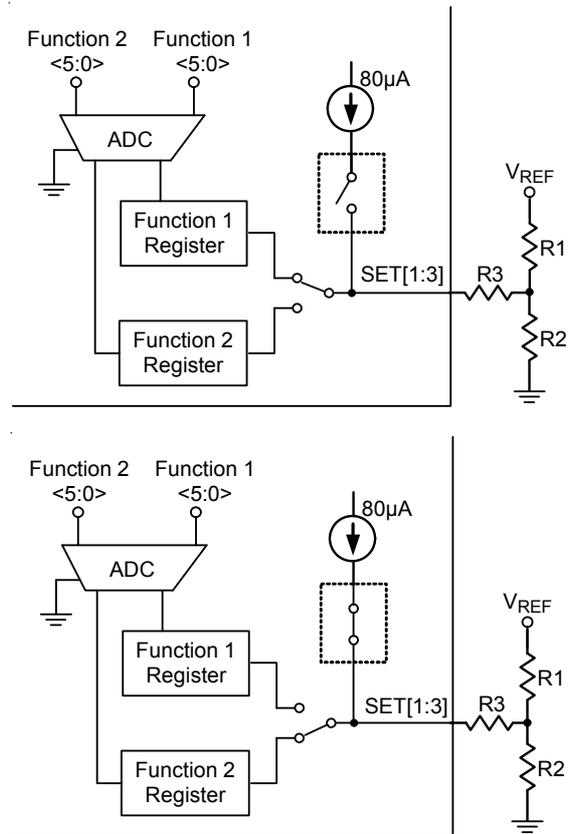


Figure 5. Multi-Function Pin Setting Mechanism with a R3 Resistor to Fine Tune the Set Voltage of Function2

Figure 6 shows operating mechanism for TSEN pins. There is only voltage divider Function to program VR. The internal current source is used to thermal sensing. The Function for program VR can be represented as

$$V_{Function1} = \frac{R2}{R1+R2} \times 3.2V$$

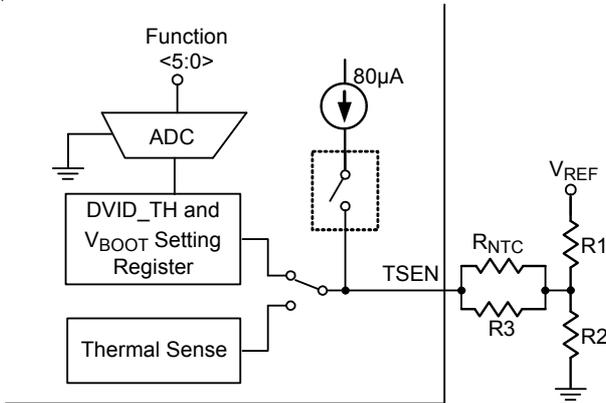


Figure 6. Multi-Function Pin Setting Mechanism for TSEN

TSEN and VR_HOT

The VR_HOT signal is an open-drain signal which is used for VR thermal protection. When the sensed voltage in each TSEN pin is less than 1.092, the VR_HOT signal will be pulled-low to notify CPU that the thermal protection needs to work. According to Intel VR definition, VR_HOT signal needs acting if VR power chain temperature exceeds 100°C. Placing an NTC thermistor at the hottest area in the VR power chain and its connection is shown in Figure 7, to design the TSEN network so that V_{TSEN} = 1.092V at 100°C. The resistance accuracy of TSEN network is recommended to be 1% or higher.

$$V_{TSEN} = 80\mu A \times (R_{NTC} // R3) + (R1 // R2)$$

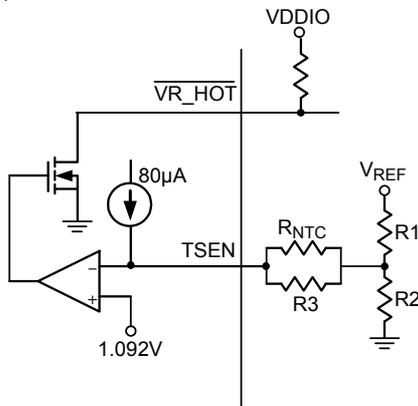


Figure 7. VR_HOT Circuit

Power Ready (POR) Detection

During start-up, the RT3601EA detects the voltage at the voltage input pins : V_{CC} and EN. When V_{CC} > 4.45V, the RT3601EA recognizes the power state of system to be ready (POR = high) and waits for enable command at the EN pin. After POR = high and V_{EN} > 0.7V, the RT3601EA enters start-up sequence. If V_{CC} drops below low threshold (POR = low), the RT3601EA enters power down sequence and all functions will be disabled. Normally, connecting system voltage V_{TT} (1.05V) to the EN pin is recommended. 2ms (max) after the chip has been enabled, the SVID circuitry will be ready. All the protection latches (OVP, OCP, UVP) will be cleared only by V_{CC}. The condition of V_{EN} = low will not clear these latches. Figure 8 and Figure 9 show the POR detection and the timing chart for POR process, respectively.

Under-Voltage Lockout (UVLO)

During normal operation, if the voltage at the VCC pin drops below POR threshold 3.86V (min), the VR triggers UVLO. The UVLO protection forces all high-side MOSFETs and low-side MOSFETs off by shutting down internal PWM logic drivers.

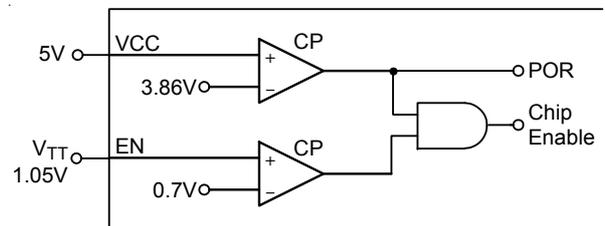


Figure 8. POR Detection

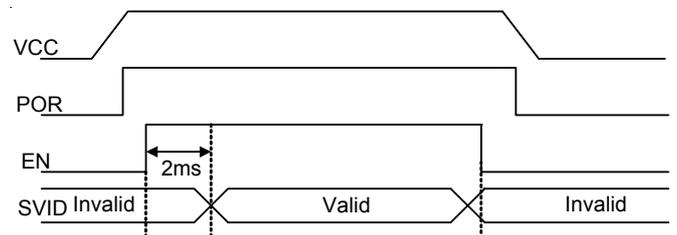


Figure 9. Timing Chart for POR Process

Switching Frequency Setting

The RT3601EA is one kind of constant on-time control. The patented CCRCOT (Constant Current Ripple COT) technology can generate an adaptive on-time with input voltage and VID code to obtain a constant current ripple, so that the output voltage ripple can be controlled nearly like a constant as different input and output voltages change.

The T_{ON} equation can be classified as below two regions.

$$V_{DAC} \geq 0.9$$

$$T_{ON} = \frac{26.2\mu \times V_{DAC}}{k_{TON} \times (V_{IN} - 0.9)} + 15n$$

$$0.3 < V_{DAC} < 0.9$$

$$T_{ON} = \frac{23.6\mu}{k_{TON} \times (V_{IN} - V_{DAC})} + 15n$$

where k_{TON} is a coefficient which can be selected by SET2, as shown in Table 3.

Table 2. SET1 Pin Setting for ICCMAX and AI Gain

| $V_{SET1} = V_{REF} \times \frac{R2}{R1+R2}$ | | | | AI Gain | ICCMAX (A) |
|--|---------|---------|------|---------|---------------|
| Min | Typical | Max | Unit | | |
| 3.75 | 25 | 46.25 | mV | 20 | 2 (OCP = 6x) |
| 54.25 | 75 | 95.75 | mV | | 4 (OCP = 6x) |
| 104.75 | 125 | 145.25 | mV | | 6 (OCP = 6x) |
| 155.25 | 175 | 194.75 | mV | | 8 (OCP = 6x) |
| 205.75 | 225 | 244.25 | mV | | 10 (OCP = 4x) |
| 256.25 | 275 | 293.75 | mV | | 12 (OCP = 4x) |
| 306.75 | 325 | 343.25 | mV | | 14 (OCP = 4x) |
| 357.25 | 375 | 392.75 | mV | | 16 (OCP = 4x) |
| 407.75 | 425 | 442.25 | mV | | 18 (OCP = 3x) |
| 458.25 | 475 | 491.75 | mV | | 20 (OCP = 3x) |
| 508.75 | 525 | 541.25 | mV | | 22 (OCP = 3x) |
| 559.25 | 575 | 590.75 | mV | | 24 (OCP = 3x) |
| 609.75 | 625 | 640.25 | mV | | 26 (OCP = 2x) |
| 660.25 | 675 | 689.75 | mV | | 28 (OCP = 2x) |
| 710.75 | 725 | 739.25 | mV | | 30 (OCP = 2x) |
| 761.25 | 775 | 788.75 | mV | | 32 (OCP = 2x) |
| 811.75 | 825 | 838.25 | mV | 80 | 2 (OCP = 6x) |
| 862.25 | 875 | 887.75 | mV | | 4 (OCP = 6x) |
| 912.75 | 925 | 937.25 | mV | | 6 (OCP = 6x) |
| 963.25 | 975 | 986.75 | mV | | 8 (OCP = 6x) |
| 1013.75 | 1025 | 1036.25 | mV | | 10 (OCP = 4x) |
| 1064.25 | 1075 | 1085.75 | mV | | 12 (OCP = 4x) |
| 1114.75 | 1125 | 1135.25 | mV | | 14 (OCP = 4x) |
| 1165.25 | 1175 | 1184.75 | mV | | 16 (OCP = 4x) |
| 1215.75 | 1225 | 1234.25 | mV | | 18 (OCP = 3x) |
| 1266.25 | 1275 | 1283.75 | mV | | 20 (OCP = 3x) |
| 1316.75 | 1325 | 1333.25 | mV | | 22 (OCP = 3x) |
| 1367.25 | 1375 | 1382.75 | mV | | 24 (OCP = 3x) |
| 1417.75 | 1425 | 1432.25 | mV | | 26 (OCP = 2x) |
| 1468.25 | 1475 | 1481.75 | mV | | 28 (OCP = 2x) |
| 1518.75 | 1525 | 1531.25 | mV | | 30 (OCP = 2x) |
| 1569.25 | 1575 | 1580.75 | mV | | 32 (OCP = 2x) |

Table 3. SET2 Pin Setting for k_{TON} and OCS

| $V_{SET2} = V_{REF} \times \frac{R2}{R1+R2}$ | | | | TONSET (k _{TON}) | OCS (%) |
|--|---------|---------|------|----------------------------|---------|
| Min | Typical | Max | Unit | | |
| 3.75 | 25 | 46.25 | mV | 15 | 120 |
| 54.25 | 75 | 95.75 | mV | | 140 |
| 104.75 | 125 | 145.25 | mV | | 160 |
| 155.25 | 175 | 194.75 | mV | | 180 |
| 205.75 | 225 | 244.25 | mV | 13 | 120 |
| 256.25 | 275 | 293.75 | mV | | 140 |
| 306.75 | 325 | 343.25 | mV | | 160 |
| 357.25 | 375 | 392.75 | mV | | 180 |
| 407.75 | 425 | 442.25 | mV | 12 | 120 |
| 458.25 | 475 | 491.75 | mV | | 140 |
| 508.75 | 525 | 541.25 | mV | | 160 |
| 559.25 | 575 | 590.75 | mV | | 180 |
| 609.75 | 625 | 640.25 | mV | 11 | 120 |
| 660.25 | 675 | 689.75 | mV | | 140 |
| 710.75 | 725 | 739.25 | mV | | 160 |
| 761.25 | 775 | 788.75 | mV | | 180 |
| 811.75 | 825 | 838.25 | mV | 10 | 120 |
| 862.25 | 875 | 887.75 | mV | | 140 |
| 912.75 | 925 | 937.25 | mV | | 160 |
| 963.25 | 975 | 986.75 | mV | | 180 |
| 1013.75 | 1025 | 1036.25 | mV | 9 | 120 |
| 1064.25 | 1075 | 1085.75 | mV | | 140 |
| 1114.75 | 1125 | 1135.25 | mV | | 160 |
| 1165.25 | 1175 | 1184.75 | mV | | 180 |
| 1215.75 | 1225 | 1234.25 | mV | 8 | 120 |
| 1266.25 | 1275 | 1283.75 | mV | | 140 |
| 1316.75 | 1325 | 1333.25 | mV | | 160 |
| 1367.25 | 1375 | 1382.75 | mV | | 180 |
| 1417.75 | 1425 | 1432.25 | mV | 7 | 120 |
| 1468.25 | 1475 | 1481.75 | mV | | 140 |
| 1518.75 | 1525 | 1531.25 | mV | | 160 |
| 1569.25 | 1575 | 1580.75 | mV | | 180 |

For better efficiency of the given load range, the maximum switching frequency is suggested to be :

$$F_{SW(MAX)} = \frac{VID1 + I_{ccTDC} \cdot (DCR + R_{ON_LS,max} - R_{LL})}{[V_{IN(MAX)} + I_{ccTDC} \cdot (R_{ON_LS,max} - R_{ON_HS,max})] \cdot (T_{ON} - T_D + T_{ON,VAR}) + I_{ccTDC} \cdot R_{ON_LS,max} \cdot T_D}$$

where $F_{SW(MAX)}$ is the maximum switching frequency, VID1 is the typical VID of application, $V_{IN(MAX)}$ is the maximum application input voltage, I_{ccTDC} is the thermal design current of application. The $R_{ON_HS,max}$ is the maximum equivalent high-side $R_{DS(ON)}$, $R_{ON_LS,max}$ is the maximum equivalent low-side $R_{DS(ON)}$. T_D is the summation of the high-side MOSFET delay time and the rising time, $T_{ON,VAR}$ is the T_{ON} variation value. DCR is the inductor DCR, and R_{LL} is the loadline setting. In addition, Richtek provides a Microsoft Excel-based spreadsheet to help design the R_{TON} for the RT3601EA.

When load increases, on-time keeps constant. The off-time width will be reduced so that loading can load more power from input terminal to regulate output voltage. Hence, the loading current usually increases in case the switching frequency also increases. Higher switching frequency operation can reduce power components' size and PCB space, trading off the whole efficiency since switching related loss increases, vice versa.

Current Sense

In the RT3601EA, the current signal is used for load-line setting and over-current protection (OCP). The inductor current sense method adopts the lossless current sensing for allowing high efficiency as illustrated in Figure 10. If RC network time constant matches inductor time constant L_x/DCR , an expected load transient waveform can be designed. If $R_x C_x$ network time constant is larger than inductor time constant L_x/DCR , V_{CORE} waveform has a sluggish droop during load transient. If $R_x C_x$ network is smaller than inductor time constant L_x/DCR , a worst V_{CORE} waveform will sag to create an undershooting to fail the specification. R_x is highly recommended as two 0603 size resistors in series to enhance the I_{OUT} reporting accuracy. C_x is suggested X7R type for the application. Figure 11 shows the variety $R_x C_x$ constant corresponding to the output waveforms.

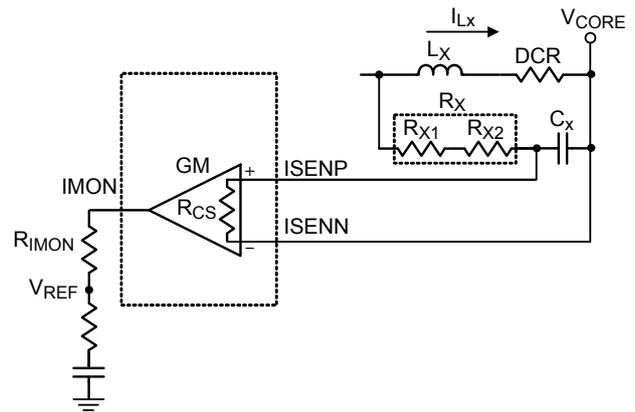


Figure 10. Lossless Current Sense Method for Single Phase

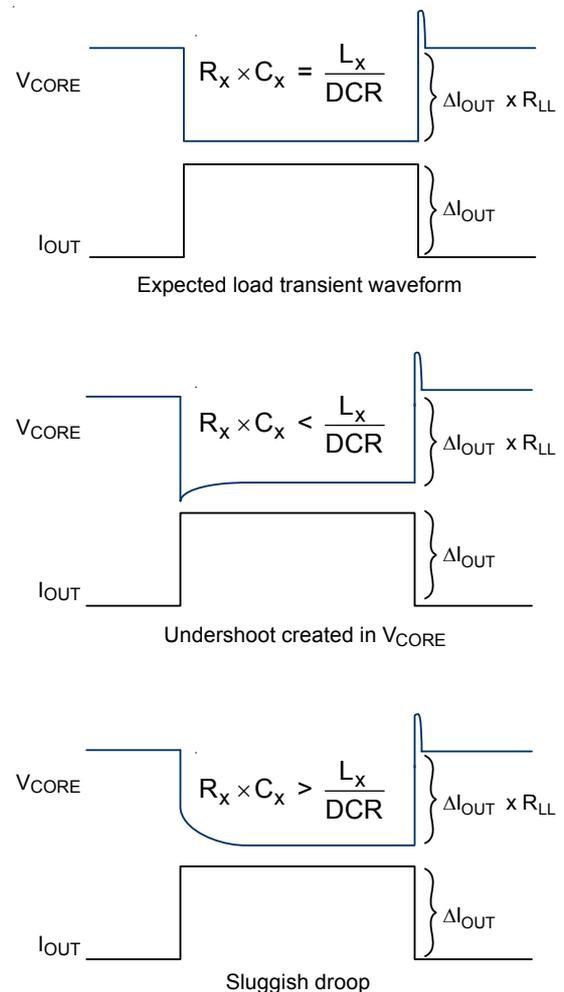


Figure 11. All Kind of $R_x C_x$ Constants

Thermal Compensation for Current Sense

Since the copper wire of inductor has a positive temperature coefficient. And hence, temperature compensation is necessary for the lossless inductor current sense. For single phase thermal compensation, Figure 12. shows a not only simple but also effective way to compensate temperature variation. An NTC thermistor is put in the current sensing network and it can be used to compensate DCR variation due to temperature is changed.

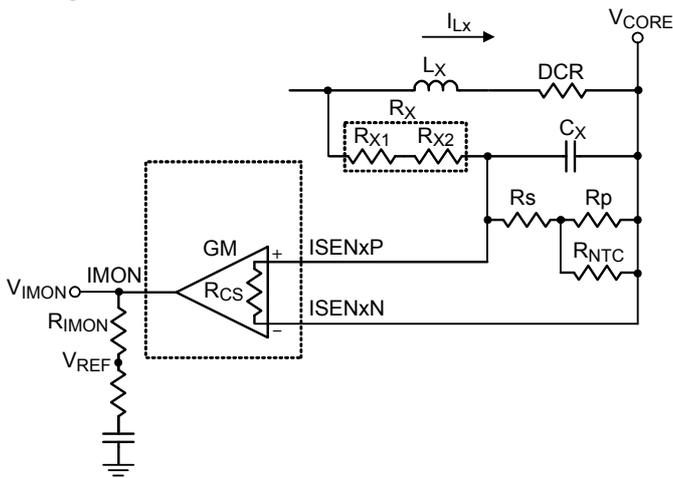


Figure 12. Thermal Compensation method for Single Phase

The current sense network equation is as follows :

$$\Delta V_{IMON} = V_{IMON} - V_{REF} = \frac{I_{LX} \times DCR \times \frac{R_S + (R_P // R_{NTC})}{R_X + (R_S + R_P // R_{NTC})}}{R_{CS}} \times R_{IMON}$$

Usually, R_P is set equal to $R_{NTC} (25^\circ C)$. R_S is selected to linearize the NTC's temperature characteristic. For a given NTC, design is to get R_X and R_S to compensate the temperature variation of the sense resistor.

Let

$$R_{EQU} = R_S + (R_P // R_{NTC})$$

According to current sense network, the corresponding equation is represented as follows :

$$\frac{L_X}{DCR} = C_X \times \frac{R_{EQU} \times R_X}{R_{EQU} + R_X}$$

Next, let

$$m = \frac{L_X}{DCR \times C_X}$$

Then

$$m \times \left(R_X + R_S + \frac{R_{NTC} \times R_P}{R_{NTC} + R_P} \right) = R_X \times \left(R_S + \frac{R_{NTC} \times R_P}{R_{NTC} + R_P} \right)$$

Step1 : Given the two system temperature T_R and T_H at which are compensated.

Step2 : Two equations can be listed as

$$m(T_R) \times \left(R_X + R_S + \frac{R_{NTC}(T_R) \times R_P}{R_{NTC}(T_R) + R_P} \right) = R_X \times \left(R_S + \frac{R_{NTC}(T_R) \times R_P}{R_{NTC}(T_R) + R_P} \right)$$

$$m(T_H) \times \left(R_X + R_S + \frac{R_{NTC}(T_H) \times R_P}{R_{NTC}(T_H) + R_P} \right) = R_X \times \left(R_S + \frac{R_{NTC}(T_H) \times R_P}{R_{NTC}(T_H) + R_P} \right)$$

Step3 : Usually R_P is set to equal to $R_{NTC} (T_R)$. And hence, there are two equations and two unknowns, R_X and R_S can be found out.

Current Monitor, IMON

The RT3601EA includes a current monitor (IMON) function which can be used to detect over-current protection and maximum processor current ICCMAX, and also sets a part of current gain in the load-line setting. It produces an analog voltage proportional to output current between the IMON and VREF pins.

Load-Line (Droop) Setting

The G-NAVP™ topology can set load-line (droop) via the current loop and voltage loop, the load-line is a slope between load current I_{CC} and output voltage V_{sen} as shown in Figure 13. Figure 14 shows the voltage control and current loop. By using both loops, the load-line (droop) can be set easily. The load-line set equation is :

$$R_{LL} = \frac{A_i}{A_v} = \frac{\frac{k_i}{2} \times \frac{DCR}{R_{CS}} \times R_{OUT}}{\frac{R_2}{R_1}} = \frac{\frac{k_i}{2} \times DCR}{\frac{R_2}{R_1}} \text{ (m}\Omega\text{)}$$

where $R_{OUT} = R_{CS}$

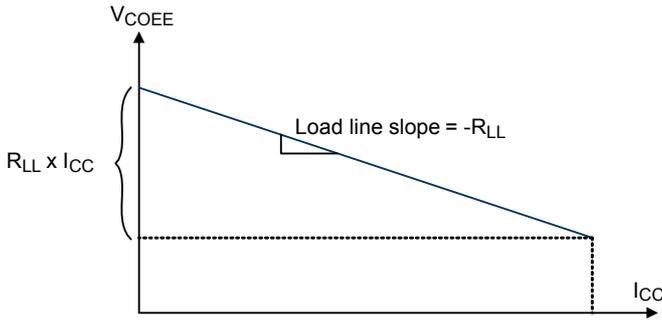


Figure 13. Load-Line (Droop)

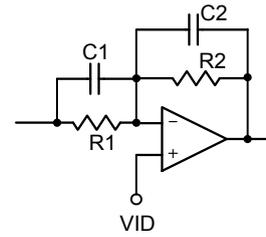


Figure 15. Type I compensator

Differential Remote Sense Setting

The VR provides differential remote-sense inputs to eliminate the effects of voltage drops along the PC board traces, CPU internal power routes and socket contacts for Main and AUX1 rails. The CPU contains on-die sense pins, V_{CC_SENSE} and V_{SS_SENSE}. Connect RGND to V_{SS_SENSE} and connect FB to V_{CC_SENSE} with a resistor to build the negative input path of the error amplifier as shown in Figure 16. The V_{DAC} and the precision voltage reference are referred to RGND for accurate remote sensing.

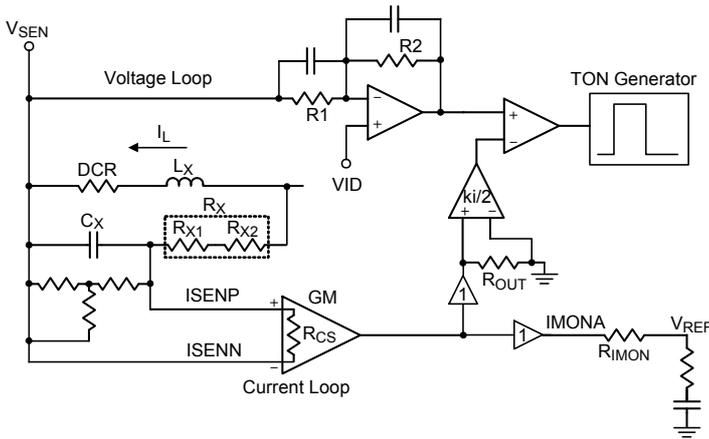


Figure 14. Voltage Loop and Current Loop

Compensator Design

The compensator of the RT3601EA doesn't need a complex type II or type III compensator to optimize control loop performance. It can adopt a simple type I compensator (one pole, one zero) in the G-NAVP™ topology to achieve constant output impedance design for Intel IMVP8 ACLL specification. The one pole one zero compensator is shown as Figure 15. The transfer function of compensator should be design as following transfer function to achieve constant output impedance, i.e. Zo(s) = load-line slope in the entire frequency range :

$$G_{CON}(S) \approx \frac{A_I}{R_{LL}} \frac{1 + \frac{s}{\omega \times f_{SW}}}{1 + \frac{s}{\omega_{ESR}}}$$

where A_I is current loop gain, R_{LL} is load-line, f_{SW} is switching frequency and ω_{ESR} is a pole that should be located at 1/(C_{OUT} x ESR). Then, the C1 and C2 should be designed as follows :

$$C1 = \frac{1}{R1 \times \pi \times f_{SW}} \quad C2 = \frac{C_{OUT} \times ESR}{R2}$$

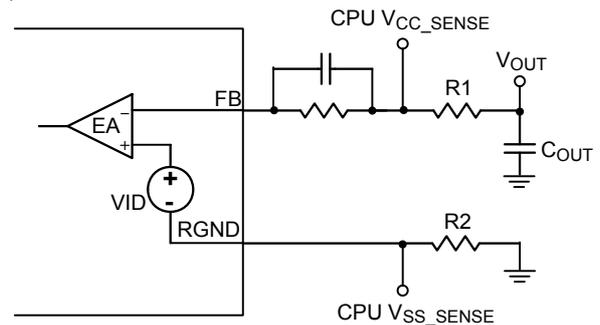


Figure 16. Remote Sensing Circuit

Maximum Processor Current Setting, ICCMAX

The maximum processor current ICCMAX can be set by SET1 pin. ICCMAX register is set by an external voltage divider with the multi-function mechanism. Table 2 shows the ICCMAX setting on SET1 pin.

Table 4. SET1 Pin Setting for PSYS and DVID_Width

| $\Delta V_{SET1} = 80\mu A \times \frac{R1 \times R2}{R1 + R2}$ | | | | PSYS | DVID_Width (μs) |
|---|---------|--------|------|---------|------------------------|
| Min | Typical | Max | Unit | | |
| 5.5 | 100 | 194.5 | mV | Enable | 5.36 |
| 209.5 | 300 | 390.5 | mV | Enable | 4.69 |
| 413.5 | 500 | 586.5 | mV | Enable | 2.68 |
| 617.5 | 700 | 782.5 | mV | Enable | 2.01 |
| 821.5 | 900 | 978.5 | mV | Disable | 5.36 |
| 1025.5 | 1100 | 1174.5 | mV | Disable | 4.69 |
| 1229.5 | 1300 | 1370.5 | mV | Disable | 2.68 |
| 1433.5 | 1500 | 1566.5 | mV | Disable | 2.01 |

Table 5. TSEN Setting for DVID_TH and VBOOT

| $V_{TSEN} = V_{REF} \times \frac{R2}{R1+R2}$ | | | | DVID_TH (mV) | VBOOT (V) |
|--|---------|------|------|--------------|-----------|
| Min | Typical | Max | Unit | | |
| 4 | 50 | 96 | mV | 15 | 0 |
| 105 | 150 | 195 | mV | | 1.05 |
| 206 | 250 | 294 | mV | | 1.2 |
| 307 | 350 | 393 | mV | | 1.35 |
| 408 | 450 | 492 | mV | 30 | 0 |
| 509 | 550 | 591 | mV | | 1.05 |
| 610 | 650 | 690 | mV | | 1.2 |
| 711 | 750 | 789 | mV | | 1.35 |
| 812 | 850 | 888 | mV | 60 | 0 |
| 913 | 950 | 987 | mV | | 1.05 |
| 1014 | 1050 | 1086 | mV | | 1.2 |
| 1115 | 1150 | 1185 | mV | | 1.35 |
| 1216 | 1250 | 1284 | mV | Disable | 0 |
| 1317 | 1350 | 1383 | mV | | 1.05 |
| 1418 | 1450 | 1482 | mV | | 1.2 |
| 1519 | 1550 | 1581 | mV | | 1.35 |

Dynamic VID (DVID) Compensation

When VID transition event occurs, a charge current will be generated in the loop to cause DVID performance is deteriorated by this induced charge current, the phenomenon is called droop effect. The droop effect is shown in Figure 17. When VID up transition occurs, the output capacitor will be charged by inductor current. Since current signal is sensed in inductor, an induced charge current will appear in control loop. The induced charge current will produce a voltage drop in R1 to cause output voltage to have a droop effect. Due to this, VID transition performance will be deteriorated.

The RT3601EA provides a DVID compensation function. By the DVID compensation to cancel the real induced charge current signal and the virtual charge current signal is defined in Figure 18. Figure 19 shows the operation of cancelling droop effect. A virtual charge current signal is established first and then VID signal plus virtual charge current signal to be generated on the FB pin. Hence, an induced charge current signal flows to R1 and is cancelled to reduce droop effect.

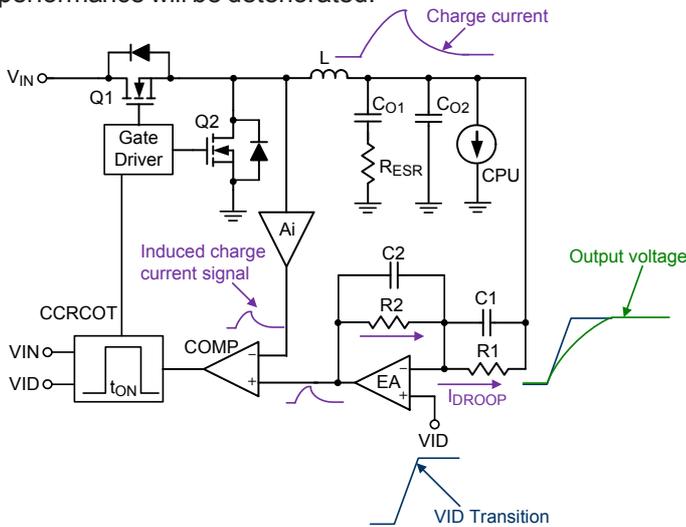


Figure 17. Droop Effect in VID transition

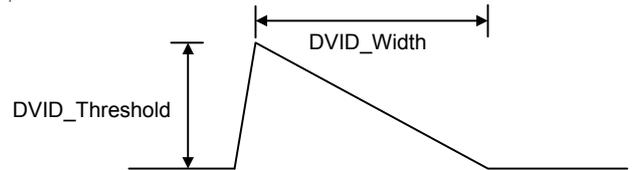


Figure 18. Definition of Virtual Charge Current Signal

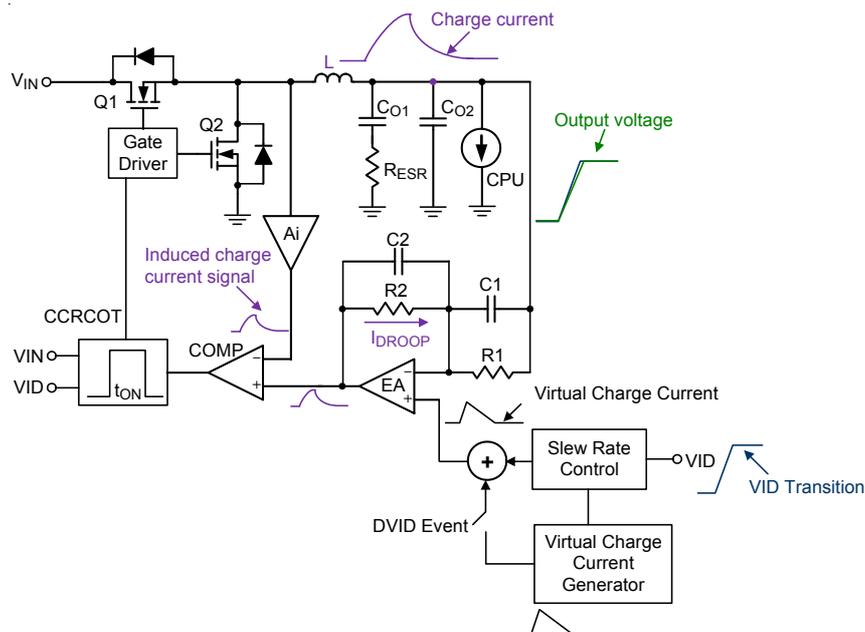


Figure 19. DVID Compensation

System Input Power Monitor, PSYS

The RT3601EA provides PSYS function to monitor total platform system power, and the obtained information will be provided directly to the CPU via the SVID interface. The PSYS function can be enabled/disabled by the SET1 pin. The PSYS function can be described as in Figure 20. When the maximum PSYS voltage $V_{PSYS} = 3.2V$, the RT3601EA will generate an 8-bit code, FF, which will be stored in the 1Bh register. To choose the resistor value R, for example, if the maximum current from the PSYS "Meter" $I = 320\mu A$ in conjunction with $V_{PSYS} = 3.2V$, $R = V_{PSYS} / I = 10k\Omega$ can be obtained.

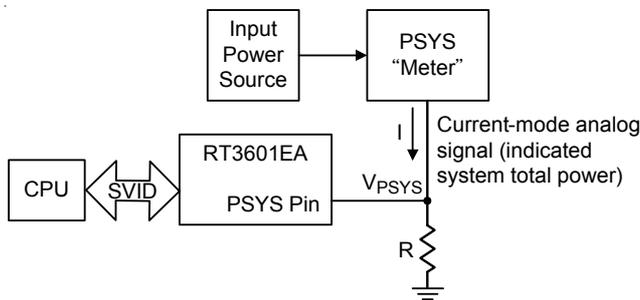


Figure 20. PSYS Function Block Diagram

Table 4 and Table 5 show the DVID width, DVID threshold, PSYS function and VBOOT on SET1 and TSEN. For example, 15mV DVID threshold and 2.68 μs DVID width are designed (VBOOT set as 1.05V, PSYS function is disable). According to the Table 4 and Table 5, the DVID threshold set voltage should be between 0.1286V and 0.1316V and DVID width set voltage should be between 0.1351V to 0.1651V. Please note that a high accuracy resistor is needed for this setting, <1% error tolerance is recommended.

Ramp Compensation

The G-NAVP™ topology is one type of ripple based control that has fast transient response and can lower BOM cost. However, ripple based control usually has no good noise immunity. The RT3601EA provides the ramp compensation to increase noise immunity and reduce jitter at the switching node. Figure 21 shows the ramp compensation.

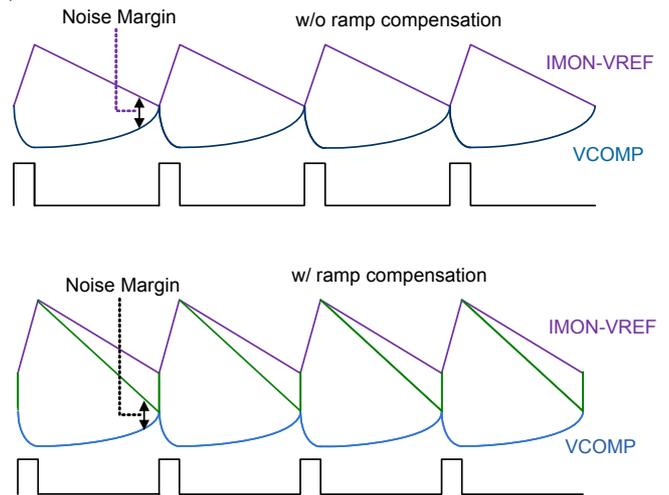


Figure 21. Ramp Compensation

Quick Response (QR) Mechanism

When the transient load step-up becomes quite large, it is difficult for loop response to meet the energy transfer. Hence, that output voltage generate undershoot to fail specification. The RT3601EA has Quick Response (QR) mechanism being able to improve this issue. It adopts a nonlinear control mechanism which can disable interleaving function and simultaneously turn on all UGATE one pulse at instantaneous step-up transient load to restrain the output voltage drooping. Figure 22 shows the QR behavior.

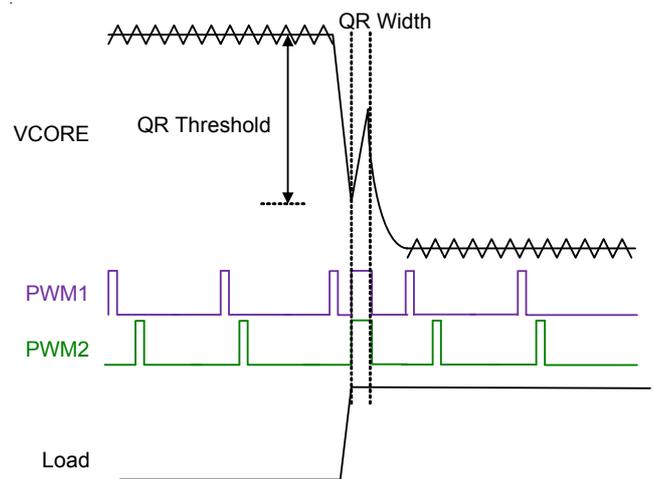


Figure 22. Quick Response Mechanism

The output voltage signal behavior needs to be detected so that QR mechanism can be triggered. The output voltage signal is via a remote sense line to connect at the VSEN pin which is shown in Figure 23. The QR mechanism needs to set QR width and QR threshold. Both definitions are shown in Figure 22. A proper QR mechanism set can meet different applications. The SET3 pin can set QR threshold and QR width by an external voltage divider with the multi-function mechanism. Table 6 shows the QR_TH and QR_WIDTH on the SET3 pin.

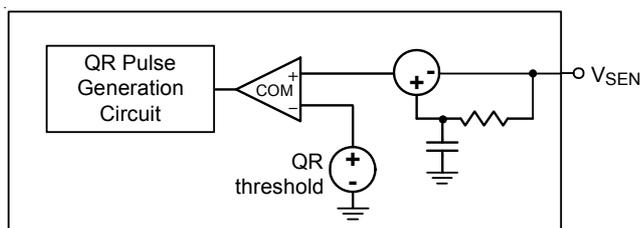


Figure 23. Simplified QR Trigger schematic

Table 6. SET3 Pin Setting for QR Threshold and QR Width

| $V_{SET3} = V_{REF} \times \frac{R2}{R1+R2}$ | | | | QR_TH (mV) | | QR_WIDTH (% of On-Time) |
|--|---------|---------|------|------------|---------|----------------------------|
| Min | Typical | Max | Unit | PS0 | PS1 | |
| 3.75 | 25 | 46.25 | mV | Disable | Disable | 160% |
| 54.25 | 75 | 95.75 | mV | | | 130% |
| 104.75 | 125 | 145.25 | mV | | | 100% |
| 155.25 | 175 | 194.75 | mV | | | 70% |
| 205.75 | 225 | 244.25 | mV | 10 | 10 | 160% |
| 256.25 | 275 | 293.75 | mV | | | 130% |
| 306.75 | 325 | 343.25 | mV | | | 100% |
| 357.25 | 375 | 392.75 | mV | | | 70% |
| 407.75 | 425 | 442.25 | mV | 15 | 15 | 160% |
| 458.25 | 475 | 491.75 | mV | | | 130% |
| 508.75 | 525 | 541.25 | mV | | | 100% |
| 559.25 | 575 | 590.75 | mV | | | 70% |
| 609.75 | 625 | 640.25 | mV | 20 | 20 | 160% |
| 660.25 | 675 | 689.75 | mV | | | 130% |
| 710.75 | 725 | 739.25 | mV | | | 100% |
| 761.25 | 775 | 788.75 | mV | | | 70% |
| 811.75 | 825 | 838.25 | mV | 25 | 25 | 160% |
| 862.25 | 875 | 887.75 | mV | | | 130% |
| 912.75 | 925 | 937.25 | mV | | | 100% |
| 963.25 | 975 | 986.75 | mV | | | 70% |
| 1013.75 | 1025 | 1036.25 | mV | 30 | 30 | 160% |
| 1064.25 | 1075 | 1085.75 | mV | | | 130% |
| 1114.75 | 1125 | 1135.25 | mV | | | 100% |
| 1165.25 | 1175 | 1184.75 | mV | | | 70% |
| 1215.75 | 1225 | 1234.25 | mV | 35 | 35 | 160% |
| 1266.25 | 1275 | 1283.75 | mV | | | 130% |
| 1316.75 | 1325 | 1333.25 | mV | | | 100% |
| 1367.25 | 1375 | 1382.75 | mV | | | 70% |
| 1417.75 | 1425 | 1432.25 | mV | 40 | 40 | 160% |
| 1468.25 | 1475 | 1481.75 | mV | | | 130% |
| 1518.75 | 1525 | 1531.25 | mV | | | 100% |
| 1569.25 | 1575 | 1580.75 | mV | | | 70% |

For example, 20mV QR threshold and 0.7 x TON QR width are set. According to Table 6, the set voltage should be between 0.7607V and 0.7907V. Please note that a high accuracy resistor is needed for this setting accuracy, <1% error tolerance is recommended.

Zero Load-Line Setting and Anti-overshoot function

The SET2 pin can be enabled/disabled zero load-line function and can be enabled/disabled anti-overshoot function. Table 7 and Table 8 show the zero load-line function, anti-overshoot function, IPSK and anti-overshoot threshold on SET2 pin and SET3 pin.

When DVID slew rate increases, loop response is difficult to meet energy transfer so that output voltage generates overshoot to fail specification. The RT3601EA has anti-overshoot function being able to help improve this issue. The VR will turn off low-side MOSFET when output voltage ramps up to the target VID (ALERT signal be pulled low). This function also can improve the overshoot during the load transient condition. When anti-overshoot function is triggered, the UGATE and LGATE signal will be masked to reduce the overshoot amplitude.

Table 7. SET2 Pin Setting for Anti-Overshoot and Zero Load-Line

| $\Delta V_{SET2} = 80\mu A \times \frac{R1 \times R2}{R1 + R2}$ | | | | VR Address | Zero Load-Line | ANTIOVS |
|---|---------|--------|------|------------|----------------|---------|
| Min | Typical | Max | Unit | | | |
| 4.5 | 50 | 95.5 | mV | 00 | Disable | Disable |
| 106.5 | 150 | 193.5 | mV | | | Enable |
| 208.5 | 250 | 291.5 | mV | | Enable | Disable |
| 310.5 | 350 | 389.5 | mV | | | Enable |
| 412.5 | 450 | 487.5 | mV | 01 | Disable | Disable |
| 514.5 | 550 | 585.5 | mV | | | Enable |
| 616.5 | 650 | 683.5 | mV | | Enable | Disable |
| 718.5 | 750 | 781.5 | mV | | | Enable |
| 820.5 | 850 | 879.5 | mV | 02 | Disable | Disable |
| 922.5 | 950 | 977.5 | mV | | | Enable |
| 1024.5 | 1050 | 1075.5 | mV | | Enable | Disable |
| 1126.5 | 1150 | 1173.5 | mV | | | Enable |
| 1228.5 | 1250 | 1271.5 | mV | 03 | Disable | Disable |
| 1330.5 | 1350 | 1369.5 | mV | | | Enable |
| 1432.5 | 1450 | 1467.5 | mV | | Enable | Disable |
| 1534.5 | 1550 | 1565.5 | mV | | | Enable |

Table 8. SET3 Pin Setting for IPSK and ANTIOVS_TH

| $\Delta V_{SET3} = 80\mu A \times \frac{R1 \times R2}{R1 + R2}$ | | | | IPSK | ANTIOVS_TH(mV) |
|---|---------|--------|------|----------------|----------------|
| Min | Typical | Max | Unit | | |
| 4.5 | 50 | 95.5 | mV | 150mV / Avgain | 10 |
| 106.5 | 150 | 193.5 | mV | | 20 |
| 208.5 | 250 | 291.5 | mV | | 30 |
| 310.5 | 350 | 389.5 | mV | | 40 |
| 412.5 | 450 | 487.5 | mV | 100mV / Avgain | 10 |
| 514.5 | 550 | 585.5 | mV | | 20 |
| 616.5 | 650 | 683.5 | mV | | 30 |
| 718.5 | 750 | 781.5 | mV | | 40 |
| 820.5 | 850 | 879.5 | mV | 50V / Avgain | 10 |
| 922.5 | 950 | 977.5 | mV | | 20 |
| 1024.5 | 1050 | 1075.5 | mV | | 30 |
| 1126.5 | 1150 | 1173.5 | mV | | 40 |
| 1228.5 | 1250 | 1271.5 | mV | 0mV / Avgain | 10 |
| 1330.5 | 1350 | 1369.5 | mV | | 20 |
| 1432.5 | 1450 | 1467.5 | mV | | 30 |
| 1534.5 | 1550 | 1565.5 | mV | | 40 |

Over-Current Protection

The RT3601EA has dual OCP mechanism. One is named SUM-OCP, the other is called per phase OC. The over current protection (OCP) forces high-side MOSFET and low-side MOSFET off by shutting down internal PWM logic drivers. The RT3601EA provides SUM-OCP which is 160% of I_{MON_04}. I_{MON_04} is the current that makes V_{IMON} – V_{REF} = 0.4. When output current is higher than the SUM-OCP threshold, SUM-OCP is latched with a 40µs delay time to prevent false trigger. Besides, the SUM-OCP function is masked when dynamic VID transient occurs and after dynamic VID transition, SUM-OCP is masked for 80µs. The other one is SPIKE-OCP which should trip when the output current exceeds per phase OC threshold during first DVID. Per phase OC threshold is dependent on IMAX level as shown in Table 2. When output current is higher than the per phase OC threshold, SPIKE-OCP is latched with a 0.5µs delay time to prevent false trigger.

Output Over-Voltage Protection

There are two conditions for OVP. One is when VSEN is respect to VID voltage. The other is when VSEN is lower limit to 1V. For VSEN is respect to VID voltage, OVP condition is detected when VSEN pin is 350mV more than VID. For VSEN is lower limit to 1V, OVP is occurred when VSEN is higher than 1V. When OVP is detected, the high-side gate voltage UGATE_x is pulled low and the low-side gate voltage LGATE_x is pulled high. OVP is latched with a 0.5µs delay- to prevent false trigger.

Negative Voltage Protection

Since the OVP latch continuously turns on all low-side MOSFETs of the VR, the VR will suffer negative output voltage. When the VSEN detects a voltage below –0.05V after triggering OVP, the VR triggers NVP to turn off all low-side MOSFETs of the VR while the high-side MOSFETs remain off. After triggering NVP, if the output voltage rises above 0V, the OVP latch restarts to turn on all low-side MOSFETs. Therefore, the output voltage may bounce between 0V and –0.05V due to OVP latch and NVP triggering. The NVP function will be active only after OVP is triggered.

Under-Voltage Protection

When the VSEN pin voltage is 350mV less than VID, UVP will be latched. When UVP latched, the both UGATE_x and LGATE_x are pulled low. A 3µs delay is used in UVP detection circuit to prevent false trigger. Besides, the UVP function is masked when dynamic VID transient occurs and after dynamic VID transition, UVP is masked for 80µs.

Design Step :

The RT3601EA Excel based design tool is available. Users can contact your Richtek representative to get the spreadsheet. Three main design procedures of the RT3601EA design, first step is loop design, second step is pin setting design, and the last step is protection settings. The following design example is to explain the RT3601EA design procedure :

| | Specification |
|-------------------------|---------------|
| Input Voltage | 19V |
| No. of Phase | 1 |
| Normal VID | 1.3V |
| ICCMAX | 22A |
| Load-Line | 6mΩ |
| Fast Slew Rate | 33.75mV/µs |
| MAX Switching Frequency | 600kHz |

The output filter requirements of VRTB specification are as follows :

Output Inductor : 0.22µH/0.875mΩ

Output Ceramic Capacitor : 396µF (18pcs)

Loop Design :

- On time setting: Using the specification, then can get that T_{ON} is 160ns.

The k_{TON} parameter can be calculated after the on-time is decided.

$$T_{ON} = \frac{26.2\mu \times V_{DAC}}{k_{TON} \times (V_{IN} - 0.9)} + 15n$$

Choosing the nearest on-time setting k_{TON} = 13

- Current sensor adopts lossless RC filter to sense current signal in DCR. For getting an expected load transient waveform $R_X C_X$ time constant needs to match L_X / DCR . $C_X = 0.47\mu F$, $R_{NTC} = 4.7k\Omega$ and $R_P = 4.7k\Omega$ are set, then

$$R_{EQU} = R_S + (R_P // R_{NTC})$$

$$\frac{L_X}{DCR} = C_X \times \frac{R_{EQU} \times R_X}{R_{EQU} + R_X}$$

By using the design tool, R_S and R_X can be determined, are equal to 845Ω and 768Ω , respectively.

- IMON resistor network design :

$$R_{IMON} = \frac{\Delta V_{IMON} \times 2.15k}{ICCMAX \times DCR \times \frac{R_{EQU}}{R_X + R_{EQU}}} = 58k\Omega$$

- Load-line design : $6m\Omega$ droop is requirement, because DCR and k_i are decided to $0.875m\Omega$ and 80 , respectively ($k_i = A_I$ Gain). The voltage loop A_V gain is also can be determined by following equation :

$$R_{LL} = \frac{A_I}{A_V} = \frac{\frac{k_i}{2} \times DCR}{\frac{R_2}{R_1}}$$

$R_1 = 10k\Omega$ is usually decided and here R_2 is chosen to $47k\Omega$.

- Typical compensator design can use the following equations to design C_1 and C_2 values

$$C_1 = \frac{1}{R_1 \times \pi \times F_{SW}} \approx 270pF$$

$$C_2 = \frac{C_{OUT} \times ESR}{R_2} \approx 47pF$$

For Intel platform, in order to induce the band width to enhance transient performance to meet Intel's criterion, the zero location can be designed close to $1/10$ of the switching frequency or less than the $1/10$ of switching frequency.

Pin Setting Design :

SET1 resistor network design: From above designs, parameter of A_I Gain is 80 . The $ICCMAX$ is designed as $22A$. The $PSYS$ function is decided to Enable and $DVID$

width is set to $5.36\mu s$. By using the information, the two equation can be listed by using multi-function pin setting mechanism :

$$3.2 \times \frac{R_2}{R_1 + R_2} = 1326.29mV$$

$$80\mu \times \frac{R_1 \times R_2}{R_1 + R_2} = 100.09mV$$

$R_1 = 3.01k\Omega$ and $R_2 = 2.13k\Omega$.

- SET2 resistor network design : From above designs, parameters of k_{TON} is 13 . The OCP threshold is designed as $1.2 \times ICCMAX$. The zero load-line function is decided to disable and anti-overshoot is decided to enable. The VR address is set to 0 . By using the information, the two equation can be listed by using multi-function pin setting mechanism:

$$3.2 \times \frac{R_2}{R_1 + R_2} = 225.22mV$$

$$80\mu \times \frac{R_1 \times R_2}{R_1 + R_2} = 150.14mV$$

$R_1 = 26.66k\Omega$ and $R_2 = 2.01k\Omega$.

- SET3 resistor network design : From above designs, the QR_TH is set to $20mV$ and QR width is designed as $0.7 \times T_{ON}$. The $IPSK$ is set to $100mV / Avgain$ and $ANTIOVS_TH$ is set to $20mV$. By using the information, the two equation can be listed by using multi-function pin setting mechanism :

$$3.2 \times \frac{R_2}{R_1 + R_2} = 775.75mV$$

$$80\mu \times \frac{R_1 \times R_2}{R_1 + R_2} = 550.53mV$$

$R_1 = 28.38k\Omega$ and $R_2 = 9.08k\Omega$.

- TSEN resistor network design : The $DVID$ threshold is $30mV$ and the Boot voltage is set to $0V$. By using the information, the equation can be shown as below :

$$3.2 \times \frac{R_2}{R_1 + R_2} = 450.44mV$$

Protection Settings :

- OVP/UVP protections: When the VSEN pin voltage is 350mV higher than VID, the OVP will be latched. When the VSEN pin voltage is 350mV lower than VID, the UVP will be latched.
- TSEN and VR_HOT design : Using the following equation to calculate related resistances for VR_HOT setting.

$$V_{TSEN} = 80\mu \times (R_3 // R_{NTC}) + (R_1 // R_2)$$

NTC thermistor $R_{NTC(25^\circ C)} = 100k\Omega$ and its $\beta = 4485$. When temperature is $100^\circ C$, the $R_{NTC(90^\circ C)} = 6.75k\Omega$. According to TSEN pins for multi-function mechanism, three equations can be got as following for Main VR rail :

$$V_{TSEN(25^\circ C)} = 80\mu \times (R_3 // R_{NTC(25^\circ C)}) + (R_1 // R_2) = 1.624V$$

$$V_{TSEN(90^\circ C)} = 80\mu \times (R_3 // R_{NTC(100^\circ C)}) + (R_1 // R_2) = 1.092V$$

$$3.2 \times \frac{R_2}{R_1 + R_2} = 450.44mV$$

$R_1 = 54.83k\Omega$, $R_2 = 8.98k\Omega$ and $R_3 = 48.7k\Omega$.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is $125^\circ C$. The junction-to-ambient thermal resistance, θ_{JA} , is highly package dependent. For a WQFN-28L 4x4, the thermal resistance, θ_{JA} , is $28.5^\circ C/W$ on a standard JEDEC 51-7 high effective-thermal-

conductivity four-layer test board. The maximum power dissipation at $T_A = 25^\circ C$ can be calculated as below :

$$P_{D(MAX)} = (125^\circ C - 25^\circ C) / (28.5^\circ C/W) = 3.5W \text{ for a WQFN-28L 4x4 package.}$$

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA} . The derating curves in Figure 24 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

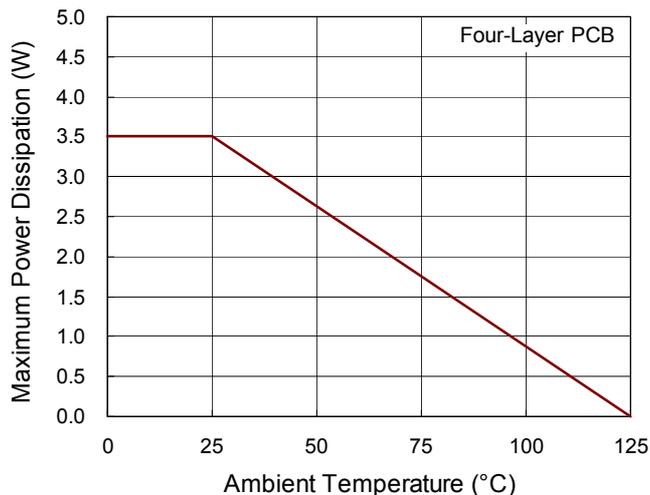
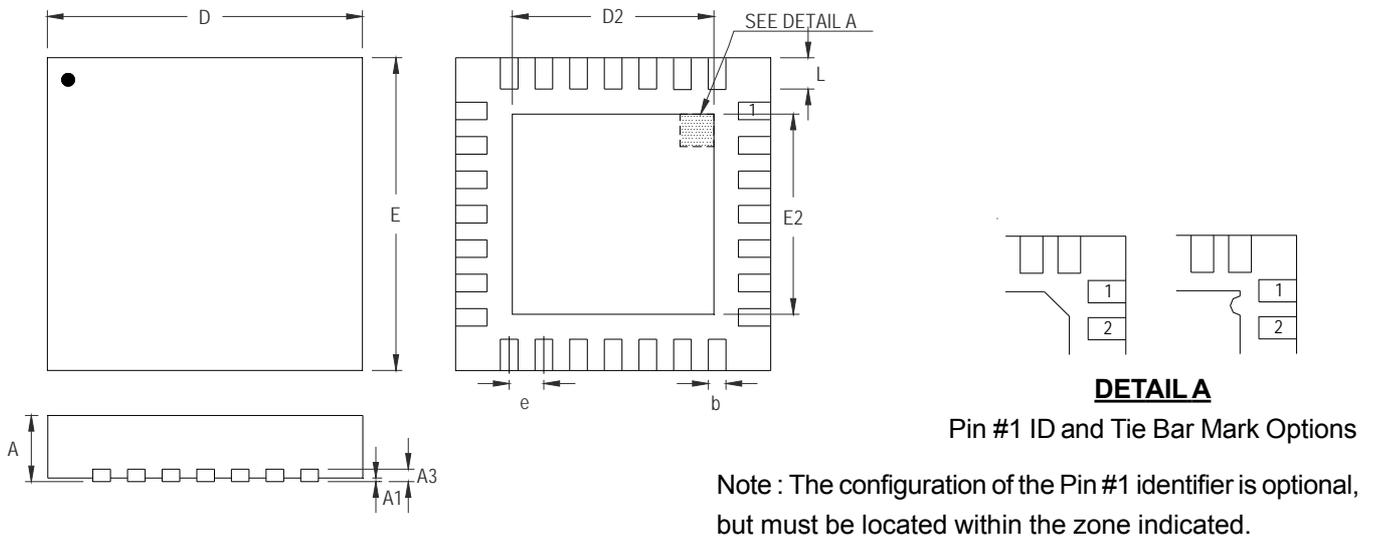


Figure 24. Derating Curve of Maximum Power Dissipation

Outline Dimension



| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|--------|---------------------------|-------|----------------------|-------|
| | Min | Max | Min | Max |
| A | 0.700 | 0.800 | 0.028 | 0.031 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| A3 | 0.175 | 0.250 | 0.007 | 0.010 |
| b | 0.150 | 0.250 | 0.006 | 0.010 |
| D | 3.900 | 4.100 | 0.154 | 0.161 |
| D2 | 2.350 | 2.450 | 0.093 | 0.096 |
| E | 3.900 | 4.100 | 0.154 | 0.161 |
| E2 | 2.350 | 2.450 | 0.093 | 0.096 |
| e | 0.400 | | 0.016 | |
| L | 0.350 | 0.450 | 0.014 | 0.018 |

W-Type 28L QFN 4x4 Package

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