MediaTek

MT6318 PMIC Specification

Datasheet

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Revision History

Revision	Date (yyyy/mm/dd)	Author	Comments
0.1	2005/09/09	Cathy Chen	Initial release.
0.2	2006/05/09	HI Chen	Revision
0.3	2006/06/19	Naomi Ko	English review and document reformatting.
1.0	2006/10/11	Cathy Chen	Complete the electrical spec. and append the waveform. Correct some descriptions.

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16 Programmable under voltage lockout protection
17 Power-on reset and start-up timer
18 96-pin TFBGA package

1.2 Applications

GSM/GPRS mobile handsets, basic phones and high-end phones.

1.3 General Description

The MT6318 is a power management system chip optimized for GSM/GPRS handsets, especially those based on the MediaTek MT621x/MT622x system solution. MT6318 contains 11 LDOs, one to power each of the critical GSM/GPRS sub-blocks. Sophisticated controls are available for power-up during battery charging, for the keypad interface, and for the RTC alarm. The MT6318 is optimized for maximum battery life.

The 2-step RTC LDO design allows the RTC circuit to stay alive without a battery for several hours.

The MT6318 battery charger can be used with a lithium-ion (Li+) battery.

The SIM interface provides the level shift between SIM card and microprocessor.

The MT6318 is available in a 96-pin TFBGA package. The operating temperature range is -25℃ to +85℃.

1.4 Ordering Information

ORDER #	MARKING	TEMP. RANGE	PACKAGE
MT6318A	MT6318A/AY	-25℃ to +85℃	TFBGA - 96L

1.5 Pin Assignments and Descriptions

Figure 1: MT6318 TFBGA 96(7x7 mm^2) Pin Assignments

	1	2	3	4	5	6	7	8	9	10	
A	LED_KP	C2+	C1+	C1+	PWRIN4	FB_BL	BLDRV	PWRIN3	PWRBB	BAT_ BACKUP	A
B	VO_G	VO_R	CS_KP	DC_OV	PWRIN4	CS_BL	RST CAP	PWRIN3	INT	BAT_ON	B
C	V_USB	VO_B	GND4	GND4	PWRIN4	GND4	GND4	PWRIN3	RTC _SEL	VIO	C
D	USB	GDR VUSB	GND1	GND4	PWRIN4	GND4	GND3	GND3	PWRIN2	PWRIN2	D
E	AC	GDR VAC	GND1	GND1			GND3	GND3	VD_ SEL	VA_SW	E
F	VBAT	ISENSE	GND1	GND1			GND3	SPICS	RESET	VIBR	F
G	VN	SEL2	GND1	GND1	GND2	GND2	GND2	SPICK	SRCLK EN	VRTC	G
H	VTCXO	SEL1	SEL1 _EN	GND2	ISENSE _OUT	GND2	GND2	SIO	SIM VCC	SIM RST	H
J	PWRIN1	PWRIN1	PWRIN1	VB_OUT	AUDP	AUDN	SIMIO	SPIDAT	SRST	VD	J
K	VA	BP/REF	VMC	VM_ SEL	SPK+	SPK-	PWR KEY	VSIM	SIM CLK	SCLK	K
	1	2	3	4	5	6	7	8	9	10	

Table 1: MT6188 Pin Descriptions

Pin	Symbol	Input (I), Output (O), or Analog (A)	Description
Control			
K7	PWRKEY	I	Power on button input. Active low.
A9	PWRBB	I	Power on/off from microprocessor. Active high.
G9	SRCLKEN	I	VTCXO and VA enable. High = enable. Low = disable.
H9	SIMVCC	I	VSIM enable. High = enable. Low = disable.
B10	BAT_ON	I	Indication that Li-ion battery is inserted. High = no battery. Low = battery inserted.
B4	DC_OV	I	DC/DC protection input. OV threshold voltage is 1V.
K4	VM_SEL	I	External memory supply selection. 1 = 2.8V, 0 = 1.8V.
H3	SEL1_EN	I	Enable the “pre-charge indication” function. 1 = enable, 0 = disable. (Note1)
C9	RTC_SEL	I	VRTC output voltage selection. 1 = 1.5V, 0 = 1.2V (Note1)
E9	VD_SEL	I	VD output voltage selection. 1 = 1.8V/1.5V, 0 = 1.2V/0.9V (depending on the register PWR_SAVE setting).
Charger Control			
E1	AC	IA	AC-DC adaptor input
D1	USB	IA	USB power input
C1	V_USB	OA	3.3V USB power output
B9	INT	O	Interrupt PIN. Active low. This pin informs the BB if an AC or USB voltage is detected, or if OVP (AC > 9V) is detected. Is reset to normal high after BB has communicated with the PMIC through SPI.
D2	GDRVUSB	OA	Control output to the gate of the external p-channel FET for the USB charger.
E2	GDRVAC	OA	Control output to the gate of the external p-channel FET for the AC charger.
F2	ISENSE	OA	Charger current sensing input
H2	SEL1	OA	Control output to the gate of the external PMOS for the AC charger input as power source.
G2	SEL2	OA	Control output to the gate of the external PMOS for the VBAT input as power source.
SIM Interface			
J7	SIMIO	I/O	Non level-shifted SIM data (3V)
H10	SIMRST	I	Non level-shifted SIM reset input (3V)
K9	SIMCLK	I	Non level-shifted SIM clock input (3V)
H8	SIO	I/O	Level-shifted SIM data (1.8/3V)
J9	SRST	O	Level-shifted SIM reset output (1.8/3V)
K10	SCLK	O	Level-shifted SIM clock output (1.8/3V)
Reset			
B7	RSTCAP	IA	Reset delay time capacitance
F9	RESET	O	System reset. Low active.

Power-Related			
F1	VBAT	IA	Battery input voltage
J1, J2, J3, D9, D10, A8, B8, C8, A5, B5, C5, D5	PWRIN	IA	Power input
J4	VB_OUT	OA	Battery output voltage. Switchable.
H5	ISENSE_OUT	OA	ISENSE output voltage. Switchable.
K2	BP/VREF	OA	Bandgap reference and bypass capacitance
D3, E3, E4, F3, F4, G3, G4, G5, G6, G7, H4, H6, H7, D7, D8, E7, E8, F7, C3, C4, C6, C7, D4, D6	GND		Ground
J10	VD	OA	Digital core supply
C10	VIO	OA	Digital IO supply
K1	VA	OA	Analog supply
E10	VA_SW	OA	Auxiliary analog supply. Switchable.
H1	VTCXO	OA	TCXO supply
G1	VM	OA	Memory supply
K8	VSIM	OA	SIM supply
G10	VRTC	OA	RTC supply
K3	VMC	OA	Memory card supply
Miscellaneous			
F10	VIBR	OA	Vibrator driver
A3	C1+	A	Charge pump capacitor. Positive terminal.
A4	C1-	A	Charge pump capacitor. Negative terminal.
A2	C2+	A	DC/DC output back-up capacitor. Positive terminal.
A10	BAT_BACKUP	OA	Backup battery pin for 2-step RTC
Speaker Amplifier			
J5	AUDP	IA	Audio positive input
J6	AUDN	IA	Audio negative input
K5	SPK+	OA	Speaker positive output
K6	SPK-	OA	Speaker negative output
LED Driver			
B2	VO_R	IA	R LED current driver
B1	VO_G	IA	G LED current driver
C2	VO_B	IA	B LED current driver
A1	LED_KP	OA	KP LED driver
B3	CS_KP	IA	KP LED current sensor
A7	BLDRV	OA	Control output to the gate of the external FET for the backlight DC-DC converter.
B6	CS_BL	IA	Voltage sensor input for external BL FET current
A6	FB_BL	IA	Voltage sensor input from white LED ballast resistor
SPI Interface			
F8	SPICS	I	Serial port select input
G8	SPICK	I	Serial port clock input
J8	SPIDAT	IO	Serial port I/O

Note1: The state of these pins is latched when MT6318 starts up. The state can changed only by powering down and powering up MT6318 again.

2 Electrical Characteristics

2.1 Absolute Maximum Ratings over Operating Free-Air Temperature Range

Stresses beyond those listed under Table 2 may cause permanent damage to the device. These numbers are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2: Absolute Maximum Ratings

Parameter	Conditions	Min.	Typical	Max.	Unit
Free-air temperature range		-40		85	℃
Storage temperature range		-65		150	℃
Battery input voltage range				5.5	V
ESD robustness	HBM	2000			V
Charger input withstand				15	V

2.2 Recommended Operating Range

Table 3: Operation Condition

Parameter	Conditions	Min.	Typical	Max.	Unit
Operating temperature range		-25		85	℃

2.3 Electrical Characteristics

Table 4: General Electrical Specifications

VBAT = 3 V ~ 5 V, minimum loads applied on all outputs, unless other noted. Typical values are at T_A = 25 ℃.

Parameter	Conditions	Min.	Typical	Max.	Unit
Switch-Off Mode: Supply Current					
VBAT < 2.5 V	RTC LDO OFF		10	20	µA
2.5 V < VBAT < 3.3 V	VBAT=3.3V		37	70	µA
3.3 V < VBAT	VBAT=4.2V		43	85	µA
Operation: Supply Current					
All outputs on	VBAT=4.2V		295	500	µA
VSIM, VTXCO off; all others on	VBAT=4.2V		240	400	µA
Under Voltage (UV)					
Under voltage falling threshold 1	UV_SEL[1:0] = 00	2.85	2.9	2.95	V
Under voltage falling threshold 2	UV_SEL[1:0] = 01	2.7	2.75	2.8	V
Under voltage falling threshold 3	UV_SEL[1:0] = 10	2.55	2.6	2.65	V
Under voltage falling threshold 4	UV_SEL[1:0] = 11	2.35	2.5	2.65	V
Under voltage rising threshold	UV_SEL[1:0] = xx	3.1	3.2	3.3	V

Reset Generator					
Output High		V_{IO}-0.5			V
Output Low				0.3	V
Output Current			1		mA
On Delay Time per Unit Capacitance		1.5	2.5	4	ms/nF
Power Key Input					
High Voltage		0.7*VBAT			V
Low Voltage				0.3*VBAT	V
Control Input Voltage					
PWRBB Input High		1.0			V
PWRBB Input Low				0.2	V
Other Control Input High		2.0			V
Other Control Input Low				0.5	V
Thermal Shutdown					
Threshold			150		degree
Hysteresis			40		degree
LDO Enable Response Time			250		µs

2.4 Regulator Output

Table 5: Regulator Specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
Charge Pump Regulator – For keypad and RGB LED drivers					
Output ripple			±50		mV
Efficiency	I_{out} = 80 mA, V_{out} = 4.5 V		62		%
Switching frequency			900		kHz
Output current	Normal load		80		mA
	No load		2		mA
Response time: rising	LEDKP ON (80mA load)		1.5		µs
Response time: falling	LEDKP OFF (80mA load)		90		µs
Start-up Time			250		µs
Feedback voltage		150	200	250	mV
DC/DC Converter					
Efficiency	6 LEDs' load		85		%
Switch on max. Duty cycle		65	75	85	%
Switching frequency		675	900	1180	kHz
Voltage for BL FET current sense (CS_BL)		0.13	0.15	0.23	V
Feedback voltage (FB_BL)		0.35	0.4	0.65	V
Over-voltage threshold (DC_OV)	L to H	0.95	1.0	1.05	V
	H to L	0.75	0.8	0.85	V
Digital Core Voltage					
Output voltage (V_D)	VD_SEL=L & PWR_SAVE_SPI=H		0.9		V

	VD_SEL=L & PWR_SAVE_SPI=L	1.1	1.2	1.3	V
	VD_SEL=H & PWR_SAVE_SPI=H	1.4	1.5	1.6	V
	VD_SEL=H & PWR_SAVE_SPI=L	1.7	1.8	1.9	V
Output current (Id_max)			200		mA
Line regulation				5	mV
Load regulation				30	mV
Digital IO Voltage					
Output voltage (V_IO)		2.7	2.8	2.9	V
Output current (Iio_max)			100		mA
Line regulation				5	mV
Load regulation				30	mV
Analog Voltage					
Output voltage (V_A)		2.7	2.8	2.9	V
Output current (Ia_max)			150		mA
Line regulation				5	mV
Load regulation				20	mV
Output noise voltage	f = 10 Hz to 100 kHz		50		uVrms
Ripple rejection	10 Hz < freq. < 3 kHz		65		dB
	3 kHz < freq. < 100 kHz		40		dB
VTCXO Voltage					
Output voltage (V_TCXO)		2.7	2.8	2.9	V
Output current (Itcxo_max)			20		mA
Line regulation				4	mV
Load regulation				4	mV
Output noise voltage	f = 10 Hz to 100 kHz		50		µVrms
Ripple rejection	10 Hz < freq. < 3 kHz		65		dB
	3 kHz < freq. < 100 kHz		40		dB
RTC Voltage					
1st stage output voltage		2.65	2.75	2.85	V
2nd stage output voltage (V_RTC)	RTC_SEL=H	1.3	1.5	1.65	V
	RTC_SEL=L	1.05	1.2	1.32	V
Output current limit (Irtc_max)	1st stage RTC		1.1		mA
Off reverse input current			1		µA
External Memory Voltage					
Output voltage (V_M)	VMSEL=L	1.7	1.8	1.9	V
	VMSEL=H	2.7	2.8	2.9	V
Output current (Im_max)			150		mA
Line regulation				8	mV
Load regulation				30	mV
SIM Voltage					
Output voltage (V_SIM)	VSIMSEL=L	1.71	1.8	1.89	V
	VSIMSEL=H	2.82	3.0	3.18	V
Output current (Isim_max)			20		mA

Line regulation				4	mV
Load regulation				15	mV
Memory Card Voltage					
Output voltage (V_MC)	VMCSEL=L	2.7	2.8	2.9	V
	VMCSEL=H	2.87	3.0	3.13	V
Output current (Imc_max)			250		mA
Line regulation				5	mV
Load regulation				35	mV
KP_LED Voltage					
Output voltage (V_KP)			4.3		V
Output current (I_KP)				80	mA
R/G/B LED					
Source current 1 (I_R/G/B)		8	12	16	mA
Source current 2		11	16	21	mA
Source current 3		14	20	26	mA
Source current 4		16	24	32	mA
USB Voltage					
Output voltage (V_USB)		3.15	3.3	3.45	V
Line regulation				5	mV
Load regulation				10	mV
Output current (Iusb_max)			20		mA
Auxiliary Analog Voltage					
Output voltage (VA_SW)	VA_SW_SEL=L	2.7	2.8	2.9	V
	VA_SW_SEL=H	3.15	3.3	3.45	V
Line regulation				5	mV
Load regulation				15	mV
Output current (Iswa_max)			50		mA
Vibrator Voltage					
Output voltage (V_VIBR)	VIBSEL=L	1.7	1.8	1.9	V
	VIBSEL=H	3.05	3.2	3.35	V
Output current (Ivibr_max)			200		mA

2.5 SPI Switchable Powers

Table 6: Power Switch Specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
VB_OUT	VBSSEL_SPI[1] = 1				
	VBHSEL = 0	VBAT*0.99*0.5		VBAT*1.01*0.5	V
	VBHSEL = 1	VBAT*0.99		VBAT*1.01	V
ISENSE_OUT	VBSSEL_SPI[0] = 1				
	VBHSEL = 0	ISENSE*0.99*0.5		ISENSE*1.01*0.5	V
	VBHSEL = 1	ISENSE*0.99		ISENSE*1.01	V

2.6 Speaker Amplifier

Table 7: Speaker Amplifier Specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
RMS Power	8Ω load, VBAT = 5 V		800		mW
	8Ω load, VBAT = 3.3 V		400		mW
THD+N	1KHz, Po=0.25Wrms, 4V		0.007	0.3	%
PSRR	20 Hz ~ 1 kHz, diff. mode		55		dB
Shutdown current	“Speaker On” bit = 0			1	µA
Quiescent power supply current	VBAT = 4.2 V, no input			4.0	mA
Gain adjustment		0		21	dB
Gain adjustment steps	Refer to Table 23, Index 1 (Charger/Speaker Control)		3		dB

2.7 SIM Interface

Table 8: SIM Interface Specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
Interface to MT621X					
Vih(SIMCLK,SIMRST)		Vio-0.6			V
Vil (SIMCLK,SIMRST)				0.6	V
Vilsimio	Vol ≤ 0.4 V, Iol = 1 mA			0.23	V
	Vol ≤ 0.4 V, Iol = 0 mA			0.335	V
Vihsimio, Vohsimio	Iih, Ioh = ±20 µA	Vio-0.6			V
Iilsimio	Vil = 0 V			-0.9	mA
Volsimio	Vil = 0.4 V			0.42	V
SIMIO pull-up resistance to Vio		16	20	24	kΩ
Interface to 3 V SIM Card					
Volrst	I = 20 µA			0.4	V
Vohrst	I = -200 µA	0.9*VSIM			V
Volclk	I = 20 µA			0.4	V
Vohclk	I = -200 µA	0.9*VSIM			V
Vil				0.4	V
Vihsio , Vohsio	I = ±20 µA	VSIM-0.4			V
Iil	Vil = 0 V			-1	mA
Vol	Iol = 1 mA, SIMIO ≤ 0.23 V			0.4	V
Interface to 1.8 V SIM Card					
Volrst	I = 20 µA			0.2*VSIM	V
Vohrst	I = -200 µA	0.9*VSIM			V
Volclk	I = 20 µA			0.2*VSIM	V
Vohclk	I = -200 µA	0.9*VSIM			V
Vil				0.4	V
Vihsio , Vohsio	I = ±20 µA	VSIM-0.4			V
Iil	Vil = 0 V			-1	mA

Vol	Iol = 1 mA, SIMIO ≤ 0.23 V			0.4	V
SIM Card Interface Timing					
SIO pull-up resistance to VSIM		8	10	12	kΩ
SRST, SIO rise/fall times	VSIM = 3, 1.8 V, load with 30 pF			1	µs
SCLK rise/fall times	VSIM = 3 V, CLK load with 30 pF			18	ns
	VSIM = 1.8 V, CLK load with 30 pF			50	ns
SCLK frequency	CLK load with 30 pF	5			MHz
SCLK duty cycle	SIMCLK Duty = 50%, fsimclk = 5 MHz	47		53	%
SCLK propagation delay			30	50	ns

2.8 Charger Circuit

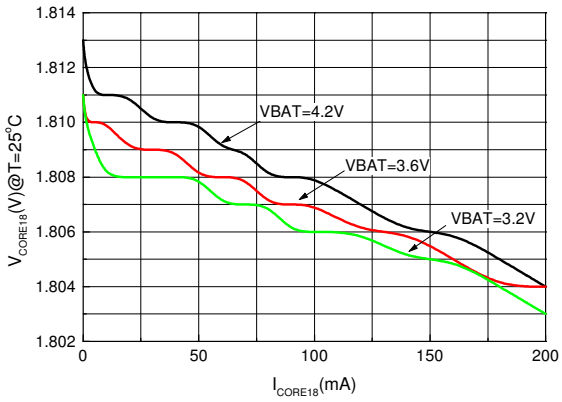
Table 9: Charger Specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
AC charger input voltage		4.2		15	V
AC charger detect on threshold (Vchg_on)		VBAT		9.0	V
USB charger detect on threshold		2.2		5.5	V
Maximum charging current (AC charging)	VBAT>=3.3V		0.16 / R_{sense}		A
Pre-charging current	VBAT<2.3V		10		mA
	VBAT>=2.3V	5/ R_{sense}	10/ R_{sense}	15/ R_{sense}	mA
Pre-charging off threshold			3.3		V
Pre-charging off hysteresis			0.3		V
CC mode to CV mode threshold		4.15	4.2	4.25	V
BAT_ON (Vih)		2.4		2.6	V
GDRVAC/GDRVUSB rising time (T_r)	BAT_ON, or OV	1		5	µs
Over voltage protection threshold (OV)			4.3		V

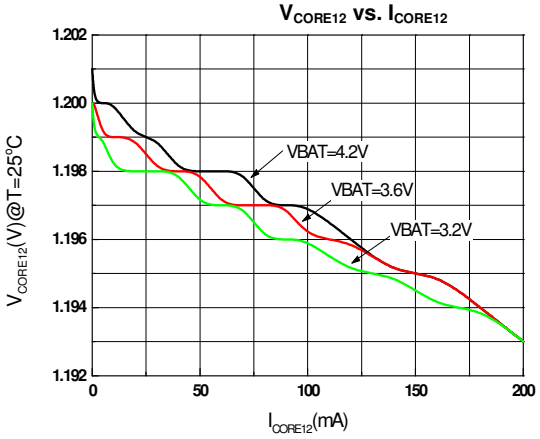
2.9 Electrical Characteristics Waveform

(V_PWRIN=3.0V-5.0V, C_{VA}= C_{VIO}=C_{VM}=C_{VMC}=4.7µF, C_{VD}=C_{VUSB}=C_{VA_SW} =C_{VTCXO}=C_{VSIM}=C_{VIBR}=2.2µF, C_{VTCXO}=$C_{BP/VREF}$=1uF, C_{VRTC}=0.1µF, minimum loads applied on all outputs, unless otherwise noted. Typical values are at T_A=+25°C.)

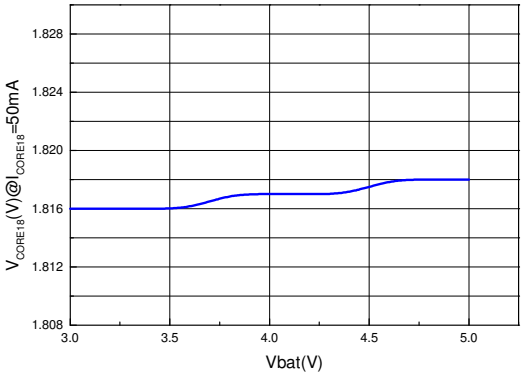
V_{CORE18} vs. I_{CORE18}



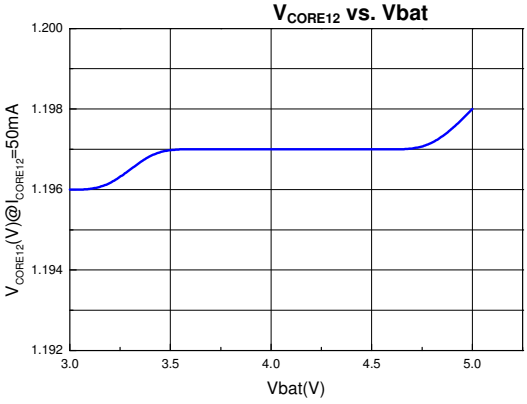
V_{CORE12} vs. I_{CORE12}



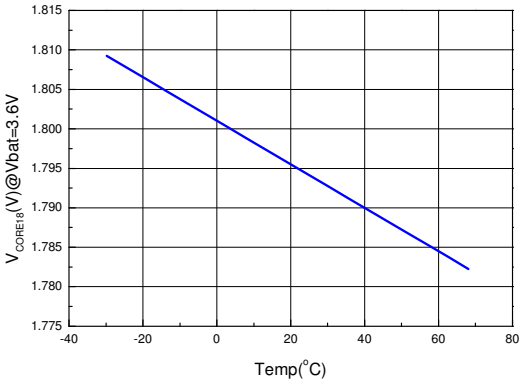
V_{CORE18} vs. Vbat



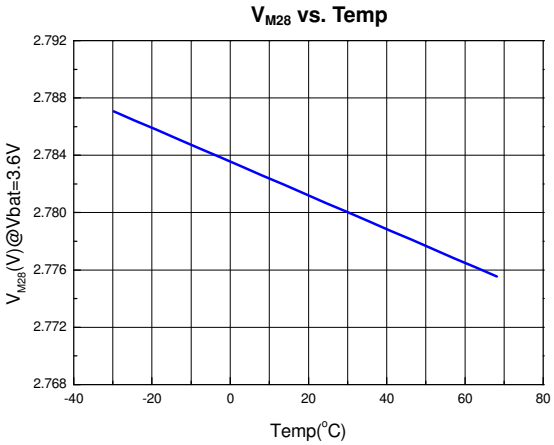
V_{CORE12} vs. Vbat



V_{CORE18} vs. Temp

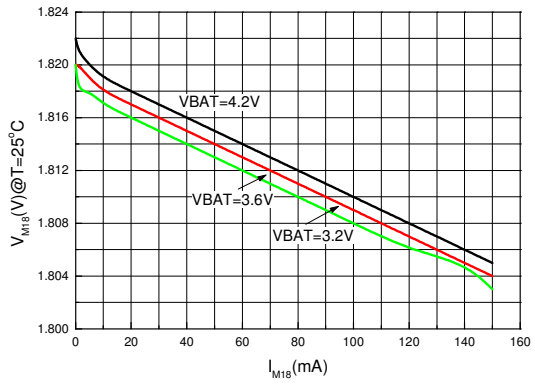


V_{M28} vs. Temp

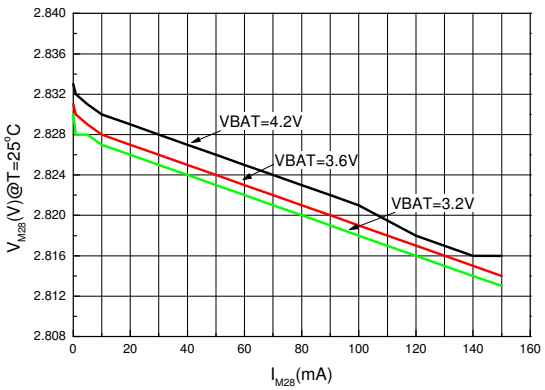


Electrical Characteristics (continued)

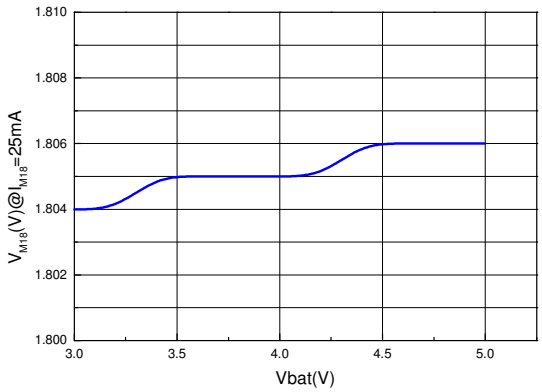
V_{M18} vs. I_{M18}



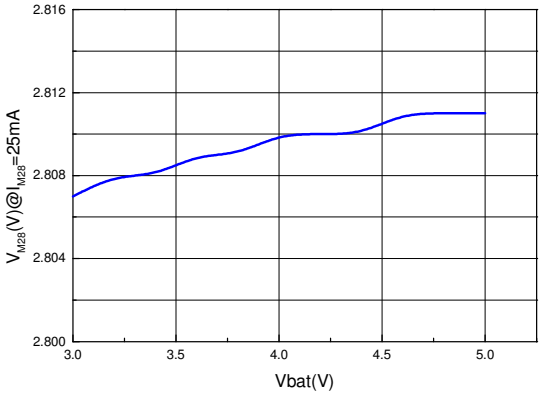
V_{M28} vs. I_{M28}



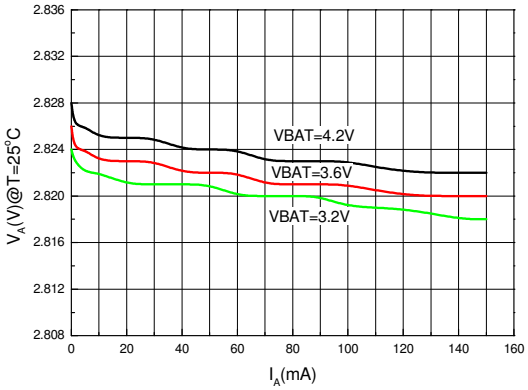
V_{M18} vs. Vbat



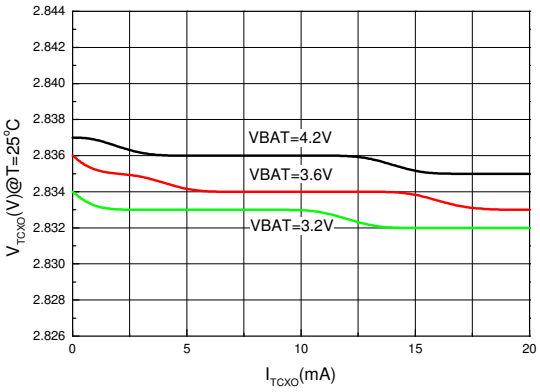
V_{M28} vs. Vbat



V_A vs. I_A

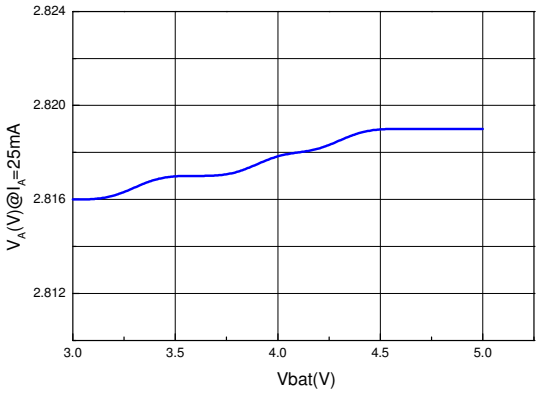


V_{TCXO} vs. I_{TCXO}

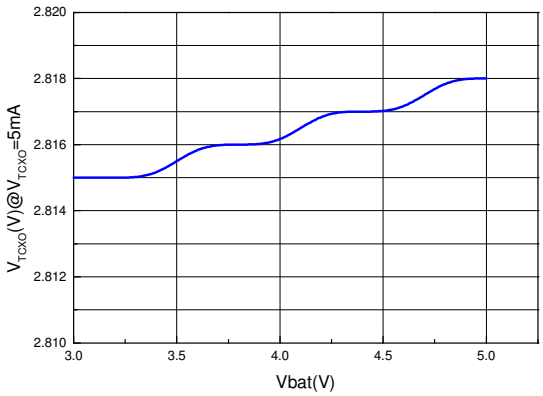


Electrical Characteristics (continued)

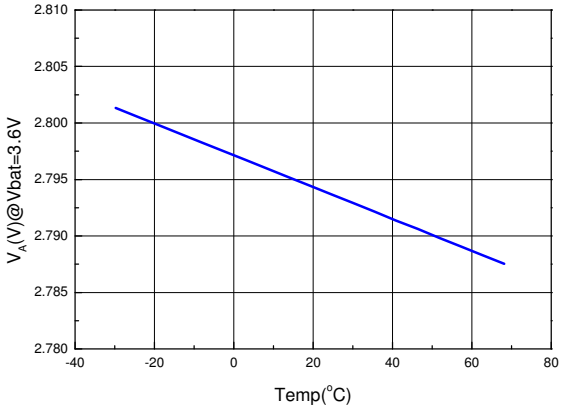
V_A vs. Vbat



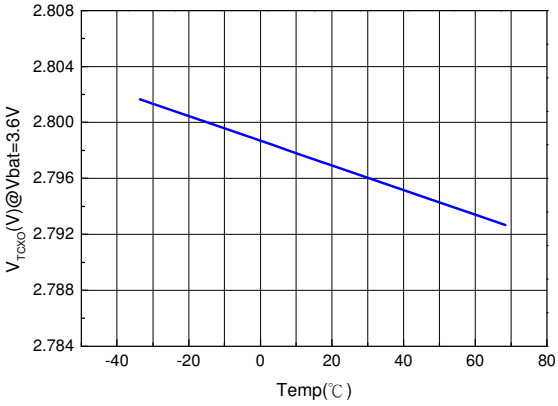
V_{TCXO} vs. Vbat



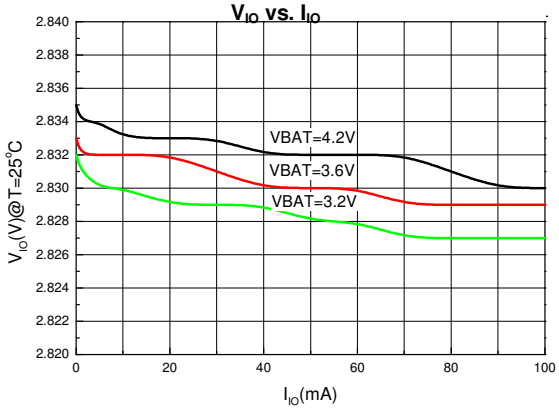
V_A vs. Temp



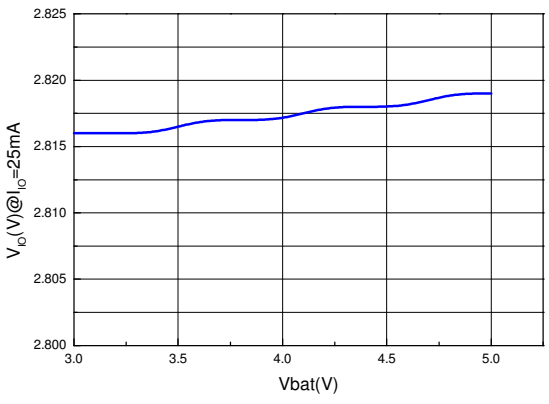
V_{TCXO} vs. Temp



V_{IO} vs. I_{IO}

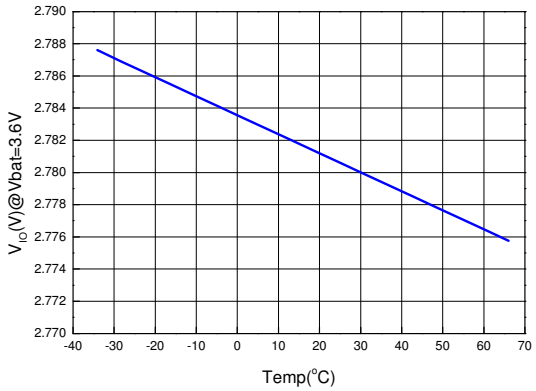


V_{IO} vs. Vbat

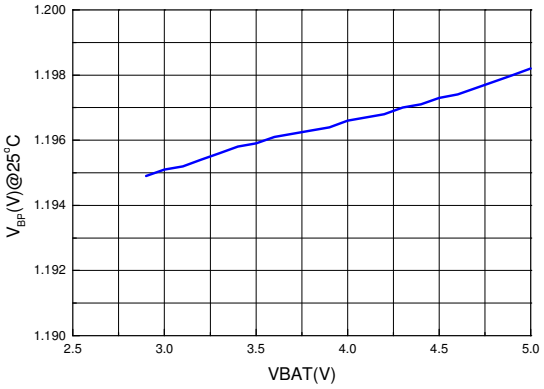


Electrical Characteristics (continued)

V_{IO} vs. Temp

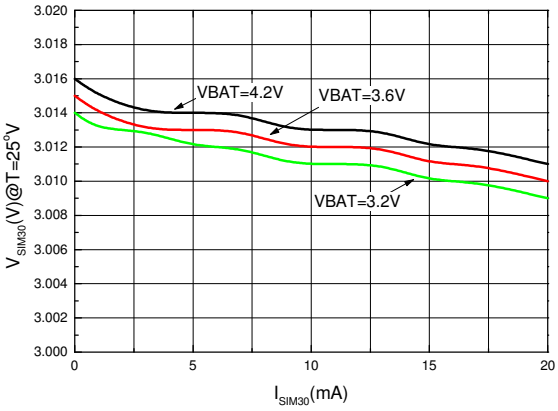


V_{REF} vs. Vbat

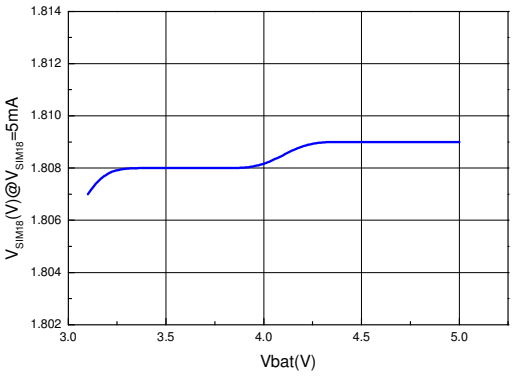


V_{SIM18} vs. I_{SIM18}

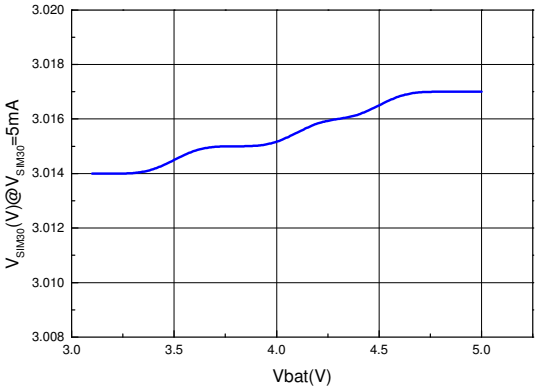
V_{SIM30} vs. I_{SIM30}



V_{SIM18} vs. Vbat

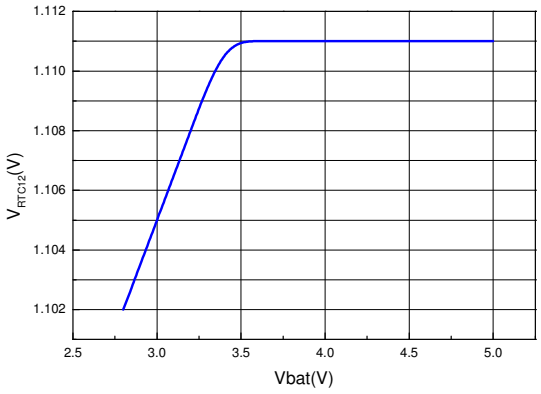


V_{SIM30} vs. Vbat

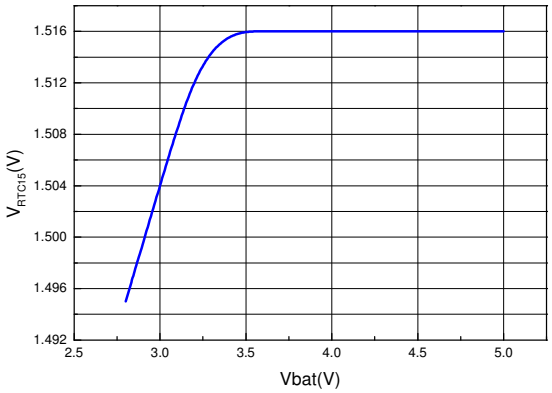


Electrical Characteristics (continued)

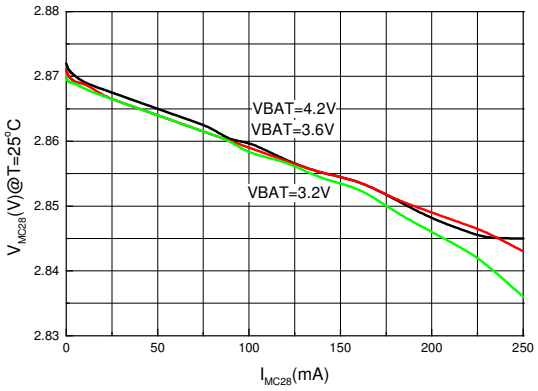
V_{RTC12} vs. Vbat



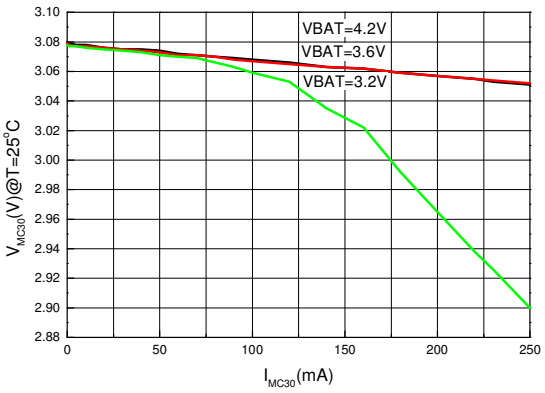
V_{RTC15} vs. Vbat



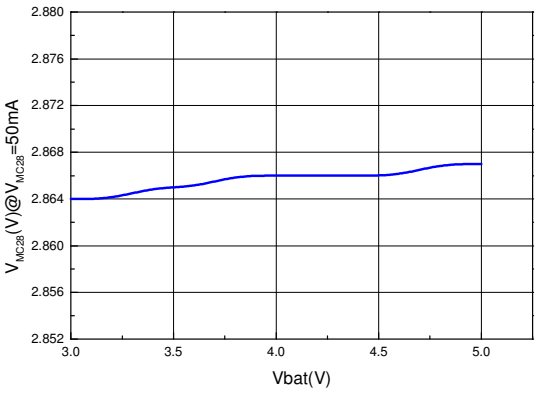
V_{MC28} vs. I_{MC28}



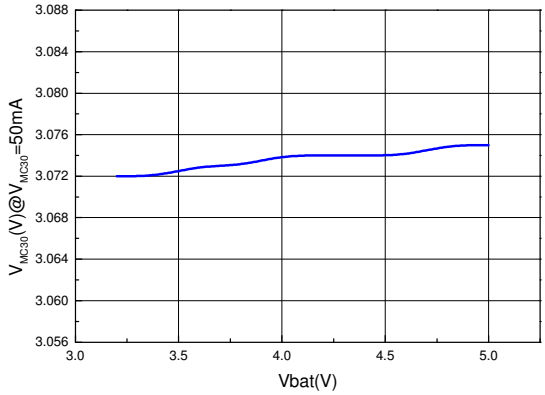
V_{MC30}vs. I_{MC30}



V_{MC28} vs. Vbat

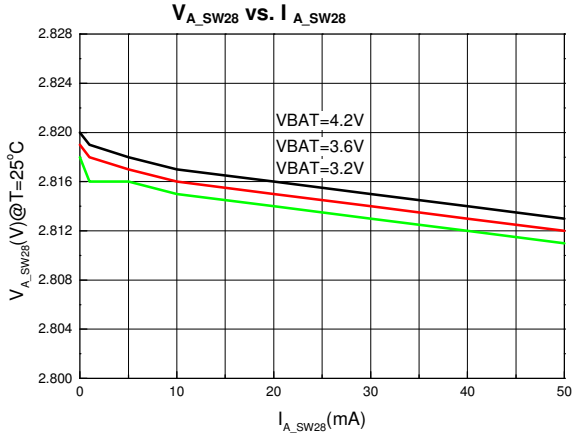


V_{MC30} vs. Vbat

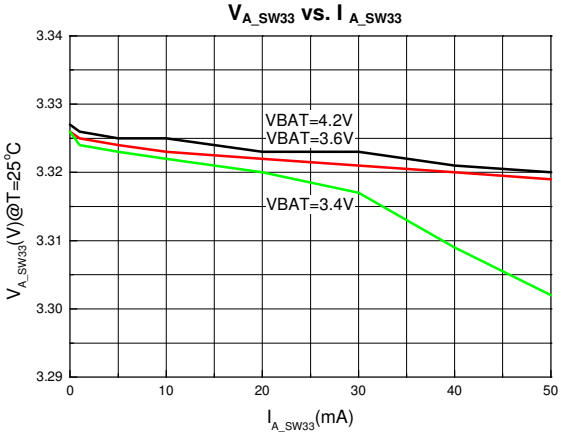


Electrical Characteristics (continued)

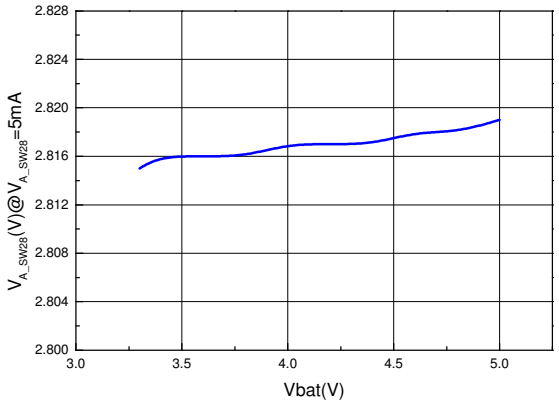
V_{A_SW28} vs. I_{A_SW28}



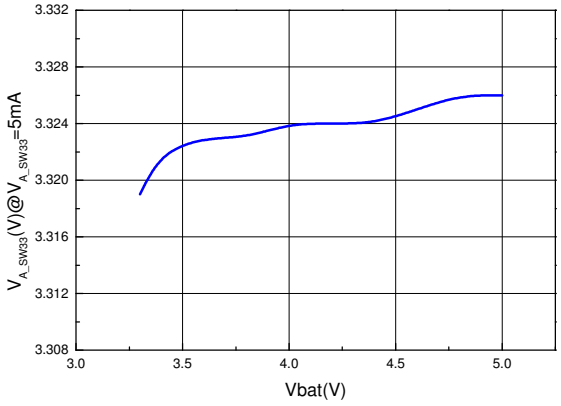
V_{A_SW33} vs. I_{A_SW33}



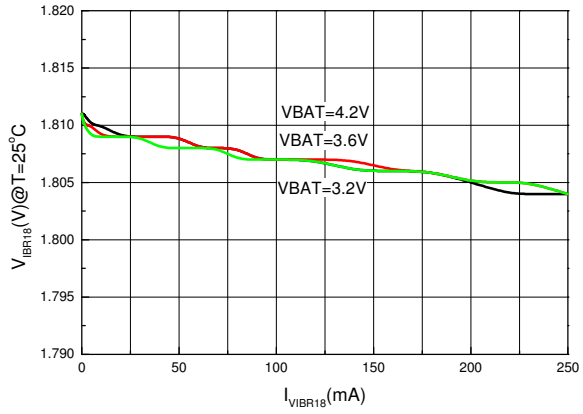
V_{A_SW28} vs. Vbat



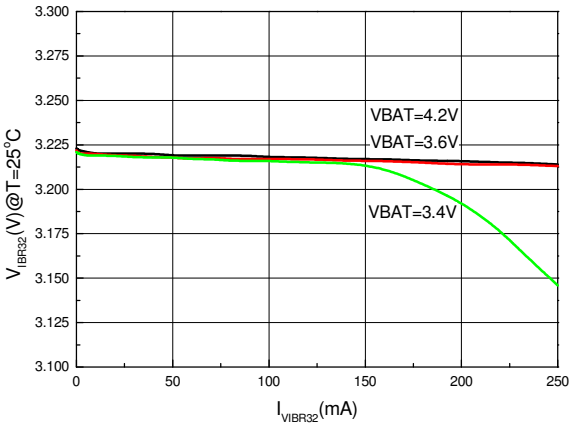
V_{A_SW33} vs. Vbat



V_{IBR18} vs. I_{IBR18}

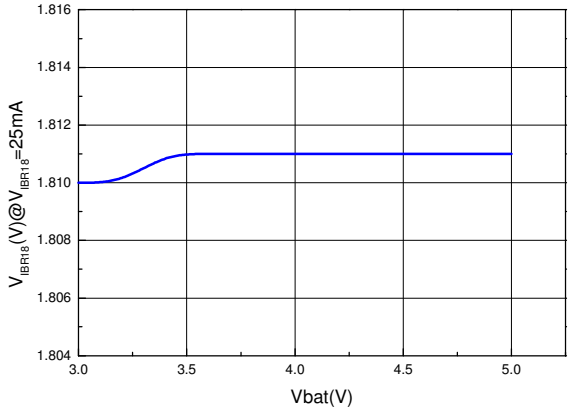


V_{IBR32} vs. I_{IBR32}

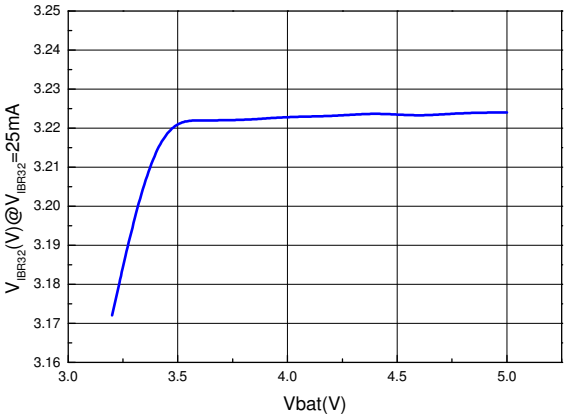


Electrical Characteristics (continued)

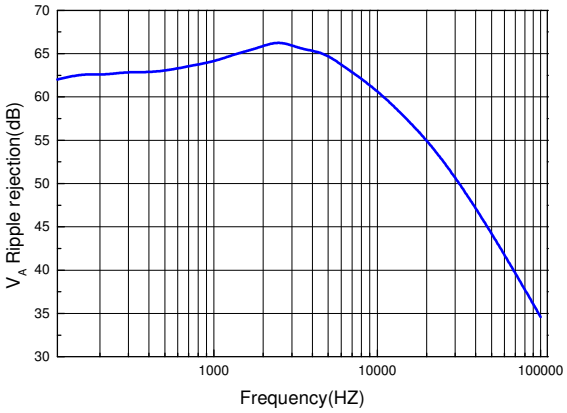
V_{IBR18} vs. Vbat



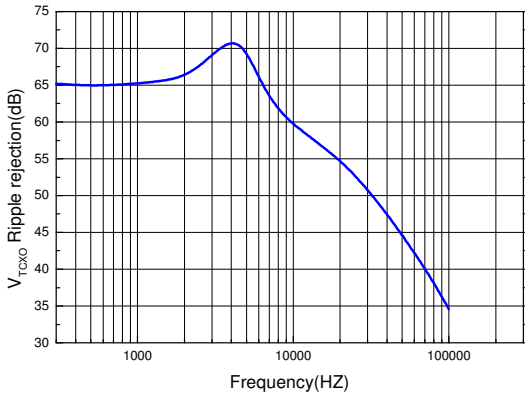
V_{IBR32} vs. Vbat



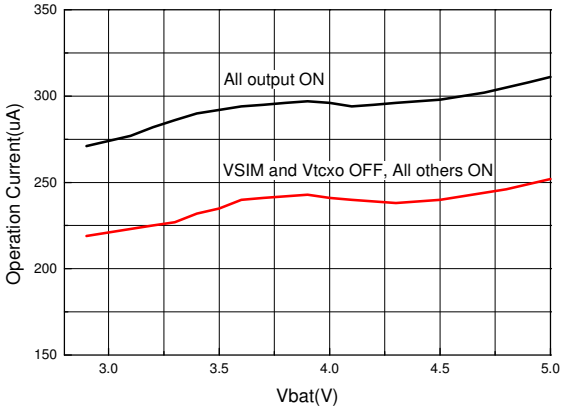
V_A Ripple Rejection vs. Frequency



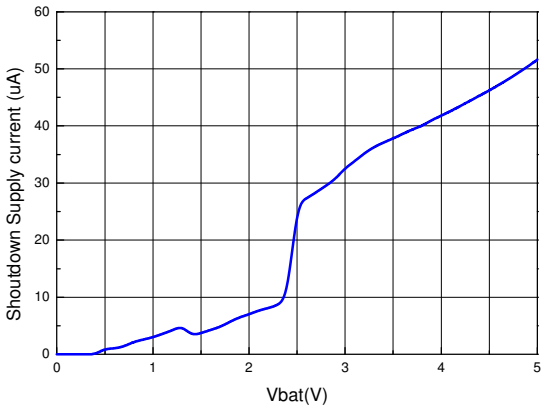
V_{TCXO} Ripple Rejection vs. Frequency



Operation Current vs. Vbat

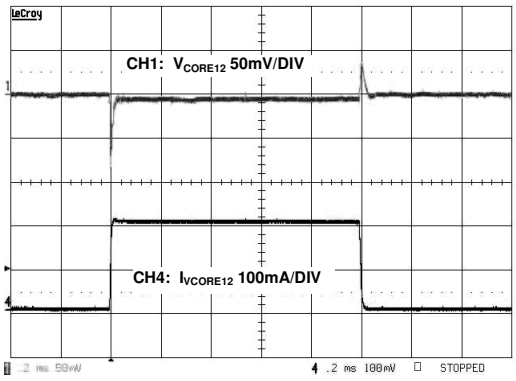


Shutdown Current vs. Vbat

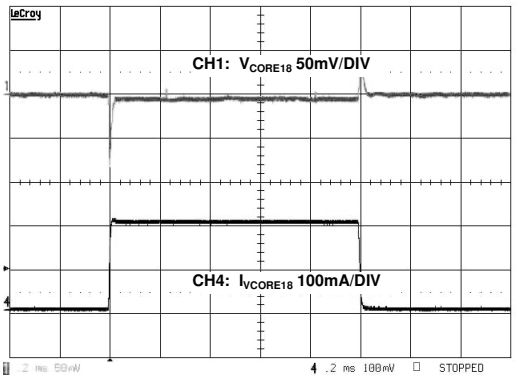


Electrical Characteristics (continued)

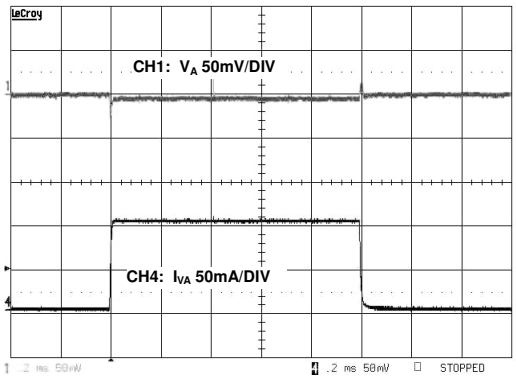
V_{CORE12} Load Transient



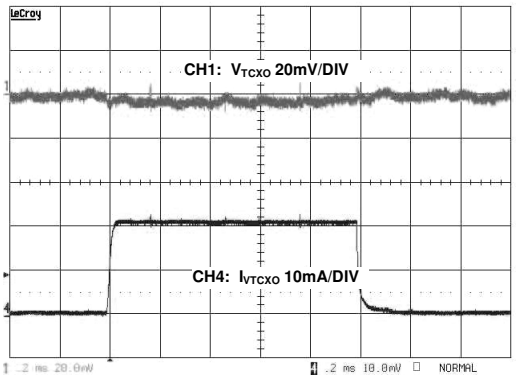
V_{CORE18} Load Transient



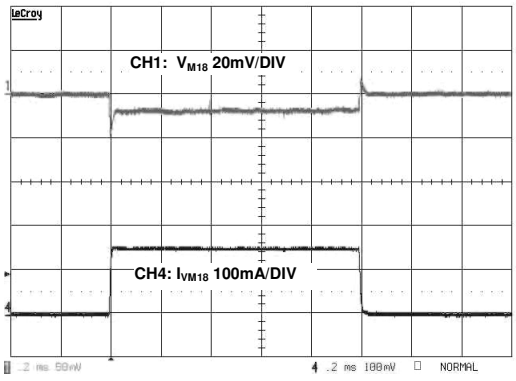
V_A Load Transient



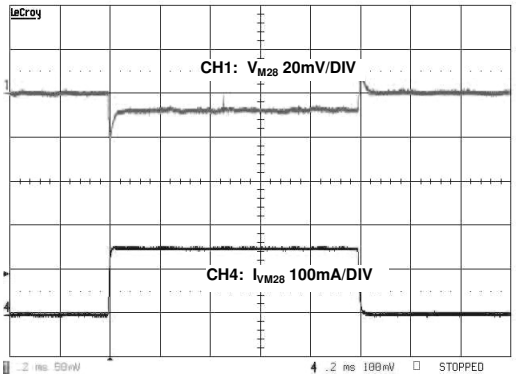
V_{TCXO} Load Transient



V_{M18} Load Transient

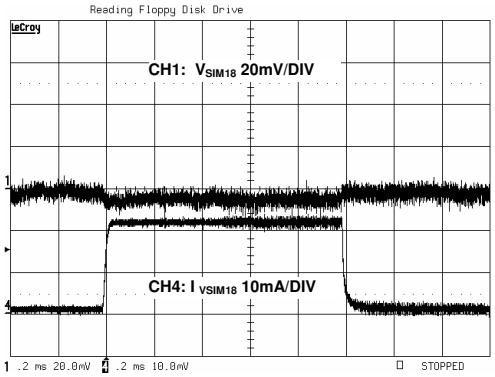


V_{M28} Load Transient

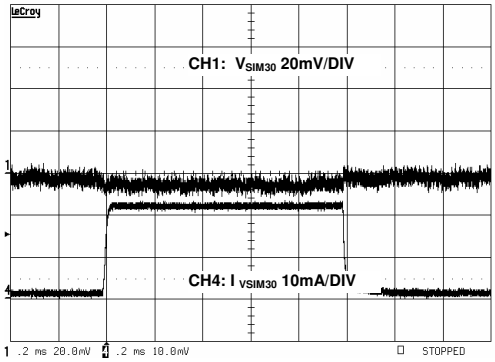


Electrical Characteristics (continued)

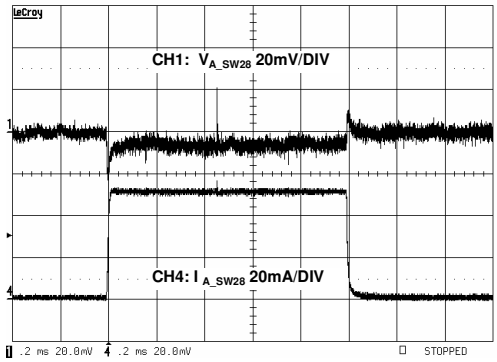
V_{SIM18} Load Transient



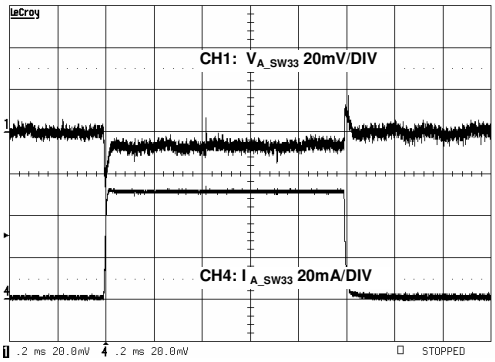
V_{SIM30} Load Transient



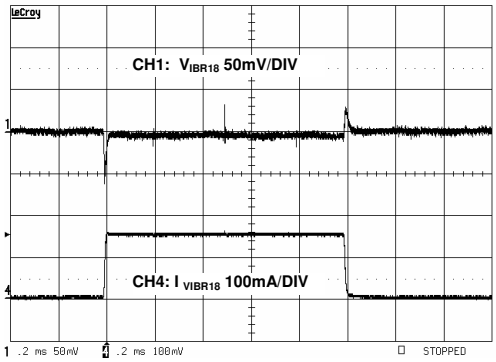
V_{A_SW28} Load Transient



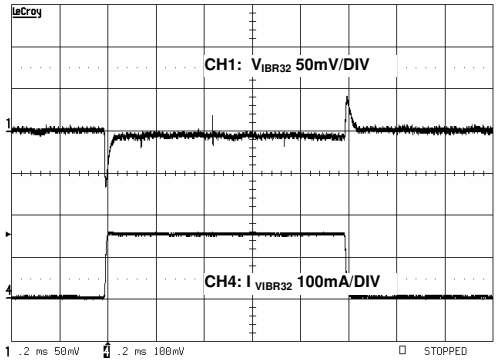
V_{A_SW33} Load Transient



V_{IBR18} Load Transient

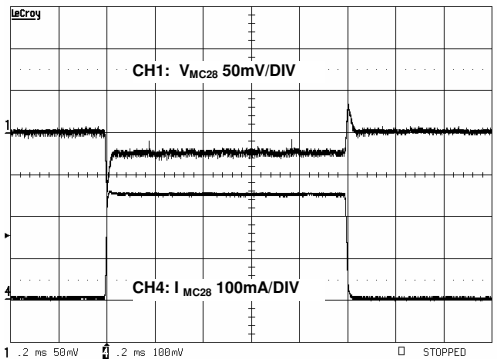


V_{IBR32} Load Transient

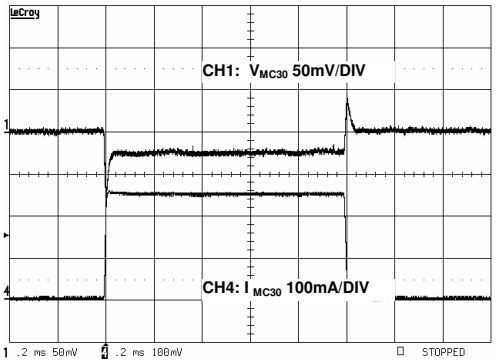


Electrical Characteristics (continued)

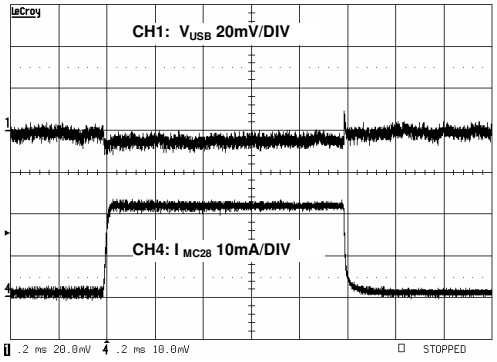
V_{MC28} Load Transient



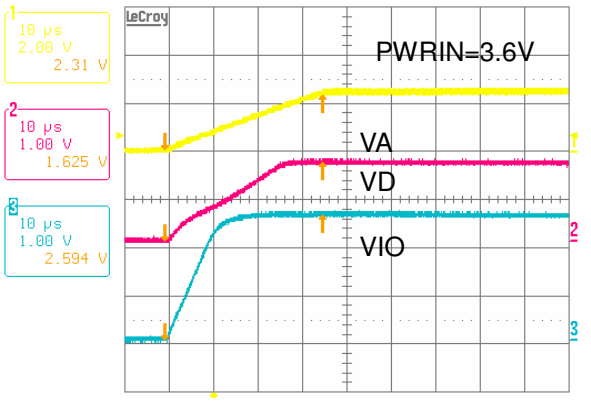
V_{MC30} Load Transient



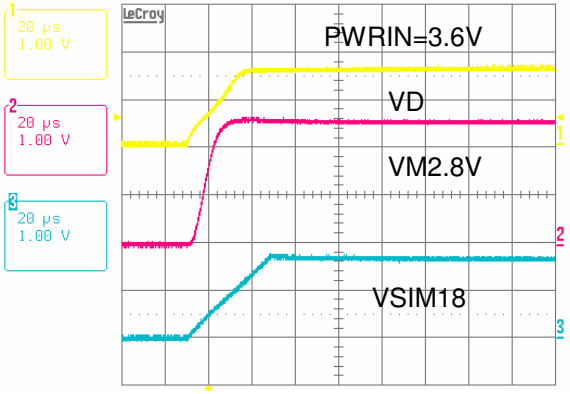
V_{USB} Load Transient



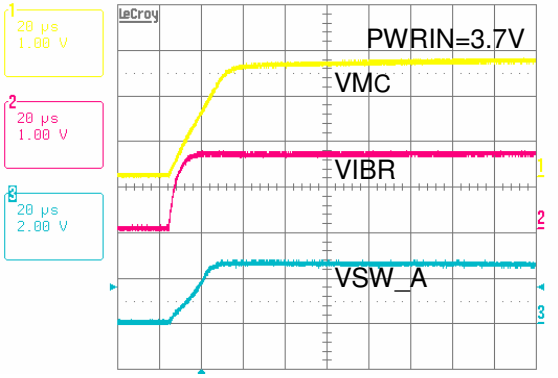
Power ON



Power ON

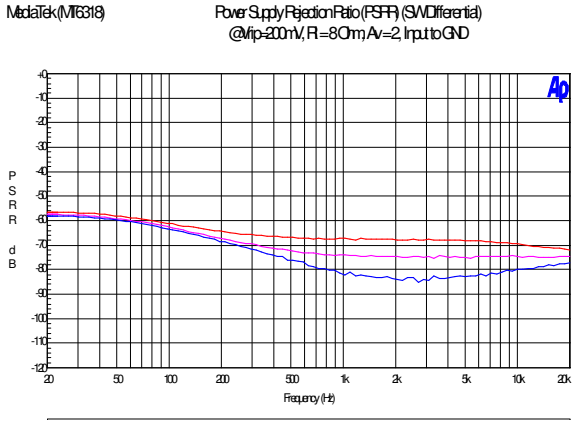


Power ON

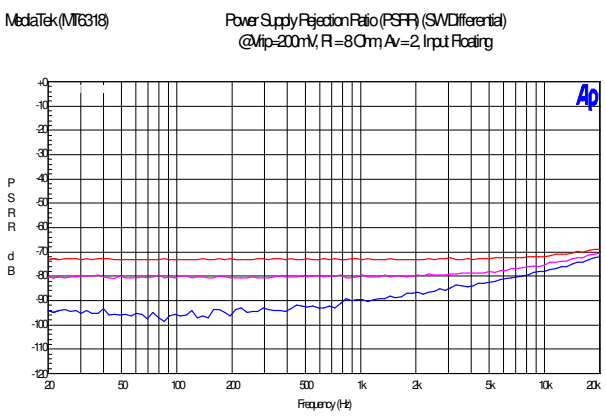


Electrical Characteristics (continued)

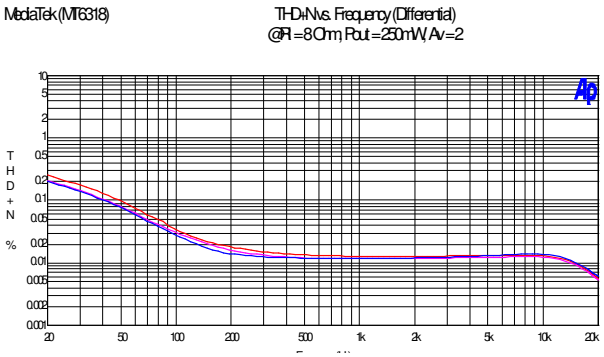
Audio Amplifier PSRR (Input to GND)



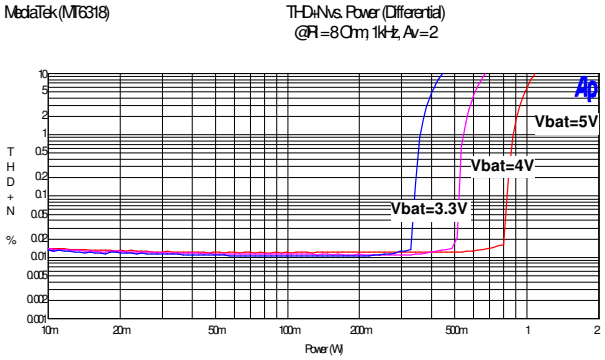
Audio Amplifier PSRR (Input Floating)



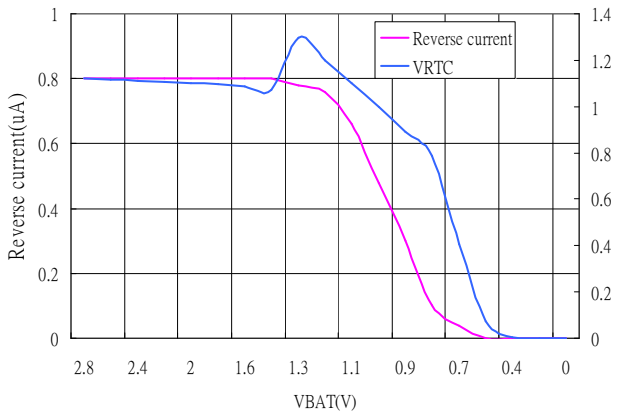
THD+N vs Frequency



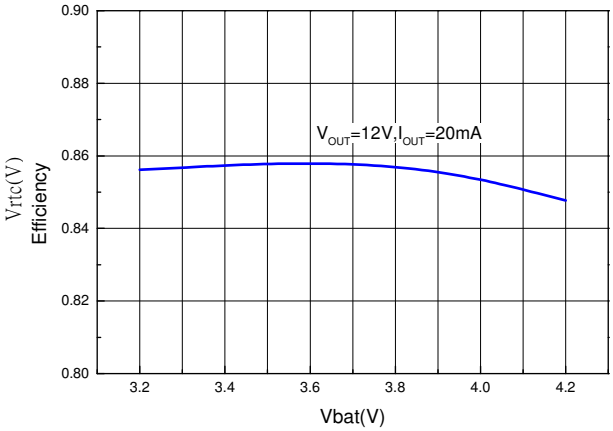
THD+N vs Output Power



2 STEP RTC

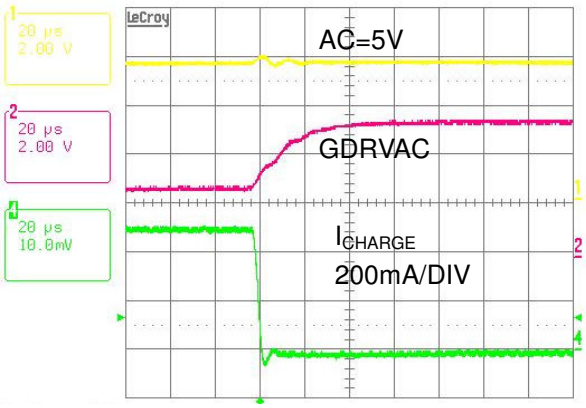


DC/DC Efficiency for BL

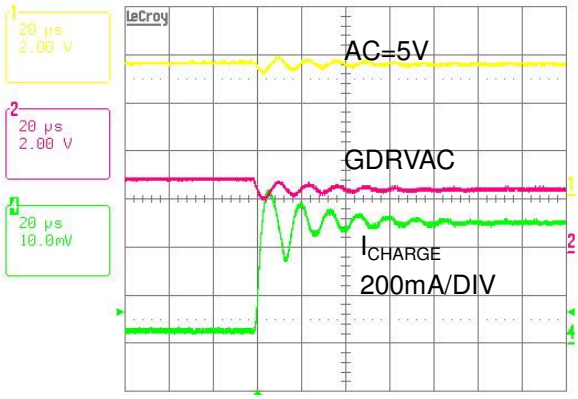


Electrical Characteristics (continued)

Charger Enable



Charger Disable



3 Pin Assignments

Figure 2: MT6318 TFBGA 96(7x7 mm^2) Pin Assignments

	1	2	3	4	5	6	7	8	9	10	
A	LED_KP	C2+	C1+	C1+	PWRIN4	FB_BL	BLDRV	PWRIN3	PWRBB	BAT_ BACKUP	A
B	VO_G	VO_R	CS_KP	DC_OV	PWRIN4	CS_BL	RST CAP	PWRIN3	INT	BAT_ON	B
C	V_USB	VO_B	GND4	GND4	PWRIN4	GND4	GND4	PWRIN3	RTC _SEL	VIO	C
D	USB	GDR VUSB	GND1	GND4	PWRIN4	GND4	GND3	GND3	PWRIN2	PWRIN2	D
E	AC	GDR VAC	GND1	GND1			GND3	GND3	VD_ SEL	VA_SW	E
F	VBAT	ISENSE	GND1	GND1			GND3	SPICS	RESET	VIBR	F
G	VN	SEL2	GND1	GND1	GND2	GND2	GND2	SPICK	SRCLK EN	VRTC	G
H	VTCXO	SEL1	SEL1 _EN	GND2	ISENSE _OUT	GND2	GND2	SIO	SIM VCC	SIM RST	H
J	PWRIN1	PWRIN1	PWRIN1	VB_OUT	AUDP	AUDN	SIMIO	SPIDAT	SRST	VD	J
K	VA	BP/REF	VMC	VM_ SEL	SPK+	SPK-	PWR KEY	VSIM	SIM CLK	SCLK	K
	1	2	3	4	5	6	7	8	9	10	

Table 10: MT6188 Pin Descriptions

Pin	Symbol	Input (I), Output (O), or Analog (A)	Description
Control			
K7	PWRKEY	I	Power on button input. Active low.
A9	PWRBB	I	Power on/off from microprocessor. Active high.
G9	SRCLKEN	I	VTCXO and VA enable. High = enable. Low = disable.
H9	SIMVCC	I	VSIM enable. High = enable. Low = disable.
B10	BAT_ON	I	Indication that Li-ion battery is inserted. High = no battery. Low = battery inserted.
B4	DC_OV	I	DC/DC protection input. OV threshold voltage is 1V.
K4	VM_SEL	I	External memory supply selection. 1 = 2.8V, 0 = 1.8V.
H3	SEL1_EN	I	Enable the “pre-charge indication” function. 1 = enable, 0 = disable. (Note1)
C9	RTC_SEL	I	VRTC output voltage selection. 1 = 1.5V, 0 = 1.2V (Note1)
E9	VD_SEL	I	VD output voltage selection. 1 = 1.8V/1.5V, 0 = 1.2V/0.9V (depending on the register PWR_SAVE_SPI setting).
Charger Control			
E1	AC	IA	AC-DC adaptor input
D1	USB	IA	USB power input
C1	VUSB	OA	3.3V USB power output
B9	INT	O	Interrupt PIN. Active low. This pin informs the BB if an AC or USB voltage is detected, or if OVP (AC > 9V) is detected. Is reset to normal high after BB has communicated with the PMIC through the SPI.
D2	GDRVUSB	OA	Control output to the gate of the external p-channel FET for the USB charger.
E2	GDRVAC	OA	Control output to the gate of the external p-channel FET for the AC charger.
F2	ISENSE	OA	Charger current sensing input
H2	SEL1	OA	Control output to the gate of the external PMOS for the AC charger input as power source.
G2	SEL2	OA	Control output to the gate of the external PMOS for the VBAT input as power source.
SIM Interface			
J7	SIMIO	I/O	Non level-shifted SIM data (3V)
H10	SIMRST	I	Non level-shifted SIM reset input (3V)
K9	SIMCLK	I	Non level-shifted SIM clock input (3V)
H8	SIO	I/O	Level-shifted SIM data (1.8/3V)
J9	SRST	O	Level-shifted SIM reset output (1.8/3V)
K10	SCLK	O	Level-shifted SIM clock output (1.8/3V)
Reset			
B7	RSTCAP	IA	Reset delay time capacitance
F9	RESET	O	System reset. Low active.

Power-Related			
F1	VBAT	IA	Battery input voltage
J1, J2, J3, D9, D10, A8, B8, C8, A5, B5, C5, D5	PWRIN	IA	Power input
J4	VB_OUT	OA	Battery output voltage. Switchable.
H5	ISENSE_OUT	OA	ISENSE output voltage. Switchable.
K2	BP/VREF	OA	Bandgap reference and bypass capacitance
D3, E3, E4, F3, F4, G3, G4, G5, G6, G7, H4, H6, H7, D7, D8, E7, E8, F7, C3, C4, C6, C7, D4, D6	GND		Ground
J10	VD	OA	Digital core supply
C10	VIO	OA	Digital IO supply
K1	VA	OA	Analog supply
E10	VA_SW	OA	Auxiliary analog supply. Switchable.
H1	VTCXO	OA	TCXO supply
G1	VM	OA	Memory supply
K8	VSIM	OA	SIM supply
G10	VRTC	OA	RTC supply
K3	VMC	OA	Memory card supply
Miscellaneous			
F10	VIBR	OA	Vibrator driver
A3	C1+	A	Charge pump capacitor. Positive terminal.
A4	C1-	A	Charge pump capacitor. Negative terminal.
A2	C2+	A	DC/DC output back-up capacitor. Positive terminal.
A10	BAT_BACKUP	OA	Backup battery pin for 2-step RTC
Speaker Amplifier			
J5	AUDP	IA	Audio positive input
J6	AUDN	IA	Audio negative input
K5	SPK+	OA	Speaker positive output
K6	SPK-	OA	Speaker negative output
LED Driver			
B2	VO_R	IA	R LED current driver
B1	VO_G	IA	G LED current driver
C2	VO_B	IA	B LED current driver
A1	LED_KP	OA	KP LED driver
B3	CS_KP	IA	KP LED current sensor
A7	BLDRV	OA	Control output to the gate of the external FET for the backlight DC-DC converter.
B6	CS_BL	IA	Voltage sensor input for external BL FET current
A6	FB_BL	IA	Voltage sensor input from white LED ballast resistor
SPI Interface			
F8	SPICS	I	Serial port select input
G8	SPICK	I	Serial port clock input
J8	SPIDAT	IO	Serial port I/O

Note1: The state of these pins is latched when MT6318 starts up. The state can changed only by powering down and powering up MT6318 again.

4 Introduction

4.1 Overview

This document describes the specifications for the MT6318 power management IC (PMIC), including its functional requirements and electrical characteristics. MT6318 supports the MT621x series baseband chips for multimedia phones, GPRS phones and color LCD GSM-only phones.

To complete a GSM/GPRS mobile handset, where power saving is a paramount issue, a device that supports power-related functions and control by the MMI is required. This functional block must support the following main features:

1. Low drop-out (LDO) regulators,
2. Switching DC/DC and charge pump with high operation efficiency and low standby currents,
3. Power-on reset and start-up timers,
4. Battery charging circuits,
5. Thermal overload protection,
6. Under-voltage lockout protection, and,
7. Over-voltage lockout protection.

For the MT621x series baseband chips, PMIC provides the following supply voltage and current and functionality to complete a GSM/GPRS mobile handset:

A. Power source: one Li-ion battery cell

B. Charger for the Li-ion battery

C. Power-up sequencer and protection logic

D. Eleven low drop-out regulator outputs

Table 11: LDO Regulators

Item	LDO	Voltage	Current	Description
1	VD	* 1.8V/1.5V / 1.2V/0.9V	200 mA	Digital core
2	VMC	2.8V / 3.0V	250 mA	Memory card (MS, SD, MMC)
3	VIO	2.8V	100 mA	Digital IO
4	VA	2.8V	150 mA	Analog and mixed signal
5	VA_SW	2.8V / 3.3V	50 mA	Auxiliary analog circuit
6	VRTC	* 1.5V / 1.2V	0.6 mA	Real-time clock
7	VM	1.8V / 2.8V	150 mA	External memory, selectable
8	VSIM	1.8V / 3.0V	20 mA	SIM card, selectable
9	VTCXO	2.8V	20 mA	13/26 MHz reference clock
10	VUSB	3.3V	20 mA	USB IO
11	VIBR	1.8V / 3.2V	200 mA	Vibrator

* The VD LDO and VRTC LDO have options available.

- VD output voltage can be configured as 1.8 V or 1.2 V. The 1.5 V and 0.9 V are power-down modes that can be controlled either by the SRCLKEN pin or by the PWR_SAVE_SPI software register.
- VRTC output voltage can be configured as 1.5 V or 1.2 V.

E. Four LED drivers:

Table 12: LED Drivers

Regulator	Type	Current	Description
LED_R	Current regulator	12/16/20/24 mA	Drives the red LED
LED_G	Current regulator	12/16/20/24 mA	Drives the green LED
LED_B	Current regulator	12/16/20/24 mA	Drives the blue LED
LED_KP	Voltage feedback current regulator	80 mA	Drives the keypad LEDs

The output current ratings for the above regulators already include a 50% margin on their nominal current consumption, e.g. if a regulator output is listed as 150 mA, the peak consumption current is 100 mA. In the active state, the phone consumes peak output current at each regulator, which must be considered for the thermal design.

F. LCD backlight white LED driver control

To avoid a high-voltage process, only the control part is implemented in this PMIC. The external driver capability is specified as follows in Table 13.

Table 13: LCD Backlight Driver

Driver	Type	Current	Description
V_BL	DC/DC switch, using inductor	80 mA	Drives the white backlight LEDs

G. 400 mW single channel audio amplifier

H. SPI 3wire interface

4.2 Terms and Definitions

Term	Definition
BB	Baseband chip
ESD	Electrostatic discharge
HBM	Human body model
LDO	Low drop-out regulator
OV	Over-voltage protection, for when the battery voltage exceeds a set threshold.
OVP	Over-voltage protection, for when the charger voltage exceeds a set threshold.
PMIC	Power management integrated chip
PSRR	Power supply rejection ratio
UV	Under-voltage

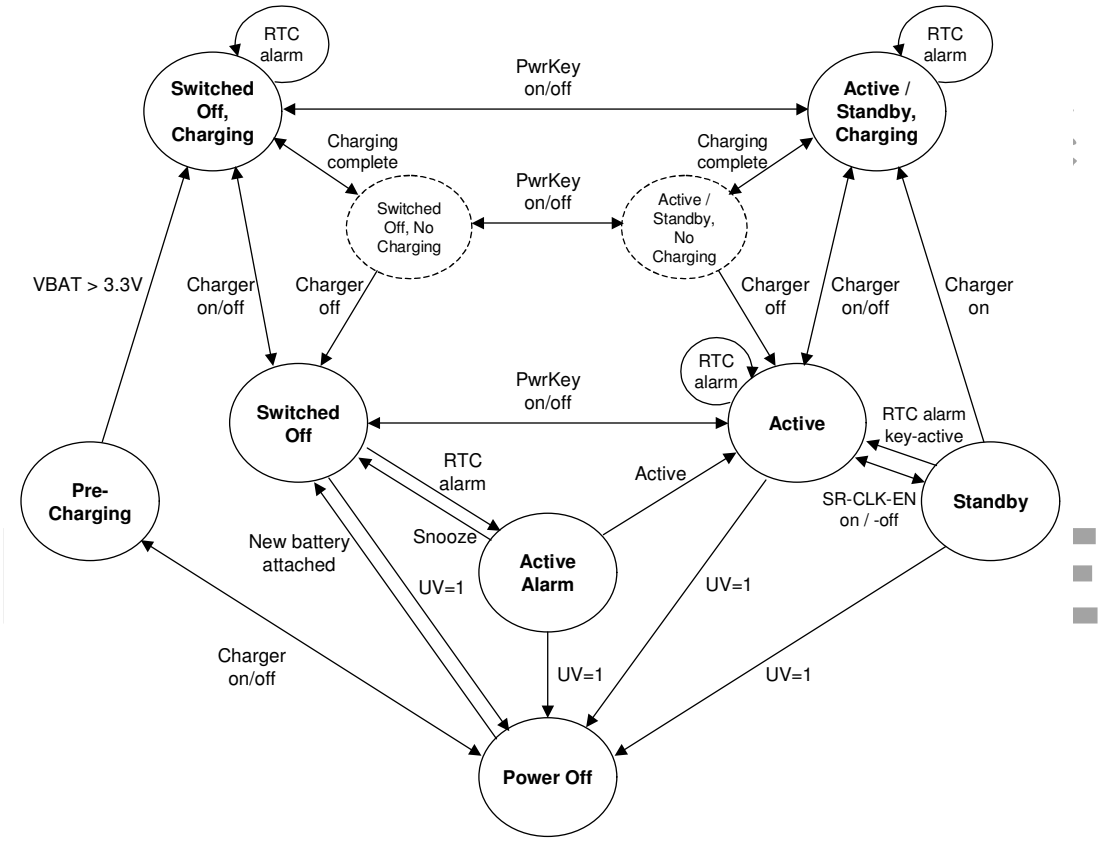
5 Functional Description

5.1 General

Power management is one of the most important functions in this PMIC. The power management function applies proper management procedures and control functions to the mobile handset's battery, charger, and power supply. More specifically, the management criterion is to provide power to the mobile phone while extending the standby/active time as long as possible.

To describe more clearly the functionality of the PMIC, the operation state diagram of a typical mobile phone is illustrated in Figure 3. The block diagram implemented in PMIC is shown further below to describe the relationships between different states.

Figure 3: Power Management State Diagram



Note that the above diagram includes many software activities. PMIC reacts to only part of the states. The state diagram can be then simplified as follows:

Figure 4: PMIC Hardware State

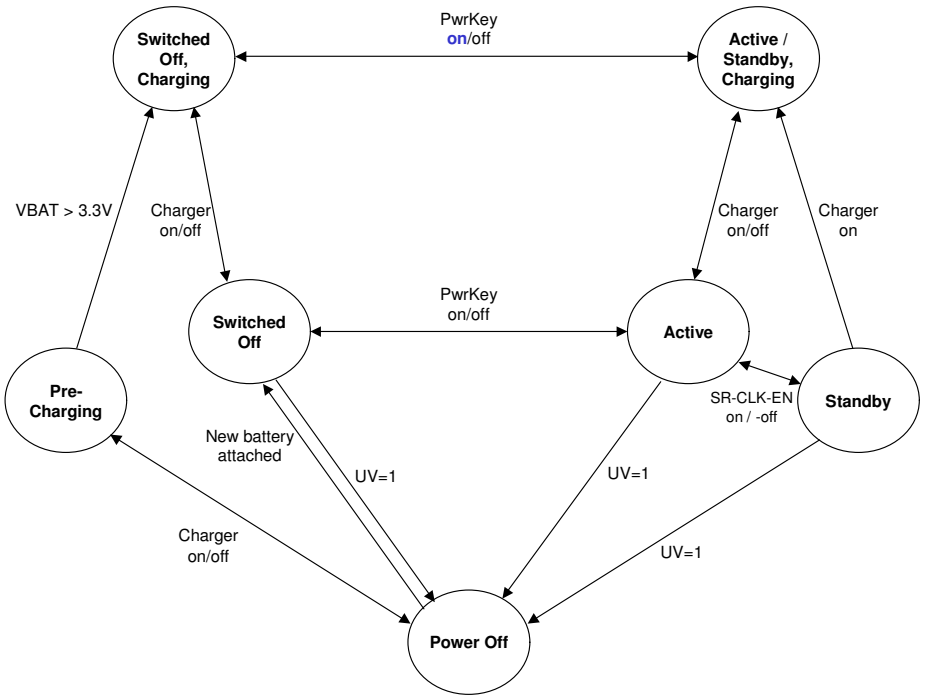


Table 14: Phone State Descriptions

State	Description
Power Off	No battery is connected, or a battery is connected but the battery is deeply discharged, i.e. VBAT < 3.3 V. In this state, only the VRTC LDO is enabled. VRTC is disabled when VBAT < 2.5 V.
Switched Off	A battery is connected to the phone but the phone is switched off. The battery voltage is higher than 3.3 V. In this state, VRTC is enabled, and all other LDOs are disabled.
Pre-Charging	The charger is connected to the mobile, but VBAT < 3.3 V. Slow charging is activated by the PMIC charger circuits. Charging at 50 mA constant current. When VBAT is charged up to 3.3 V, the detection circuit in PMIC enables normal charging and pulls the UV signal low, and enables all LDO outputs.
Standby	The phone is powered up but the 13 MHz reference clock is disabled, part of the BB chip runs on the 32 kHz clock. In this state, the VTCXO LDO is disabled; the VD, VIO, VM, VA and VRTC LDOs are enabled.
Active	The phone is powered up and running on the 13 MHz reference clock. All LDOs are enabled, and the mobile radio task is running.
Active Alarm	The phone is woken up via the RTC alarm, and all LDOs are enabled, but only the alarm task is scheduled. No radio activities are scheduled.
Switched Off, Charging	The mobile has a charger connected, the BB chip is active and running on the 13 MHz reference clock but only charging software is scheduled, no radio nor MMI tasks are activated. The LCD screen only shows the battery charging status.
Active, Charging	The mobile has a charger connected, the BB chip is active and running on the 13 MHz reference clock with regular mobile radio and MMI tasks activated. The LCD screen shows the battery charging status and all normal tasks.

Table 15: Extreme Case Definitions

Term	Definition
Under voltage (UV)	When PWRIN < 2.9 V in the switched-on condition (active or idle). PMIC goes to the power-off state.
Over voltage protection (OVP)	When AC > 9.0 V, a hardware over voltage protection circuit (OVP) is activated to turn off charging. The charger status register D7 is set to 1 when OVP occurs. PMIC keeps charging off until the AC voltage returns to the normal range.
Over voltage (OV)	When VBAT > 4.3 V, a hardware over voltage protection circuit (OV) is activated to turn off charging. PMIC keeps charging off until VBAT returns to the normal range. Normally VBAT does not exceed 4.2 V during charging, but if something wrong happens during charging, OV protects the battery pack from being overcharged.
Thermal overload (THR)	Thermal overload protection function. When phone is in the active state and PMIC reach the overheating condition then PMIC shuts down completely.

Table 16: LDO Turn On Table

Conditions							Operations							
THR	UV (PWRIN)	CHDET	PWRKEY	PWRBB	SRCLKEN	PWRIN < 2.5V	VTCXO	VRTC	VA	VD, VIO, VM	VUSB	VMC	VSIM	VA_SW
L	H	X	X	X	X	H	Off	Off	Off	Off	Off	Off	Off	Off
L	H	X	X	X	X	L	Off	On	Off	Off	Off	Off	Off	Off
L	L	L	H	L	X	L	Off	On	Off	Off	Off	Off	Off	Off
L	L	H	X	X	H	L	On	On	VA_SEL/VB_OUT = 0, VA = VD VA_SEL/VB_OUT = 1, VA = VTCXO	On	USB_PWR	VMC	SIMVCC	VA_SW = 0 Off VA_SW = 1, VA
					L	L	Off	On	VA_SEL/VB_OUT = 0, VA = VD VA_SEL/VB_OUT = 1, VA = VTCXO	On	USB_PWR	VMC	SIMVCC	VA_SW = 0 Off VA_SW = 1, VA
L	L	X	L	X	H	L	On	On	VA_SEL/VB_OUT = 0, VA = VD VA_SEL/VB_OUT = 1, VA = VTCXO	On	USB_PWR	VMC	SIMVCC	VA_SW = 0 Off VA_SW = 1, VA
					L	L	Off		VA_SEL/VB_OUT = 0, VA = VD VA_SEL/VB_OUT = 1, VA = VTCXO	On	USB_PWR	VMC	SIMVCC	VA_SW = 0 Off VA_SW = 1, VA
L	L	X	X	H	H	L	On	On	VA_SEL/VB_OUT = 0, VA = VD VA_SEL/VB_OUT = 1, VA = VTCXO	On	USB_PWR	VMC	SIMVCC	VA_SW = 0 Off VA_SW = 1, VA
					L	L	Off		VA_SEL/VB_OUT = 0, VA = VD VA_SEL/VB_OUT = 1, VA = VTCXO	On	USB_PWR	VMC	SIMVCC	VA_SW = 0 Off VA_SW = 1, VA
H	X	X	X	X	X	L	Off	On	Off	Off	Off	Off	Off	Off

- 'X' means either high or low; the setting does not matter.
- During pre-charging, an external switch can be used to supply power to the LDOs (VD, VIO, VM, VRTC, VA and VTCXO).
- The USB LDO regulates PWRIN to 3.3 V for the BB (USB IO). The VUSB 3.3 V LDO output on/off follows the control bit USB_PWR (Register 1 [3]). When the USB_PWR control bit is set to "off", the VUSB output voltage must drop below 0.3 V within 1 ms. (VUSB output is shunt with a 1 µF capacitor.)

5.2 State Timing

In this section the power on/off, wake up, charging and reset sequences are described in detail. For the following timing diagrams, the phone state is shown in the x-axis, and the y-axis shows the related signals. The text above represents the transition events.

Figure 5: Power Key State Timing

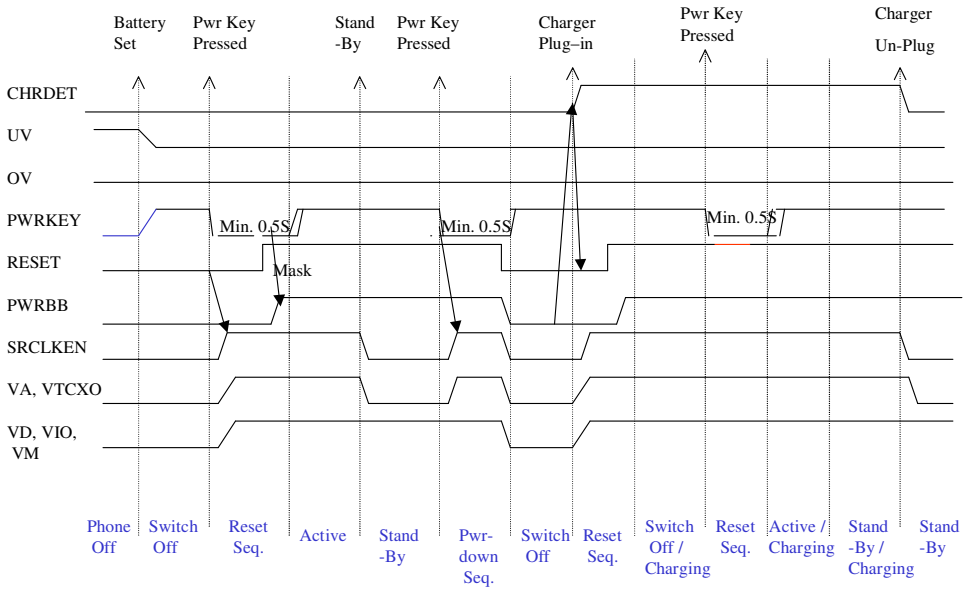


Figure 6: State Timing for Wake-up, Paging and Standby

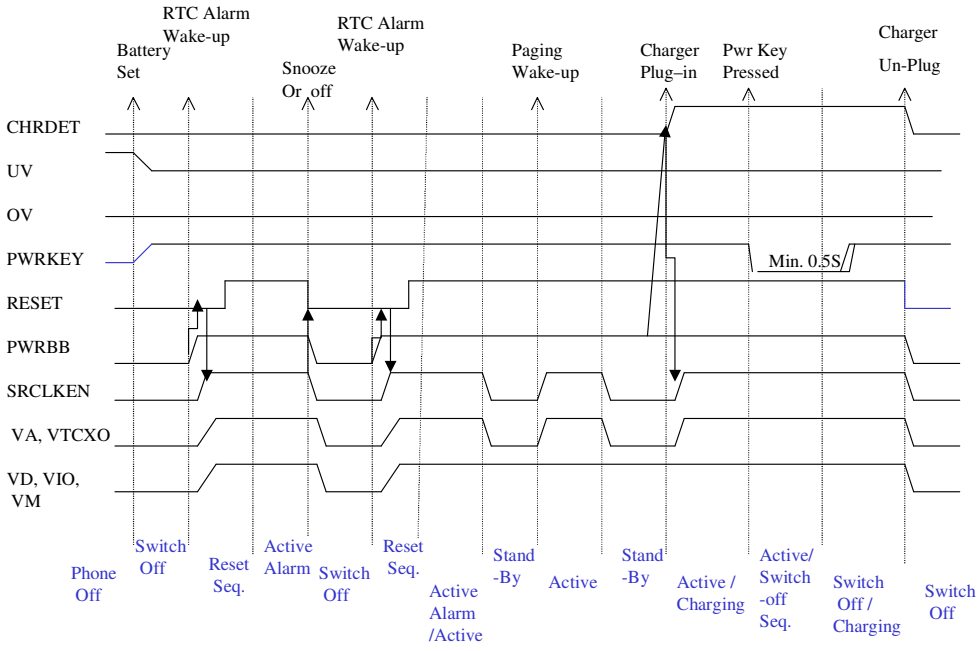
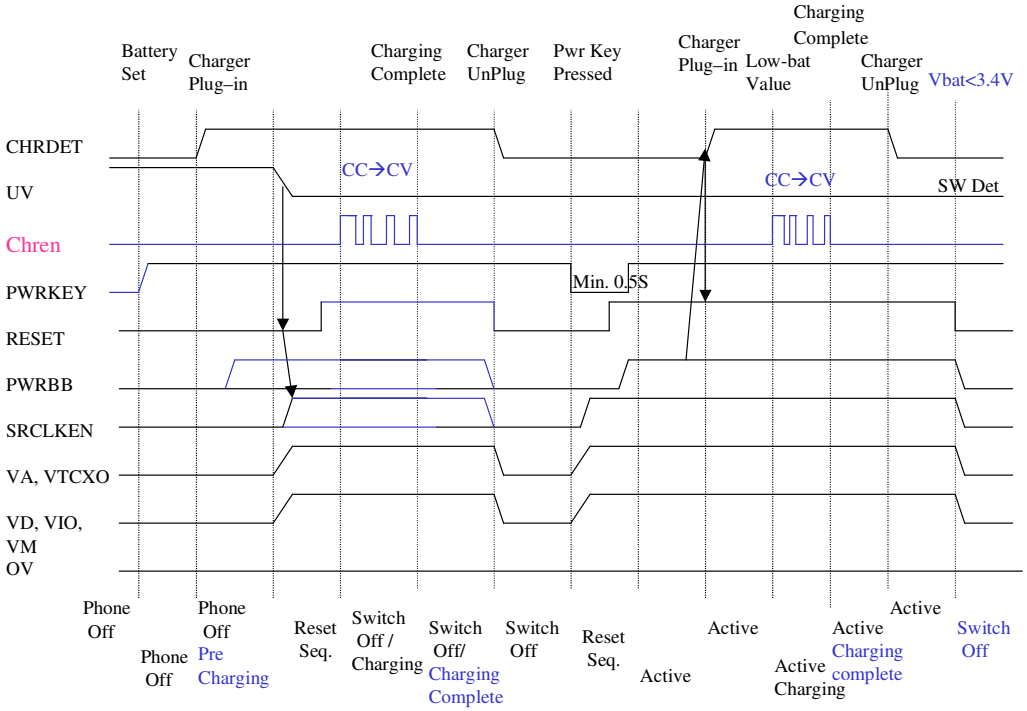
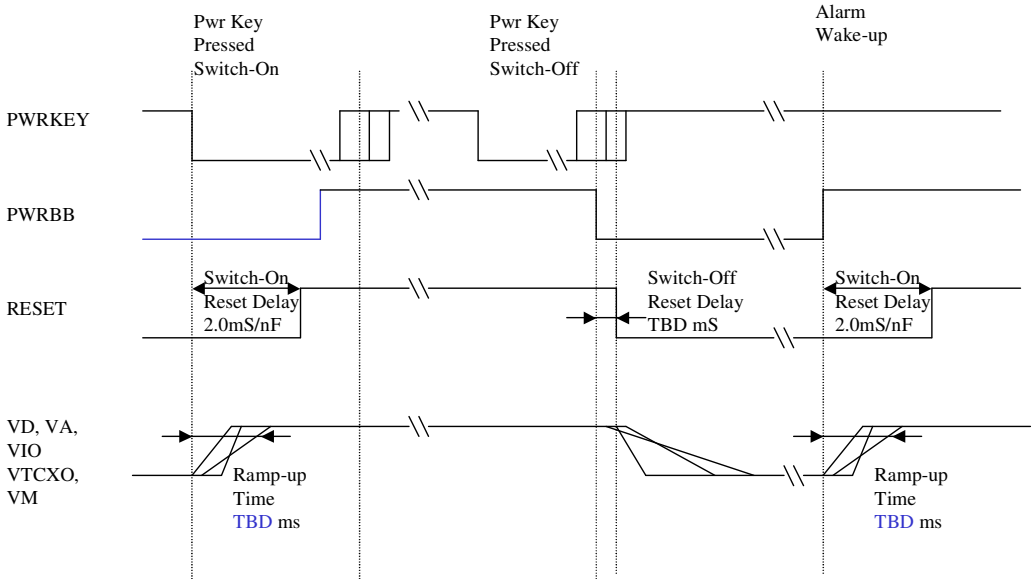


Figure 7: Charger State Timing



*Chren is PMIC internal signal

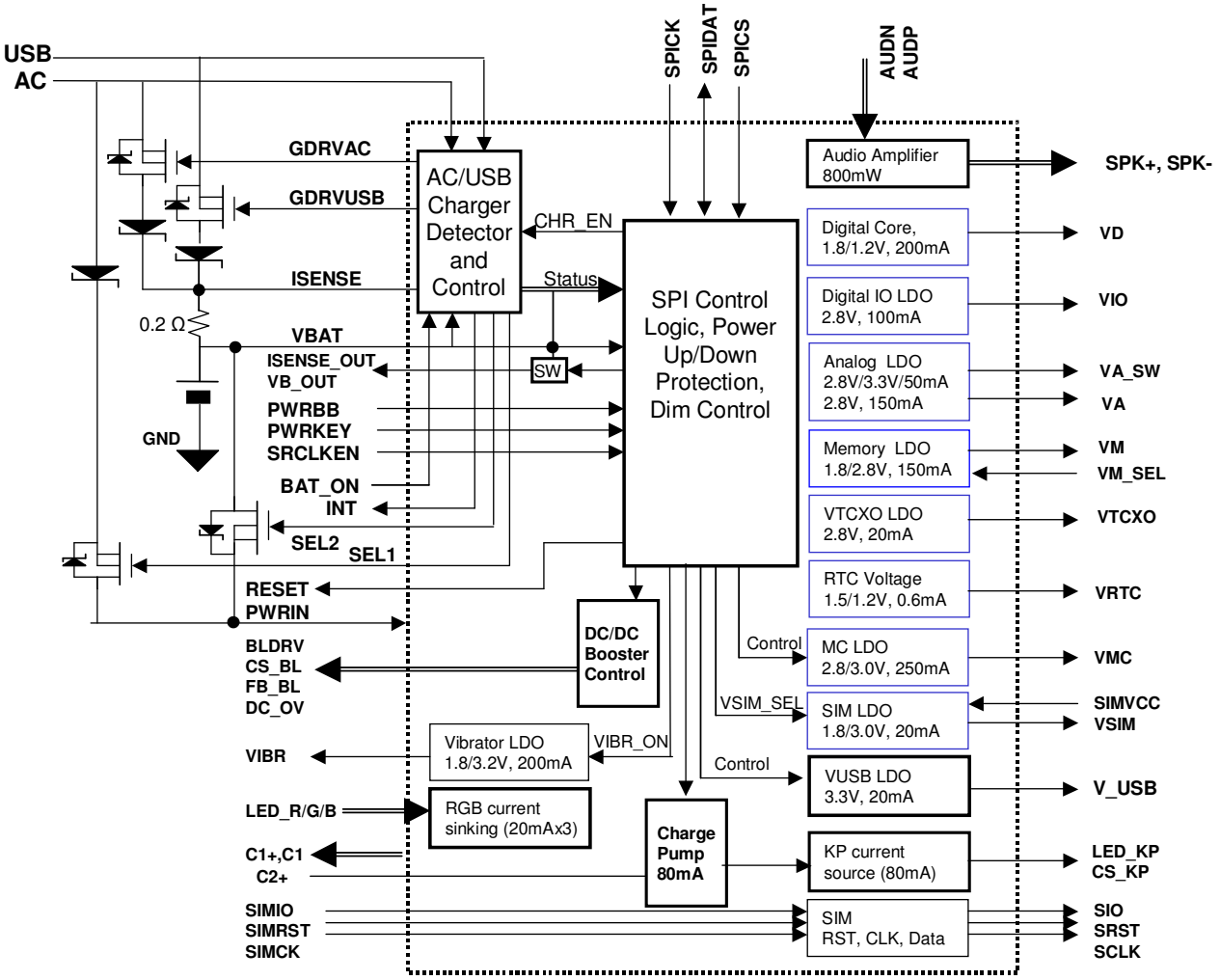
Figure 8: Reset Timing



5.3 PMIC Functional Blocks

To describe each block of the PMIC in detail, the overall hardware block diagram of PMIC is depicted in Figure 9. More detailed descriptions for each sub-block are provided in the following sections.

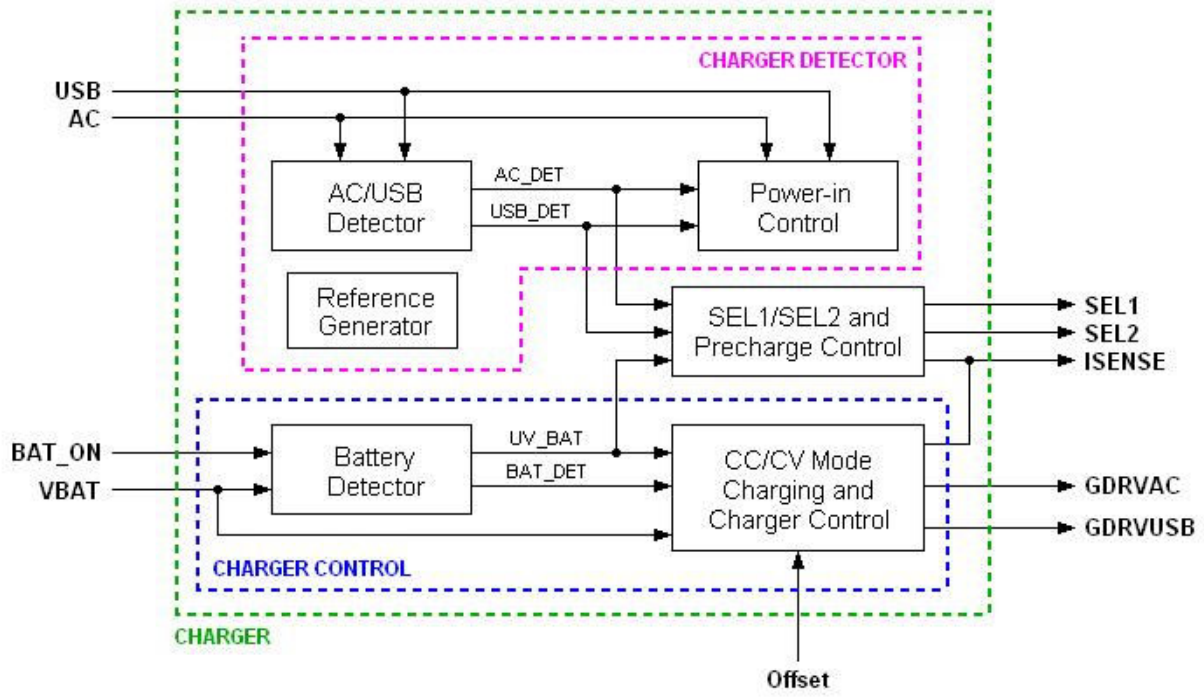
Figure 9: PMIC Block Diagrams



5.3.1 Charger Circuit

The charger circuit in PMIC is mainly comprised of 3 sub-functions. Figure 10 shows the block diagram of the charger in detail.

Figure 10: PMIC Charger Block Diagrams



5.3.1.1 Charger Detector

The charger detector senses the charging voltage from either a standard AC-DC adaptor or a USB connection. When the charging input voltage is greater than the pre-determined threshold, the charging process is triggered. This detector resists higher input voltages than other parts of the PMIC; i.e. if an excess charging source is detected (> 9.0 V), the charger detector stops the charging process to avoid burning out the whole chip or even the whole phone.

If both AC and USB chargers are detected, the charging source uses the AC source.

When the presence of a charger voltage (either AC or USB) is detected, an interrupt output pin INT becomes active (pull LOW). The INT is also active when the AC or USB regulator is removed. The PMIC resets INT to HIGH after the BB chip reads the PMIC through the SPI.

5.3.1.2 Charger Control

When the charger is on, this block controls the charging phase and turns on the appropriate LDOs according to the battery status. The battery voltage is constantly monitored: if the voltage is greater than 4.3 V, charging is stopped immediately to prevent permanent damage to the battery.

In CC mode, several charging currents can be set by programming Register 1 [2:0]. When AC charging, the charging current can be up to 800 mA. When USB charging, the charging control first clamps the charging current to 87.5 mA. After the BB communicates with the USB host and if the power class is announced as 450 mA, the BB sets the register via SPI, and the PMIC charger releases the charging current limit to 450 mA. For more details, refer to Table 25.

The BB can disable the USB task by setting Register 1 [1] (USB_PWR) to 0 via the SPI. After the USB regulator shuts off the USB host is virtually disconnected while the charging process resumes its previous state. If the phone is in the switched-off state before USB power is inserted, the BB must wake up to determine the USB power class.

The other case is when the phone is in the switched-on state before USB power is inserted. The already-awake BB must determine the USB power class for proper charging as well as for the USB data transfer operation. The MMI allows the user to utilize the USB simply as a charger only, as described above.

Due to process variation, the charging current may vary form chip to chip. To compensate for this variation, an offset value is set in the PMIC. The PMIC reads this compensation value and applied the charging current offset when the phone is in the charging state. This compensation value may be calculated during the phone production calibration process, or it may be constantly observed by the BB while the phone is charging. The offset value is set by the BB software (Register 10 [2:0]).

5.3.1.3 Control for Pre-Charge Indication

The PMIC provides 2 control signals SEL1 and SEL2 for the application that shows pre-charge status on the LCD. In normal cases, VBAT is selected (SEL2 turned on) as the power input to the PMIC.

Under battery low conditions (VBAT < 3.3 V), the AC charger source is selected (SEL1 turned on) to substitute for the power normally provided by VBAT, allowing the BB to power up and at least light up the LED to show the charging status. However, if customers do not connect the two external switches, the pre-charging status is not displayed.

SEL1 is turned on only in the pre-charging state, SEL1 and SEL2 must not be turned on simultaneously at any time. During the pre-charging state, when VBAT passes 3.3 V, the PMIC switches SEL1 off and SEL2 on to have the VBAT supply the whole system as under normal conditions.

Table 17 lists the SEL 1 and SEL 2 states for each phone state.

Table 17: SEL1 and SEL2 Settings for Each Phone State

Initial Phone State	Initial Charging State	Condition	Description	PMIC Settings	
Not Charging					
Switched on, idle	X (Not charging)	VBAT > 3.3 V	Can make a phone call	SEL2 on	X
		VBAT < 3.3 V	Low battery warning every 30 s		
		VBAT = 3.3 V	Software shutdown		
		PWRIN = 2.9 V	PMIC shutdown		
Switched on, talking	X (Not charging)	VBAT > 3.3 V	Talking		
		VBAT = 3.3 V	Call dropped → low battery warning every 30 s		
Powered off, switched off	X (Not charging)	X	X		
Switched On, Charging					
Switched on, talking	Normal charging	VBAT ≥ 3.3 V	Talking	SEL2 on	A different charging current can be selected via the SPI in CC mode.
	CC mode charging	VBAT < 3.3 V	Call dropped → return to idle		
Switched on, idle	Normal charging	PWRIN ≥ 2.9 V	In idle		
Switched Off, Charging					
Powered off	Pre-charging	VBAT < 3.3 V	Pre-charge and power-on key disabled	SEL1 on	CC mode charging at 50 mA
Powered off → switched off transition	Pre-charging	VBAT = 3.3 V	Pre-charge and power-on key enabled	SEL1 off → (delay) → SEL2 on. During this transient, pre-charging is ongoing.	CC mode charging at 50 mA
Switched off	Normal charging	VBAT > 3.3 V	Only charger task is activated.	SEL2 on	A different charging current can be selected via the SPI in CC mode.

When charging the PMIC uses GRVAC and GDRVUSB pins to control the current flow through the external MOSs, and at the same time maintains the current control loop by sensing the voltage drop ISENSE across the external current sensor resistor (0.2 Ω). Note that the charging current limit is 450 mA for USB and 800 mA for AC.

Battery charging states include No Charge mode, Constant Current (CC) charge mode (pre-charge, constant current), and Constant Voltage(CV) charge mode (Figure 11). No matter what state the phone is in, the PMIC charger handles the charging state transition and reflects the status in Register 0 (charger status) for the BB to read.

Figure 11: Charging States Diagram

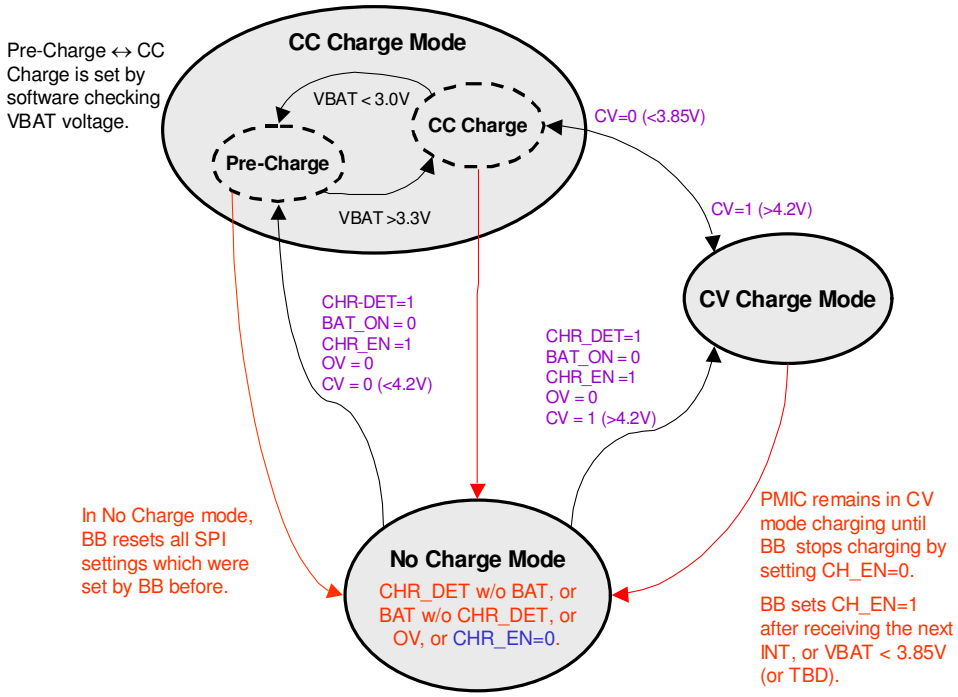


Table 18: Charger State Transition

Current State	Transition Conditions	Next State
No Charge	CHR_DET = 1, CV = 0, BAT_ON = 0	CC Charge mode
	CHR_DET = 1, CV = 1, BAT_ON = 0	CV Charge mode
CC Charge	CHR_DET = 0 BAT_ON = 1	No Charge mode
	CV = 1	CV Charge mode
CV Charge	CHR_DET = 0 BAT_ON = 1	No Charge
	CV=0	CC Charge mode

Note: CHR_DET is internal used bit in PMIC, which is related to USB_DET or AC_DET according to the table in below:

Table 19: CHR_DET Internal Bit

AC_DET	USB_DET	CHR_DET
0	0	No charging
0	1	USB regulator for charging
1	0	AC regulator for charging
1	1	AC regulator for charging
Illegal charger	0	No charging
Illegal charger	1	No charging

The BB can stop the charging by setting CHR_EN (Register 1 [7]) to 0 via the SPI, this means that although PMIC handle the charging process automatically, BB is the true master to manage the charging process. This control mechanism allows the BB to command the PMIC doing elegant trickling charging if necessary.

Pin BAT_ON (Register 0 [5]) turns off the charger immediately if the pin goes high (> 2.5±0.1 V). This function is designated to block the charger input in case the battery is accidentally removed. During charging, the disconnection of the battery might cause the VBAT voltage to surge, damaging the chip before the over-voltage protection can be turned on.

Note that UV is the internal signal that indicates the too-low condition of the battery voltage. The high-to-low UV threshold can be set in the 2-bit UV_SEL register with 2.9V/2.75V/2.6V/2.5V settings. The low-to-high threshold UV is 3.2 V. The hysteresis prevents the state from bouncing back and forth between pre-charge and other states. Recall that UV serves as the under voltage lock up signal (Figure 4). When UV=1, the battery is too weak to sustain an eligible phone call, therefore the PMIC moves into the powered-off state. To provide a pleasant user interface, in the switched on condition, the BB chip monitors the battery voltage: once VBAT is less than 3.3 V, the MMI issues an alert sound and/or displays a battery low message on the LCD to inform the user. For phones using this PMIC, the alert sound may be any user-specified chime rather than by traditional alerter.

Table 20 shows the charging states, and their responses to various conditions.

Table 20: Charging Control

State	CHR_EN	CHR_DET	VBAT < 3.3/3.0 V	CV (VBAT > 4.2 V)	BAT_ON (battery inserted)	Operation
No charging	X	L	X	X	L	Wait for CHR_DET transition
Charger detection	L	H	L	X	L	Wait for CHR_EN
Pre-charging	X	H	H	L	L	Monitor UV and CHR_DET (see Note)
CC charging	H	H	L	L	L	Monitor CV and CHR_DET
CV charging	H	H	L	H	L	Monitor CHR_DET
Pause charging	L	H	X	X	L	No charge; keep the current state. (For BB to emulate trickle charge)
Emergency stop	X	H	X	X	H	Turn off charger → powered off state

Note: The threshold voltage to determine the VBAT signal is 3.3 V for pre-charge state to CC mode, and 3.0 V for returning to pre-charge mode. This hysteresis is designed to prevent the state from bouncing back and forth between charge modes in events such as a surge of current demanded.

Figure 12: I-V Curve of Li-Ion Battery Charging

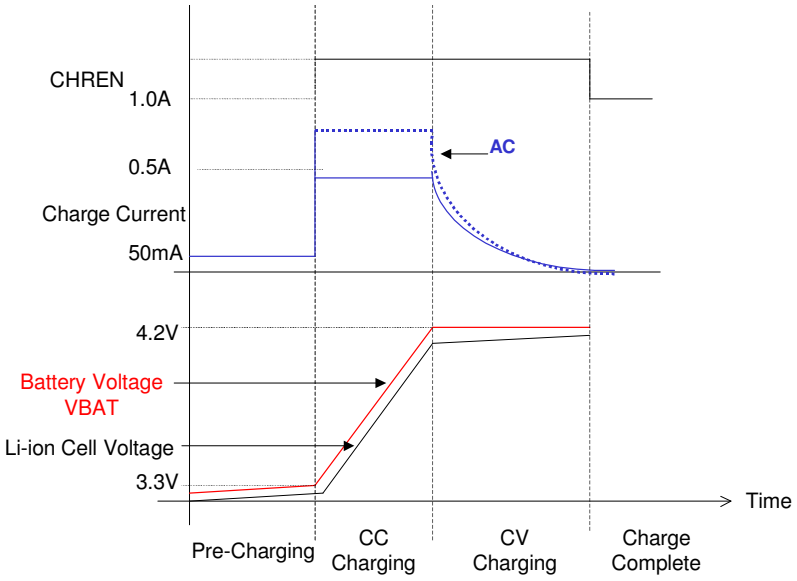


Table 21: Operation for Different Charging Sources

AC	USB	Phone State	Operation
Off	Off	Any state	No charging.
Off	On	Power off	Use USB to start pre-charge and turn on USB regulator. No matter what power class the USB attached can provide, PMIC charges the battery with constant pre-charge current. Since the BB is still off, no charge status is shown.
		Switch off	Use USB as the charging source. Turn on (VTCXO, VM, VD, VIO, VA) LDOs and USB regulator, then the BB triggers the USB function to determine the host's power class. After the BB sets the appropriate current limit, then the PMIC starts normal charging procedure and BB runs the charging management task to display the charging state.
		Switch on	Use USB as the charging source. First initiate the USB function to determine the host's power class. After the BB sets the appropriate current limit, then the PMIC starts normal charging procedure and BB runs the charging management task to display the charging state.
On	Off	Power off	Start pre-charge. Use SEL1 to select the AC charger source for PWRIN then turn on (VTCXO, VM, VD, VIO, VA) LDOs. BB runs the charging management task to display the charging state.
		Switch off	Turn on (VTCXO, VM, VD, VIO, VA) LDOs. BB runs the charging management task to display the charging state.
		Switch on	Follow normal charging procedure.
On	On	Power off	Use AC to start pre-charging. Can also use SEL1 to select the AC charger source for PWRIN. Turn on (VTCXO, VM, VD, VIO, VA) LDOs. BB runs the charging management task to display the charging state. Turn on the USB regulator.
		Switch off	Use AC as the charging source. Turn on (VTCXO, VM, VD, VIO, VA) LDOs to start normal charging procedure. BB runs the charging management task to display the charging state. USB regulator is turned on also.
		Switch on	Use AC as the charging source to start normal charging procedure. USB regulator is turned on also.

Note: The LDOs (VTCXO, VM, VD, VIO, VA) listed here are turned on/off by the PMIC itself. Other drivers like BL and RGB can be turned on via BB through SPI.

5.3.2 Low Dropout Regulator (LDOs) and Reference

The MT6318 integrates eleven LDOs that are optimized for their given functions by balancing quiescent current, dropout voltage, line/load regulation, ripple rejection, and output noise.

1. **Digital Core LDO (VD)**
   The digital core LDO is a regulator that sources 200 mA (max) with a 1.8 V or 1.2 V output voltage selection based on the supply voltage requirement of the BB chipset. The LDO also provides 1.5 V/0.9 V power-down modes that can be controlled either by the SRCLKEN pin or by the PWR_SAVE_SPI software register (Register 8 [5]). The digital core LDO supplies the BB circuitry in the handset, and is optimized for a very low quiescent current.

2. **Digital IO LDO (VIO)**
   The digital IO LDO is a regulator that sources 100 mA (max) with a 2.8 V output voltage. The LDO supplies the BB circuitry in the handset, and is optimized for a very low quiescent current. This LDO powers up at the same time as the digital core LDO.

3. **Analog LDO (VA)**
   The analog LDO is a regulator that sources 150 mA (max) with a 2.8 V output voltage. The LDO supplies the analog sections of the BB chipsets and is optimized for low frequency ripple rejection in order to reject the ripple coming from the RF power amplifier burst frequency at 217 Hz.

4. **TCXO LDO (VTCXO)**
   The TCXO LDO is a regulator that sources 20 mA (max) with a 2.8 V output voltage. The LDO supplies the temperature compensated crystal oscillator, which needs its own ultra low noise supply and very good ripple rejection ratio.

5. **RTC LDO (VRTC)**
   PMIC features a 2-step RTC that keeps RTC alive for a long time after the battery has been removed. The 1st LDO charges a backup battery on the BAT_BACKUP pin to ~2.6 V. Also, when the battery is removed, the first stage prevents the backup battery from leaking back to VBAT. The 2nd LDO regulates the 2.6 V supply to a 1.5 V/1.2 V optional RTC voltage. The RTC voltage can be set by the RTC_SEL pin while the BB is alive; the setting is retained while the BB is powered down. When the backup battery is fully charged, the high backup battery voltage, low reverse current leakage and the low 2nd LDO operating current sustain the RTC block for even tens of hours with the absence of the main battery.

6. **Memory LDO (VM)**
   The memory LDO is a regulator that sources 150 mA (max) with a 1.8 V or 2.8 V output voltage selection based on the supply specs of the memory chips. The LDO supplies the memory circuitry in the handset, and is optimized for a very low quiescent current. This LDO powers up at the same time as the digital core LDO.

7. **SIM LDO (VSIM)**
   The SIM LDO is a regulator that sources 20 mA (max) with a 1.8 V or 3.0 V output voltage selection based on the supply specs of subscriber identity module (SIM) card. The LDO supplies the SIMs in the handset, and is controlled independently of the other LDOs.

8. **Memory Card LDO (VMC)**
   The memory card LDO is a regulator that sources 250 mA (max) with a 2.8 V or 3.0 V output voltage selection. The LDO supplies the memory card (MS, SD, MMC) in the handset, and is controlled independently of the other LDOs.

9. **Auxiliary Analog Circuit LDO (VA_SW)**
   The auxiliary analog circuit LDO is a regulator that sources 50 mA (max) with 2.8 V or 3.3 V output voltage selection based on the VA_SW_SEL register setting (Register F [7]). It can be switched on/off by register control.

10. **USB IO LDO (VUSB)**
    The USB IO LDO is a regulator that sources 20 mA (max) with a 3.3 V output voltage. The LDO output on/off follows the control bit USB_PWR (Register 1 [3]). When the USB_PWR control bit is set to off, the VUSB output voltage drops below 0.3 V within 1 ms. (VUSB output is shunt with a 1 µF capacitor.)

11. **Vibrator LDO (VIBR)**
    The vibrator LDO is a regulator that sources 200 mA (max) with a 1.8 V or 3.2 V output voltage selection based on the VIBSEL register setting (Register E [1]). This LDO can be powered on/off by register control (Register 8 [0]).

12. **Reference Voltage Output (VREF)**
    The reference voltage output is a low noise, high PSRR and high precision reference with a guaranteed accuracy of 1.5% over temperature. The output is used as a system reference in MT6318 internally. However for accurate specs of every LDO output voltage, avoid loading the reference voltage; only bypass it to GND with a minimum 100 nF capacitance.

5.3.3 LED Drivers

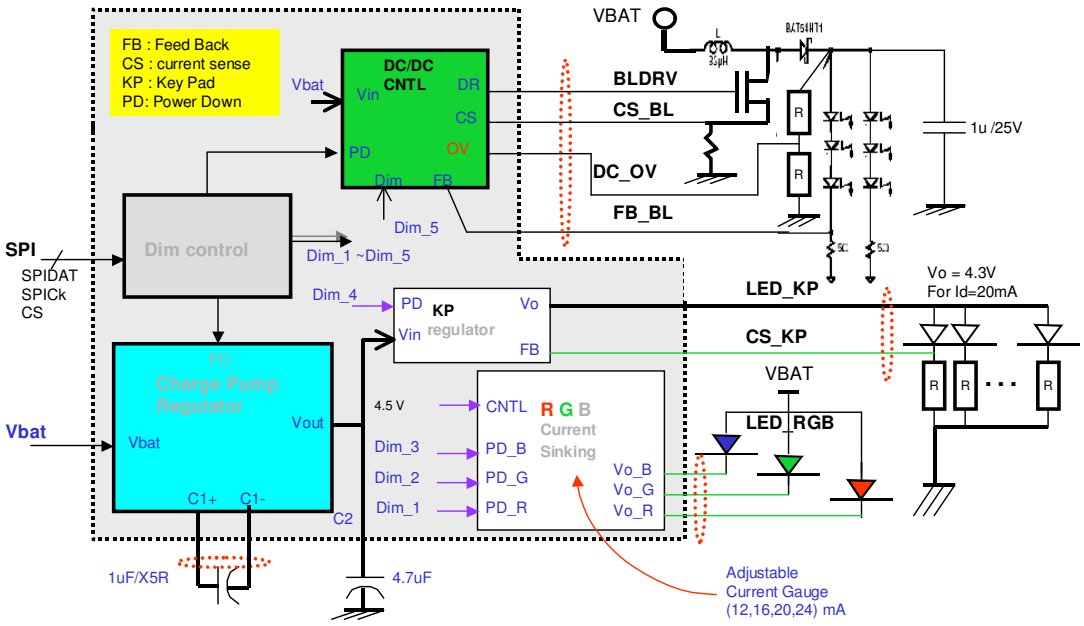
PMIC provides 4 independent drivers. Three of them use an identical structure to drive 3 different LEDs (R, G, B). The fourth is dedicated to driving the keypad LEDs. The reason for separating the LED drivers into 2 groups is phone feature oriented. First, for the colorful backlight display when a call is incoming, three independent drivers can be used to blend many illuminating colors easily. Second, LEDs for a bar type phone's LCD and keypad normally do not turn on at the same time. Therefore a 2-step architecture is beneficial for pin count saving and power efficiency.

The first common block for the keypad (KP) and R/G/B LED drivers is a switching capacitor type DC/DC (charge pump circuit) that boosts VBAT to 4.5 V (note VBAT < 4.2 V). This charge pump circuit features a driving capability control option for reduced current consumption and start-up inrush current.

The KP LED driver is a voltage feedback type regulator available to supply 80 mA for up to 4 parallel KP LEDs. External ballast resistors are necessary and serially connected to each LED, but only one provides feedback voltage to the PMIC. Moderate variations in light intensity for different LEDs in the KP is not a critical issue, therefore this configuration is simpler and saves the PMIC on pin count.

The R/G/B LED drivers are 3 identical current regulators (Figure 13). The 3 external LEDs connect their anodes to VBAT and their cathodes to 3 pins of the PMIC (LED_R/G/B). No ballast resistor is needed for these 3 LEDs; each current regulator is capable of setting its current to 12, 16, 20 or 24 mA via the control registers (Registers 3~5 [6:5]).

Figure 13: LED Driver Block Diagram



5.3.4 Control for Backlight Driver

The backlight (BL) driver control is responsible for controlling the external boost DC/DC converter, which is required to drive up to 6 white LEDS (2 legs, 3 in series). BLDRV connects to the gate of the external MOSFET; CS_BL senses the current flow through the MOSFET, and FB_BL feeds the voltage drop on ballast resistor back to the PMIC for LED light intensity control. DC_OV helps prevent the over-voltage of the output.

5.3.5 Dimming Control

Brightness can be controlled by programming the MT6318's internal registers to change the driver's output pulse duty cycle and frequency.

5.3.5.1 Pulse Duty Cycle

For all drivers, the output duty cycle is adjusted by selecting the corresponding driver's PWM_D value according to the following relationship:

(R/G/B/KP) PWM duty cycle = (PWM_D + 1) low's , and 32 - (PWM_D +1) high's;

where PWM_D ranges from 0 to 31.

5.3.5.2 Frequency

For R/G/B and KP, the output frequency is changed by adjusting Register 9 [3:0] DIV value. All 4 LED drivers share the same DIV setting. The output frequency is governed by:

(R,G,B,KP) PWM frequency = 800k / 25 / (DIV+1) / 32;

where DIV ranges from 0 to15.

For BL, the output frequency is changed by adjusting BL_DIV (Register 9 [7:4]) and also Bypass (Register 7 [5]). The output frequency is governed by:

When bypass = 0,
(BL) PWM frequency = 800k / 25 / (BL_DIV+1) / 32

When bypass = 1,
(BL) PWM frequency = 800k / (BL_DIV+1) / 32

where BL_DIV ranges from 0 to 15.

5.3.6 Battery Voltage Monitor

PMIC outputs both VBAT and ISENSE voltage to VB_OUT and ISENSE_OUT pins. In addition, the divide-by-two option is supported. This function facilitates monitoring of the VBAT and ISENSE voltages by the BB, to control the charging process.

5.3.7 Speaker Amplifier

The speaker amplifier in MT6318 can be configured as either differential input or single-ended input. The amplifier is controlled by Register 2 [1]. The input must be AC-coupled. Refer to Register 1 [6:4] for the gain setting.

5.3.8 SPI

PMIC uses a 3wire interface to connect to the BB. This bi-directional serial bus interface allows the BB to write commands to and read status from PMIC. The bus protocol employs a 16-bit proprietary format. The descriptions for the 3 signals are listed in Table 22.

Table 22: SPI Definition

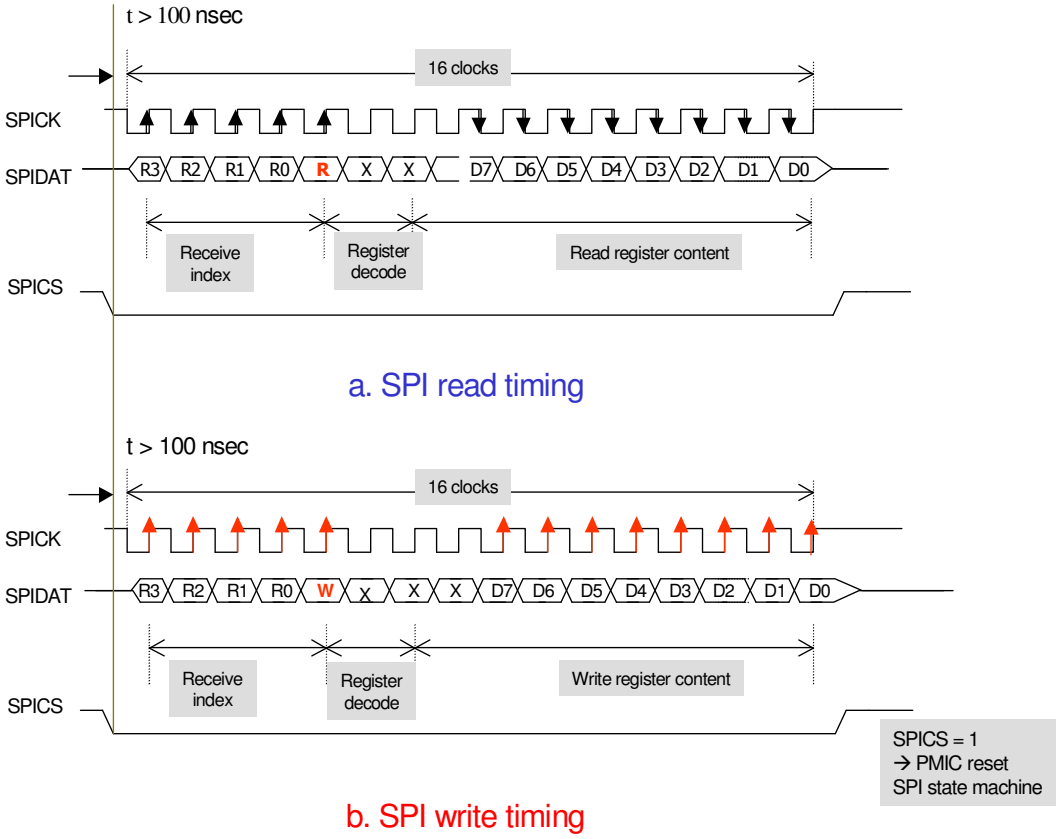
Signal Name	Attribute	Direction	Description
SPICK	Edge triggered	BB → PMIC	Serial bus clock
SPIDAT	Level	BB ↔ PMIC	Serial data
SPICS	Active low	BB → PMIC	PMIC SPI bus selection

When SPICS goes low, this bus is active. The BB transfers the 4 register index bits followed by a read/write bit, then waits 3 clock cycles for the PMIC SPI state machine to decode the operation for the succeeding 8 data bits.

The state machine counts for 16 clocks to complete the data transfer. If fewer than 16 clocks are received during the time that SPICS = 0 then only part of the data has been transferred. On the other hand, if more than 16 clocks are received, the extra data is ignored.

The first SPICK is started 100 ns after the SPICS is asserted low.

Figure 14: SPI Bus Timing



*Read = BB reading from PMIC, Write= BB writing to PMIC

5.4 Register Table and Descriptions

See the next page for the register table (Table 23).

Table 23: Register Control Table

Index	Name	D7	D6	D5	D4	D3	D2	D1	D0
0	Charger Status	OV_SPI	CHR_DET	BAT_ON	AC_DET	USB_DET	PWRKEY_DEB	CV	CHRG_DIS
		R	R	R	R	R	R	R	R
1	Charger / Speaker Control	CHR_EN	AMPGAIN_2	AMPGAIN_1	AMP_GAIN_0	USB_PWR	CLASS_D2	CLASS_D1	CLASS_D0
		RW	RW	RW	RW	RW	RW	RW	RW
		1	0	0	0	0	0	0	0
2	LDO Status	VD	VA	VM	VRTC	VTCXO	VSIM	AUDIO_SEL	DIM_CK_ON
		R	R	R	R	R	R	RW	RW
3	R LED Driver	ON	CURLIM1	CURLIM0	PWM_D4	PWM_D3	PWM_D2	PWM_D1	PWM_D0
		RW	RW	RW	RW	RW	RW	RW	RW
		0	0	0	0	0	0	0	0
4	G LED Driver	ON	CURLIM1	CURLIM0	PWM_D4	PWM_D3	PWM_D2	PWM_D1	PWM_D0
		RW	RW	RW	RW	RW	RW	RW	RW
		0	0	0	0	0	0	0	0
5	B LED Driver	ON	CURLIM1	CURLIM0	PWM_D4	PWM_D3	PWM_D2	PWM_D1	PWM_D0
		RW	RW	RW	RW	RW	RW	RW	RW
		0	0	0	0	0	0	0	0
6	KP LED Driver	ON	Reserved	Reserved	PWM_D4	PWM_D3	PWM_D2	PWM_D1	PWM_D0
		RW			RW	RW	RW	RW	RW
		0			0	0	0	0	0
7	BL LED Driver	ON	Reserved	BYPASS	PWM_D4	PWM_D3	PWM_D2	PWM_D1	PWM_D0
		RW		RW	RW	RW	RW	RW	RW
		0		0	0	0	0	0	0
8	Misc.	CHR_PUMP_EN	VA_SW	PWR_SAVE_SPI	VA_SEL	VMC	VSIMSEL	SPEAKER	VIBRATOR
		RW	RW	RW	RW	RW	RW	RW	RW
		0	0	0	0	0	0	0	0
9	Dim Clock	BL_DIV3	BL_DIV2	BL_DIV1	BL_DIV0	DIV_3	DIV_2	DIV_1	DIV_0
		RW	RW	RW	RW	RW	RW	RW	RW
		0	0	0	0	0	0	0	0
A	Charger Control 2	Reserved	Reserved	Reserved	Reserved	OV_SPI_CLR	CHOFST[2]	CHOFST[1]	CHOFST[0]
						W	RW	RW	RW
							0	1	1
B	Bandgap Setting	Reserved	Reserved	Reserved	Reserved	UV_SEL[1]	UV_SEL[0]	Reserved	Reserved
						RW	RW		
						0	0		
C	LDO_TEST1_EN	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
D	LDO_TEST2_EN	Reserved	Reserved	INT_DRV	RESET_DRV	Reserved	Reserved	Reserved	Reserved
				RW	RW				
				1	1				
E	Charge Pump Control	PUMPCLCTRL	PUMPDSEL_1	PUMPDSEL_0	PUMPSSEL_1	PUMPSSEL_0	Reserved	VIBSEL	USB_CHR_EN
		RW	RW	RW	RW	RW		RW	RW
		0	1	1	0	0		0	0
F	Extras	VA_SW_SEL	VBSSEL_SPI[1]	VBSSEL_SPI[0]	VBHSEL	VMCSEL	Reserved	PUMPDELAY[1]	PUMPDELAY[0]
		RW	RW	RW	RW	RW		RW	RW
		0	0	0	0	0		1	1

Table 24: Register Index 0: Charger Status Register

Register Index 0: Charger Status (Read Only)			
Bit	**Name**	**Value**	**Description**
D7	OV_SPI	0	Charger OV has not occurred (AC < 9V)
		1	Charger OV has occurred (AC > 9V)
D6	CHR_DET	0	Charger not detected
		1	Charger detected
D5	BAT_ON	0	Battery is connected
		1	Battery is not connected
D4	AC_DET	0	AC power not detected
		1	AC power detected
D3	USB_DET	0	USB power not detected
		1	USB power detected
D2	PWRKEY_DEB	0	Debounced power key is asserted.
		1	Debounced power key is not asserted.
D1	CV	0	Not in CV mode.
		1	In CV mode.
D0	CHRG_DIS	0	Charging.
		1	Not charging.

Note: If CV = 0 and CHARG_DIS=0, then this the charger is in CC mode.

Table 25: Register Index 1: Charger/Speaker Amplifier Control

Register Index 1: Charger/Speaker Control			
Bit	**Name**	**Value**	**Description**
D7	CHR_EN	0	Pause charging
		1	Enable charging (Default)
D6~D4	AMPGAIN[2:0]	0~7	Speaker amplifier gain setting 0~21 dB (Default = 000)
D3	USB_PWR	0	Turn off USB regulator (Default)
		1	Turn on USB regulator
D2~D0	CLASS_D(2:0)	0	Charge current clamp to 50 mA
		1	Charge current clamp to 90 mA
		2	Charge current clamp to 150 mA
		3	Charge current clamp to 225 mA
		4	Charge current clamp to 300 mA
		5	Charge current clamp to 450 mA
		6	Charge current clamp to 650 mA
		7	Charge current clamp to 800 mA

Table 26: Register Index 2: LDO Status

Register Index 2: LDO Status (Read Only)			
Bit	**Name**	**Value**	**Description**
D7	VD	0	Digital LDO off
		1	Digital LDO on
D6	VA	0	Analog LDO off
		1	Analog LDO on
D5	VM	0	Memory LDO off
		1	Memory LDO on
D4	VRTC	0	RTC LDO off
		1	RTC LDO on
D3	VTCXO	0	13/26 MHZ VTCXO LDO off
		1	13/26 MHZ VTCXO LDO on
D2	VSIM	0	SIM LDO off
		1	SIM LDO on
D1	AUDIO_SEL	0	Fully-differential speaker amplifier input
		1	Single-ended speaker amplifier input
D0	DIM_CK_ON	0	Dimming clock off
		1	Dimming clock on. Set the register to 1 when DC-DC (BL LED) or Charge-pump or KPLED or RGB driver is enabled.

Table 27: Register Index 3: R LED Driver

Register Index 3: R LED Driver			
Bit	**Name**	**Value**	**Description**
D7	ON	0	Power down (Default)
		1	Power on
D6~D5	CURLIM(1:0)	0	Current limit = 12 mA (Default)
		1	Current limit = 16 mA
		2	Current limit = 20 mA
		3	Current limit = 24 mA
D4~D0	PWM_D(4:0)	0~31	Duty cycle = (PWM_D(4:0)+1)/32 (Default = 0)

Table 28: Register Index 4: G LED Driver

Register Index 4: G LED Driver			
Bit	**Name**	**Value**	**Description**
D7	ON	0	Power down (Default)
		1	Power on
D6~D5	CURLIM(1:0)	0	Current limit = 12 mA (Default)
		1	Current limit = 16 mA
		2	Current limit = 20 mA
		3	Current limit = 24 mA
D4~D0	PWM_D(4:0)	0~31	Duty cycle = (PWM_D(4:0)+1)/32 (Default = 0)

Table 29: Register Index 5: B LED Driver

Register Index 5: B LED Driver			
Bit	**Name**	**Value**	**Description**
D7	ON	0	Power down (Default)
		1	Power on
D6~D5	CURLIM(1:0)	0	Current limit = 12 mA (Default)
		1	Current limit = 16 mA
		2	Current limit = 20 mA
		3	Current limit = 24 mA
D4~D0	PWM_D(4:0)	0~31	Duty cycle = (PWM_D(4:0)+1)/32 (Default = 0)

Table 30: Register Index 6: KP LED Driver

Register Index 6: KP LED Driver			
Bit	**Name**	**Value**	**Description**
D7	ON	0	Power down (Default)
		1	Power on
D6	Reserved		
D5	Reserved		
D4~D0	PWM_D(4:0)	0~31	Duty cycle = (PWM_D(4:0)+1)/32 (Default = 0)

Table 31: Register Index 7: BL LED Driver

Register Index 7: BL LED Driver			
Bit	**Name**	**Value**	**Description**
D7	ON	0	Power down (Default)
		1	Power on
D6	Reserved		
D5	BYPASS	0	No bypass (Default)
		1	Bypass divide-by-25 counter.
D4~D0	PWM_D(4:0)	0~31	Duty cycle = (PWM_D(4:0)+1)/32 (Default = 0)

Note: When bypass = 0, PWM frequency = DC-DC switching frequency / 25 / (BL_DIV+1) / 32, div = 0~15.
When bypass = 1, PWM frequency = DC-DC switching frequency / (BL_DIV+1) / 32, div = 0~15.

Table 32: Register Index 8: Miscellaneous

Register Index 8: Miscellaneous Driver			
Bit	**Name**	**Value**	**Description**
D7	CHR_PUMP_EN	0	Power down (Default)
		1	Power on
D6	VA_SW	0	Auxiliary analog output switch off (Default)
		1	Auxiliary analog output switch on
D5	PWR_SAVE	0	VD = normal voltage output
		1	If 1.8 V is selected as Vcore voltage, then when PWR_SAVE = 1, and SRCLKEN = 0 (i.e. the BB enters sleep mode), the Vcore is switched to 1.5 V. If 1.2 V is selected as Vcore voltage, then when PWR_SAVE = 1, and SRCLKEN = 0 (i.e. the BB enters sleep mode), the Vcore is switched to 0.9 V
D4	VA_SEL	0	VA enable signal determination, same as VD (Default)
		1	VA enable signal determination, same as VTCXO
D3	VMC	0	VMC power off (Default)
		1	VMC power on
D2	VSIMSEL	0	VSIM = 1.8 V (Default)
		1	VSIM = 3.0 V
D1	SPEAKER	0	Audio amplifier power off (Default)
		1	Audio amplifier power on
D0	VIBRATOR	0	Vibrator driver power off (Default)
		1	Vibrator driver power on

** When turned on, VB_OUT is actually same as VBAT. VB_OUT is floating when the phone is switched off in order to stop current leaks to the BB.

Table 33: Register Index 9: DIM Clock

Register Index 9: DIM Clock			
Bit	**Name**	**Value**	**Description**
D7~D4	BL_DIV	15~0	Backlight frequency division control (Default = 0)
D3~D0	DIV	15~0	R,G,B,KP frequency division control (Default = 0)

Table 34: Register Index A: Charger Control_2

Register Index A: Charger Control 2			
Bit	**Name**	**Value**	**Description**
D7~D4	Reserved		
D3	OV_SPI_CLR (W only)	0	When written with 0, clears OV condition.
		1	No effect.
D2~D0	CHOFST[2:0]	7~0	Charging current offset. (Default is b'100 = 4)

Note: When OV_SPI_CLR is written with a 0, the ov_spi condition is cleared. Writing a 1 has no effect. If read, it returns the same value as Register 0 [7] (ov_spi).

Table 35: Register Index B: Bandgap Settings

Register Index B: Bangap Settings			
Bit	**Name**	**Value**	**Description**
D7~D4	Reserved		
D3~D2	UV_SEL[1:0]	3	Set UV falling threshold voltage to 2.50 V (Sync. with DDLO)
		2	Set UV falling threshold voltage to 2.60 V
		1	Set UV falling threshold voltage to 2.75 V
		0	Set UV falling threshold voltage to 2.90 V
D1	Reserved		
D0	Reserved		

Table 36: Register Index C: LDO Test 1 EN

Register Index C: LDO TEST1 EN			
Bit	**Name**	**Value**	**Description**
D7~D0	Reserved		

Note: For LDO_TEST1 and LDO_TEST2, the pin combination must be: (TEST_MODE = 1) AND (SIMVCC = 1).

Table 37: Register Index D: LDO Test 2 EN

Register Index D: LDO TEST2 EN			
Bit	**Name**	**Value**	**Description**
D7	Reserved		
D6	Reserved		
D5	INT_DRV	0	Set Interrupt pad driving strength (Default = 1)
		1	
D4	RESET_DRV	0	Set Reset pad driving strength (Default = 1)
		1	
D3~D0	Reserved		

Note: For LDO_TEST1 and LDO_TEST2, the pin combination must be: (TEST_MODE = 1) AND (SIMVCC = 1).

Table 38: Register Index E: Charge Pump

Register Index E: Charge Pump Control			
Bit	**Name**	**Value**	**Description**
D7	PUMPCLCTRL	0	Charge pump control signal (Default = 0)
		1	
D6~D5	PUMPDSEL[1:0]	3~0	Charge pump control signal (Default = b'11 = 3)
D4~D3	PUMPSSEL[1:0]	3~0	Charge pump control signal (Default = 0)
D2	Reserved		
D1	VIBSEL	0	VIBR = 1.8 V (Default)
		1	VIBR = 3.2 V
D0	USB_CHR_EN	0	Disable USB charging. For OTG. (Default)
		1	Enable USB charging

Table 39: Register Index F: Extras

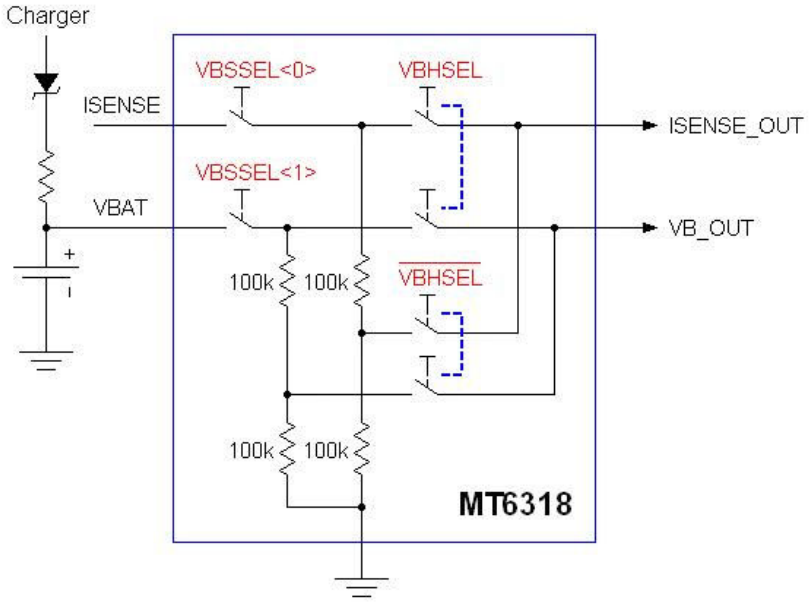
Register Index F: Extras			
Bit	**Name**	**Value**	**Description**
D7	VA_SW_SEL	0	VA_SW = 2.8 V (Default)
		1	VA_SW = 3.3 V
D6	VBSSEL_SPI[1]	0	VB_OUT disable (Default) (see Note)
		1	VB_OUT enable
D5	VBSSEL_SPI[0]	0	ISENSE_OUT disable (Default) (see Note)
		1	ISENSE_OUT enable
D4	VBHSEL	0	VB_OUT = 0.5*VBAT; ISENSE_OUT = 0.5*ISENSE_OUT (see Note)
		1	VB_OUT = VBAT; ISENSE_OUT = ISENSE_OUT
D3	VMCSEL	0	VMC=2.8 V (Default)
		1	VMC=3.0 V
D2	Reserved		
D1~D0	PUMPDELAY[1:0]	3	Charge pump softstart time delay = 600 µs (Default = 3)
		2	Charge pump softstart time delay = 500 µs
		1	Charge pump softstart time delay = 400 µs
		0	Charge pump softstart time delay = 200 µs

Note: Charge pump delay is controlled as follows:

- When CHR_PUMP_EN = 1, after PUMPDELAY (200, 400, 500, or 600 µs), the PUMPDSEL changes from the default value (b'11) to the new PUMPDSEL value.
- When CHR_PUMP_EN = 0, or a reset is asserted, PUMPDSEL reverts back to the default value b'11.

VBSSEL_SPI<1:0> function blocks:

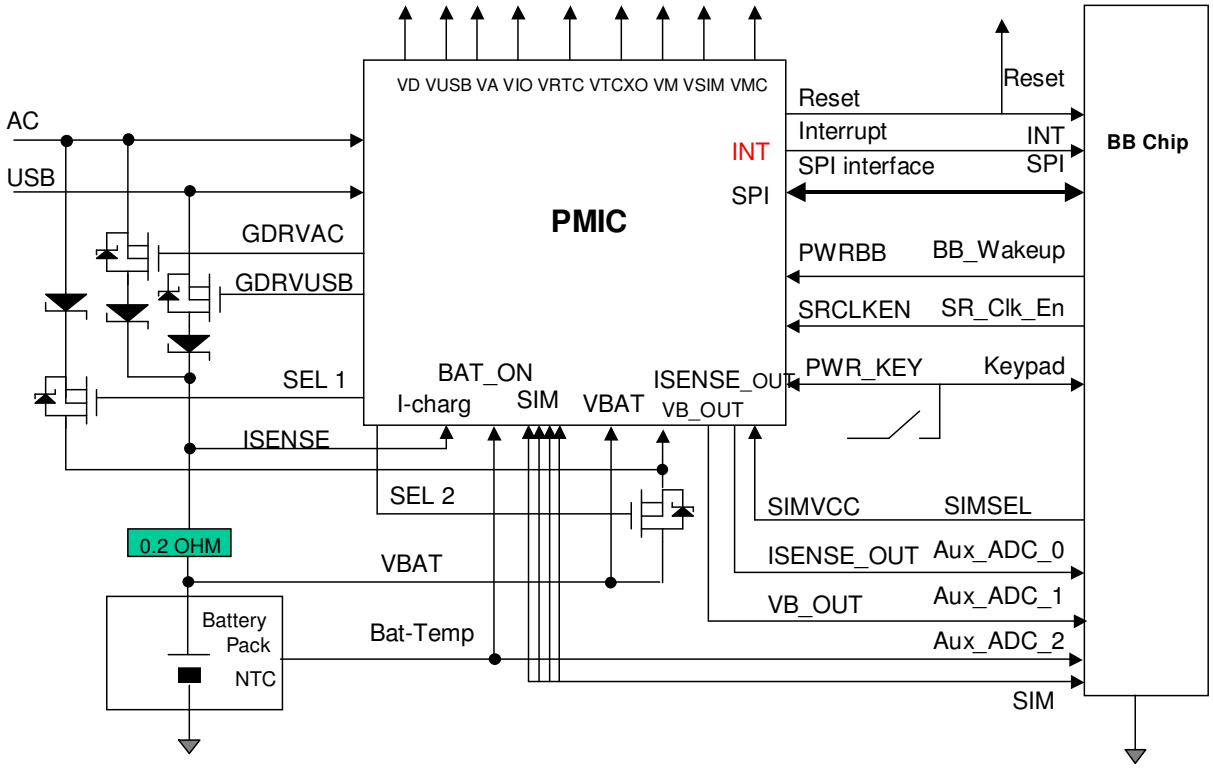
Figure 15: ISENSE_OUT and VB_OUT Block



5.5 Connection to the Baseband

The following schematic illustrates a typical application for this PMIC to connect with an MT621X BB. Refer to the application paragraph (Section 6.2) for other possible connections.

Figure 16: Connection to the BB



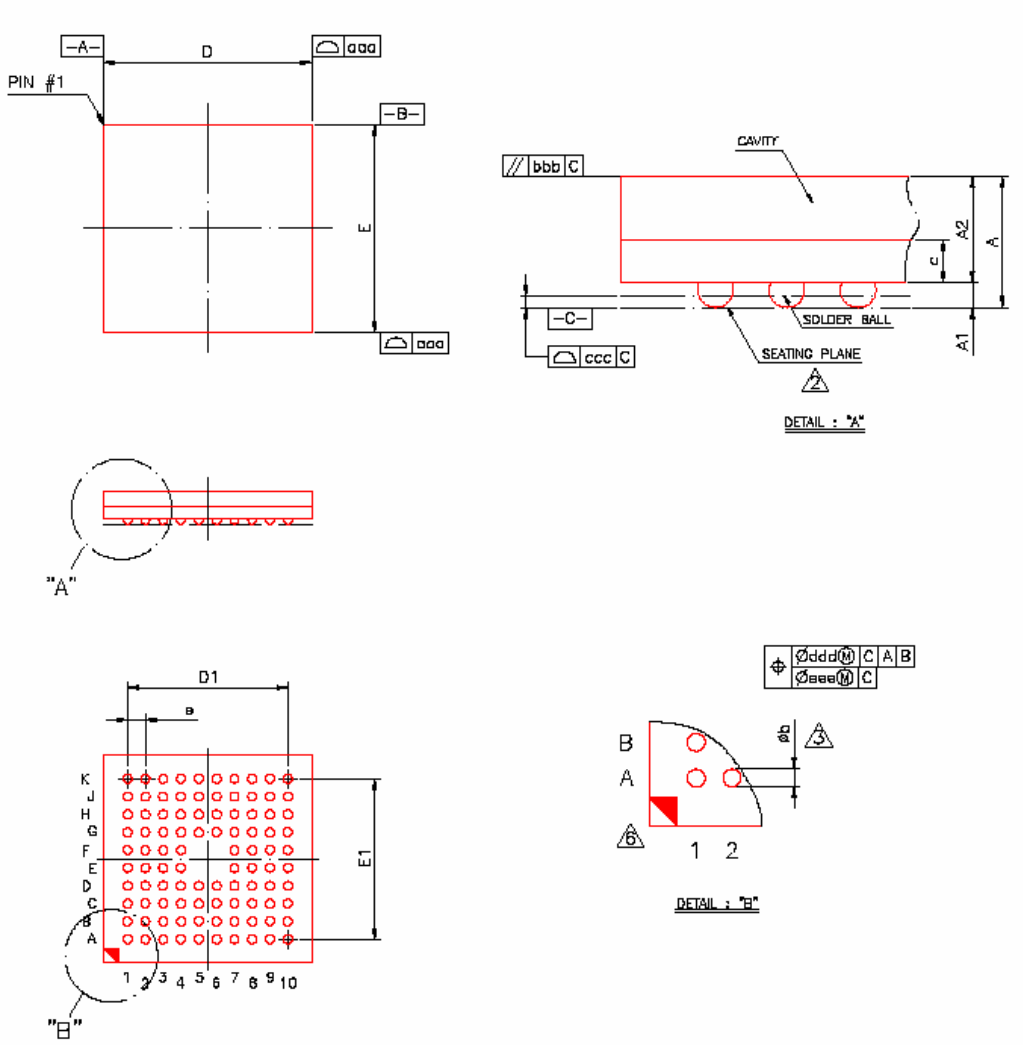
6 MT6318 Packaging

6.1 Package Dimensions

Based on the current pin count and board layout concern, TFBGA is the preferred package for this PMIC.

See the next page for the MT6318 package dimensions (Figure 17).

Figure 17: MT6318 Package Dimensions



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.20	---	---	0.047
A1	0.16	0.21	0.26	0.006	0.008	0.010
A2	0.84	0.89	0.94	0.033	0.035	0.037
c	0.32	0.36	0.40	0.013	0.014	0.016
D	6.90	7.00	7.10	0.272	0.276	0.280
E	6.90	7.00	7.10	0.272	0.276	0.280
D1	---	5.40	---	---	0.213	---
E1	---	5.40	---	---	0.213	---
e	---	0.60	---	---	0.024	---
b	0.25	0.30	0.35	0.010	0.012	0.014
aaa	0.15			0.006		
bbb	0.20			0.008		
ccc	0.10			0.004		
ddd	0.15			0.006		
eee	0.08			0.003		
MD/ME	10/10			10/10		

NOTE :

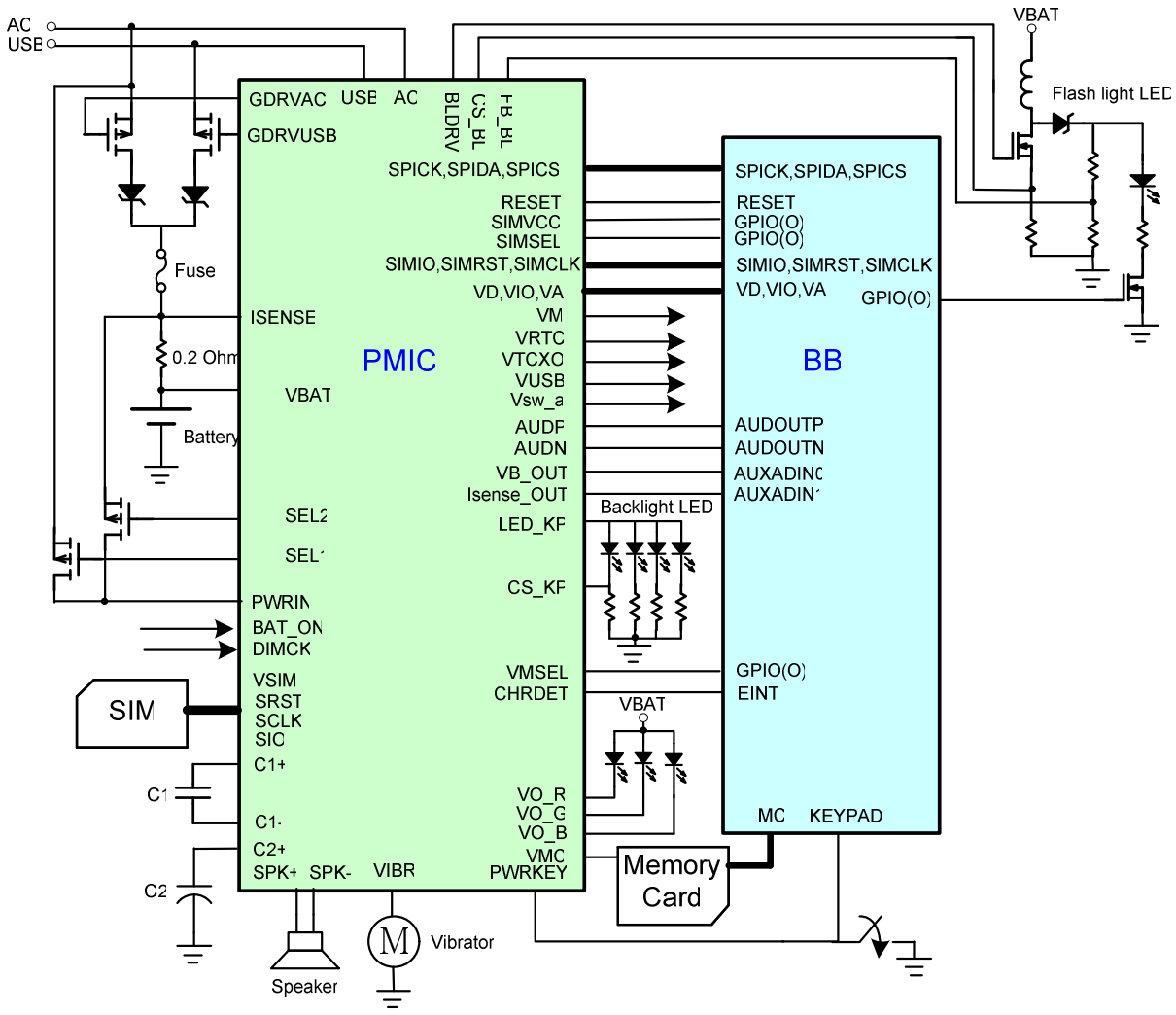
1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
5. REFERANCE DOCUMENT : JEDEC MO-207
6. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.

6.2 Application Examples

A typical application example is shown in Figure 18. Main features are listed as below:

1. Charging using USB or AC-DC adaptor.
2. Shows charging status during pre-charging if charging with adaptor power.
3. Supports power for the memory card.
4. Supports Class AB audio amplifier for a loud speaker.
5. Supports up to 4 white LEDs for the main LCD backlight.
6. Supports up to 300 mA for flash LEDs.
7. Supports 3 independent LED drivers (any color).
8. Supports dim control for all LED drivers.
9. Battery removal protection.

Figure 18: Application Example



Appendix

BAT_ON Functional Circuit Example (with BAT Temperature Sensor)

Figure 19: BAT_ON Connection with Battery Temperature Sensor Example

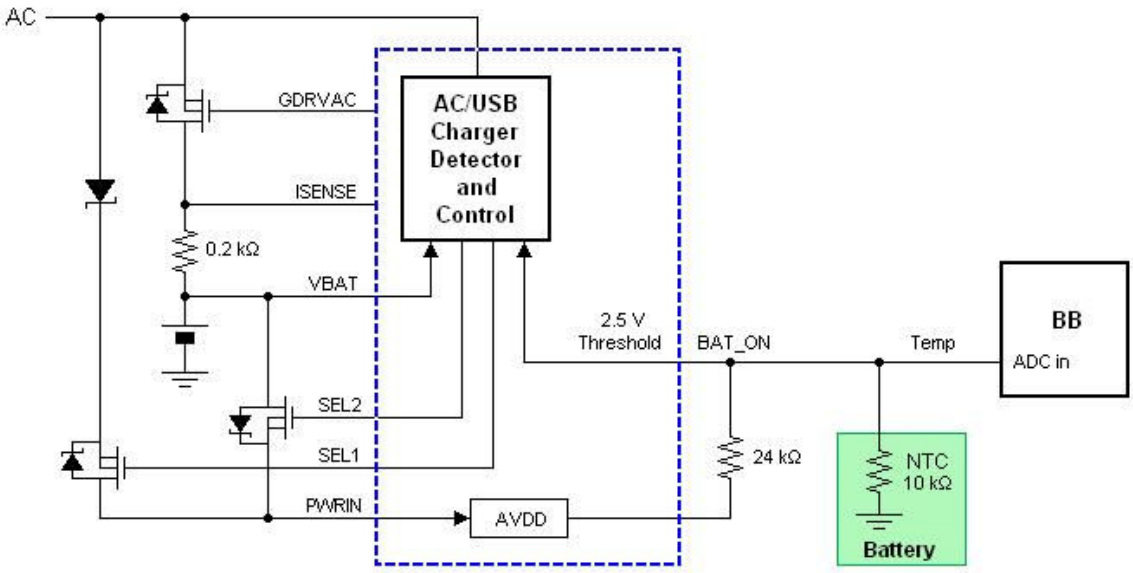
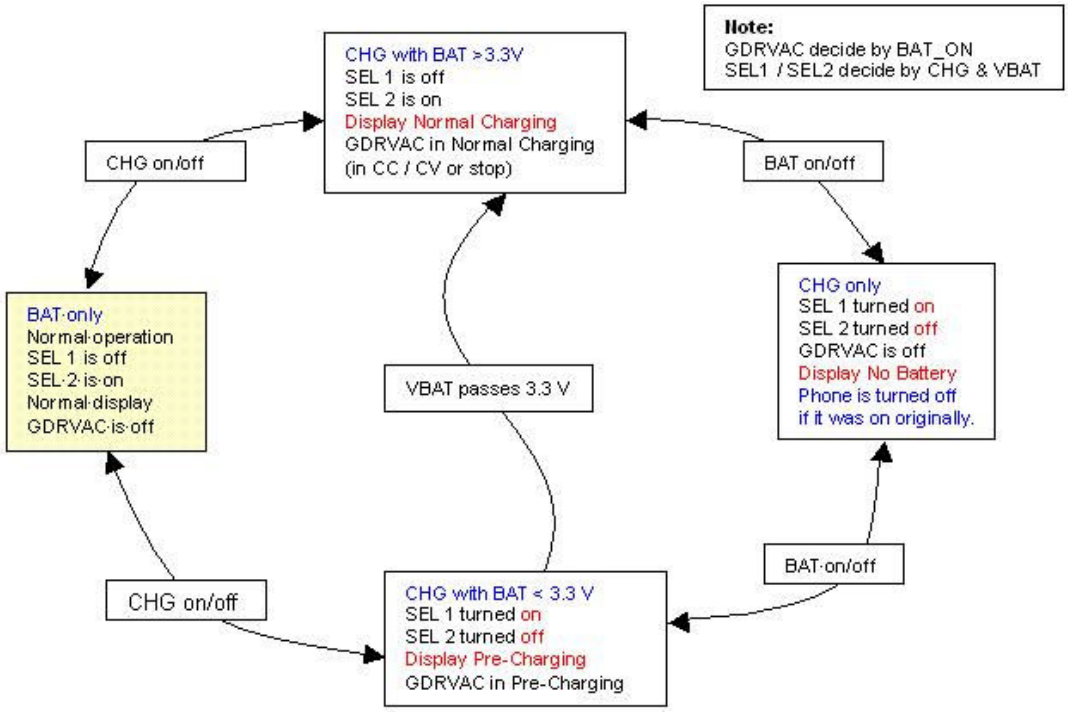


Figure 20: CHG/BAT State Diagram



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