RTL8101L

RTL8101L-LF

RTL8101L-GR

SINGLE-CHIP FAST ETHERNET CONTROLLER AND MC'97 CONTROLLER WITH POWER MANAGEMENT

DATASHEET

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USING THIS DOCUMENT

This document provides detailed user guidelines to achieve the best performance when implementing a 2-layer board PC design with the RTL8101L Single-Chip Fast Ethernet Controller and MC'97 Controller with Power Management control.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
1.5	2006/04/20	First official release.

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1. General Description

The Realtek RTL8101L is a highly integrated and cost-effective single-chip Fast Ethernet controller that provides 32-bit performance, PCI bus master capability, and full compliance with IEEE 802.3u 100Base-TX specifications and IEEE 802.3x Full Duplex Flow Control. It also supports the Advanced Configuration Power management Interface (ACPI), PCI power management for modern operating systems that are capable of Operating System Directed Power Management (OSPM) to achieve the most efficient power management possible. The RTL8101L no longer supports CardBus mode (the RTL8139C does).

In addition to the ACPI feature, the RTL8101L supports remote wake-up (including AMD Magic Packet, LinkChg, and Microsoft® wake-up frame) in both ACPI and APM environments. The RTL8101L is capable of performing an internal reset through the application of auxiliary power. When auxiliary power is applied and the main power remains off, the RTL8101L is ready and waiting for a Magic Packet or Link Change to wake the system up. Also, the LWAKE pin provides 4 different output signals including active high, active low, positive pulse, and negative pulse. The versatility of the RTL8101L LWAKE pin provides motherboards with Wake-On-LAN (WOL) functionality.

The RTL8101L also supports Analog Auto-Power-down, that is, the analog part of the RTL8101L can be shut down temporarily according to user requirements or when the RTL8101L is in a power down state with the wakeup function disabled. In addition, when the analog part is shut down and the IsolateB pin is low (i.e. the main power is off), then both the analog and digital parts stop functioning and the power consumption of the RTL8101L is negligible. The RTL8101L also supports an auxiliary power auto-detect function, and will auto-configure related bits of their own PCI power management registers in PCI configuration space.

PCI Vital Product Data (VPD) is also supported to provide the information that uniquely identifies hardware (i.e., the OEM brand name of the RTL8101L LAN card). The information may consist of part number, serial number, and other detailed information.

To provide cost down support, the RTL8101L is capable of using a 25MHz crystal or OSC as its internal clock source.

The RTL8101L keeps network maintenance costs low and eliminates usage barriers. It is the easiest way to upgrade a network from 10 to 100Mbps. It also supports full-duplex operation, making 200Mbps bandwidth possible at no additional cost. To improve compatibility with other brands' products, the RTL8101L is also capable of receiving packets with InterFrameGap no less than 40 Bit-Time. The RTL8101L is highly integrated and requires no 'glue' logic or external memory.

The RTL8101L includes a PCI and Expansion Memory Share Interface (Realtek patent) for a boot ROM and can be used in diskless workstations, providing maximum network security and ease of management.

2. Features

2.1. Ethernet Controller Features

- 100 pin LQFP
- Integrated Fast Ethernet MAC, Physical chip, and transceiver in one chip
- 10Mbps and 100Mbps operation
- Supports 10Mbps and 100Mbps N-way Auto-negotiation
- PCI local bus single-chip Fast Ethernet controller
- Complies with PCI Revision 2.2
- Supports PCI clock 16.75MHz-40MHz
- Supports PCI target fast back-to-back transaction
- Provides PCI bus master data transfers and PCI memory space or I/O space mapped data transfers of RTL8101L's operational registers
- Supports PCI VPD (Vital Product Data)
- Supports ACPI, PCI power management
- Supports 25MHz crystal or 25MHz OSC as the internal clock source. The frequency deviation of either crystal or OSC must be within 50 PPM.
- Complies with to PC99/PC2001 standard
- Supports Wake-On-LAN function and remote wake-up (Magic Packet, LinkChg and Microsoft® wake-up frame)
- Supports 4 Wake-On-LAN (WOL) signals (active high, active low, positive pulse, and negative pulse)
- Supports auxiliary power-on internal reset, for remote wake-up when main power remains off
- Supports auxiliary power auto-detect, and sets the related capability of power management registers in PCI configuration space
- Includes a programmable PCI burst size and early Tx/Rx threshold
- Supports a 32-bit general-purpose timer with the external PCI clock as clock source to generate a timer-interrupt
- Contains two large (2Kbyte) independent receive and transmit FIFOs
- Advanced power saving mode when LAN function or wakeup function is not used
- Uses 93C46 (64*16-bit EEPROM) to store resource configuration, ID parameter, and VPD data
- Supports LED pins for various network activity indications
- Supports loopback capability
- Half/Full duplex capability
- Supports Full Duplex Flow Control (IEEE 802.3x)
- 3.3V power supply, 3.3V and 5V I/O tolerance
- Interface for 128K byte (max) Boot ROM for both EEPROM and Flash Memory

2.2. MC'97 Controller Features

- MC'97 compatible digital controller chip
- PCI local bus single-chip Fast Ethernet controller
- 32-bit PCI bus master and PCI v 2.2 compliant
- PCI Bus Power Management Interface Specification v 1.1 compliant
- High performance bus master DMA for data transfer
- AC'97 v 2.2 compliant
- Supports 16-bit modem line (LINE1)
- Full-duplex operation for simultaneous LINE1 transactions
- Low latency GPIO updated
- 8 double-WORD (16 samples) FIFO depth for each bus master of LINE1-OUT/IN
- 3.3V power supply, 3.3V and 5V I/O tolerance

3. System Applications

- Ethernet Network Interface Controller
- Lan On Motherboard
- Embedded System

4. Block Diagram

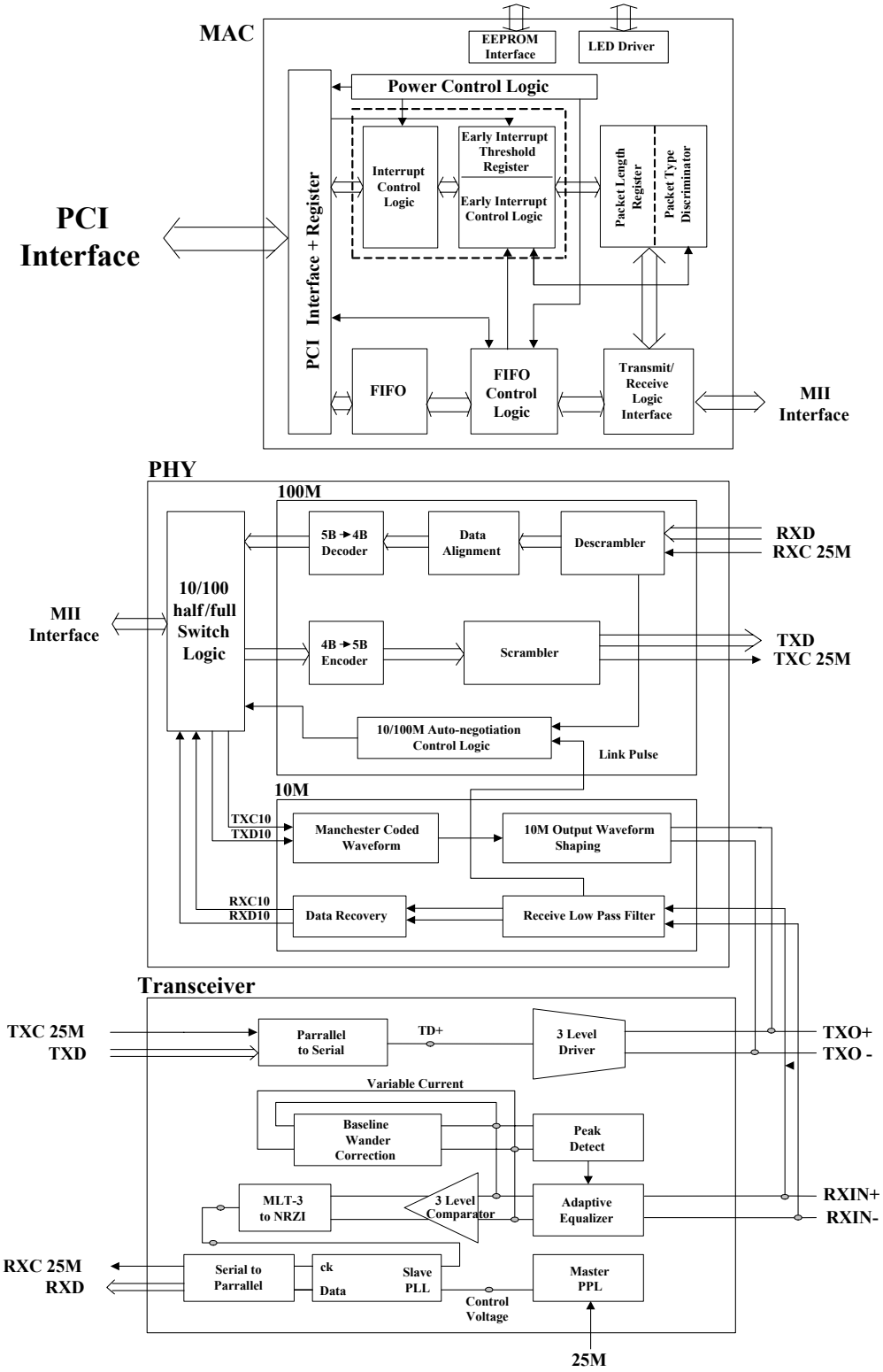


Figure 1. Block Diagram

5. Pin Assignments

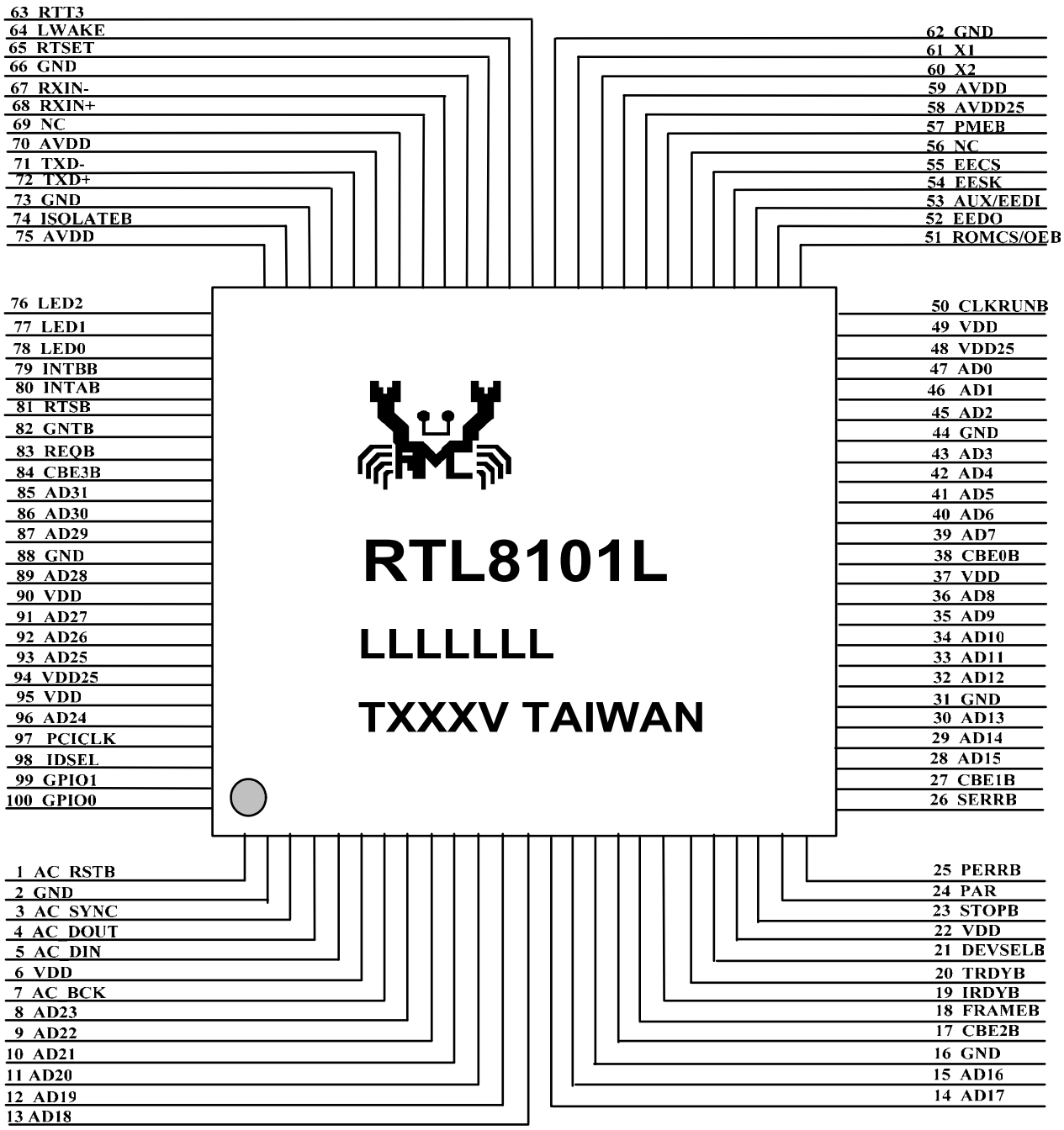


Figure 2. Pin Assignments

5.1. Package Identification

Green package is indicated by a 'G' in the location marked 'T' in Figure 2. Lead (Pb)-Free package is indicated by an 'L'. The version is indicated by the letter shown in the location marked 'V'.

6. Pin Descriptions

The following signal type codes are used in the tables:

I: Input.

O: Output.

T/S: Tri-State bi-directional input/output pin.

S/T/S: Sustained Tri-State.

O/D: Open Drain.

Note that some pins have multiple functions. See Figure 2, on page 5, for a graphical representation.

6.1. Power Management/Isolation Interface

Table 1. Power Management/Isolation Interface

Symbol	Type	Pin No	Description
PMEB (PME#)	O/D	57	Power Management Event. Open drain, active low. Used by the RTL8101L to request a change in its current power management state and/or to indicate that a power management event has occurred.
ISOLATEB (ISOLATE#)	I	74	Isolate Pin: Active low. Isolates the RTL8101L from the PCI bus. The RTL8101L does not drive its PCI outputs (excluding PME#) and does not sample its PCI input (including RST# and PCICLK) as long as the Isolate pin is asserted.
LWAKE	O	64	LAN WAKE-UP Signal. Signals to the motherboard that it should execute the wake-up process. The motherboard must support Wake-On-LAN (WOL). There are 4 output choices, active high, active low, positive pulse, and negative pulse, that may be asserted from the LWAKE pin. See the LWACT bit in Table 20. CONFIG 1: Configuration Register 1, page 27, for the setting of this output signal. The default output is an active high signal. When a PME event is received, LWAKE and PMEB assert at the same time if LWPME (bit4, CONFIG4) is set to 0. If LWPME is set to 1, LWAKE asserts only when PMEB asserts and ISOLATEB is low. This pin is a 3.3V signaling output pin.

6.2. PCI Interface

Table 2. PCI Interface

Symbol	Type	Pin No	Description
AD31-0	T/S	85-87, 89, 91-93, 96, 8-15, 28-30, 32-36, 39-43, 45-47	PCI address and data multiplexed pins. AD31-24 are shared with BootROM data pins, while AD16-0 are shared with BootROM address pins.
C/BE3-0	T/S	84, 17, 27, 38	PCI bus command and byte enables multiplexed pins.
CLK	I	97	Clock: This PCI Bus clock provides timing for all transactions and bus phases, and is input to PCI devices. The rising edge defines the start of each phase. The clock frequency ranges from 0 to 33MHz.
DEVSELB	S/T/S	21	Device select: As a bus master, the RTL8101L samples this signal to insure that a PCI target recognizes the destination address for the data transfer. As a target, the RTL8101L asserts this signal low when it recognizes its target address after FRAMEB is asserted.
FRAMEB	S/T/S	18	Cycle frame: As a bus master, this pin indicates the beginning and duration of an access. FRAMEB is asserted low to indicate the start of a bus transaction. While FRAMEB is asserted, data transfer continues. When FRAMEB is deasserted, the transaction is in the final data phase. As a target, the device monitors this signal before decoding the address to check if the current transaction is addressed to it.
GNTB	I	82	Grant: This signal is asserted low to indicate to the RTL8101L that the central arbiter has granted ownership of the bus to the RTL8101L. This input is used when the RTL8101L is acting as a bus master.
REQB	T/S	83	Request: The RTL8101L will assert this signal low to request the ownership of the bus from the central arbiter.
IDSEL	I	98	Initialization device select: This pin allows the RTL8101L to identify when configuration read/write transactions are intended for it.
INTAB	O/D	80	INTAB: Used to request an interrupt. It is asserted low when an interrupt condition occurs, as defined by the Interrupt Status, Interrupt Mask and Interrupt Enable registers.
IRDYB	S/T/S	19	Initiator ready: This indicates the initiating agent's ability to complete the current data phase of the transaction. As a bus master, this signal will be asserted low when the RTL8101L is ready to complete the current data phase transaction. This signal is used in conjunction with the TRDYB signal. Data transaction takes place at the rising edge of CLK when both IRDYB and TRDYB are asserted low. As a target, this signal indicates that the master has put data on the bus.
TRDYB	S/T/S	20	Target ready: This indicates the target agent's ability to complete the current phase of the transaction. As a bus master, this signal indicates that the target is ready for the data during write operations and with the data during read operations. As a target, this signal will be asserted low when the (slave) device is ready to complete the current data phase transaction. This signal is used in conjunction with the IRDYB signal. Data transaction takes place at the rising edge of CLK when both IRDYB and TRDYB are asserted low.

Symbol	Type	Pin No	Description
PAR	T/S	24	Parity: This signal indicates even parity across AD31-0 and C/BE3-0 including the PAR pin. As a master, PAR is asserted during address and write data phases. As a target, PAR is asserted during read data phases.
PERRB	S/T/S	25	Parity Error: When the RTL8101L is the bus master and a parity error is detected, the RTL8101L asserts both SERR bit in ISR and Configuration Space command bit 8 (SERRB enable). Next, it completes the current data burst transaction, then stops operation and resets itself. After the host clears the system error, the RTL8101L continues its operation. When the RTL8101L is the bus target and a parity error is detected, the RTL8101L asserts this PERRB pin low.
SERRB	O/D	26	System Error: If an address parity error is detected and Configuration Space Status register bit 15 (detected parity error) is enabled, RTL8101L asserts both SERRB pin low and bit 14 of Status register in Configuration Space.
STOPB	S/T/S	23	Stop: Indicates the current target is requesting the master to stop the current transaction.
RSTB	I	81	Reset: When RSTB is asserted low, the RTL8101L performs an internal system hardware reset. RSTB must be held for a minimum of 120 ns.

6.3. EEPROM Interface

Table 3. EEPROM Interface

Symbol	Type	Pin No	Description
AUX/EEDI	I/O	53	1. Aux. Power Detect: This pin is used to notify the RTL8101L of the existence of Aux. power during initial power-on or a PCI reset. This pin should be pulled high to the Aux. power via a resistor to detect the Aux. power. Doing so, will enable wakeup support from ACPI D3 cold or APM power-down. If this pin is not pulled high, the RTL8101L assumes that no Aux. power exists.
EESK	O	54	The MA2-0 pins are switched to EESK, EEDI, EEDO in 93C46 programming or auto-load mode.
EEDO	O, I	52	The MA2-0 pins are switched to EESK, EEDI, EEDO in 93C46 programming or auto-load mode.
EECS	O	55	EEPROM chip select.

6.4. Power Pins

Table 4. Power Pins

Symbol	Type	Pin No	Description
VDD	P	6, 22, 37, 49, 90, 95	+3.3V (Digital)
AVDD	P	59, 70, 75	+3.3V (Analog)
VDD25	P	48, 94	+2.5V (Digital)
AVDD25	P	58	+2.5V (Analog)
DGND	P	2, 16, 31, 44, 88	Digital Ground
AGND	p	62, 66, 73	Analog Ground

6.5. LED Interface

Table 5. LED Interface

Symbol	Type	Pin No	Description					
LED0, 1, 2	O	78, 77, 76	LED Pins					
				LEDS1-0	**00**	**01**	**10**	**11**
				LED0	TX/RX	TX/RX	TX	TX
				LED1	LINK100	LINK10/100	LINK10/100	LINK100
				LED2	LINK10	FULL	RX	LINK10
			During power down mode, the LEDs are OFF. If LED1 is pulled low by a 10K resistor, the RT8101L runs in modem-only mode and a 93C46 is not necessary.					

6.6. Attachment Unit Interface

Table 6. Attachment Unit Interface

Symbol	Type	Pin No	Description
TXD+ TXD-	O O	72 71	10/100Base-T Transmit (TX) data.
RXIN+ RXIN-	I I	68 67	10/100Base-T Receive (RX) data.
X1	I	61	25MHz Crystal/OSC Input.
X2	O	60	Crystal Feedback Output. This output is used in a crystal connection only. It must be left open when X1 is driven with an external 25MHz oscillator.

6.7. AC-Link Pins

Table 7. AC-Link Pins

Symbol	Type	Pin No	Description
AC_RSTB	O	1	MC'97 Reset: Hardware reset to Codec.
AC_SYNC	O	3	MC'97 SYNC: 48Khz fixed rate sample sync to Codec.
AC_DOUT	O	4	MC'97 Serial Data Out: Serial data output to Codec.
AC_DIN	I	5	MC'97 Serial Data In: Serial data input from Codec.
AC_BCK	I	7	MC'97 Bit Clock: 12.288Mhz serial data clock generated by Codec.
INTBB	O/D	79	INTBB is used for function 1 device (Modem) to request an interrupt.
GPIO0	I/O	100	General Purpose I/O pins: Both can be programmed as input or output by bit0-1 of PCI GPIO Setup Register.
GPIO1	I/O	99	

6.8. Test and Other Pins

Table 8. Test and Other Pins

Symbol	Type	Pin No	Description
RTT3	TEST	63	Chip test pin.
RTSET	I/O	65	This pin must be pulled low by a resistor.
CLKRUNB	I/O	50	Clock run: This signal is used by the RTL8101L to request starting (or speeding up) the clock, CLK. CLKRUNB also indicates the clock status. For the RTL8101L, CLKRUNB is an open drain output as well as an input. The RTL8101L requests the central resource to start, speed up, or maintain the interface clock by the assertion of CLKRUNB. For the host system, it is an S/T/S signal. The host system (central resource) is responsible for maintaining CLKRUNB asserted, and for driving it high to the negated (deasserted) state.
ROMCS/OEB	O	51	ROM Chip select and Output Enable: This is the chip select signal and output enable of the Boot PROM.
NC	-	56, 69	Reserved.

7. Ethernet Controller Register Descriptions

The RTL8101L provides the following set of operational registers mapped into PCI memory space or I/O space.

Table 9. Register Descriptions

Offset	R/W	Tag	Description
0000h	R/W	IDR0	ID Register 0. ID registers 0-5 are only permitted to read/write via 4-byte access. Read access can be byte, word, or double word access. The initial value is auto-loaded from the EEPROM EthernetID field.
0001h	R/W	IDR1	ID Register 1.
0002h	R/W	IDR2	ID Register 2.
0003h	R/W	IDR3	ID Register 3.
0004h	R/W	IDR4	ID Register 4.
0005h	R/W	IDR5	ID Register 5.
0006h-0007h	-	-	Reserved.
0008h	R/W	MAR0	Multicast Address Register 0. The MAR register 0-7 are only permitted to read/write via 4-byte access. Read access can be byte, word, or double-word access. The driver is responsible for initializing these registers.
0009h	R/W	MAR1	Multicast Address Register 1.
000Ah	R/W	MAR2	Multicast Address Register 2.
000Bh	R/W	MAR3	Multicast Address Register 3.
000Ch	R/W	MAR4	Multicast Address Register 4.
000Dh	R/W	MAR5	Multicast Address Register 5.
000Eh	R/W	MAR6	Multicast Address Register 6.
000Fh	R/W	MAR7	Multicast Address Register 7.
0010h-0013h	R/W	TSD0	Transmit Status of Descriptor 0.
0014h-0017h	R/W	TSD1	Transmit Status of Descriptor 1.
0018h-001Bh	R/W	TSD2	Transmit Status of Descriptor 2.
001Ch-001Fh	R/W	TSD3	Transmit Status of Descriptor 3.
0020h-0023h	R/W	TSAD0	Transmit Start Address of Descriptor 0.
0024h-0027h	R/W	TSAD1	Transmit Start Address of Descriptor 1.
0028h-002Bh	R/W	TSAD2	Transmit Start Address of Descriptor 2.
002Ch-002Fh	R/W	TSAD3	Transmit Start Address of Descriptor 3.
0030h-0033h	R/W	RBSTART	Receive (Rx) Buffer Start Address.
0034h-0035h	R	ERBCR	Early Receive (Rx) Byte Count Register.
0036h	R	ERSR	Early Rx Status Register.
0037h	R/W	CR	Command Register.
0038h-0039h	R/W	CAPR	Current Address of Packet Read.
003Ah-003Bh	R	CBR	Current Buffer Address. The initial value is 0000h. It reflects total received byte-count in the Rx buffer.
003Ch-003Dh	R/W	IMR	Interrupt Mask Register.

Offset	R/W	Tag	Description
003Eh-003Fh	R/W	ISR	Interrupt Status Register.
0040h-0043h	R/W	TCR	Transmit (Tx) Configuration Register.
0044h-0047h	R/W	RCR	Receive (Rx) Configuration Register.
0048h-004Bh	R/W	TCTR	Timer CounT Register. This register contains a 32-bit general-purpose timer. Writing any value to this register will reset the original timer and start a count from zero.
004Ch-004Fh	R/W	MPC	Missed Packet Counter. Indicates the number of packets discarded due to Rx FIFO overflow. It is a 24-bit counter. After s/w reset, MPC is cleared. Only the lower 3 bytes are valid. When any value is written, MPC will be reset also.
0050h	R/W	9346CR	93C46 Command Register.
0051h	R/W	CONFIG0	Configuration Register 0.
0052h	R/W	CONFIG1	Configuration Register 1.
0053H	-	-	Reserved.
0054h-0057h	R /W	TimerInt	Timer Interrupt Register. Once having written a non-zero value to this register, the Timeout bit of the ISR register will be set whenever the TCTR reaches that value. The Timeout bit will never be set whilst the TimerInt register is zero.
0058h	R/W	MSR	Media Status Register.
0059h	R/W	CONFIG3	Configuration register 3.
005Ah	R/W	CONFIG4	Configuration register 4.
005Bh	-	-	Reserved.
005Ch-005Dh	R/W	MULINT	Multiple Interrupt Select.
005Eh	R	RERID	PCI Revision ID = 10h.
005Fh	-	-	Reserved.
0060h-0061h	R	TSAD	Transmit Status of All Descriptors.
0062h-0063h	R/W	BMCR	Basic Mode Control Register.
0064h-0065h	R	BMSR	Basic Mode Status Register.
0066h-0067h	R/W	ANAR	Auto-Negotiation Advertisement Register.
0068h-0069h	R	ANLPAR	Auto-Negotiation Link Partner Register.
006Ah-006Bh	R	ANER	Auto-Negotiation Expansion Register.
006Ch-006Dh	R	DIS	Disconnect Counter.
006Eh-006Fh	R	FCSC	False Carrier Sense Counter.
0070h-0071h	R/W	NWAYTR	N-way Test Register.
0072h-0073h	R	REC	RX_ER Counter.
0074h-0075h	R/W	CSCR	CS Configuration Register.
0076-0077h	-	-	Reserved.
0078h-007Bh	R/W	PHY1_PARM	PHY parameter 1.
007Ch-007Fh	R/W	TW_PARM	Twister parameter.
0080h	R/W	PHY2_PARM	PHY parameter 2.
0081-0083h	-	-	Reserved.
0084h	R/W	CRC0	Power Management CRC register0 for wakeup frame 0.

Offset	R/W	Tag	Description
0085h	R/W	CRC1	Power Management CRC register1 for wakeup frame 1.
0086h	R/W	CRC2	Power Management CRC register2 for wakeup frame 2.
0087h	R/W	CRC3	Power Management CRC register3 for wakeup frame 3.
0088h	R/W	CRC4	Power Management CRC register4 for wakeup frame 4.
0089h	R/W	CRC5	Power Management CRC register5 for wakeup frame 5.
008Ah	R/W	CRC6	Power Management CRC register6 for wakeup frame 6.
008Bh	R/W	CRC7	Power Management CRC register7 for wakeup frame 7.
008Ch–0093h	R/W	Wakeup0	Power Management wakeup frame0 (64bit).
0094h–009Bh	R/W	Wakeup1	Power Management wakeup frame1 (64bit).
009Ch–00A3h	R/W	Wakeup2	Power Management wakeup frame2 (64bit).
00A4h–00ABh	R/W	Wakeup3	Power Management wakeup frame3 (64bit).
00ACh–00B3h	R/W	Wakeup4	Power Management wakeup frame4 (64bit).
00B4h–00BBh	R/W	Wakeup5	Power Management wakeup frame5 (64bit).
00BCh–00C3h	R/W	Wakeup6	Power Management wakeup frame6 (64bit).
00C4h–00CBh	R/W	Wakeup7	Power Management wakeup frame7 (64bit).
00CCh	R/W	LSBCRC0	LSB of the mask byte of wakeup frame0 within offset 12 to 75.
00CDh	R/W	LSBCRC1	LSB of the mask byte of wakeup frame1 within offset 12 to 75.
00CEh	R/W	LSBCRC2	LSB of the mask byte of wakeup frame2 within offset 12 to 75.
00CFh	R/W	LSBCRC3	LSB of the mask byte of wakeup frame3 within offset 12 to 75.
00D0h	R/W	LSBCRC4	LSB of the mask byte of wakeup frame4 within offset 12 to 75.
00D1h	R/W	LSBCRC5	LSB of the mask byte of wakeup frame5 within offset 12 to 75.
00D2h	R/W	LSBCRC6	LSB of the mask byte of wakeup frame6 within offset 12 to 75.
00D3h	R/W	LSBCRC7	LSB of the mask byte of wakeup frame7 within offset 12 to 75.
00D4h-00D7h	-	-	Reserved.
00D8h	R/W	Config5	Configuration register 5.
00D9h-00FFh	-	-	Reserved.

7.1. Receive Status Register in RX Packet Header

Table 10. Receive Status Register in RX Packet Header

Bit	R/W	Symbol	Description
15	R	MAR	Multicast Address Received. This bit set to 1 indicates that a multicast packet has been received.
14	R	PAM	Physical Address Matched. This bit set to 1 indicates that the destination address of this packet matches the value written in ID registers.
13	R	BAR	Broadcast Address Received. This bit set to 1 indicates that a broadcast packet is received. BAR, MAR bit will not be set simultaneously.
12-6	-	-	Reserved.
5	R	ISE	Invalid Symbol Error (100Base-TX only). This bit set to 1 indicates that an invalid symbol was encountered during the reception of this packet.
4	R	RUNT	Runt Packet Received. This bit set to 1 indicates that the received packet length is smaller than 64 bytes (i.e. media header + data + CRC < 64 bytes)
3	R	LONG	Long Packet. This bit set to 1 indicates that the size of the received packet exceeds 4k bytes.
2	R	CRC	Cyclic Redundancy Check (CRC) Error. When set, indicates that a CRC error occurred on the received packet.
1	R	FAE	Frame Alignment Error. When set, indicates that a frame alignment error occurred on this received packet.
0	R	ROK	Receive OK. When set, indicates that a good packet was received.

7.2. Transmit Status Register (TSD0-3)(Offset 0010h-001Fh, R/W)

The read-only bits (CRS, TABT, OWC, CDH, NCC3-0, TOK, TUN) will be cleared by the RTL8101L when the Transmit Byte Count (bits 12-0) in the corresponding Tx descriptor is written. It is not affected when software writes to these bits. These registers are only permitted to be written via double-word access. After a software reset, all bits except the OWN bit are reset to 0.

Table 11. Transmit Status Register

Bit	R/W	Symbol	Description
31	R	CRS	Carrier Sense Lost. This bit is set to 1 when the carrier is lost during transmission of a packet.

Bit	R/W	Symbol	Description
30	R	TABT	Transmit Abort. This bit is set to 1 if the transmission of a packet was aborted. This bit is read only, writing to this bit is not affected.
29	R	OWC	Out of Window Collision. This bit is set to 1 if the RTL8101L encountered an 'out of window' collision during the transmission of a packet.
28	R	CDH	CD HeartBeat. The NIC watches for a collision signal (i.e., CD Heartbeat signal) during the first 6.4µs of the InterFrame Gap following a transmission. This bit is set if the transceiver fails to send this signal. This bit is cleared in 100Mbps mode.
27-24	R	NCC3-0	Number of Collision Count. Indicates the number of collisions encountered during the transmission of a packet.
23-22	-	-	Reserved.
21-16	R/W	ERTXTH5-0	Early Tx Threshold. Specifies the threshold level in the Tx FIFO to begin the transmission. When the byte count of the data in the Tx FIFO reaches this level, (or the FIFO contains at least one complete packet) the RTL8101L will transmit this packet. 000000 = 8 bytes These fields count from 000001 to 111111 in units of 32 bytes. This threshold must be prevented from exceeding 2k bytes.
15	R	TOK	Transmit OK. Set to 1 indicates that the transmission of a packet was completed successfully and no transmit underrun has occurred.
14	R	TUN	Transmit FIFO Underrun. Set to 1 if the Tx FIFO was exhausted during the transmission of a packet. The RTL8101L can re-transfer data if the Tx FIFO underruns. That is, when TSD<TUN>=1, TSD<TOK>=0 and ISR<TOK>=1 (or ISR<TER>=1).
13	R/W	OWN	OWN. The RTL8101L sets this bit to 1 when the Tx DMA operation of this descriptor has completed. The driver must set this bit to 0 when the Transmit Byte Count (bits 0-12) is written. The default value is 1.
12-0	R/W	SIZE	Descriptor Size. The total size in bytes of the data in this descriptor. If the packet length is more than 1792 bytes (0700h), the Tx queue will be invalid, i.e. the next descriptor will be written only after the OWN bit of that long packet's descriptor has been set.

7.3. ERSR: Early RX Status Register (Offset 0036h, R)

Table 12. ERSR: Early RX Status Register

Bit	R/W	Symbol	Description
7-4	-	-	Reserved.
3	R	ERGood	Early Rx Good packet. This bit is set whenever a packet is completely received and the packet is good. Writing a 1 to this bit will clear it.
2	R	ERBad	Early Rx Bad packet. This bit is set whenever a packet is completely received and the packet is bad. Writing a 1 to this bit will clear it.
1	R	EROVW	Early Rx OverWrite. This bit is set when the RTL8101L's local address pointer is equal to CAPR. In Early Mode, this is different from buffer overflow. It happens when the RTL8101L detects an Rx error and wants to fill another packet data from the beginning address of that error packet. Writing a 1 to this bit will clear it.
0	R	EROK	Early Rx OK. The power-on value is 0. It is set when the Rx byte count of the arriving packet exceeds the Rx threshold. After the whole packet is received, the RTL8101L will set ROK or RER in ISR and clear this bit simultaneously. Setting this bit will invoke an ROK interrupt.

7.4. Command Register (Offset 0037h, R/W)

This register is used for issuing commands to the RTL8101L. These commands are issued by setting the corresponding bits for the function. A global software reset along with individual reset and enable/disable for transmitter and receiver are provided here.

Table 13. Command Register

Bit	R/W	Symbol	Description
7-5	-	-	Reserved.
4	R/W	RST	Reset. Setting to 1 forces the RTL8101L to a software reset state which disables the transmitter and receiver, reinitializes the FIFOs, resets the system buffer pointer to the initial value (Tx buffer is at TSAD0, Rx buffer is empty). The values of IDR0-5 and MAR0-7 and PCI configuration space will have no changes. This bit is 1 during the reset operation, and is cleared to 0 by the RTL8101L when the reset operation is complete.
3	R/W	RE	Receiver Enable. When set to 1, makes the idle receive state machine active. This bit will read back as a 1 whenever the receive state machine is active. After initial power-up, software must ensure that the receiver has completely reset before setting this bit. This bit will be reset after PCI reset deassertion.
2	R/W	TE	Transmitter Enable. When set to 1, and the transmit state machine is idle, the transmit state machine will become active. This bit will read back as a 1 whenever the transmit state machine is active. After initial power-up, software must ensure that the transmitter has completely reset before setting this bit. This bit will be reset after PCI reset deassertion.
1	-	-	Reserved.
0	R	BUFE	Buffer Empty. RX Buffer Empty. There are no packets stored in the RX buffer ring.

7.5. Interrupt Mask Register (Offset 003Ch-003Dh, R/W)

This register masks the interrupts that can be generated from the Interrupt Status Register. A hardware reset will clear all mask bits. Setting a mask bit allows the corresponding bit in the Interrupt Status Register to cause an interrupt. The Interrupt Status Register bits are always set to 1 if the condition is present, regardless of the state of the corresponding mask bit.

Table 14. Interrupt Mask Register

Bit	R/W	Symbol	Description
15	R/W	SERR	System Error Interrupt. 1: Enable 0: Disable
14	R/W	TimeOut	Time Out Interrupt. 1: Enable 0: Disable
13	R/W	LenChg	Cable Length Change Interrupt. 1: Enable 0: Disable
12-7	-	-	Reserved.
6	R/W	FOVW	Rx FIFO Overflow Interrupt. 1: Enable 0: Disable
5	R/W	PUN/LinkChg	Packet Underrun/Link Change Interrupt. 1: Enable 0: Disable
4	R/W	RXOVW	Rx Buffer Overflow Interrupt. 1: Enable 0: Disable
3	R/W	TER	Transmit Error Interrupt. 1: Enable 0: Disable
2	R/W	TOK	Transmit OK Interrupt. 1: Enable 0: Disable
1	R/W	RER	Receive Error Interrupt. 1: Enable 0: Disable
0	R/W	ROK	Receive OK Interrupt. 1: Enable 0: Disable

7.6. Interrupt Status Register (Offset 003Eh-003Fh, R/W)

This register indicates the source of an interrupt when the INTA pin goes active. Enabling the corresponding bits in the Interrupt Mask Register (IMR) allows bits in this register to produce an interrupt. When an interrupt is active, one or more bits in this register are set to 1. The interrupt Status Register reflects all current pending interrupts, regardless of the state of the corresponding mask bit in the IMR. Writing a 1 to any bit will reset that bit, but writing a 0 has no effect.

Table 15. Interrupt Status Register

Bit	R/W	Symbol	Description
15	R/W	SERR	System Error. Set to 1 when the RTL8101L signals a system error on the PCI bus.
14	R/W	TimeOut	Time Out. Set to 1 when the TCTR register reaches the value of the TimerInt register.
13	R/W	LenChg	Cable Length Change. Cable length is changed after Receiver is enabled.
12 - 7	-	-	Reserved.
6	R/W	FOVW	Rx FIFO Overflow. Set when an overflow occurs on the Rx status FIFO.
5	R/W	PUN/LinkChg	Packet Underrun/Link Change. Set to 1 when CAPR is written but Rx buffer is empty, or when link status is changed.
4	R/W	RXOVW	Rx Buffer Overflow. Set when receive (Rx) buffer ring storage resources have been exhausted.
3	R/W	TER	Transmit (Tx) Error. Indicates that a packet transmission was aborted, due to excessive collisions, according to the TXRR's setting.
2	R/W	TOK	Transmit (Tx) OK. Indicates that a packet transmission has completed successfully.
1	R/W	RER	Receive (Rx) Error. Indicates that a packet has either a CRC error or Frame Alignment Error (FAE). Collided frames will not be recognized as CRC errors if the length of the frame is shorter than 16 bytes.
0	R/W	ROK	Receive (Rx) OK. In normal mode, indicates the successful completion of a packet reception. In early mode, indicates that the Rx byte count of the arriving packet exceeds the early Rx threshold.

7.7. Transmit Configuration Register (Offset 0040h-0043h, R/W)

This register defines the Transmit Configuration for the RTL8101L. It controls such functions as Loopback, programmable InterFrame Gap, Fill and Drain Thresholds, and maximum DMA burst size.

Table 16. Transmit Configuration Register

<table>
<tr><th>Bit</th><th>R/W</th><th>Symbol</th><th>Description</th></tr>
<tr><td>31</td><td>-</td><td>-</td><td>Reserved.</td></tr>
<tr><td>30~26</td><td>R</td><td>HWVERID_A</td><td>Hardware Version ID A.
<table>
<tr><th></th><th>Bit30</th><th>Bit29</th><th>Bit28</th><th>Bit27</th><th>Bit26</th><th>Bit23</th><th>Bit22</th></tr>
<tr><td>RTL8139</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>RTL8139A</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>RTL8139A-G</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>RTL8139B</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>RTL8130</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>RTL8139C</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>RTL8100</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>RTL8100B
RTL8100C
RTL8139D</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>RTL8139C+</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>RTL8101L</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>Reserved</td><td colspan="7">Other combinations.</td></tr>
</table></td></tr>
<tr><td>25, 24</td><td>R/W</td><td>IFG1, 0</td><td>InterFrame Gap time.
This field allows the user to adjust the InterFrame Gap time below the standard: 9.6µs for 10Mbps, 960ns for 100Mbps. The time can be programmed from 9.6µs to 8.4µs (10Mbps) and 960ns to 840ns (100Mbps). Note that any value other than (1, 1) will violate the IEEE 802.3 standard.
The formula for the InterFrame Gap is:
10Mbps: 8.4µs + 0.4(IFG(1:0)) µs
100Mbps: 840ns + 40(IFG(1:0)) ns</td></tr>
<tr><td>23, 22</td><td>R</td><td>HWVERID_B</td><td>Hardware Version ID B.</td></tr>
<tr><td>21~19</td><td>-</td><td>-</td><td>Reserved.</td></tr>
<tr><td>18, 17</td><td>R/W</td><td>LBK1, LBK0</td><td>Loopback test.
There will be no packets on the TX+/- lines under the Loopback test condition. The loopback function must be independent of the link state.
00: Normal operation
01: Reserved
10: Reserved
11: Loopback mode</td></tr>
<tr><td>16</td><td>R/W</td><td>CRC</td><td>Append CRC.
Setting to 1 means that there is no CRC appended at the end of a packet. Setting to 0 means that there is a CRC appended at the end of a packet.</td></tr>
<tr><td>15~11</td><td>-</td><td>-</td><td>Reserved.</td></tr>
</table>

Bit	R/W	Symbol	Description
10~8	R/W	MXDMA2, 1, 0	Max DMA Burst Size per Tx DMA Burst. This field sets the maximum size of transmit DMA data bursts according to the following table: 000 = 16 bytes 001 = 32 bytes 010 = 64 bytes 011 = 128 bytes 100 = 256 bytes 101 = 512 bytes 110 = 1024 bytes 111 = 2048 bytes
7-4	R/W	TXRR	Tx Retry Count. These are used to specify additional transmission retries in multiple of 16 (IEEE 802.3 CSMA/CD retry count). If the TXRR is set to 0, the transmitter will re-transmit 16 times before aborting due to excessive collisions. If the TXRR is set to a value greater than 0, the transmitter will re-transmit a number of times equals to the following formula before aborting: Total retries = 16 + (TXRR * 16) The TER bit in the ISR register or transmit descriptor will be set when the transmission fails and reaches to this specified retry count.
3-1	-	-	Reserved.
0	W	CLRABT	Clear Abort. Setting this bit to 1 causes the RTL8101L to retransmit the packet at the last transmitted descriptor when this transmission was aborted. Setting this bit is only permitted in the transmit abort state.

7.8. Receive Configuration Register (Offset 0044h-0047h, R/W)

This register is used to set the receive configuration for the RTL8101L. Receive properties such as accepting error packets, runt packets, setting the receive drain threshold etc. are controlled here.

Table 17. Receive Configuration Register

Bit	R/W	Symbol	Description
31-28	-	-	Reserved.
27-24	R/W	ERTH3, 2, 1, 0	Early Rx threshold bits. These bits are used to select the Rx threshold multiplier of a whole packet that has been transferred to the system buffer in early mode whilst the frame protocol is under the RTL8101L's definition. 0000 = No early Rx threshold / 0001 = 1/16 0010 = 2/16 / 0011 = 3/16 0100 = 4/16 / 0101 = 5/16 0110 = 6/16 / 0111 = 7/16 1000 = 8/16 / 1001 = 9/16 1010 = 10/16 / 1011 = 11/16 1100 = 12/16 / 1101 = 13/16 1110 = 14/16 / 1111 = 15/16
23-18	-	-	Reserved.
17	R/W	MulERINT	Multiple Early Interrupt select. When this bit is set, any received packet invokes early interrupt according to MULINT<MISR[11:0]> setting in early mode. When this bit is reset, the packets of familiar protocols (IPX, IP, NDIS, etc) invoke early interrupt according to RCR<ERTH[3:0]> setting in early mode. The packets of unfamiliar protocols will invoke early interrupt according to the setting of MULINT<MISR[11:0]>.
16	R/W	RER8	Receive Error 8 bytes. 1: The RTL8101L accepts error packets with a length of 8~64 bytes. 0: The RTL8101L accepts error packets with a length larger than 64 bytes. The power-on default is zero. If AER or AR is set, the RER (Receive Error) will be set when the RTL8101L receives an error packet with a length larger than 8 bytes. RER8 is irrelevant in this situation.

Bit	R/W	Symbol	Description
15~13	R/W	RXFTH2, 1, 0	Rx FIFO Threshold. Specifies the Rx FIFO Threshold level. When the number of received data bytes from a packet that is being received into the RTL8101L's Rx FIFO has reached this level (or the FIFO contains a complete packet), the receive PCI bus master function will begin to transfer the data from the FIFO to the host memory. This field sets the threshold level according to the following table: 000 = 16 bytes 001 = 32 bytes 010 = 64 bytes 011 = 128 bytes 100 = 256 bytes 101 = 512 bytes 110 = 1024 bytes 111 = No Rx threshold. The RTL8101L begins the transfer of data after receiving a whole packet in the FIFO.
12, 11	R/W	RBLEN1, 0	Rx Buffer Length. This field indicates the size of the Rx ring buffer: 00 = 8k + 16 bytes 01 = 16k + 16 bytes 10 = 32K + 16 bytes 11 = 64K + 16 bytes
10~8	R/W	MXDMA2, 1, 0	Max DMA Burst Size per Rx DMA Burst. This field sets the maximum size of the receive DMA data bursts: 000 = 16 bytes 001 = 32 bytes 010 = 64 bytes 011 = 128 bytes 100 = 256 bytes 101 = 512 bytes 110 = 1024 bytes 111 = Unlimited
7	R/W	WRAP	Wraps packet data into the beginning of the Rx buffer. 0: The RTL8101L will transfer the rest of the packet data into the beginning of the Rx buffer if this packet has not been completely moved into the Rx buffer and the transfer has arrived at the end of the Rx buffer. 1: The RTL8101L will keep moving the rest of the packet data into the memory immediately after the end of the Rx buffer, if this packet has not been completely moved into the Rx buffer and the transfer has arrived at the end of the Rx buffer. The software driver must reserve at least 1.5 Kbytes buffer to accept the remainder of the packet. We assume that the remainder of the packet is X bytes. The next packet will be moved into the memory from the X byte offset at the top of the Rx buffer. This bit is invalid when the Rx buffer is set to 64 Kbytes.
6	-	-	Reserved.

Bit	R/W	Symbol	Description
5	R/W	AER	Accept Error Packet. 1: Packets with CRC errors, alignment errors, and/or collided fragments will be accepted. 0: Packets with the above errors will be rejected.
4	R/W	AR	Accept Runt. This bit allows the receiver to accept packets that are smaller than 64 bytes. The packet must be at least 8 bytes long to be accepted as a runt. 1: Accept 0: Reject
3	R/W	AB	Accept Broadcast packets. 1: Accept 0: Reject
2	R/W	AM	Accept Multicast packets. 1: Accept 0: Reject
1	R/W	APM	Accept Physical Match packets. 1: Accept 0: Reject
0	R/W	AAP	Accept All Packets. Set to 1 to accept all packets with a physical destination address. 1: Accept 0: Reject

7.9. 9346CR: 93C46 Command Register (Offset 0050h, R/W)

This register is used for issuing commands to the RTL8101L. These commands are issued by setting the corresponding bits for the function. A warm software reset along with individual reset and enable/disable for transmitter and receiver are also provided.

Table 18. 9346CR: 93C46 Command Register

Bit	R/W	Symbol	Description		
7-6	R/W	EEM1-0	Operating Mode: These 2 bits set the RTL8101L operating mode.		
			EEM1	**EEM0**	**Operating Mode**
			0	0	Normal: RTL8101L network/host communication mode.
			0	1	Auto-load: Entering this mode will force the RTL8101L to load the contents of the 93C46 as if an RSTB signal had been asserted. This auto-load operation will take about 2ms. After it is completed, the RTL8101L goes back to normal mode automatically (EEM1 = 0 EEM0 = 0) and all other registers are reset to default values.
			1	0	93C46 Programming: In this mode both network and host bus master operations are disabled. The 93C46 can be directly accessed via bit3-0 which now reflects the states of EECS, EESK, EEDI, & EEDO pins respectively.
			1	1	Config Register Write Enable: Before writing to CONFIG0, 1, 3, 4 registers, and bit 13, 12, and 8 of BMCR (offset 62h-63h), the RTL8101L must be placed in this mode. This will protect the RTL8101L's configuration from accidental change.
4-5	-	-	Reserved.		
3	R/W	EECS	These bits reflect the state of EECS, EESK, EEDI, and EEDO pins in auto-load or 93C46 programming mode.		
2	R/W	EESK			
1	R/W	EEDI			
0	R	EEDO			

7.10. CONFIG 0: Configuration Register 0 (Offset 0051h, R/W)

Table 19. CONFIG 0: Configuration Register 0

Bit	R/W	Symbol	Description
7	R	SCR	Scrambler Mode. Always 0.
6	R	PCS	PCS Mode. Always 0.
5	R	T10	10Mbps Mode. Always 0.
4-3	R	PL1, PL0	10Mbps Medium Type. Always (PL1, PL0) = (1, 0).
2-0	R	BS2, BS1, BS0	Select Boot ROM size (Auto-loaded from EEPROM).

BS2	BS1	BS0	Description
0	0	0	No Boot ROM
0	0	1	8K Boot ROM
0	1	0	16K Boot ROM
0	1	1	32K Boot ROM
1	0	0	64K Boot ROM
1	0	1	128K Boot ROM
1	1	0	unused
1	1	1	unused

7.11. CONFIG 1: Configuration Register 1 (Offset 0052h, R/W)

Table 20. CONFIG 1: Configuration Register 1

Bit	R/W	Symbol	Description
7-6	R/W	LEDS1-0	Refer to section 6.5 LED Interface, page 9, for a detailed LED pin description. The initial value of these bits comes from the 93C46.
5	R/W	DVRLOAD	Driver Load. Software may use this bit to make sure that the driver has been loaded. 1: Driver loaded 0: Driver not loaded When the command register bits IOEN, MEMEN, and BMEN of the PCI configuration space are written, the RTL8101L will clear this bit automatically.
4	R/W	LWACT	LWAKE active mode: The LWACT bit and LWPTN bit in CONFIG4 register are used to program the LWAKE pin's output signal. Depending on the combination of these two bits, there may be 4 choices of LWAKE signal, i.e., active high, active low, positive (high) pulse, and negative (low) pulse. The output pulse width is about 150ms. The default value of each of these two bits is 0, i.e., the default output signal of the LWAKE pin is an active high signal.

LWAKE Output		LWACT = 0	LWACT = 1
LWPTN	0	Active high*	Active low
	1	Positive pulse	Negative pulse

* Default value.

Bit	R/W	Symbol	Description
3	R	MEMMAP	Memory Mapping. Operational registers are mapped into PCI memory space.
2	R	IOMAP	I/O Mapping. Operational registers are mapped into PCI I/O space.
1	R/W	VPD	Set to enable Vital Product Data. VPD data is stored in the 93C46 from within offset 40h-7Fh.
0	R/W	PMEn	Power Management Enable. Writable only when the 93C46CR register EEM1:0 = [1:1]. Let A denote the New_Cap bit (bit 4 of the Status Register) in the PCI Configuration space offset 06H. Let B denote the Cap_Ptr register in the PCI Configuration space offset 34H. Let C denote the Cap_ID (power management) register in the PCI Configuration space offset 50H. Let D denote the power management registers in the PCI Configuration space offset from 52H to 57H. Let E denote the Next_Ptr (power management) register in the PCI Configuration space offset 51H. **PMEn Description** 1: A=1, B=50h, C=01h, D valid, E=0 0: A=B=C=E=0, D not valid

7.12. Media Status Register (Offset 0058h, R/W)

This register allows configuration of device and PHY options, and provides PHY status information.

Table 21. Media Status Register

<table>
<tr><th>Bit</th><th>R/W</th><th>Symbol</th><th>Description</th></tr>
<tr><td>7</td><td>R/W</td><td>TXFCE/
LdTXFCE</td><td>Tx Flow Control Enable.
Flow control is valid in full-duplex mode only. This register’s default value comes from the 93C46.</td></tr>
<tr><td></td><td></td><td></td><td>
<table>
<tr><th>RTL8101L</th><th>Remote</th><th>TXFCE/LdTXFCE</th></tr>
<tr><td>ANE = 1</td><td>NWAY FLY mode</td><td>R/O</td></tr>
<tr><td>ANE = 1</td><td>NWAY mode only</td><td>R/W</td></tr>
<tr><td>ANE = 1</td><td>No NWAY</td><td>R/W</td></tr>
<tr><td>ANE = 0 & full-duplex mode</td><td>-</td><td>R/W</td></tr>
<tr><td>ANE = 0 & half-duplex mode</td><td>-</td><td>Invalid</td></tr>
</table>

NWAY FLY mode: NWay with flow control capability.
NWAY mode only: NWay without flow control capability.
</td></tr>
<tr><td>6</td><td>R/W</td><td>RXFCE</td><td>RX Flow control Enable.
Flow control is enabled in full-duplex mode only. The default value comes from the 93C46.</td></tr>
<tr><td>5</td><td>-</td><td>-</td><td>Reserved.</td></tr>
<tr><td>4</td><td>R</td><td>Aux_Status</td><td>Aux. Power present Status.
1: Aux. Power is present
0: Aux. Power is absent
The value of this bit is fixed after each PCI reset.</td></tr>
<tr><td>3</td><td>R</td><td>SPEED_10</td><td>Speed. Set when current media is 10Mbps. Reset when current media is 100Mbps.</td></tr>
<tr><td>2</td><td>R</td><td>LINKB</td><td>Inverse of Link status.
0: Link OK
1: Link Fail.</td></tr>
<tr><td>1</td><td>R</td><td>TXPF</td><td>Transmit Pause Flag.
Set when the RTL8101L sends a pause packet. Reset when the RTL8101L sends a timer done packet.</td></tr>
<tr><td>0</td><td>R</td><td>RXPF</td><td>Receive Pause Flag.
Set when the RTL8101L is in backoff state because a pause packet was received.
Reset when the pause state is cleared.</td></tr>
</table>

7.13. CONFIG 3: Configuration Register3 (Offset 0059h, R/W)

Table 22. CONFIG 3: Configuration Register3

Bit	R/W	Symbol	Description
7	R	GNTSel	Grant Select. Sets the Frame's asserted time after the Grant signal has been asserted. Frame and Grant are PCI signals. 1: Delay one clock from GNT assertion 0: No delay
6	R/W	PARM_En	Parameter Enable (Used in 100Mbps mode only). 0: The 9346CR register EEM1:0 = [1:1] will enable the PHY1_PARM, PHY2_PARM, and TW_PARM registers to be written via software. 1: Allows parameters to be auto-loaded from the 93C46, and disables writing to PHY1_PARM, PHY2_PARM and TW_PARM registers via software. PHY1_PARM and PHY2_PARM can be auto-loaded from the EEPROM in this mode. The parameter auto-load process is executed each time the Link is OK in 100Mbps mode.
5	R/W	Magic	Magic Packet. This bit is valid when the PWEn bit of the CONFIG1 register is set. The RTL8101L will assert the PMEB signal to wakeup the operating system when a Magic Packet is received. Once the RTL8101L has been enabled for Magic Packet wakeup, it scans all incoming packets addressed to the node for a specific data sequence that indicates to the controller that this is a Magic Packet. A Magic Packet must also meet the basic requirements of: Destination address + Source address + data + CRC. The destination address may be the node ID of the receiving station or a multicast address, which includes the broadcast address. The specific sequence consists of 16 duplications of a 6-byte ID register, with no breaks nor interrupts. This sequence can be located anywhere within the packet, but must be preceded by a synchronization stream, 6 bytes of FFh. The device will also accept a multicast address, as long as the 16 duplications of the IEEE MAC address match the address of the ID register. If the Node ID is 11h 22h 33h 44h 55h 66h, then the magic packet's format is similar to the following: Destination address + source address + MISC + FF FF FF FF FF FF + MISC + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + 11 22 33 44 55 66 + MISC + CRC
4	R/W	LinkUp	Link Up. This bit is valid when the PWEn bit of CONFIG1 register is set. The RTL8101L, when in an adequate power state, will assert the PMEB signal to wakeup the operating system when the cable connection is re-established.
3	-	-	Reserved.

Bit	R/W	Symbol	Description
2	R	CLKRUN_En	CLKRUN Enable. 1: Enable CLKRUN 0: Disable CLKRUN
1	-	-	Reserved.
0	R	FBtBEn	Fast-Back-to-Back Enable. Set to 1 to enable Fast-Back-to-Back.

7.14. CONFIG 4: Configuration Register4 (Offset 005Ah, R/W)

Table 23. CONFIG 4: Configuration Register4

Bit	R/W	Symbol	Description
7	R/W	RxFIFOAutoClr	Receive FIFO buffer Auto-Clear. When set to 1, the RTL8101L will clear the Rx FIFO buffer automatically.
6	R/W	AnaOff	Analog Power Off. This bit cannot be auto-loaded from EEPROM (93C46). 1: Turns off the analog power of the RTL8101L internally 0: Normal working state. This is also the power-on default value
5	R/W	LongWF	Long Wake-up Frame. The initial value comes from EEPROM auto-load. 0: The RTL8101L supports up to 8 wake-up frames, each with masked bytes selected from offset 12 to 75 1: The RTL8101L supports up to 5 wake-up frames, each with a 16-bit CRC algorithm for MS Wakeup Frame support. The low byte of the 16-bit CRC should be placed in the corresponding CRC register, and the high byte of the 16-bit CRC should be placed in the corresponding LSB CRC register. Wake-up frames 0 and 1 are the same as above, except that the masked bytes start from offset 0 to 63. Wake-up frames 2 and 3 are merged into one long wake-up frame with masked bytes selected from offset 0 to 127. Wake-up frames 4, 5, 6, and 7 are merged into another 2 long wake-up frames. Refer to 10.5 PCI Power Management Functions, page 66, for a detailed description.
4	R/W	LWPME	LWAKE vs. PMEB. 1: LWAKE can only be asserted when PMEB is asserted and ISOLATEB is low 0: LWAKE and PMEB are asserted at the same time
3	-	-	Reserved.
2	R/W	LWPTN	LWAKE Pattern. See the LWACT bit in Table 20. CONFIG 1: Configuration Register 1, page 27.
1	-	-	Reserved.

Bit	R/W	Symbol	Description
0	R/W	PBWakeup	Pre-Boot Wakeup. The initial value comes from EEPROM auto-load. 1: Pre-Boot Wakeup disabled (suitable for CardBus and MiniPCI applications) 0: Pre-Boot Wakeup enabled

7.15. Multiple Interrupt Select Register (Offset 005Ch-005Dh, R/W)

Note: The following is true when MulERINT=0 (bit17, RCR). When MulERINT=1, any received packet invokes an early interrupt according to the MISR[11:0] setting in Early Mode.

If the received packet data is not a familiar protocol (IPX, IP, NDIS, etc.) to the RTL8101L, RCR<ERTH[3:0]> will not be used to transfer data in early mode. This register will be written to the received data length in order to make an early Rx interrupt for the unfamiliar protocol.

Table 24. Multiple Interrupt Select Register

Bit	R/W	Symbol	Description
15-12	-	-	Reserved.
11-0	R/W	MISR11-0	Multiple Interrupt Select Register. Indicates that the RTL8101L made an Rx interrupt after transferring byte data into the system memory. If the value of these bits is zero, there will be no early interrupt when the RTL8101L prepares to execute the first PCI transaction of the received data. Bit1, 0 must be zero. The ERTH3-0 bits should not be set to 0 when the multiple interrupt select register is used.

7.16. PCI Revision ID (Offset 005Eh, R)

Table 25. PCI Revision ID

Bit	R/W	Symbol	Description
7-0	R	Revision ID	The value in PCI Configuration Space offset 08h is 10h.

7.17. Transmit Status of All Descriptors (TSAD) Register (Offset 0060h-0061h, R/W)

Table 26. Transmit Status of All Descriptors (TSAD) Register

Bit	R/W	Symbol	Description
15	R	TOK3	TOK bit of Descriptor 3.
14	R	TOK2	TOK bit of Descriptor 2.
13	R	TOK1	TOK bit of Descriptor 1.
12	R	TOK0	TOK bit of Descriptor 0.
11	R	TUN3	TUN bit of Descriptor 3.
10	R	TUN2	TUN bit of Descriptor 2.
9	R	TUN1	TUN bit of Descriptor 1.
8	R	TUN0	TUN bit of Descriptor 0.
7	R	TABT3	TABT bit of Descriptor 3.
6	R	TABT2	TABT bit of Descriptor 2.
5	R	TABT1	TABT bit of Descriptor 1.
4	R	TABT0	TABT bit of Descriptor 0.
3	R	OWN3	OWN bit of Descriptor 3.
2	R	OWN2	OWN bit of Descriptor 2.
1	R	OWN1	OWN bit of Descriptor 1.
0	R	OWN0	OWN bit of Descriptor 0.

7.18. Basic Mode Control Register (Offset 0062h-0063h, R/W)

Table 27. Basic Mode Control Register

Bit	Name	Description/Usage	Default/Attribute
15	Reset	This bit sets the status and control registers of the PHY (register 0062-0074H) to the default state. This bit is self-clearing. 1: Software reset 0: Normal operation	0, RW
14	-	Reserved.	-
13	Spd_Set	This bit sets the network speed. 1: 100Mbps 0: 10Mbps. This bit's initial value comes from the 93C46	0, RW
12	Auto Negotiation Enable (ANE)	This bit enables/disables the NWay auto-negotiation function. 1: Enable auto-negotiation, bit13 will be ignored. 0: Disables auto-negotiation, bit13 and bit8 will determine the link speed and the data transfer mode, respectively. This bit's initial value comes from the 93C46.	0, RW
11-10	-	Reserved.	-
9	Restart Auto Negotiation	This bit allows the NWay auto-negotiation function to be reset. 1: Re-start auto-negotiation 0: Normal operation	0, RW
8	Duplex Mode	This bit sets the duplex mode. 1: Full-duplex 0: Normal operation. This bit's initial value comes from the 93C46.	0, RW
7-0	-	Reserved.	-

7.19. Basic Mode Status Register (Offset 0064h-0065h, R)

Table 28. Basic Mode Status Register

Bit	Name	Description/Usage	Default/Attribute
15	100Base-T4	1: Enable 100Base-T4 support 0: Disable 100Base-T4 support	0, RO
14	100Base_TX_ FD	1: Enable 100Base-TX full-duplex support 0: Disable 100Base-TX full-duplex support	1, RO
13	100BASE_TX_HD	1: Enable 100Base-TX half-duplex support 0: Disable 100Base-TX half-duplex support	1, RO
12	10Base_T_FD	1: Enable 10Base-T full-duplex support 0: Disable 10Base-T full-duplex support	1, RO
11	10_Base_T_HD	1: Enable 10Base-T half-duplex support 0: Disable 10Base-T half-duplex support	1, RO
10-6	-	Reserved.	-
5	Auto Negotiation Complete	1: Auto-negotiation process completed 0: Auto-negotiation process not completed	0, RO
4	Remote Fault	1: Remote fault condition detected (cleared on read) 0: No remote fault condition detected.	0, RO
3	Auto Negotiation	1: Link has not experienced fail state 0: Link experienced fail state	1, RD
2	Link Status	1: Valid link established 0: No valid link established	0, RO
1	Jabber Detect	1: Jabber condition detected 0: No jabber condition detected	0, RO
0	Extended Capability	1: Extended register capability 0: Basic register capability only	1, RO

7.20. Auto-Negotiation Advertisement Register (Offset 0066h-0067h, R/W)

This register contains the advertised abilities of this device, as are transmitted to its link partner during auto-negotiation.

Table 29. Auto-Negotiation Advertisement Register

Bit	Name	Description/Usage	Default/Attribute
15	NP	Next Page bit. 1: Transmitting the protocol specific data page 0: Transmitting the primary capabilities data page	0, RO
14	ACK	1: Acknowledge reception of link partner capability data word	0, RO
13	RF	Remote Fault. 1: Advertise remote fault detection capability 0: Do not advertise remote fault detection capability	0, RW
12-11	-	Reserved.	-
10	Pause	1: Flow control supported by local node 0: Flow control not supported by local mode	The default value comes from EEPROM, RO
9	T4	1: 100Base-T4 supported by local node 0: 100Base-T4 not supported by local node	0, RO
8	TXFD	1: 100Base-TX full-duplex supported by local node 0: 100Base-TX full-duplex not supported by local node	1, RW
7	TX	1: 100Base-TX supported by local node 0: 100Base-TX not supported by local node	1, RW
6	10FD	1: 10Base-T full-duplex supported by local node 0: 10Base-T full-duplex not supported by local node	1, RW
5	10	1: 10Base-T supported by local node 0: 10Base-T not supported by local node	1, RW
4-0	Selector	Binary encoded selector supported by this node. Currently only CSMA/CD <00001> is specified. No other protocols are supported.	<00001>, RW

7.21. Auto-Negotiation Link Partner Ability Register (Offset 0068h-0069h, R)

This register contains the advertised abilities of the Link Partner as received during Auto-negotiation. If Next Pages are supported, the content changes after a successful auto-negotiation.

Table 30. Auto-Negotiation Link Partner Ability Register

Bit	Name	Description/Usage	Default/Attribute
15	NP	Next Page bit. 1: Transmitting the protocol specific data page 0: Transmitting the primary capability data page	0, RO
14	ACK	1: Link partner acknowledges reception of local node's capability data word	0, RO
13	RF	1: Link partner is indicating a remote fault	0, RO
12-11	-	Reserved.	-
10	Pause	1: Flow control supported by link partner 0: Flow control is not supported by link partner	0, RO
9	T4	1: 100Base-T4 supported by link partner 0: 100Base-T4 not supported by link partner	0, RO
8	TXFD	1: 100Base-TX full duplex is supported by link partner 0: 100Base-TX full duplex not supported by link partner	0, RO
7	TX	1: 100Base-TX supported by link partner 0: 100Base-TX not supported by link partner	0, RO
6	10FD	1: 10Base-T full duplex supported by link partner 0: 10Base-T full duplex not supported by link partner	0, RO
5	10	1: 10Base-T is supported by link partner 0: 10Base-T not supported by link partner	0, RO
4-0	Selector	Link Partner's binary encoded node selector. Currently only CSMA/CD <00001> is specified.	<00000>, RO

7.22. Auto-Negotiation Expansion Register (Offset 006Ah-006Bh, R)

This register contains additional NWay auto-negotiation status information.

Table 31. Auto-Negotiation Expansion Register

Bit	Name	Description/Usage	Default/Attribute
15-5	-	Reserved. These bits are always set to 0.	-
4	MLF	Multiple Link Fault. 1: Fault occurred 0: No fault occurred	0, RO
3	LP_NP_ABLE	Status indicating whether the link partner supports Next Page negotiation. 1: Supported 0: Not supported	0, RO
2	NP_ABLE	This bit indicates whether the local node is able to send additional Next Pages.	0, RO
1	PAGE_RX	This bit is set when a new Link Code Word Page has been received. The bit is automatically cleared when the auto negotiation link partner's ability register (register 5) is read.	0, RO
0	LP_NW_ABLE	1: Link partner supports NWay auto negotiation.	0, RO

7.23. Disconnect Counter (Offset 006Ch-006Dh, R)

Table 32. Disconnect Counter

Bit	Name	Description/Usage	Default/Attribute
15-0	DCNT	This 16-bit counter increments by 1 for every disconnect event. It rolls over when full. It is cleared to zero by a read command.	h'[0000], R

7.24. False Carrier Sense Counter (Offset 006Eh-006Fh, R)

This counter provides information required to implement the 'FalseCarriers' attribute within the MAU managed object class, Clause 30 of the IEEE 802.3u specification.

Table 33. False Carrier Sense Counter

Bit	Name	Description/Usage	Default/Attribute
15-0	FCSCNT	This 16-bit counter increments by 1 for each false carrier event. It is cleared to zero by a read command.	h'[0000], R

7.25. NWay Test Register (Offset 0070h-0071h, R/W)

Table 34. NWay Test Register

Bit	Name	Description/Usage	Default/Attribute
15-8	-	Reserved.	-
7	NWLPBK	1: Set NWay to loopback mode	0, RW
6-4	-	Reserved.	-
3	ENNWLE	1: LED0 Pin indicates linkpulse	0, RW
2	FLAGABD	1: Auto negotiation experienced ability detect state	0, RO
1	FLAGPDF	1: Auto negotiation experienced parallel detection fault state	0, RO
0	FLAGLSC	1: Auto negotiation experienced link status check state	0, RO

7.26. RX_ER Counter (Offset 0072h-0073h, R)

Table 35. RX_ER Counter

Bit	Name	Description/Usage	Default/Attribute
15-0	RXERCNT	This 16-bit counter increments by 1 for each valid packet received. It is cleared to zero by a read command.	h'[0000], R

7.27. CS Configuration Register (Offset 0074h-0075h, R/W)

Table 36. CS Configuration Register

Bit	Name	Description/Usage	Default/Attribute
15	Testfun	1: Auto negotiation to speed up internal timer	0, WO
14-10	-	Reserved.	-
9	LD	Active low TPI link disable signal. When low, TPI still transmits link pulses and TPI maintains a good link state.	1, RW
8	HEARTBEAT	The HEARTBEAT function is only valid in 10Mbps mode. 1: HEARTBEAT enable 0: HEARTBEAT disable	1, RW
7	JBEN	1: Enable jabber function 0: Disable jabber function	1, RW
6	F_LINK_100	Used to login a forced good link at 100Mbps for diagnostics purposes. 1: Disable 0: Enable	1, RW
5	F_Connect	Assertion of this bit forces the disconnect function to be bypassed.	0, RW
4	-	Reserved.	-
3	Con_status	This bit indicates the status of the connection. 1: Valid connected link detected 0: Disconnected link detected	0, RO
2	Con_status_En	Assertion of this bit configures the LED1 pin to indicate connection status.	0, RW
1	-	Reserved.	-
0	PASS_SCR	Bypass Scramble.	0, RW

7.28. Config5: Configuration Register 5 (Offset 00D8h, R/W)

This register, unlike other Config registers, is not protected by the 93C46 Command register. There is no need to enable the Config register write prior to writing to Config5.

Table 37. Config5. Configuration Register 5

Bit	R/W	Symbol	Description
7	-	-	Reserved.
6	R/W	BWF	Broadcast Wakeup Frame. 1: Enable Broadcast Wakeup Frame with Destination ID field mask bytes of FF FF FF FF FF FF 0: Default value. Disable Broadcast Wakeup Frame with Destination ID field mask bytes of FF FF FF FF FF FF
5	R/W	MWF	Multicast Wakeup Frame. 1: Enable Multicast Wakeup Frame with mask bytes of only the Destination ID field, which is a multicast address 0: Default value. Disable Multicast Wakeup Frame with mask bytes of only the Destination ID field, which is a multicast address
4	R/W	UWF	Unicast Wakeup Frame. 1: Enable Unicast Wakeup Frame with mask bytes of only the Destination ID field, which is its own physical address 0: Default value. Disable Unicast Wakeup Frame with mask bytes of only the Destination ID field, which is its own physical address
3	R/W	FIFOAddrPtr	FIFO Address Pointer (Realtek internal use only). The power-on default value of this bit is 0.
2	R/W	LDPS	Link Down Power Saving mode. 1: Disable 0: Enable. When the cable is disconnected (Link Down), the analog part will power itself down (PHY Tx part and part of the Twister) automatically except for the PHY Rx part and the part of the twister that monitors the SD signal in case the cable is reconnected and the Link should be established again
1	R/W	LANWake	LANWake signal enable/disable. 1: Enable LANWake signal 0: Disable LANWake signal
0	R/W	PME_STS	PME_Status bit. Always sticky/can be reset by PCI RST# and software. 1: The PME_Status bit may be reset by PCI reset or by software 0: The PME_Status bit may only be reset by software

8. MC'97 Controller Register and Descriptor Descriptions

Table 38. MC'97 Registers

Offset	R/W	Description
0000h	R/W	Starting Descriptor Index for LINE1-Out
0001h	R	Current Descriptor Index for LINE1-Out
0002h	R/W	Last Descriptor Index for LINE1-Out
0003h	R	LINE1-Out DMA Status Register
0004h-0005h	R/W	LINE1-Out DMA Control Register
0006h-0007h	R	Residual Samples Count in Current LINE1-Out Descriptor Register
0008h-000Bh	-	Reserved
000Ch-000Fh	R/W	LINE1-Out Descriptor Base Address Register
0010h	R/W	Starting Descriptor Index for LINE1-In
0011h	R	Current Descriptor Index for LINE1-In
0012h	R/W	Last Descriptor Index for LINE1-In
0013h	R	LINE1-In DMA Status Register
0014h-0015h	R/W	LINE1-In DMA Control Register
0016h-0017h	R	Residual Samples Count in Current LINE1-In Descriptor Register
0018h-001Bh	-	Reserved
001Ch-001Fh	R/W	LINE1-In Descriptor Base Address Register
0020h-0021h	R/W	AC-LINK Control register
0022h-0023h	R/W	AC-LINK Status and Index register
0024h-0025h	R/W	AC-LINK Data Port
0026h-0027h	R/W	MC97 GPIO Control Register
0028h-0029h	R	MC97 GPIO Status Register
002Ah-002Bh	R/W	Interrupt Status Register
002Ch-002Dh	R/W	PCI GPIO Setup Register (PCIGPIO)
002Eh-002Fh	R/W	PCI GPIO Status Register (PCIGPIOSR)

8.1. Starting Descriptor Index for LINE-Out (Offset 0000h, R/W)

Table 39. Starting Descriptor Index for LINE-Out

Bit	R/W	Symbol	Description
7-5	-	-	Reserved
4-0	R/W	LO_SDILO	Assign the first descriptor to be run when LINE1-Out bus master starts.

8.2. Current Descriptor Index for LINE-Out (Offset 0001h, RO)

Table 40. Current Descriptor Index for LINE-Out

Bit	R/W	Symbol	Description
7-5	-	-	Reserved
4-0	R	LO_CDILO	Indicates the current descriptor is running.

8.3. Last Descriptor Index for LINE-Out (Offset 0002h, R/W)

Table 41. Last Descriptor Index for LINE-Out

Bit	R/W	Symbol	Description
7-5	-	-	Reserved
4-0	R	LO_LDILO	Assign the last descriptor to be run. After the last transaction has been completed for this last descriptor, the LINE-Out bus master should stop.

8.4. LINE-Out DMA Status Register (Offset 0003h, RO)

Table 42. LINE-Out DMA Status Register

Bit	R/W	Symbol	Description
7-2	-	-	Reserved
1	R	LO_Curr_Last	Current descriptor is the last descriptor. This bit will be auto-cleared
0	R	LO_LH	The LINE-Out bus master is not active or the last descriptor has finished transaction. This bit will be auto cleared by H/W when bus master is active.

8.5. LINE-Out DMA Control Register (Offset 0004h-0005h, R/W)

Table 43. LINE-Out DMA Control Register

Bit	R/W	Symbol	Description
15-12	-	-	Reserved
11-8	R/W	LO_DMA_TH	LINE-OUT DMA Threshold Control. 0, 1: When the FIFO is empty, DMA will be triggered. 2, 3: When the sample number in FIFO < 2, DMA will be triggered. … E, F: When the sample number in FIFO < 14, DMA will be triggered. Once LINE1-Out DMA is triggered, DMA will continuously read from system memory until the samples number in the FIFO is equal to the threshold.
7	R/W	LO_RS_DMA	Set to clear all registers (offset at 0000h ~ 0007h) related to DMA, and output FIFO should be flushed. This bit is auto cleared and should be set only when DMA is halted
6-5	-	-	Reserved
4	R/W	FIFOUNIE	FIFO Under-Run Interrupt Enable. 1: Enable interrupt caused by FIFO under-run 0: Disable interrupt caused by FIFO under-run even the 'FIFO_un' is set
3	R/W	LO_CDIE	Current Descriptor Interrupt Enable: 1: Enable interrupt caused by current descriptor has finished its transaction 0: Disable interrupt caused by current descriptor even the 'Curr_End' is set
2	R/W	LO_LDIE	Last Descriptor Interrupt Enable. 1: Enable interrupt caused by the last descriptor has finished its transaction 0: Disable interrupt caused by the last descriptor even the 'Last_End' is set

Bit	R/W	Symbol	Description
1	R/W	LO_PDMA	Pause LINE-Out DMA. 1: The LINE1-Out DMA is paused. FIFO request to PCI bus is frozen, residual data in FIFO send to AC-LINK is also froze, whether controller should continuously send the latest data before FIFO froze depends on the BU setting for descriptor 0: Resume DMA
0	R/W	LO_Start	LINE-Out DMA Start/Stop. 1: Start bus master transaction, and the first descriptor assigned in 'Starting Descriptor Index' 0: Stop bus master transaction

8.6. Residual Samples Count in Current LINE-Out Descriptor Register (Offset 0006h - 0007h, R/W)

Table 44. Residual Samples Count in Current LINE-Out Descriptor Register

Bit	R/W	Symbol	Description
15-0	R	LO_RSS	The residual samples number should be read in system memory for current descriptor. (sample: a 16-bit word)

8.7. LINE-Out Descriptor Base Address Register (Offset 000Ch – 000Fh, R/W)

Table 45. LINE-Out Descriptor Base Address Register

Bit	R/W	Symbol	Description
31-2	R/W	LO_DBA	LINE-Out Descriptor Base Address [31:2]
1-0	R		LINE-Out Descriptor Base Address [1:0]. Hardwired to 0.

8.8. Starting Descriptor Index for LINE-In (Offset 0010h, R/W)

Table 46. Starting Descriptor Index for LINE-In

Bit	R/W	Symbol	Description
7-5	-	-	Reserved
4-0	R/W	LI_SDILI	Assign the first descriptor to be run when LINE-In bus master starts.

8.9. Current Descriptor Index for LINE-In (Offset 0011h, RO)

Table 47. Current Descriptor Index for LINE-In

Bit	R/W	Symbol	Description
7-5	-	-	Reserved
4-0	R	LI_CDILI	Indicates the current descriptor been running.

8.10. Last Descriptor Index for LINE-In (Offset 0012h, R/W)

Table 48. Last Descriptor Index for LINE-In

Bit	R/W	Symbol	Description
7-5	-	-	Reserved
4-0	R	LI_LDILI	Assign the last descriptor to be run. After the last transaction has been completed for this last descriptor, LINE-In bus master should stop.

8.11. LINE-In DMA Status Register (Offset 0013h, RO)

Table 49. LINE-In DMA Status Register

Bit	R/W	Symbol	Description
7-2	-	-	Reserved
1	R	LI_Curr_Last	Current descriptor is the last descriptor. This bit will be auto-cleared
0	R	LI_LH	The LINE-In bus master is not active or the last descriptor has finished transaction. This bit will be auto-cleared by H/W when the bus master is active.

8.12. LINE-In DMA Control Register (Offset 0014h-0015h, R/W)

Table 50. LINE-In DMA Control Register

Bit	R/W	Symbol	Description
15-12	-	-	Reserved
11-8	R/W	LI_DMA_TH	LINE-In DMA Threshold Control: 0, 1: When the FIFO is empty, DMA will be triggered. 2, 3: When the sample number in FIFO >= 2, DMA will be triggered. … E, F: When the sample number in FIFO >=14, DMA will be triggered. Once the LINE-In DMA is triggered, DMA will continuously read from System memory until the samples number in FIFO is equal to threshold.
7	R/W	LI_RS_DMA	Set to clear all registers (offset at 0010h ~ 0017h) related to DMA, and output FIFO should be flushed. This bit is auto-cleared and should be set only when DMA is halted.
6-5	-	-	Reserved
4	R/W	FIFOOVIE	FIFO Over-Run Interrupt Enable. 1: Enable interrupt caused by FIFO over-run 0: Disable interrupt caused by FIFO over-run even the ‘FIFO_ov’ is set
3	R/W	LI_CDIE	Current Descriptor Interrupt Enable. 1: Enable interrupt caused by current descriptor has finished its transaction 0: Disable interrupt caused by current descriptor even the ‘Curr_End’ is set
2	R/W	LI_LDIE	Last Descriptor Interrupt Enable. 1: Enable interrupt caused by the last descriptor has finished its transaction 0: Disable interrupt caused by the last descriptor even the ‘Last_End’ is set

Bit	R/W	Symbol	Description
1	R/W	LI_PDMA	Pause LINE-In DMA. 1: The LINE1-In DMA is paused. FIFO send to PCI bus is frozen, data in FIFO received from AC-LINK is flushed. Whether the controller should continuously send the latest data before the FIFO froze depends on the BU setting for the descriptor. 0: Resume DMA
0	R/W	LI_Start	LINE-In DMA Start/Stop. 1: Start bus master transaction. This is the first descriptor assigned in the 'Starting Descriptor Index' 0: Stop bus master transaction

8.13. Residual Samples Count in Current LINE-In Descriptor Register (Offset 0016h - 0017h, R/W)

Table 51. Residual Samples Count in Current LINE-In Descriptor Register

Bit	R/W	Symbol	Description
15-0	R	LI_RSS	The residual samples number should be read in system memory for the current descriptor (sample: a 16-bit word).

8.14. Line-In Descriptor Base Address Register (Offset 001Ch – 001Fh, R/W)

Table 52. Line-In Descriptor Base Address Register

Bit	R/W	Symbol	Description
31-2	R/W	LI_DBA	LINE-In Descriptor Base Address [31:2].
1-0	R		LINE-In Descriptor Base Address [1:0]. Hardwired to 0.

The LINE-In Descriptor Base Address (LI_DBA) points to the starting address of continuous 64 double-WORD descriptor's DMA context stored in main memory.

8.15. MC'97-Link Control Register (Offset 0020h-0021h, R/W)

Table 53. MC'97-Link Control Register

Bit	R/W	Symbol	Description
15-8	-	-	Reserved
7	R/W	MCSDLB	1: MC97_SDATAIN source comes from MC97_SDATAOUT 0: Normal (MC97_SDATAIN source comes from MC'97)
6	-	-	Reserved
5	R/W	ACLINK_WPE	AC-LINK Wake-up PME# Enable. 1: Enable a PME# when MC'97 issues a wake-up event on MC-LINK 0: Disable If it is disabled, AC-LINK wake-up event doesn't set PME_Status (PCR4C.15), but AC-LINK wake-up event (ACLINK_WES) is still indicated in INTSR.4.

Bit	R/W	Symbol	Description
4	R/W	ACLINK_WIE	AC-LINK Wake-up Interrupt Enable. 1: Enable an interrupt when MC'97 issues a wake-up event on AC-LINK 0: Disable When disabled, an AC-LINK wake-up event does not trigger an interrupt, but an AC-LINK wake-up event (ACLINK_WES) is still indicated in INTSR.4
3	R/W	ACLINK_OFF	AC-LINK Shut Off 1: Drive all AC-LINK outputs low if AC97_BITCLK is stopped, also disable Line-In buffer. It's software's responsibility to set this bit after power-down MC'97 command to enable AC-LINK wake-up event function. It means that wake-up functions defined in bit[5:4] and ACLINK_WES (INTSR.4) will be effective when this bit is set 0: Normal operation
2	R/W	ACLINK_WRST	MC'97 Warm Reset. 1: Writing a '1' to drive AC97_SYNC high at least 1.2us Writing a '1' to this bit only effective while AC97_BITCLK is stopped. If software wants to issue a warm reset while AC97_BITCLK is running, the write is ignored and this bit is unchanged 0: No effect (normal) This bit is auto cleared by hardware after warm reset had been issued.
1	R/W	ACLINK_CRST	MC'97 Cold Reset. 1: Writing a '1' to drive AC97_RESET# low for at least 1.2µs 0: No effect (normal, AC97_RESET# kept as high) This bit is auto set by hardware after cold reset had been issued.
0	R/W	GPIE	GPI Interrupt Enable. 1: The change on GPI Interrupt Status (AC-LINK status bit-0 of slot-12) will cause an interrupt on the PCI interface 0: Interrupt is not generated even if GPI Interrupt Status is set

Note 1: AC-LINK wake-up event: AC97_SDATAIN is resumed high when AC-LINK signals are shut off.
Note 2: Bit 5 and bit 3 are sticky bits preserved by consuming power from Vaux.

8.16. MC'97-Link Status and Index Register (Offset 0022h-0023h, R/W)

Table 54. MC'97-Link Status and Index Register

Bit	R/W	Symbol	Description
15	R	ACLINK_BZ	AC-LINK busy. 1: AC-LINK is busy with an MC'97 register read/write transaction 0: No access is in progress It is set when controller is doing an AC-LINK read/write transaction, it is auto cleared by hardware after the transaction has been finished or AC-LINK Read Time-Out is set. Software should check this bit before doing an AC-LINK Read/Write command. Any written data into bit[7:0] before this bit is cleared by HW will be ignored.
14	R	MC_RDY	1: MC'97 is in ready state. This bit indicates the state of bit-15 in slot-0 of AC97_SDATAIN 0: MC'97 is not ready

Bit	R/W	Symbol	Description
13	R	ACLINK_RTO	AC-LINK Read Time-Out. 1: Set when the MC'97 does not respond to a read command within 4 AC-LINK frames.· This bit is auto-cleared by hardware when the controller receives data from the MC'97 within 4 frames of the read command being issued. 0: MC'97 read completed *Note: Also cleared each time the Command Bit (ACLINK_CB) is written.*
12	R	ACLINK_RD	AC-LINK Read Data is Available. 1: The read data is available 0: The read data is not available This bit is set after data has been got from AC-LINK, and is cleared each time the Command Bit (ACLINK_CB) is written. This bit is also set when AC-LINK Read Time-Out is set. Software should ignore the read back data in this case.
11-10	-	-	Reserved
9	R	GPIO_BZ,	GPIO output data status. 1: Previous data has not been sent yet 0: Previous data sent This bit is set by hardware after software writes data into GPIOCR and the transaction on the SDATA-OUT slot-12 has not completed. It is auto-cleared by hardware after the transaction on SDATA-OUT slot-12 has completed.
8	R	GPIO_INT	GPIO Interrupt. 1: GPIO interrupt 0: No GPIO interrupt This bit reflects the state of bit 0 in Slot 12 of SDATA-IN. Bit 8 reflects the real time GPIO interrupt status on SDATA-IN from MC'97. It is latched from SDATA-IN input slot 12 bit 0 when data is valid.
7	R/W	ACLINK_CB	AC-LINK Command Bit. 1: Read mixer command 0: Write mixer command
6-0	R/W	ACLINK_CIP	AC-LINK Mixer Command Index Port

Note: AC-LINK wake-up event. AC97_SDATAIN is resumed high when AC-LINK signals are shut off.

8.17. AC-Link Data Port (Offset 0024h - 0025h, R/W)

Table 55. AC-Link Data Port

Bit	R/W	Symbol	Description
15-0	R/W	ACLINK_DP	Write: 16 bits of mixer data written to the MC'97. Read: 16 bits of mixer read from the MC'97.

Note: The written data should be sent to MC'97 when writing to ACLINK_CB.
The read data is effective if ACLINK_RD=1 (AC-LINK data is available). It is mapped into a different data port. Any read from this port will always get mixer data from the MC'97.

8.18. GPIO Control to MC'97 (Offset 0026h - 0027h, R/W)

Table 56. GPIO Control to MC'97

Bit	R/W	Symbol	Description
15-0	R/W	GPIOOD	MC'97's GPIO output data.

Note: Bit [15:0] controls the GPIO [15:0] output of MC97. Bit 15~0 are sent on SDATA-OUT slot-12 bit 19 to bit 4. Software should check ACSIR.9 (GPIO_Busy) before writing data. If GPIO_Busy is set by hardware and bit[15:0] are changed, any pending data will be overwritten.

8.19. Real Time GPIO Input Data From MC'97 (Offset 0028h - 0029h, RO)

Table 57. Real Time GPIO Input Data From MC'97

Bit	R/W	Symbol	Description
15-0	R	GPIOID	MC'97's GPIO input data.

Note 1: These bits reflect the real time GPIO input status on SDATA-IN from MC97. Bits 15~0 are latched from SDATA-IN input slot 12 bit 19~4 when data is valid.

Note 2: These bits are real-time updated according to SDATA-IN slot-12 in every frame.

8.20. Interrupt Status Register (Offset 002Ah-002Bh, R/W)

Table 58. Interrupt Status Register

Bit	R/W	Symbol	Description
15	R/W	SERR_IE	SERR# Interrupt Enable. 1: Enable interrupt when RTL8101L signals SERR# on PCI bus 0: Disable
14	R/W	SERR_IS	SERR# Interrupt Status. 1: SERR# interrupt, RTL8101L signals SERR# on PCI bus 0: No SERR# interrupt This controller will generate an SERR# interrupt when (SERR_IE=1) & (SERR# Status=1, Status[14] in configuration space). Write a '1' to clear this bit and its interrupt.
13-10	-	-	Reserved
9	R/W	PCIGPIO1_IS·	PCIGPIO1 Interrupt Status. 1: PCIGPIO1 interrupt 0: No PCIGPIO1 interrupt *Note: Only when PCIGPIOx pin is used as input. Write 1 to clear this status bit and its interrupt.*
8	R/W	PCIGPIO0_IS	PCIGPIO0 Interrupt Status. 1: PCIGPIO0 interrupt 0: No PCIGPIO0 interrupt Write 1 to clear this status bit and its interrupt.

Bit	R/W	Symbol	Description
7	R/W	FIFO_ov	LINE-In's FIFO Over-run. 1: FIFO error indicates a FIFO over-run. This will cause an interrupt if the enable bit in the Control Register is set. This bit and its interrupt should be cleared by writing a '1'. Data received after overrun occurs will not enter into FIFO.
6	R/W	LI_Curr_End	Completion of current LINE-In's descriptor. 1: The current descriptor has sent the last sample to system memory. This will cause an interrupt if the enable bit in Control Register is set. This bit and its interrupt should be cleared by writing a '1'
5	R/W	LI_Last_End	Completion of the last LINE-In's descriptor. 1: The last descriptor has sent the last sample to system memory. This will cause an interrupt if the enable bit in Control Register is set. This bit and its interrupt should be cleared by writing a '1'
4	R/W	ACLINK_WES	AC-LINK Wake-up Event Status. 1: AC-LINK wake-up event occurred 0: No wake-up event This bit is set if ACLINK wake-up event is detected. This controller will generate an interrupt when (ACLINK_WES=1) & (ACLINK_WIE=1). Write a '1' to clear this bit and its interrupt. This bit will not be set when ACLINK Shut-Off (ACCR.3) is 0. Once it is set by an ACLINK wake-up event, it can only be cleared after ACLINK Shut-Off is cleared. *Note: Bit 4 is a sticky bit, preserved by consuming power from Vaux.*
3	R/W	FIFO_un	LINE1-Out FIFO Under-run. 1: FIFO error indicates a FIFO under-run. This will cause an interrupt if the enable bit in LINE1-Out's Control Register is set. This bit and its interrupt should be cleared by writing a '1'
2	R/W	LO_Curr_End	Completion of current Line1-Out's descriptor. 1: The current LINE1-Out's descriptor has got the last sample from system memory. This will cause an interrupt if the enable bit in Control Register is set. This bit and its interrupt should be cleared by writing a '1'
1	R/W	LO_Last_End	Completion of the last LINE1-Out's descriptor. 1: The last descriptor has got the last sample from system memory. This will cause an interrupt if the enable bit in Control Register is set. This bit and its interrupt should be cleared by writing a '1'.
0	R/W	GPIS	MC'97 GPIO Interrupt Status. 1: MC'97 GPIO interrupt. The GPIO_INT (ACSIR.8) has been set 0: No MC'97 GPIO interrupt This bit is set if GPIO_INT (ACSIR.8) has been set. This controller will generate an interrupt when (GPIS=1) & (GPIE=1). Writing a '1' will clear this bit and it's interrupt.

8.21. PCI GPIO Setup Register (Offset 002Ch-002Dh, R/W)

Table 59. PCI GPIO Setup Register

Bit	R/W	Symbol	Description
15-10	-	-	Reserved
9	R/W	PCIGPIO1_PEE	PCIGPIO1 PME# Event Enable (when PCIGPIO1 is used as input). 1: Enable 0: Disable A low to high transaction on PCIGPIO1 will trigger the PCI PME# in D3 state. PCIGPIO[9:8] and PCIGPIO[1:0] are sticky bits and can be powered by Vaux.
8	R/W	PCIGPIO0_PEE	PCIGPIO0 PME# Event Enable (when PCIGPIO0 is used as input). 1: Enable 0: Disable A low to high transaction on PCIGPIO0 will trigger the PCI PME# in D3 state. PCIGPIO[9:8] and PCIGPIO[1:0] are sticky bits and can be powered by Vaux.
7-6	-	-	Reserved
5	R/W	PCIGPIO1_IE	PCIGPIO1 interrupt Enable (when PCIGPIO1 is used as input). 1: Enable 0: Disable A low to high transaction PCIGPIO1 will trigger the PCI interrupt.
4	R/W	PCIGPIO0_IE	PCIGPIO0 interrupt Enable (when PCIGPIO0 is used as input). 1: Enable 0: Disable A low to high transaction PCIGPIO0 will trigger the PCI interrupt.
3-2	-	-	Reserved
1	R/W	PCIGPIO1_PC	PCIGPIO1 Primitive Control. 1: Set PCIGPIO1 as output pin 0: Set PCIGPIO1 as input pin
0	R/W	PCIGPIO0_PC	PCIGPIO0 Primitive Control. 1: Set PCIGPIO0 as output pin 0: Set PCIGPIO0 as input pin

Note: The PME# only be asserted when RTL8101L is in D3 state.

8.22. PCI GPIO Status Register (Offset 002Eh-002Fh, R/W)

Table 60. PCI GPIO Status Register

Bit	R/W	Symbol	Description
15-10	-	-	Reserved
9	R/W	PCIGPIO1_PMES	PCIGPIO1 PME# Event Status. 1: PCIGPIO1 PME# event has occurred in D3 state. 0: No PCIGPIO1 PME# event has occurred in D3 state. Write a 1 to clear this status bit.
8	R/W	PCIGPIO0_PMES	PCIGPIO0 PME# Event Status. 1: PCIGPIO0 PME# event has occurred in D3 state. 0: No PCIGPIO0 PME# event has occurred in D3 state. Write a 1 to clear this status bit.
7-2	-	-	Reserved
1	R/W	PCIGPIO1_IOS	PCIGPIO1 Input/Output Status. 1: PCIGPIO1 is driven high by external device (input). / Drive PCIGPIO1 high (output). 0: PCIGPIO1 is driven low by external device (input). / Drive PCIGPIO1 low (output). *Note: When this pin is used as input, PCIGPIO[9:8] and PCIGPIO[1:0] are sticky bits and can be powered by Vaux.*
0	R/W	PCIGPIO0_IOS	PCIGPIO0 Input/Output Status. 1: PCIGPIO0 is driven high by external device (input). / Drive PCIGPIO0 high (output). 0: PCIGPIO0 is driven low by external device (input). / Drive PCIGPIO0 low (output). *Note: When this pin is used as input, PCIGPIO[9:8] and PCIGPIO[1:0] are sticky bits and can be powered by Vaux.*

8.23. EEPROM (93C46) Command Register (Offset 0030h, R/W)

Table 61. EEPROM (93C46) Command Register

Bit	R/W	Symbol	Description			
7-6	R/W	EEM1-0	Operating Mode: These 2 bits select the RTL8101L operating mode.			
				EEM1	**EEM0**	**Operating Mode**
				0	0	Normal (RTL8101L network/host communication mode)
				0	1	Auto-load: Entering this mode will make the RTL8101L load the contents of 93C46 like when the RSTB signal is asserted. This auto-load operation will take about 2 ms. After it is completed, the RTL8101L goes back to the normal mode automatically (EEM1 = EEM0 = 0) and all the other registers are reset to default values.
				1	0	93C46 programming: In this mode, both network and host bus master operations are disabled. The 93C46 can be directly accessed via bit3-0 which now reflect the states of EECS, EESK, EEDI, & EEDO pins respectively.
				1	1	Config register write enable: Before writing to CONFIG0, 1, 3, 4 registers, and bit13, 12, 8 of BMCR(offset 62h-63h), the RTL8101L must be placed in this mode. This will prevent RTL8101L's configurations from accidental change.
4-5	-	-	Reserved			
3	R/W	EECS	These bits reflect the state of EECS, EESK, EEDI, and EEDO pins in auto-load or 93C46 programming mode.			
2	R/W	EESK				
1	R/W	EEDI				
0	R	EEDO				

8.24. Context For Line-Out Descriptor (Offset 0000h-00FFh)

Table 62. Context For Line-Out Descriptor

Memory Address	Description
LO_DBA+0000h~0003h	DMA Address for Line-Out Descriptor 00h
LO_DBA+0004h~0007h	Buffer Size for Line-Out Descriptor 00h
LO_DBA+0008h~000Bh	DMA Address for Line-Out Descriptor 01h
LO_DBA+000Ch~000Fh	Buffer Size for Line-Out Descriptor 01h
:	:
:	:
LO_DBA+00F0h~00F3h	DMA Address for Line-Out Descriptor 1Eh
LO_DBA+00F4h~00F7h	Buffer Size for Line-Out Descriptor 1Eh
LO_DBA+00F8h~00FBh	DMA Address for Line-Out Descriptor 1Fh
LO_DBA+00FCh~00FFh	Buffer Size for Line-Out Descriptor 1Fh

8.25. Context For Line-In Descriptor (Offset 0000h-00FFh)

Table 63. Context For Line-In Descriptor

Memory Address	Description
LI_DBA+0000h~0003h	DMA Address for Line-In Descriptor 00h
LI_DBA+0004h~0007h	Buffer Size for Line-In Descriptor 00h
LI_DBA+0008h~000Bh	DMA Address for Line-In Descriptor 01h
LI_DBA+000Ch~000Fh	Buffer Size for Line-In Descriptor 01h
:	:
:	:
LI_DBA+00F0h~00F3h	DMA Address for Line-In Descriptor 1Eh
LI_DBA+00F4h~00F7h	Buffer Size for Line-In Descriptor 1Eh
LI_DBA+00F8h~00FBh	DMA Address for Line-In Descriptor 1Fh
LI_DBA+00FCh~00FFh	Buffer Size for Line-In Descriptor 1Fh

8.26. Descriptor Definition

DMA Address for Line1-Out/In Descriptor X

LxDBA+00H~03H:

31		2	1	0
DMA Start Address [31:2]			0	0

Buffer Size for Line1-Out/In Descriptor X

LxDBA+04H~07H:

31	30	29		15	14		1	0
I	BU	Reserved			Buffer Length			0

DMA Start Address [31:0]:

This is the physical start address for the descriptor's DMA operation.

I:

When set to a 1 by S/W, the controller should issue an interrupt upon completion of this buffer.

BU:

If set to a 0, the controller should continuously send the last valid data when FIFO is under-run (keep the last data, and validate the tag bit for Slot-5 on AC_DOUT).

If set to a 1, the controller continuously sends the last invalid data when FIFO is empty or under-run (keep the last data, but invalidate the tag bit for Slot-5 on AC_DOUT).

Note: The BU bit is only effective for LINE1-Out master.

Buffer Length [14:0]:

The size of the data buffer is measured in 16-bit samples. The maximum number of samples is 32767. A value of 0 means there is no sample transferred into this buffer. To achieve an efficient PCI transaction, the buffer length must be an even number.

9. EEPROM (93C46) Contents

The 93C46 is a 1K-bit EEPROM. Although it is actually addressed by words, its contents are listed below by bytes for convenience. After the valid duration of the RSTB pin or auto-load command in the 9346CR, the RTL8101L performs a series of EEPROM read operations from the 93C46 addresses 00H to 31H.

We recommend you obtain Realtek approval before changing the default settings of the EEPROM.

Table 64. EEPROM (93C46) Contents

Bytes	Contents	Description
00h	29h	These 2 bytes contain the ID code word for the RTL8101L. The RTL8101L will load the contents of EEPROM into the corresponding location if the ID word (8129h) is correct. Otherwise, the RTL8101L will not proceed with the EEPROM auto-load process.
01h	81h	
02h-05h	-	Reserved. The RTL8101L no longer supports auto-load of Vender ID and Device ID. The default values of VID and DID are hex 10EC and 8139, respectively.
06h-07h	SVID	PCI Subsystem Vendor ID, PCI configuration space offset 2Ch-2Dh.
08h-09h	SMID	PCI Subsystem ID, PCI configuration space offset 2Eh-2Fh.
0Ah	MNGNT	PCI Minimum Grant Timer, PCI configuration space offset 3Eh.
0Bh	MXLAT	PCI Maximum Latency Timer, PCI configuration space offset 3Fh.
0Ch	MSRBMCR	Bits 7-6 map to bits 7-6 of the Media Status register (MSR); Bits 5, 4, 0 map to bits 13, 12, 8 of the Basic Mode Control register (BMCR); Bits 3-2 are reserved. If the network speed is set to Auto-Detect mode (i.e. NWay mode), then Bit 1=0 means the local RTL8101L supports flow control (IEEE 802.3x). In this case, Bit 10=1 in the Auto-negotiation Advertisement Register (offset 66h-67h), and Bit 1=1 means the local RTL8101L does not support flow control. In this case, Bit 10=0 in Auto-negotiation Advertisement. This is because there are NWay switch hubs which keep sending flow control pause packets for no reason, if the link partner supports NWay flow control.
0Dh	CONFIG3	RTL8101L Configuration register 3, operational register offset 59H.
0Eh-13h	Ethernet ID	Ethernet ID. After an auto-load command or hardware reset, the RTL8101L loads the Ethernet ID to IDR0-IDR5 of RTL8101L's I/O registers.
14h	CONFIG0	RTL8101L Configuration register 0, operational registers offset 51h.
15h	CONFIG1	RTL8101L Configuration register 1, operational registers offset 52h.
16h-17h	PMC	Reserved. Do not change this field without Realtek approval. Power Management Capabilities. PCI configuration space address 52h and 53h.
18h	PMCSR	Reserved. Do not change this field without Realtek approval. Power Management Control/Status. PCI configuration space address 55h.
19h	CONFIG4	Reserved. Do not change this field without Realtek approval. RTL8101L Configuration register 4, operational registers offset 5Ah.
1Ah-1Dh	PHY1_PARM_U	Reserved. Do not change this field without Realtek approval. PHY Parameter 1-U for RTL8101L. Operational registers of the RTL8101L are from 78h to 7Bh.
1Eh	PHY2_PARM_U	Reserved. Do not change this field without Realtek approval. PHY Parameter 2-U for RTL8101L. Operational register of the RTL8101L is 80h.

Bytes	Contents	Description
1Fh	CONFIG_5	Do not change this field without Realtek approval. Bit7-6: Reserved. Bit5-4: Multi-function Select: 00b: Ethernet Controller Only 01b: MC'97 Controller Only 10b: Ethernet+MC'97 Controllers 11b:After ver F Ethernet+Auto-detect MC'97 Controllers If the RTL8101L detects the MC'97, the RTL8101L is set to Multi-function. Otherwise it set to Ethernet only. The MC'97 is only detected during power on or reset. Note: For versions A to E, 11b=Ethernet+MC'97 Controllers Bit3: Reserved. Bit2: Link Down Power Saving mode: Set to 1: Disable. Set to 0: Enable. When the cable is disconnected (Link Down), the analog part will power itself down (PHY Tx part and part of twister) automatically, except PHY Rx part and part of twister to monitor SD signal in case the cable is re-connected and the Link needs to be established again. Bit1: LANWake signal Enable/Disable Set to 1: Enable LANWake signal. Set to 0: Disable LANWake signal. Bit0: PME_Status bit properties Set to 1: The PME_Status bit can be reset by PCI reset or by software if D3cold_support_PME is 0. If D3cold_support_PME=1, the PME_Status bit is a sticky bit. Set to 0: The PME_Status bit is always a sticky bit and can only be reset by software.
20h-21h	MC97_VID	Vendor ID of the MC'97 Controller.
22h-23h	MC97_DID	Device ID of the MC'97 Controller.
24h-25h	MC97_SVID	Sub-Vendor ID of the MC'97 Controller.
26h-27h	MC97_SDID	Sub-Device ID of the MC'97 Controller.
28h-2Bh	PHY1_PARM_T	Reserved. Do not change this field without Realtek approval. PHY Parameter 1-T for the RTL8101L. Operational registers of the RTL8101L are from 78h to 7Bh.
2Ch	PHY2_PARM_T	Reserved. Do not change this field without Realtek approval.
2Dh-31h	-	Reserved.
32h-33h	CheckSum	Reserved. Do not change this field without Realtek approval. Checksum of the EEPROM content.
34h-3Eh	-	Reserved. Do not change this field without Realtek approval.
3Fh	PXE_Para	Reserved. Do not change this field without Realtek approval. PXE ROM code parameter.
40h-7Fh	VPD_Data	VPD data field. Offset 40h is the start address of the VPD data.

9.1. EEPROM Related Ethernet MAC Registers

Table 65. EEPROM Related Ethernet MAC Registers

Offset	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h-05h	IDR0 – IDR5	R/W*	-	-	-	-	-	-	-	-
51h	CONFIG0	R		-	-	-	-	BS2	BS1	BS0
		W*	-	-	-	-	-	-	-	-
52h	CONFIG1	R	LEDS1	LEDS0	DVRLOAD	LWACT	MEMMAP	IOMAP	VPD	PMEN
		W*	LEDS1	LEDS0	DVRLOAD	LWACT	-	-	VPD	PMEN
58h	MSRBMCR	R	TxFCE	RxFCE	-	-	-	-	-	-
		W*	TxFCE	RxFCE	-	-	-	-	-	-
63H		R	-	-	Spd_Set	ANE	-	-	-	FUDUP
		W*	-	-	Spd_Set	ANE	-	-	-	FUDUP
59h	CONFIG3	R	GNTDel	PARM_EN	Magic	LinkUp	-	-	-	FBtBEn
		W*	-	PARM_EN	Magic	LinkUp	-	-	-	-
5Ah	CONFIG4	R/W*	RxFIFO AutoClr	AnaOff	LongWF	LWPME	-	LWPTN	-	-
78h-7Bh	PHY1_PARM	R/W**	32-bit Read Write							
7Ch-7Fh	TW1_PARM TW2_PARM	R/W**	32-bit Read Write 32-bit Read Write							
80h	PHY2_PARM	R/W**	8-bit Read Write							
D8h	CONFIG5	R/W*	-	-	-	-	-	LDPS	LAN Wake	PME_STS

* Registers marked with type = 'W*' can be written only if bits EEM1=EEM0=1.

** Registers marked with type = 'W**' can be written only if bits EEM1=EEM0=1 and CONFIG3<PARM_EN> = 0.

9.2. EEPROM Related Power Management Registers

Table 66. EEPROM Related Power Management Registers

Configuration Space Offset	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
52h	PMC	R	Aux_I_b1	Aux_I_b0	DSI	Reserved	PMECLK	Version		
53h		R	PME_D3$_{cold}$	PME_D3$_{hot}$	PME_D2	PME_D1	PME_D0	D2	D1	Aux_I_b2
55h	PMCSR	R	PME_Status	-	-	-	-	-	-	PME_En
		W	PME_Status	-	-	-	-	-	-	PME_En

10. PCI Configuration Space Registers

10.1. PCI Configuration Space Registers

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	VID	R	1	1	1	0	1	1	0	0
01h		R	0	0	0	1	0	0	0	0
02h	DID	R	0	0	1	1	1	0	0	1
03h		R	1	0	0	0	0	0	0	1
04h	Command	R	0	PERRSP	0	0	-	BMEN	MEMEN	IOEN
		W	-	PERRSP	-	-	-	BMEN	MEMEN	IOEN
05h		R	0	0	0	0	0	-	FBTBEN	SERREN
		W	-	-	-	-	-	-	-	SERREN
06h	Status	R	FBBC	0	0	NewCap	-	0	0	0
07h		R	DPERR	SSERR	RMABT	RTABT	STABT	DST1	DST0	DPD
		W	DPERR	SSERR	RMABT	RTABT	STABT	-	-	DPD
08h	Revision ID	R	0	0	0	0	0	0	0	0
09h	PIFR	R	0	0	0	0	0	0	0	0
0Ah	SCR	R	0	0	0	0	0	0	0	0
0Bh	BCR	R	0	0	0	0	0	0	1	0
0Ch	CLS	R	0	0	0	0	0	0	0	0
0Dh	LTR	R	LTR7	LTR6	LTR5	LTR4	LTR3	LTP2	LTR1	LTR0
		W	LTR7	LTR6	LTR5	LTR4	LTR3	LTP2	LTR1	LTR0
0Eh	HTR	R	0	0	0	0	0	0	0	0
0Fh	BIST	R	0	0	0	0	0	0	0	0
10h	IOAR	R	0	0	0	0	0	0	0	IOIN
		W	-	-	-	-	-	-	-	-
11h		R/W	IOAR15	IOAR14	IOAR13	IOAR12	IOAR11	IOAR10	IOAR9	IOAR8
12h		R/W	IOAR23	IOAR22	IOAR21	IOAR20	IOAR19	IOAR18	IOAR17	IOAR16
13h		R/W	IOAR31	IOAR30	IOAR29	IOAR28	IOAR27	IOAR26	IOAR25	IOAR24
14h	MEMAR	R	0	0	0	0	0	0	0	MEMIN
		W	-	-	-	-	-	-	-	-
15h		R/W	MEM15	MEM14	MEM13	MEM12	MEM11	MEM10	MEM9	MEM8
16h		R/W	MEM23	MEM22	MEM21	MEM20	MEM19	MEM18	MEM17	MEM16
17h		R/W	MEM31	MEM30	MEM29	MEM28	MEM27	MEM26	MEM25	MEM24
18h-2Bh	RESERVED									
2Ch	SVID	R	SVID7	SVID6	SVID5	SVID4	SVID3	SVID2	SVID1	SVID0
2Dh		R	SVID15	SVID14	SVID13	SVID12	SVID11	SVID10	SVID9	SVID8
2Eh	SMID	R	SMID7	SMID6	SMID5	SMID4	SMID3	SMID2	SMID1	SMID0
2Fh		R	SMID15	SMID14	SMID13	SMID12	SMID11	SMID10	SMID9	SMID8
30h	BMAR	R	0	0	0	0	0	0	0	BROMEN
		W	-	-	-	-	-	-	-	BROMEN
31h		R	BMAR15	BMAR14	BMAR13	BMAR12	BMAR11	0	0	0
		W	BMAR15	BMAR14	BMAR13	BMAR12	BMAR11	-	-	-
32h		R/W	BMAR23	BMAR22	BMAR21	BMAR20	BMAR19	BMAR18	BMAR17	BMAR16
33h		R/W	BMAR31	BMAR30	BMAR29	BMAR28	BMAR27	BMAR26	BMAR25	BMAR24

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
34h	Cap_Ptr	R	0	1	0	1	0	0	0	0
35h-3Bh	RESERVED									
3Ch	ILR	R/W	IRL7	ILR6	ILR5	ILR4	ILR3	ILR2	ILR1	ILR0
3Dh	IPR	R	0	0	0	0	0	0	0	1
3Eh	MNGNT	R	0	0	1	0	0	0	0	0
3Fh	MXLAT	R	0	0	1	0	0	0	0	0
40h–4Fh	RESERVED									
50h	PMID	R	0	0	0	0	0	0	0	1
51h	NextPtr	R	0	0	0	0	0	0	0	0
52h	PMC	R	Aux_I_b1	Aux_I_b0	DSI	Reserved	PMECLK	Version		
53h		R	PME_D3$_{cold}$	PME_D3$_{hot}$	PME_D2	PME_D1	PME_D0	D2	D1	Aux_I_b2
54h	PMCSR	R	0	0	0	0	0	0	Power State	
		W	-	-	-	-	-	-	Power State	
55h		R	PME_Status	-	-	-	-	-	-	PME_En
		W	PME_Status	-	-	-	-	-	-	PME_En
56h–5Fh	RESERVED									
60h	VPDID	R	0	0	0	0	0	0	1	1
61h	NextPtr	R	0	0	0	0	0	0	0	0
62h	Flag VPD Address	R/W	VPDADDR7	VPDADDR6	VPDADDR5	VPDADDR4	VPDADDR3	VPDADDR2	VPDADDR1	VPDADDR0
63h		R/W	Flag	VPDADDR14	VPDADDR13	VPDADDR12	VPDADDR11	VPDADDR10	VPDADDR9	VPDADDR8
64h	VPD Data	R/W	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0
65h		R/W	Data15	Data14	Data13	Data12	Data11	Data10	Data9	Data8
66h		R/W	Data23	Data22	Data21	Data20	Data19	Data18	Data17	Data16
67h		R/W	Data31	Data30	Data29	Data28	Data27	Data26	Data25	Data24
68h-FFh	RESERVED									

10.2. PCI Configuration Space Functions

The PCI configuration space is intended for configuration, initialization, and catastrophic error handling functions. The functions of the RTL8101L's configuration space are described below.

VID: Vendor ID. This field defaults to a value of 10ECh (Realtek Semiconductor's PCI Vendor ID).

DID: Device ID. This field defaults to a value of 8139h.

Command: The command register is a 16-bit register used to provide coarse control over a device's ability to generate and respond to PCI cycles.

Table 67. PCI Configuration Space Functions

Bit	Symbol	Description
15-10	-	Reserved
9	FBTBEN	Fast Back-To-Back Enable: Config3<FBtBEn>=0:Read as 0. Write operation has no effect. The RTL8101L will not generate Fast Back-to-back cycles. When Config3<FbtBEn>=1, this read/write bit controls whether or not a master can do fast back-to-back transactions to different devices. Initialization software will set the bit if all targets are fast back-to-back capable. A value of 1 means the master is allowed to generate fast back-to-back transaction to different agents. A value of 0 means fast back-to-back transactions are only allowed to the same agent. This bit's state after RST# is 0.
8	SERREN	System Error Enable: When set to 1, the RTL8101L asserts the SERRB pin when it detects a parity error on the address phase (AD<31:0> and CBEB<3:0>).
7	ADSTEP	Address/Data Stepping: Read as 0, write operation has no effect. The RTL8101L never performs address/data stepping.
6	PERRSP	Parity Error Response: When set to 1, the RTL8101L will assert the PERRB pin on the detection of a data parity error when acting as the target, and will sample the PERRB pin as the master. When set to 0, any detected parity error is ignored and the RTL8101L continues normal operation. Parity checking is disabled after hardware reset (RSTB).
5	VGASNOOP	VGA palette SNOOP: Read as 0, write operation has no effect.
4	MWIEN	Memory Write and Invalidate cycle Enable: Read as 0, write operation has no effect.
3	SCYCEN	Special Cycle Enable: Read as 0, write operation has no effect. The RTL8101L ignores all special cycle operations.
2	BMEN	Bus Master Enable: When set to 1, the RTL8101L is capable of acting as a bus master. When set to 0, it is prohibited from acting as a PCI bus master. For normal operation this bit must be set by the system BIOS.
1	MEMEN	Memory Space Access: When set to 1, the RTL8101L responds to memory space accesses. When set to 0, the RTL8101L ignores memory space accesses.
0	IOEN	I/O Space Access: When set to 1, the RTL8101L responds to IO space access. When set to 0, the RTL8101L ignores I/O space accesses.

10.3. PCI Configuration Space Status

Status: The status register is a 16-bit register used to record status information of PCI bus related events. Reads to this register behave normally. Writes are slightly different in that bits can be reset, but not set.

Table 68. PCI Configuration Space Status

Bit	Symbol	Description
15	DPERR	Detected Parity Error. When set indicates that the RTL8101L detected a parity error, even if parity error handling is disabled in the command register PERRSP bit.
14	SSERR	Signaled System Error. When set indicates that the RTL8101L asserted the system error pin, SERRB. Writing a 1 clears this bit to 0.
13	RMABT	Received Master Abort. When set indicates that the RTL8101L terminated a master transaction with master abort. Writing a 1 clears this bit to 0.
12	RTABT	Received Target Abort. When set indicates that the RTL8101L master transaction was terminated due to a target abort. Writing a 1 clears this bit to 0.
11	STABT	Signaled Target Abort. Set to 1 whenever the RTL8101L terminates a transaction with target abort. Writing a 1 clears this bit to 0.
10-9	DST1-0	Device Select Timing. These bits encode the timing of DEVSELB. They are set to 01b (medium), indicating the RTL8101L will assert DEVSELB two clocks after FRAMEB is asserted.
8	DPD	Data Parity error Detected. This bit sets when the following conditions are met: • The RTL8101L asserts parity error (PERRB pin) or it senses the assertion of the PERRB pin by another device. • The RTL8101L operates as a bus master for the operation that caused the error. • The Command register PERRSP bit is set. Writing a 1 clears this bit to 0.
7	FBBC	Fast Back-To-Back Capable. Config3<FbtBEn>=0, Read as 0. Write operation has no effect. Config3<FbtBEn>=1, Read as 1.
6	UDF	User Definable Features. Read as 0. Write operation has no effect. The RTL8101L does not support UDF.
5	66MHz	66MHz Capable. Read as 0. Write operation has no effect. The RTL8101L has no 66MHz capability.
4	NewCap	New Capability. Config3<PMEn>=0, Read as 0. Write operation has no effect. Config3<PMEn>=1, Read as 1.
0-3	-	Reserved.

RID: Revision ID Register

The Revision ID register is an 8-bit register that specifies the RTL8101L controller revision number.

PIFR: Programming Interface Register

The programming interface register is an 8-bit register that identifies the programming interface of the RTL8101L controller.

PIFR = 00h (the PCI specification does not define any specific value for network devices).

SCR: Sub-Class Register

The Sub-class register is an 8-bit register that identifies the function of the RTL8101L. SCR = 00h indicates that the RTL8101L is an Ethernet controller.

BCR: Base-Class Register

The Base-Class Register is an 8-bit register that broadly classifies the function of the RTL8101L. BCR = 02h indicates that the RTL8101L is a network controller.

CLS: Cache Line Size

Reads will return a 0, writes are ignored.

LTR: Latency Timer Register

Specifies, in units of PCI bus clocks, the value of the latency timer of the RTL8101L.

When the RTL8101L asserts FRAMEB, its latency timer starts to count. If the RTL8101L deasserts FRAMEB prior to count expiration, the contents of the latency timer are ignored. Otherwise, after the count expires, the RTL8101L initiates transaction termination as soon as its GNTB is deasserted. Software is able to read or write, and the default value is 00H.

HTR: Header Type Register

Reads will return a 0, writes are ignored.

BIST: Built-In Self Test

Reads will return a 0, writes are ignored.

IOAR: Input Output Address Register

This register specifies the base IO address that is required to build an address map during configuration. It also specifies the number of bytes required as well as an indication that it can be mapped into IO space.

Table 69. Input Output Address Register

Bit	Symbol	Description
31-8	IOAR31-8	Base IO Address. This is set by software to the base IO address for the operational register map.
7-2	IOSIZE	IO Size. Read back as 0. This allows the PCI bridge to determine that the RTL8101L requires 256 bytes of IO space.
1	-	Reserved.
0	IOIN	IO Space Indicator. Read only. Set to 1 by the RTL8101L to indicate that it is capable of being mapped into IO space.

MEMAR: Memory Address Register

This register specifies the base memory address for memory accesses to the RTL8101L operational registers. This register must be initialized prior to accessing any of the RTL8101L's registers with memory access.

Table 70. Base Memory Address for Memory Accesses

Bit	Symbol	Description
31-8	MEM31-8	Base Memory Address. This is set by software to the base address for the operational register map.
7-4	MEMSIZE	Memory Size. These bits return 0, which indicates that the RTL8101L requires 256 bytes of Memory Space.
3	MEMPF	Memory Pre-Fetchable. Read only. Set to 0 by the RTL8101L.
2-1	MEMLOC	Memory Location Select. Read only. Set to 0 by the RTL8101L. This indicates that the base register is 32-bits wide and can be placed anywhere in the 32-bit memory space.
0	MEMIN	Memory Space Indicator. Read only. Set to 0 by the RTL8101L to indicate that it is capable of being mapped into memory space.

SVID: Subsystem Vendor ID

This field will be set to a value corresponding to the PCI Subsystem Vendor ID in the external EEPROM. If there is no EEPROM, this field will default to a value of 10ECh (Realtek Semiconductor's PCI Subsystem Vendor ID).

SMID: Subsystem ID

This field will be set to a value corresponding to the PCI Subsystem ID in the external EEPROM. If there is no EEPROM, this field will default to a value of 8139h.

BMAR: Base Memory Address Register

This register specifies the base memory address for memory accesses to the RTL8101L's operational registers. This register must be initialized prior to accessing any RTL8101L register with memory access.

Table 71. Base Memory Address for Memory Accesses

Bit	Symbol	Description
31-18	BMAR31-18	Boot ROM Base Address
17-11	ROMSIZE	These bits indicate how many Boot ROM spaces are to be supported. The Relationship between Config 0 <BS2:0> and BMAR17-11 is the following: BS2 BS1 BS0 Description 0 0 0 No Boot ROM, BROMEN=0 (R) 0 0 1 8K Boot ROM, BROMEN (R/W), BMAR12-11 = 0 (R), BMAR17-13 (R/W) 0 1 0 16K Boot ROM, BROMEN (R/W), BMAR13-11 = 0 (R), BMAR17-14 (R/W) 0 1 1 32K Boot ROM, BROMEN (R/W), BMAR14-11 = 0 (R), BMAR17-15 (R/W) 1 0 0 64K Boot ROM, BROMEN (R/W), BMAR15-11 = 0 (R), BMAR17-16 (R/W) 1 0 1 128K Boot ROM, BROMEN(R/W), BMAR16-11=0 (R), BMAR17 (R/W) 1 1 0 unused 1 1 1 unused
10-1	-	Reserved (read back 0)
0	BROMEN	Boot ROM Enable: This is used by the PCI BIOS to enable accesses to Boot ROM.

ILR: Interrupt Line Register

The Interrupt Line Register is an 8-bit read-only register used to indicate the routing of the interrupt. It is written by the POST software to set an interrupt line for the RTL8101L.

IPR: Interrupt Pin Register (Read Only IPR = 01H)

The Interrupt Pin register is an 8-bit register indicating the interrupt pin used by the RTL8101L. The RTL8101L uses an INTA interrupt pin.

MNGNT: Minimum Grant Timer (Read Only)

Specifies the minimum burst period the RTL8101L needs at a 33MHz clock rate, in units of 1/4 microseconds. This field will be set to a value from the external EEPROM. If there is no EEPROM, this field will default to a value of 20h.

MXLAT: Maximum Latency Timer (Read Only)

Indicates how long the RTL8101L is allowed access to the PCI bus, in units of 1/4 microseconds. This field will be set to a value from the external EEPROM. If there is no EEPROM, this field will default to a value of 20h.

Cap_ID: Capability ID: Read only

Read as 01h (PCI bus power management capability ID)

Next_Item_Ptr: Next Item Pointer: Read only

Read as 00h (Last capability list)

Power Management Capabilities:

Bit	Type	Function
15	R	Read as 1 (PME# can be asserted from $D3_{cold}$)
14	R	Read as 1 (PME# can be asserted from $D3_{hot}$)
13	R	Read as 0 (PME# can not be asserted from D2)
12	R	Read as 0 (PME# can not be asserted from D1)
11	R	Read as 0 (PME# can not be asserted from D0)
10	R	Read as 0 (Not support D2 state)
9	R	Read as 0 (Not support D1 state)
8:6	R	Read as 010 (consume maximum 100mA from V_{aux})
5	R	Read as 1 (Device Specific Initialization (DSI) required)
4	R	Read as 0
3	R	Read as 0 (PCI clock is not required for PME# operation)
2:0	R	Read as 010b (PCI Power Management Interface Specification Revision 1.1)

Once Vaux is not supplied, bit[15] reads as 0 to indicate PME# is not supported in $D3_{(cold)}$, and bit[8:6] reads as 000b.

PMCSR:

Bit	Type	Function
15	R/W	PME_Status. 0: Normal 1: PME# asserted
14:13	R	Data_Scale. Read as 00b
12:9	R	Data_Select. Read as 0000b
8	R/W	PME_En. 0: Disable 1: Enable
7:2	R	Read as 0
1:0	R/W	PowerState. 00: D0 01: Reserved 10: Reserved 11: $D3_{hot}$

Writing ‘1’ to bit 15 will clear it and cause the function to stop asserting PME#. Write a ‘0’ has no effect. Note that bit 15 is independent of bit 8.
Writing ‘01’ and ‘10’ to bit 1,0 has no effect on the RTL8101L. The RTL8101L terminates the cycle normally and discards the data (bit 1, 0 only).
Bit 15 and bit 8 are sticky. The System OS should clear them after booting. These 2 bits consume power from V_{aux}. Bits except bit 15/8 consume power from normal power source.
Because PCI 2.3 supports auxiliary power V_{aux}, the chip designer must pay attention to the interface of PME# related circuit and non-PME# related circuit.

10.4. Default Values After Power-on (RSTB Asserted)

Table 72. Default Values After Power-on (RSTB Asserted)

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	VID	R	1	1	1	0	1	1	0	0
01h		R	0	0	0	1	0	0	0	0
02h	DID	R	0	0	1	1	1	0	0	1
03h		R	1	0	0	0	0	0	0	1
04h	Command	R	0	0	0	0	0	0	0	0
		W	-	PERRSP	-	-	-	BMEN	MEMEN	IOEN
05h		R	0	0	0	0	0	0	0	0
		W	-	-	-	-	-	-	-	SERREN
06h	Status	R	0	0	0	NewCap	0	0	0	0
07h		R	0	0	0	0	0	0	1	0
		W	DPERR	SSERR	RMABT	RTABT	STABT	-	-	DPD
08h	Revision ID	R	0	0	0	0	0	0	0	0
09h	PIFR	R	0	0	0	0	0	0	0	0
0Ah	SCR	R	0	0	0	0	0	0	0	0
0Bh	BCR	R	0	0	0	0	0	0	1	0
0Ch	CLS	R	0	0	0	0	0	0	0	0
0Dh	LTR	R	0	0	0	0	0	0	0	0
		W	LTR7	LTR6	LTR5	LTR4	LTR3	LTP2	LTR1	LTR0
0Eh	HTR	R	0	0	0	0	0	0	0	0
0Fh	BIST	R	0	0	0	0	0	0	0	0
10h	IOAR	R	0	0	0	0	0	0	0	1
11h		R/W	0	0	0	0	0	0	0	0
12h		R/W	0	0	0	0	0	0	0	0
13h		R/W	0	0	0	0	0	0	0	0
14h	MEMAR	R	0	0	0	0	0	0	0	0
15h		R/W	0	0	0	0	0	0	0	0
16h		R/W	0	0	0	0	0	0	0	0
17h		R/W	0	0	0	0	0	0	0	0
18h | 2Bh	RESERVED(ALL 0)									
2Ch	SVID	R	1	1	1	0	1	1	0	0
2Dh		R	0	0	0	1	0	0	0	1
2Eh	SMID	R	0	0	1	1	1	0	0	1
2Fh		R	1	0	0	0	0	0	0	1
30h	BMAR	R	0	0	0	0	0	0	0	BROMEN
		W	-	-	-	-	-	-	-	BROMEN
31h		R	BMAR15	BMAR14	BMAR13	BMAR12	BMAR11	0	0	0
		W	BMAR15	BMAR14	BMAR13	BMAR12	BMAR11	-	-	-
32h		R/W	BMAR23	BMAR22	BMAR21	BMAR20	BMAR19	BMAR18	BMAR17	BMAR16
33h		R/W	BMAR31	BMAR30	BMAR29	BMAR28	BMAR27	BMAR26	BMAR25	BMAR24
34h	Cap-Ptr	R	Ptr7	Ptr6	Ptr5	Ptr4	Ptr3	Ptr2	Ptr1	Ptr0

No.	Name	Type	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
35h | 3Bh	RESERVED(ALL 0)									
3Ch	ILR	R/W	0	0	0	0	0	0	0	0
3Dh	IPR	R	0	0	0	0	0	0	0	1
3Eh	MNGNT	R	0	0	1	0	0	0	0	0
3Fh	MXLAT	R	0	0	1	0	0	0	0	0
40h | FFh	-	RESERVED(ALL 0)								

10.5. PCI Power Management Functions

The RTL8101L complies with ACPI (Rev 1.1), PCI Power Management (Rev 1.1), and the Device Class Power Management Reference Specification (V1.0a), such as to support an Operating System-Directed Power Management (OSPM) environment. To support this, the RTL8101L provides the following capabilities:

- The RTL8101L can monitor the network for a Wakeup Frame (AMD Magic Packet, LinkChg, Microsoft® wake-up frame), and notify the system via PME# should such a packet or event arrive. Then the system can be restored to a working state to process incoming jobs.
- The RTL8101L can be isolated from the PCI bus automatically via the auxiliary power circuit when the PCI bus is in B3 state, i.e. the power on the PCI bus is removed. The RTL8101L can be disabled when needed by pulling the isolate pin low to 0V.

10.5.1. Power Down Mode

When the RTL8101L is in power down mode (D1 ~ D3):

- The Rx state machine is stopped and the RTL8101L monitors the network for wakeup events. The RTL8101L will not reflect the status of any incoming packets in the ISR register and will not receive any packets into the Rx FIFO.
- The FIFO status and the packets that are already in the Rx FIFO before entering power down mode are held by the RTL8101L during power down mode.
- Transmission is stopped. PCI bus master mode is stopped. The Tx FIFO buffer is held.
- After restoration to a D0 state, PCI bus master mode transfers data to the Tx FIFO that was not moved into the Tx FIFO before the last break. A packet that was not transmitted completely before power down mode is transmitted again.

D3cold_support_PME bit (bit15, PMC register) & Aux_I_b2:0 (bit8:6, PMC register) in PCI configuration space

- If 9346 D3cold_support_PME bit (bit15, PMC) = 1, the above 4 bits depend on the existence of Aux power.
- If 9346 D3cold_support_PME bit (bit15, PMC) = 0, the above 4 bits are all 0's.

Examples:

9346 D3c_support_PME = 1

- If Aux. power exists, then PMC in PCI config space is the same as 9346 PMC, i.e. if 9346 PMC = C2 F7, then PCI PMC = C2 F7.
- Aux. power is absent, then PMC in PCI config space is the same as 9346 PMC except the above 4 bits are all 0's. I.e. if 9346 PMC = C2 F7, then PCI PMC = 02 76.

Note: In this case, if wakeup support is desired when the main power is off, it is suggested that the EEPROM PMC be set to: C2 F7 (Realtek default value). It is not recommended to set the D0_support_PME bit to 1.

9346 D3c_support_PME = 0,

- If Aux. power exists, then PMC in PCI config space is the same as 9346 PMC, i.e. if 9346 PMC = C2 77, then PCI PMC = C2 77.
- If Aux. power is absent, then PMC in PCI config space is the same as 9346 PMC except the above 4 bits are all 0's, i.e. if 9346 PMC = C2 77, then PCI PMC = 02 76.

Note: In this case, if wakeup support is not desired when main power is off, it is suggested that the 9346 PMC be set to 02 76. It is not recommended to set the D0_support_PME bit to 1.

Link Wakeup

Link Wakeup occurs when the following conditions are met:

- The LinkUp bit (CONFIG3#4) is set to 1, the PMEn bit (CONFIG1#0) is set to 1, and the RTL8101L is in isolation state, or the PME# can be asserted in the current power state.
- The Link status is re-established.

Magic Packet Wakeup

A Magic Packet Wakeup occurs when the following conditions are met:

- The destination address of the received Magic Packet matches.
- The received Magic Packet does not contain a CRC error.
- The Magic bit (CONFIG3#5) is set to 1, the PMEn bit (CONFIG1#0) is set to 1, and the RTL8101L is in isolation state, or the PME# can be asserted in the current power state.

- The Magic Packet pattern matches, i.e. 6 * FFh + MISC (can be none) + 16 * DID (Destination ID) in any part of a valid (Fast) Ethernet packet.

A Wakeup Frame event occurs only when the following conditions are met:

- The destination address of the received Wakeup Frame matches.
- The received Wakeup Frame does not contain a CRC error.
- The PMEn bit (CONFIG1#0) is set to 1.
- The 8-bit CRC* (or 16-bit CRC**) of the received Wakeup Frame matches with the 8-bit CRC (or 16-bit CRC) of the sample Wakeup Frame pattern received from the local machine's OS.
- The last masked byte*** of the received Wakeup Frame matches with the last masked byte*** of the sample Wakeup Frame pattern provided by the local machine's OS (In Long Wakeup Frame mode, the last masked byte field is replaced with the high byte of the 16-bit CRC).

***8-bit CRC:**

8-bit CRC logic is used to generate an 8-bit CRC from the masked bytes of the received Wakeup Frame packet within offset 12 to 75. Software should calculate the 8-bit Power Management CRC for each specific sample wakeup frame and store the calculated CRC in the corresponding CRC register for the RTL8101L to check whether there is a Wakeup Frame coming in.

****16-bit CRC: (Long Wakeup Frame mode, the mask bytes cover from offset 0 to 127)**

Long Wakeup Frame: The RTL8101L also supports 3 long Wakeup Frames. If the range of mask bytes of the sample Wakeup Frame, passed down by the OS to the driver, exceeds the range from offset 12 to 75, the related registers of wakeup frame 2 and 3 can be merged to support one long wakeup frame by setting the LongWF (bit0, CONFIG4). Thus, the range of effective mask bytes extends from offset 0 to 127. The low byte and high byte of the calculated 16-bit CRC should be put into register CRC2 and LSBCRC2 respectively. The mask bytes (16 bytes) should be stored in register Wakeup2 and Wakeup3. The CRC3 and LSBCRC3 have no meaning in this case and should be reset to 0. Long Wakeup Frame pairs are frames 4 and 5, and frames 6 and 7. The CRC5, CRC7, LSBCRC5, and LSBCRC7 have no meaning in this case and should be set to 0 if the RTL8101L is to support long Wakeup Frames. The RTL8101L supports 2 normal wakeup frames and 3 long wakeup frames.

*****Last Masked Byte:**

The last byte of the masked bytes of the received Wakeup Frame packet within offset 12 to 75 (in 8-bit CRC mode) should match the last byte of the masked bytes of the sample Wakeup Frame provided by the local machine's OS.

PME# Signal

The PME# signal is asserted only when the following conditions are met:

- The PMEn bit (bit0, CONFIG1) is set to 1.
- The PME_En bit (bit8, PMCSR) in PCI Configuration Space is set to 1.
- The RTL8101L may assert PME# in current power state, or when the RTL8101L is in isolation state. Refer to 10.1 PCI Configuration Space , page 57, PME_Support (bit15-11) of the PMC register.
- A Magic Packet, LinkChg, or Wakeup Frame event has occurred.

Writing a 1 to the PME_Status (bit15) of PMCSR register in the PCI Configuration Space will clear this bit and cause the RTL8101L to stop asserting a PME# (if enabled).

When the RTL8101L is in power down mode, e.g. D1-D3, the IO, and MEM are all disabled. After RST# is asserted, the power state must be changed to D0 if the original power state was $D3_{cold}$. There is no hardware enforced delays in the RTL8101L's power state. When in ACPI mode, the RTL8101L does not support PME from D0 owing to the PMC register setting (this setting comes from EEPROM).

LWAKE Signal

The RTL8101L also supports the LAN WAKE-UP function. The LWAKE pin is used to notify the motherboard to execute the wake-up process whenever the RTL8101L receives a wakeup event, such as a Magic Packet.

The LWAKE signal is asserted according to the following setting:

- LWPME bit (bit4, CONFIG4)

  0: LWAKE is asserted whenever a wakeup event occurs
  1: LWAKE can only be asserted when PMEB is asserted and ISOLATEB is low
- Bit1 of DELAY byte (offset 1Fh, EEPROM)

  0: LWAKE signal is disabled
  1: LWAKE signal is enabled

10.6. VPD (Vital Product Data)

Bit 31 of the VPD is used to issue VPD read/write commands and is also a flag used to indicate whether the transfer of data between the VPD data register and the 93C46 has completed or not.

Write VPD register (write data to the 93C46)

- Write the flag bit to 1 at the same time the VPD address is written. When the flag bit is set to 0 by the RTL8101L, the VPD data (all 4 bytes) has been transferred from the VPD data register to the 93C46.

Read VPD register (read data from the 93C46)

- Write the flag bit to a zero at the same time the VPD address is written. When the flag bit is set to one by the RTL8101L, the VPD data (all 4 bytes) has been transferred from the 93C46 to the VPD data register.

11. Functional Description

11.1. Transmit Operation

The host CPU initiates a transmit by storing an entire packet of data in one of the descriptors in the main memory. When the entire packet has been transferred to the Tx buffer, the RTL8101L is instructed to move the data from the Tx buffer to the internal transmit FIFO in PCI bus master mode. When the transmit FIFO contains a complete packet or is filled to the programmed threshold level, the RTL8101L begins packet transmission.

11.2. Receive Operation

The incoming packet is placed in the RTL8101L's Rx FIFO. Concurrently, the RTL8101L performs address filtering of multicast packets according to the hash algorithms. When the amount of data in the Rx FIFO reaches the level defined in the Receive Configuration Register, the RTL8101L requests the PCI bus to begin transferring the data to the Rx buffer in PCI bus master mode.

11.3. Wander Compensation

The RTL8101L is ANSI TP-PMD compliant and supports Input Wander and Base Line Wander (BLW) compensation in 100Base-TX mode. The RTL8101L does not require external attenuation circuitry at its receive inputs, RD+/-. It accepts TP-PMD compliant waveforms directly, requiring only 100Ω termination and a 1:1 transformer.

BLW is the change in the average DC content, over time, of an AC coupled digital transmission over a given transmission medium and is a result of the interaction between the low frequency components of a transmitted bit stream and the frequency response of the AC coupling component(s) within the transmission system. If the low-frequency content of the digital bit stream goes below the low-frequency pole of the AC coupling transformers, then the droop characteristics of the transformers will dominate, resulting in potentially serious BLW. If BLW is not compensated, packet loss can occur.

11.4. Signal Detect

The RTL8101L supports signal detect in 100Base-TX mode. The reception of normal 10Base-T link pulses and fast link pulses (defined by IEEE 802.3u Auto-negotiation) by the 100Base-TX receiver do not cause the RTL8101L to assert signal detect.

The signal detect function of the RTL8101L is incorporated to meet the specifications mandated by the ANSI FDDI TP-PMD standard as well as the IEEE 802.3 100Base-TX standard for both voltage thresholds and timing parameters.

11.5. Line Quality Monitor

The line quality monitor function is available in 100Base-TX mode. It is possible to determine the amount of Equalization being used by accessing certain test registers with the DSP engine. This provides a crude indication of connected cable length. This function allows for a quick and simple verification of the line quality in that any significant deviation from an expected register value (based on a known cable length) would indicate that the signal quality has deviated from the expected nominal case.

11.6. Clock Recovery Module

The Clock Recovery Module (CRM) is supported in 100Base-TX mode. The CRM accepts 125Mbps MLT-3 data from the equalizer. The DPLL locks onto the 125Mbps data stream and extracts a 125MHz recovered clock. The extracted and synchronized clock and data are used as required by the synchronous receive operations.

11.7. Loopback Operation

Loopback mode is normally used to verify that the logic operations up to the Ethernet cable function correctly. In loopback mode for 100Mbps, the RTL8101L takes frames from the transmit descriptor and transmits them up to internal Twister logic.

11.8. Tx Encapsulation

While operating in 100Base-TX mode, the RTL8101L encapsulates the frames that it transmits according to the 4B/5B code-groups table. The changes to the original packet data are listed below:

The first byte of the preamble in the MAC frame is replaced with the JK symbol pair.

After the CRC, the TR symbol pair is inserted.

11.9. Collision

If the RTL8101L is not in full-duplex mode, a collision event occurs when the receive input is not idle while the RTL8101L transmits. If the collision was detected during the preamble transmission, a jam pattern is transmitted after completing the preamble (including the JK symbol pair).

11.10. Rx Decapsulation

The RTL8101L continuously monitors the network when reception is enabled. When activity is recognized it starts to process the incoming data.

After detecting receive activity on the line, the RTL8101L starts to process the preamble bytes based on the mode of operation.

While operating in 100Base-TX mode, the RTL8101L expects the frame to start with the symbol pair JK in the first byte of the 8-byte preamble.

The RTL8101L checks the CRC bytes and checks whether the packet data ends with the TR symbol pair. If not, the RTL8101L reports an RSR CRC error.

The RTL8101L reports an RSR CRC error in 100Base-TX mode if an invalid symbol (4B/5B Table) is received in the middle of the frame. The RSR<ISR> bit also sets.

11.11. Flow Control

The RTL8101L supports IEEE 802.3X flow control for improved performance in full-duplex mode. It detects PAUSE packets to achieve flow control tasks.

11.11.1. Control Frame Transmission

When the RTL8101L detects that it's free receive buffer is less than 3K bytes, it sends a PAUSE packet with pause_time (=FFFFh) to inform the source station to stop transmission for the specified period of time. After the driver has processed the packets in the receive buffer and updated the boundary pointer, the RTL8101L sends another PAUSE packet with pause_time (=0000h) to wake up the source station to restart transmission.

11.11.2. Control Frame Reception

The RTL8101L enters a backoff state for a specified period of time when it receives a valid PAUSE packet with pause_time (=n). If the PAUSE packet is received while the RTL8101L is transmitting, the RTL8101L starts to back off after the current transmission completes. The RTL8101L is free to transmit the next packet when it receives a valid PAUSE packet with pause_time (=0000h) or the backoff timer (=n*512 bit time) elapses.

Note: The PAUSE operation cannot be used to inhibit transmission of MAC Control frames (e.g. PAUSE packet). NWay flow control capability can be disabled. Refer to section 9 EEPROM (93C46) Contents, page 54.

11.12. LED Functions

11.12.1. 10/100Mbps Link Monitor

The Link Monitor senses whether a station is connected and monitors link integrity.

Note: In 10/100Mbps mode, LED function is the same as that of the RTL8139C(L).

11.12.2. LED_RX

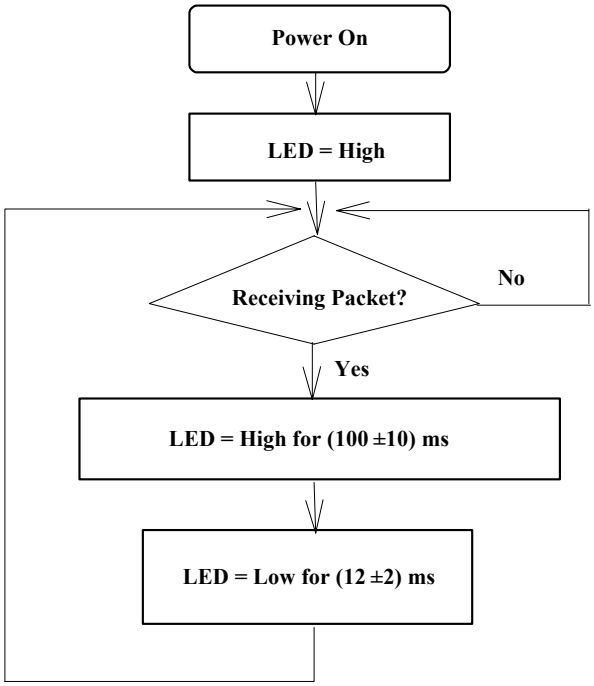


Figure 3. LED_RX

11.12.3. LED_TX

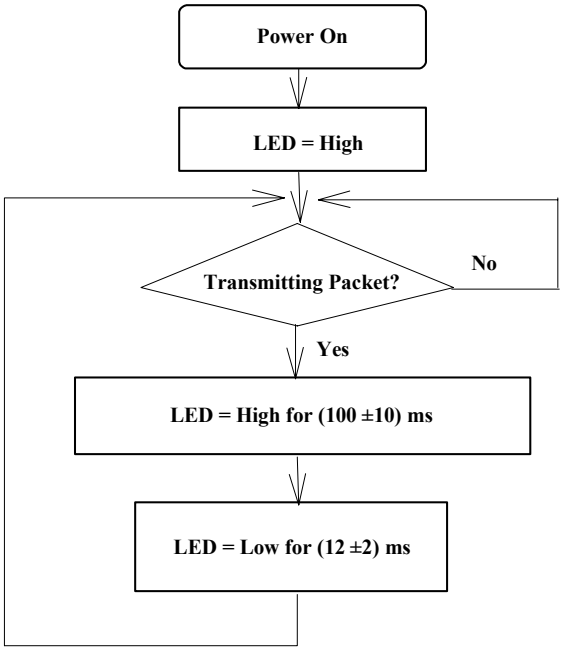


Figure 4. LED_TX

11.12.4. LED_TX+LED_RX

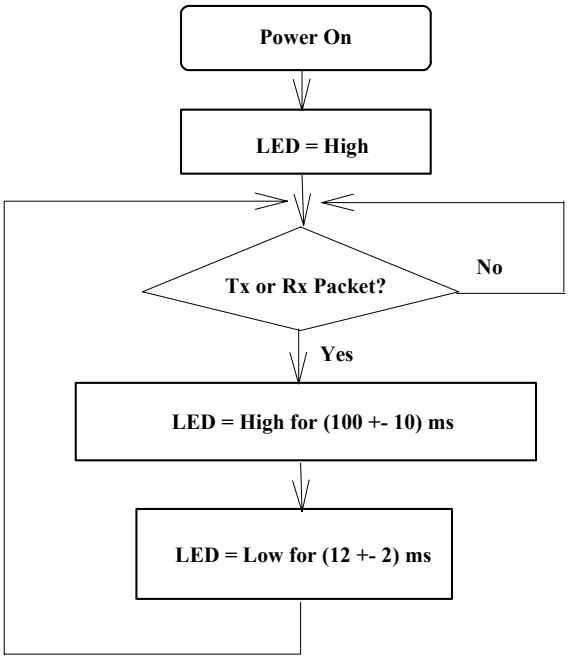


Figure 5. LED_TX+LED_RX

12. Application Diagram

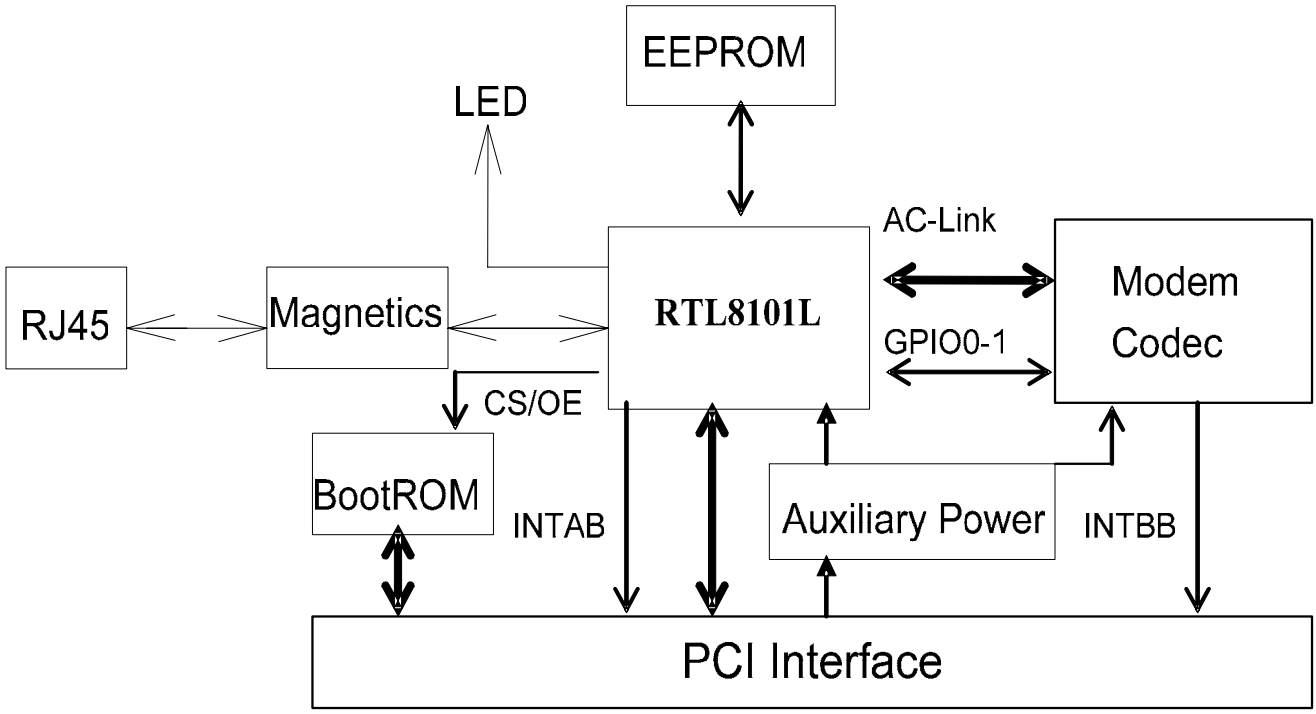


Figure 6. Application Diagram

13. Characteristics

13.1. Thermal Characteristics

Table 73. Thermal Characteristics

Parameter	Minimum	Maximum	Units
Storage temperature.	-55	+125	°C
Operating temperature.	0	70	°C

13.2. DC Characteristics

13.2.1. Supply Voltage (Vcc = 3.0V min. to 3.6V max.)

Table 74. Supply Voltage (3.0V min. to 3.6V max.)

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{OH}	Minimum High Level Output Voltage.	I_{OH}= -8mA	0.9 * Vcc	Vcc	V
V_{OL}	Maximum Low Level Output Voltage.	I_{OL}= 8mA		0.1 * Vcc	V
V_{IH}	Minimum High Level Input Voltage.		0.5 * Vcc	Vcc+0.5	V
V_{IL}	Maximum Low Level Input Voltage.		-0.5	0.3 * Vcc	V
I_{IN}	Input Current.	V_{IN}=V_{CC} or GND	-1.0	1.0	µA
I_{OZ}	Tri-State Output Leakage Current.	V_{OUT}=V_{CC} or GND	-10	10	µA
I_{CC}	Average Operating Supply Current.	I_{OUT}=0mA,		80	mA

13.3. AC Characteristics

13.3.1. PCI Bus Operation Timing

Target Read

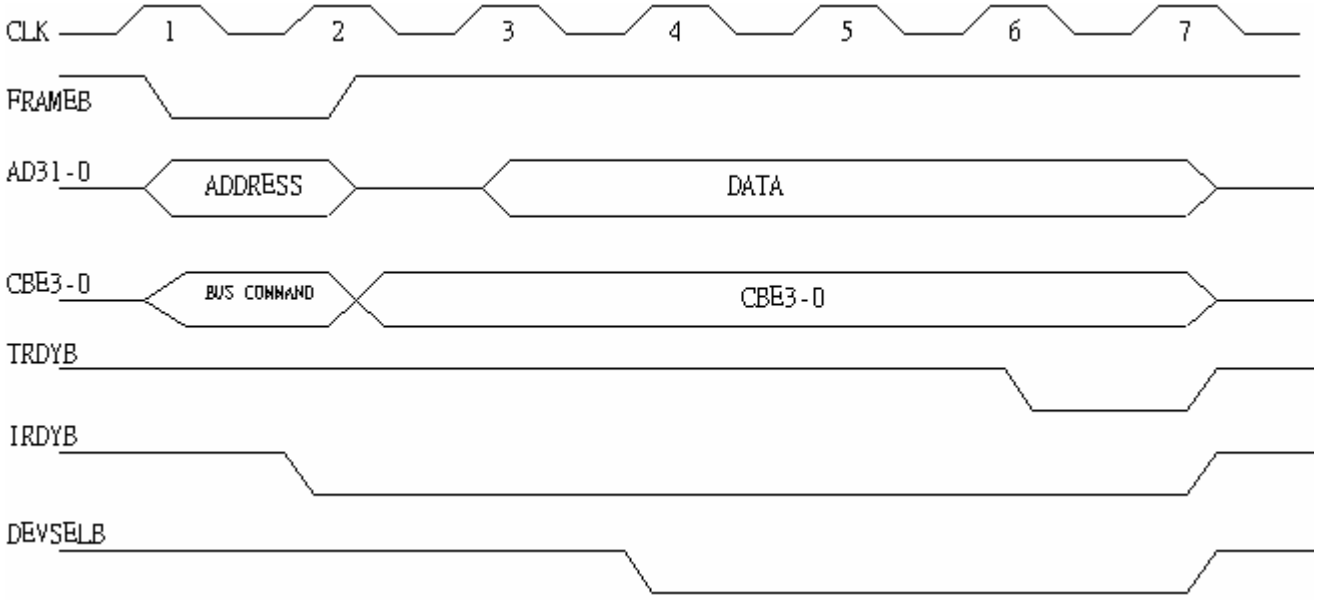


Figure 7. Target Read

Target Write

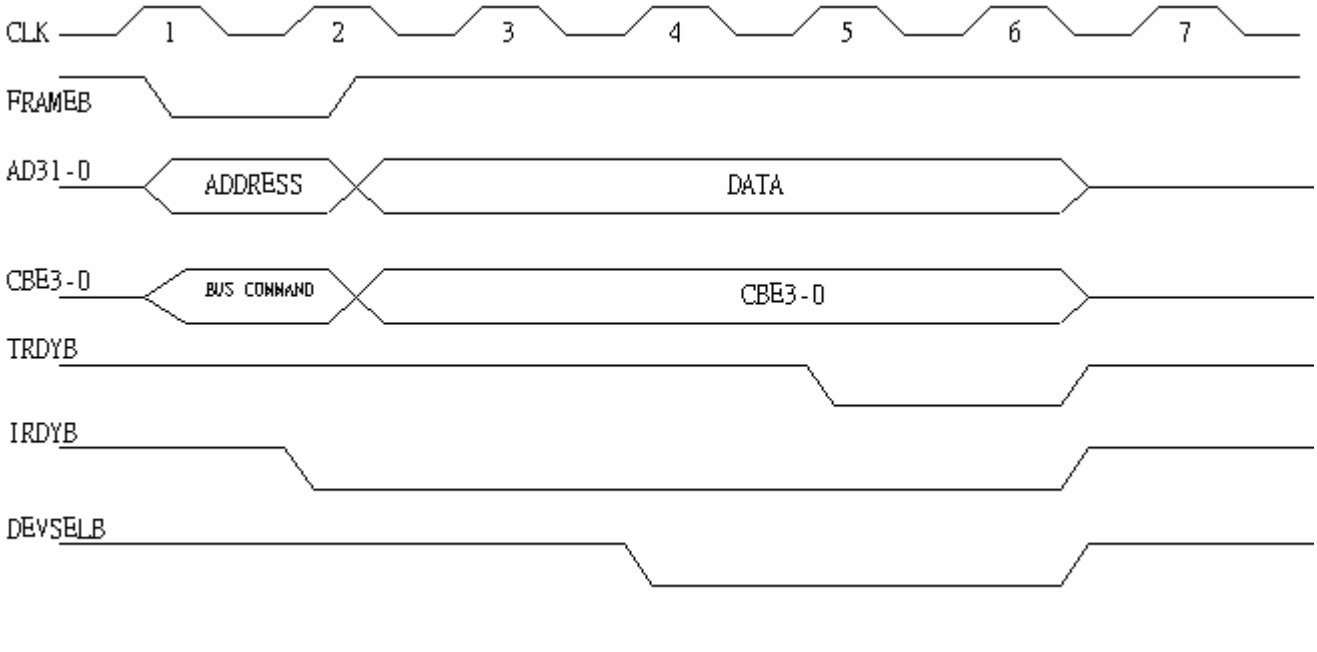


Figure 8. Target Write

Configuration Read

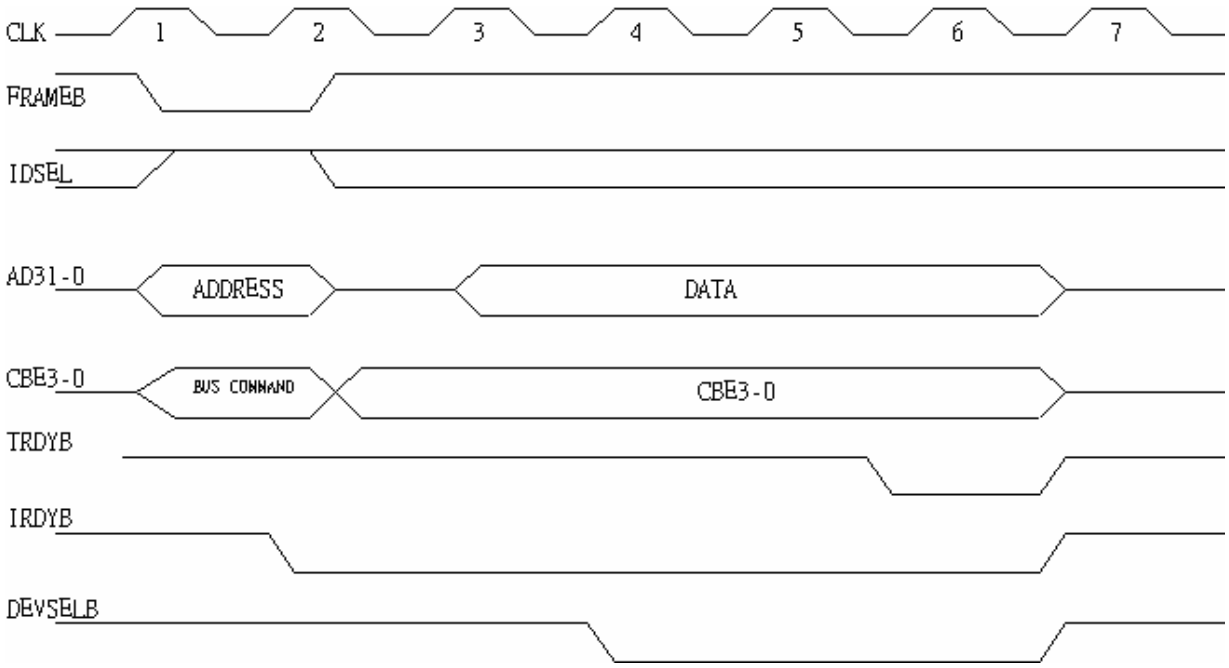


Figure 9. Configuration Read

Configuration Write

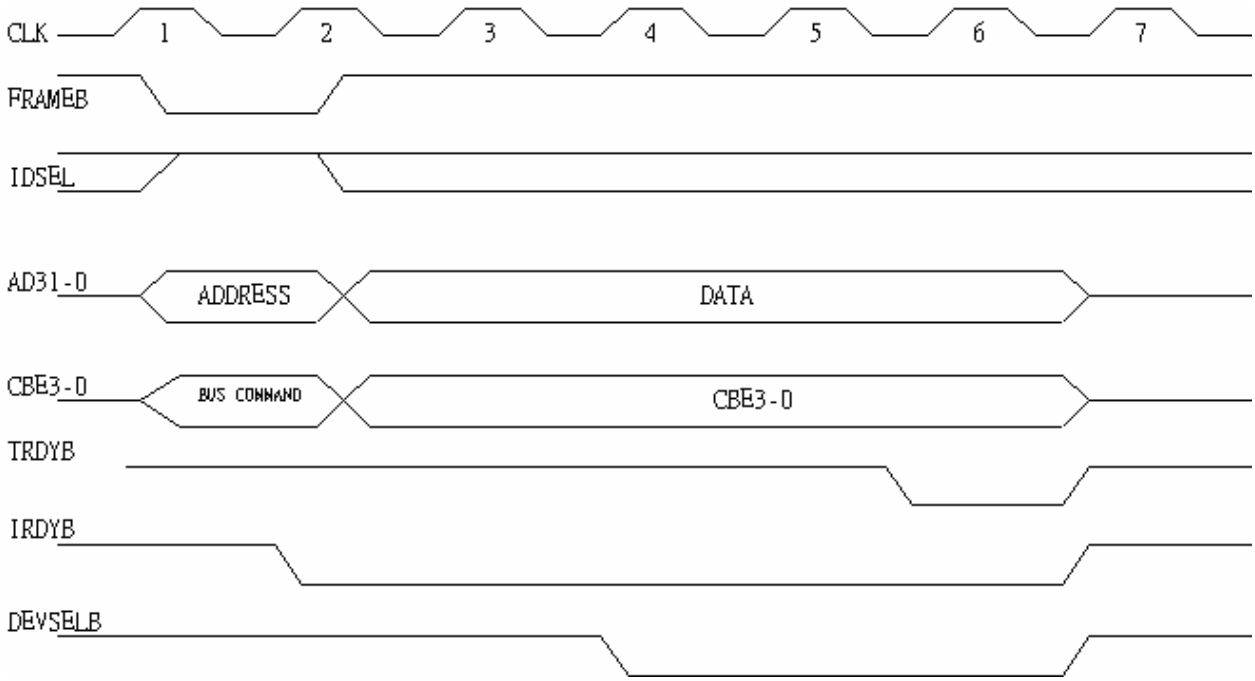


Figure 10. Configuration Write

Bus Arbitration

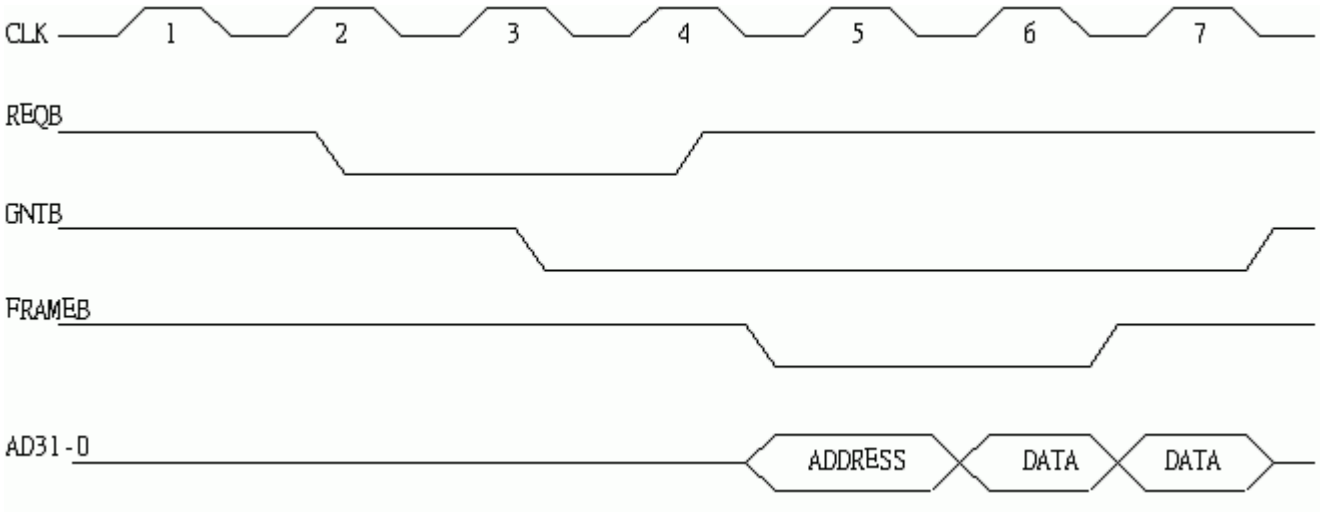


Figure 11. Bus Arbitration

Memory Read

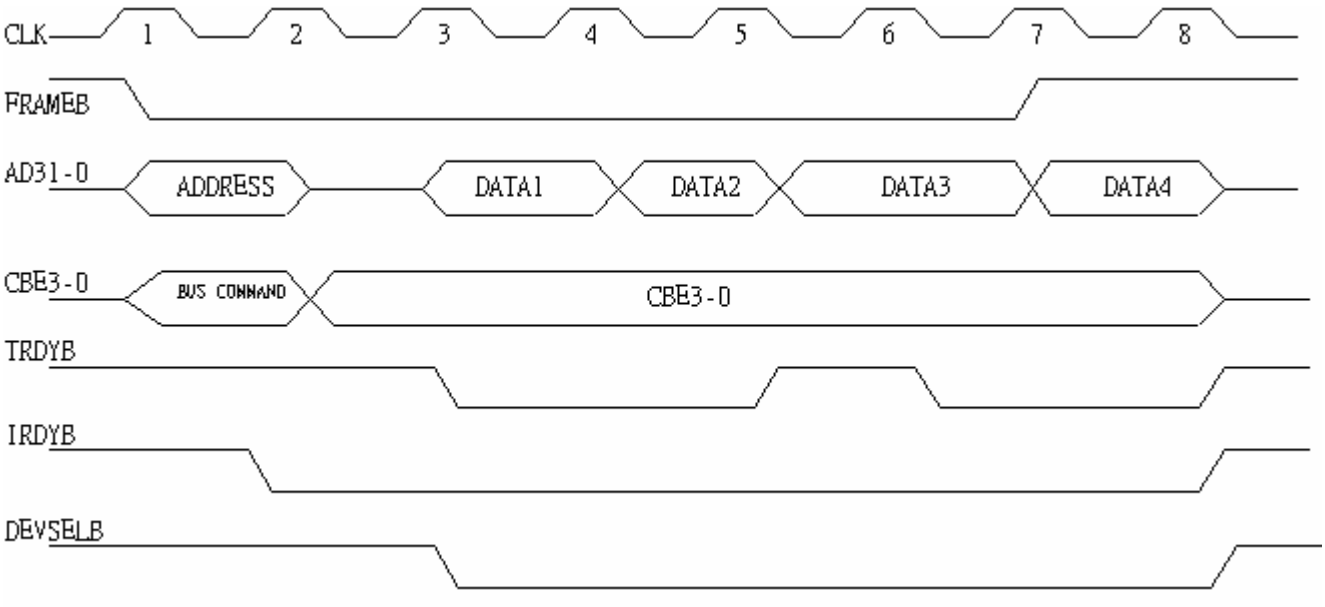


Figure 12. Memory Read

Memory Write

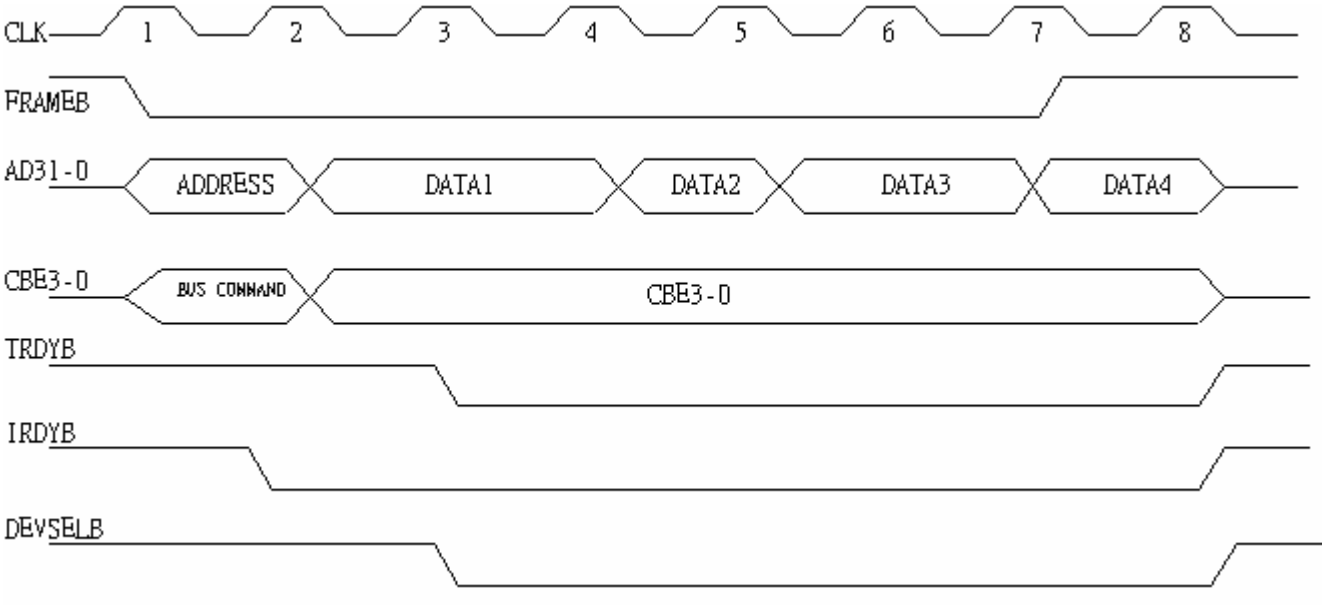


Figure 13. Memory Write

Target Initiated Termination - Retry

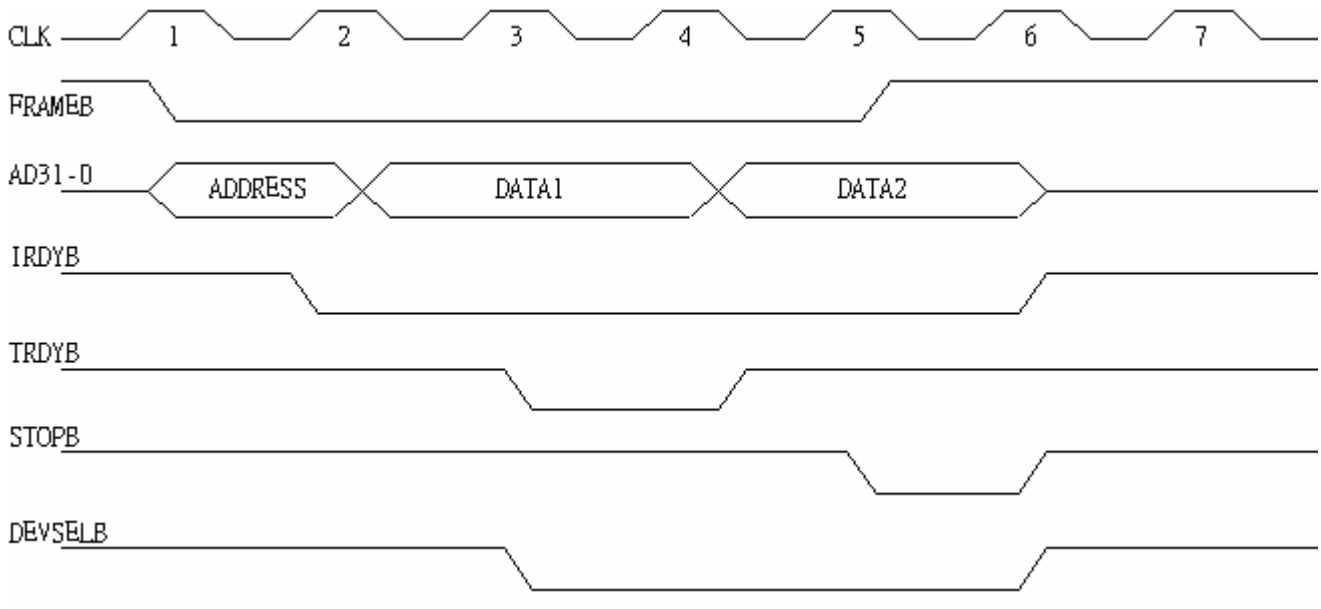


Figure 14. Target Initiated Termination - Retry

Target Initiated Termination - Disconnect

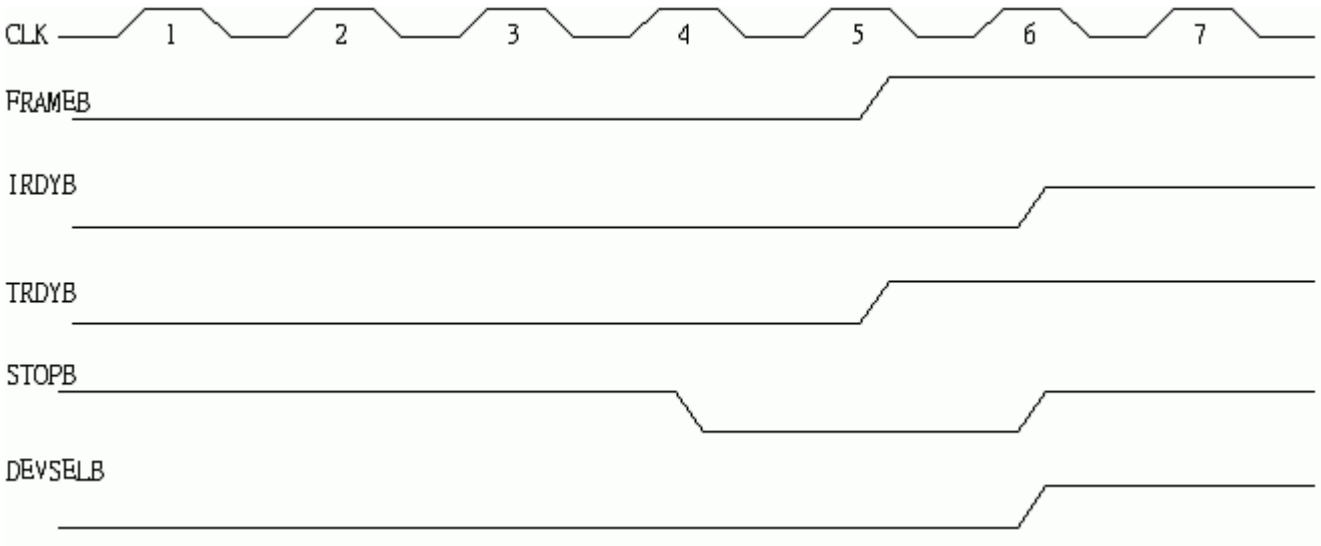


Figure 15. Target Initiated Termination - Disconnect

Target Initiated Termination - Abort

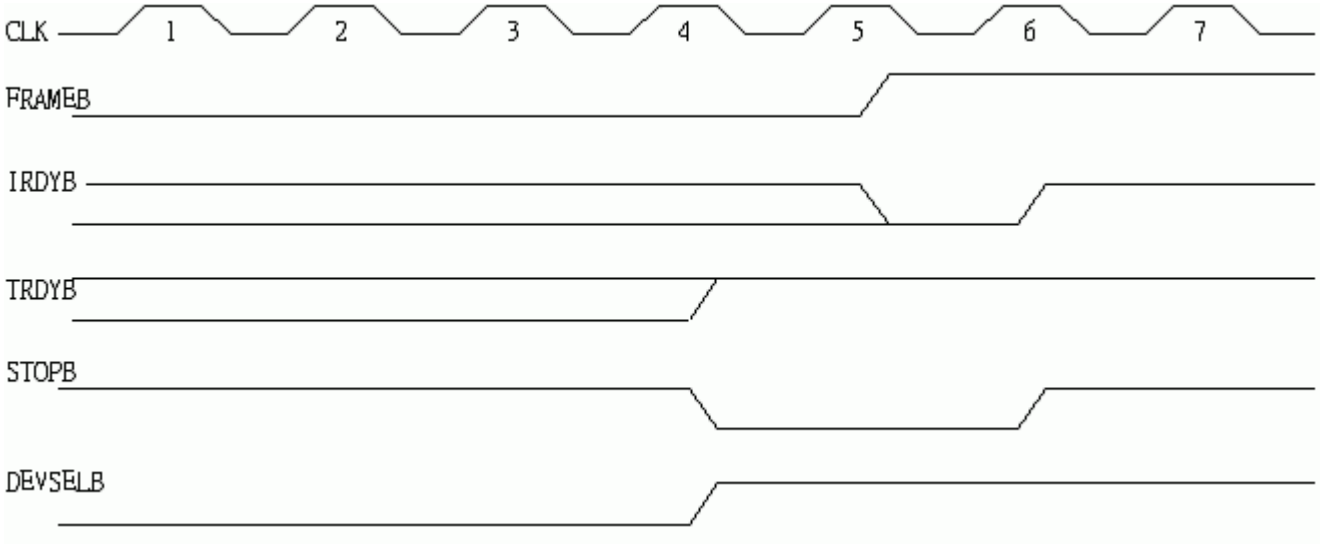


Figure 16. Target Initiated Termination - Abort

Master Initiated Termination – Abort

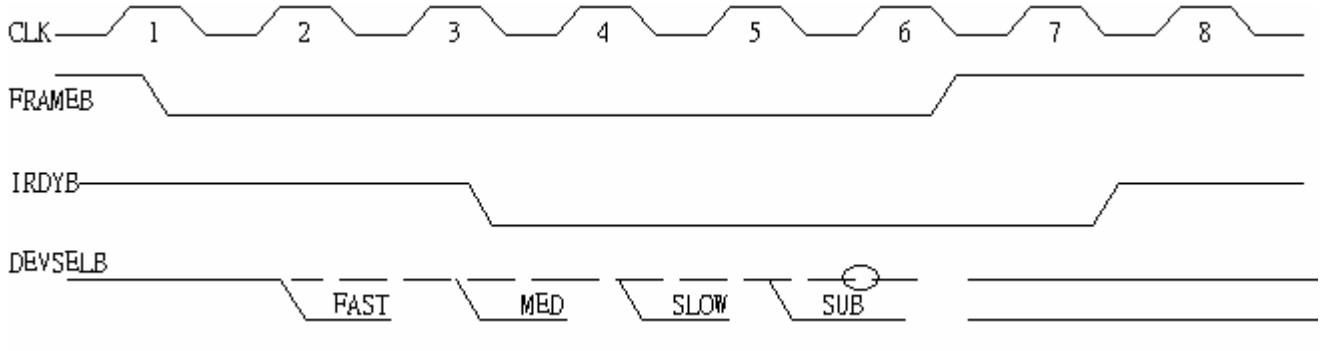


Figure 17. Master Initiated Termination – Abort

Parity Operation - One Example

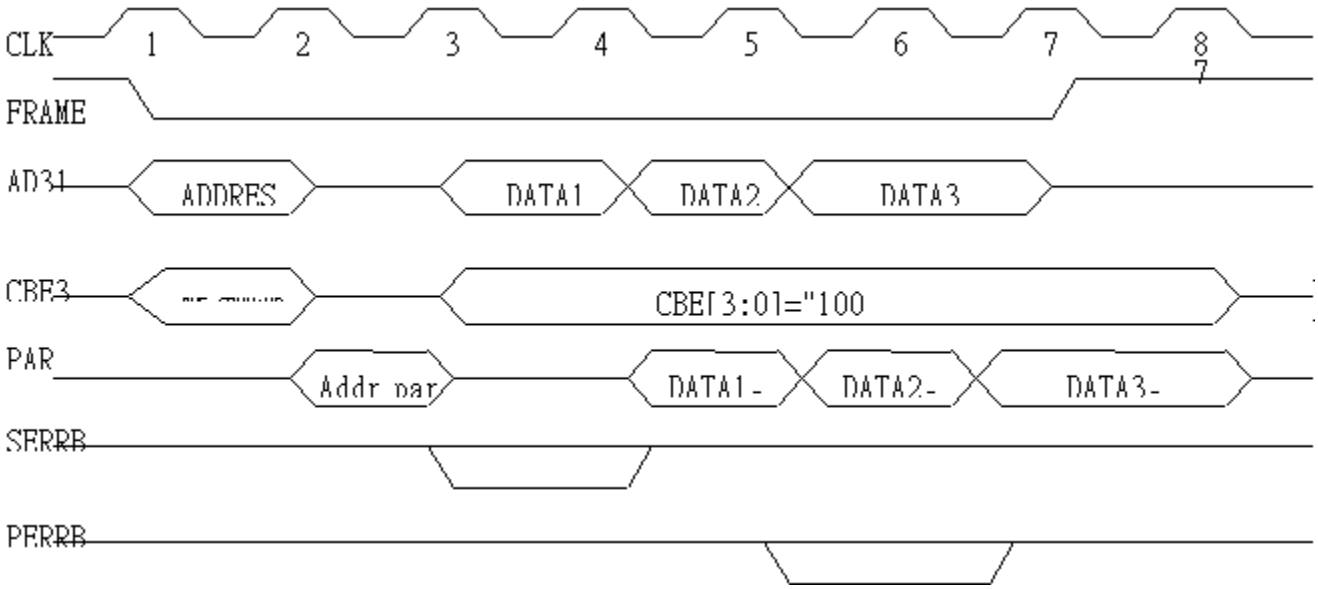
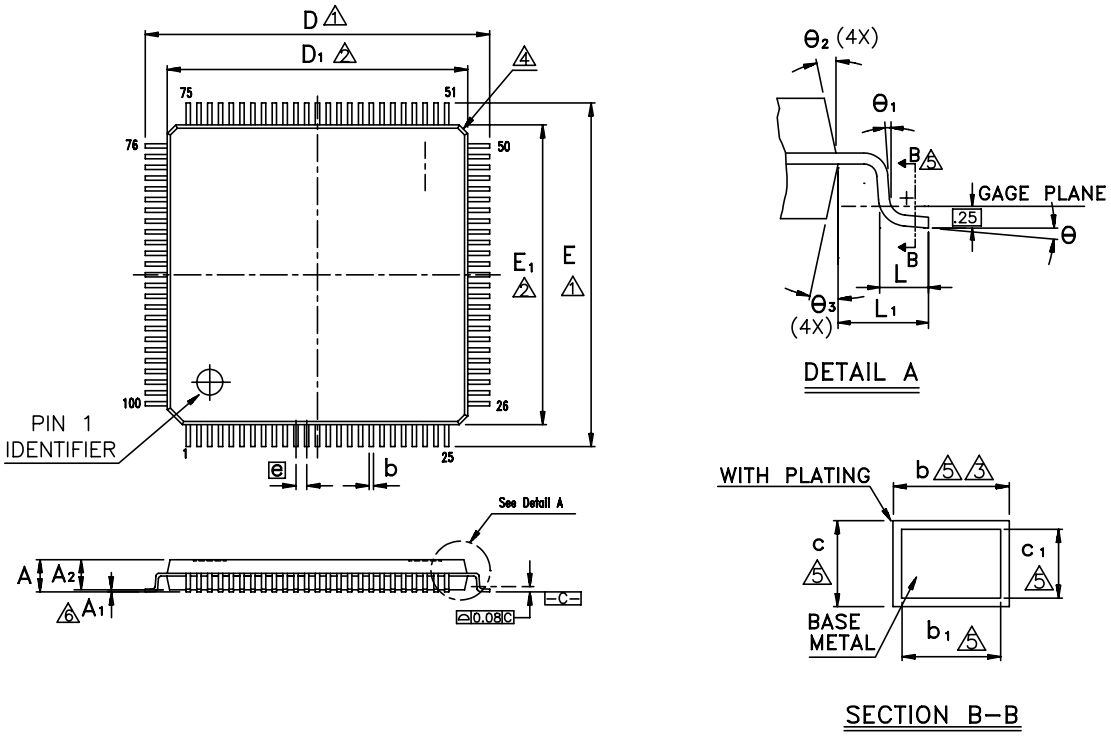


Figure 18. Parity Operation - One Example

14. Mechanical Dimensions



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.067	-	-	1.70
A1	0.000	0.004	0.008	0.00	**0.1**	0.20
A2	0.051	0.055	0.059	1.30	**1.40**	1.50
B	0.006	0.009	0.011	0.15	**0.22**	0.29
b1	0.006	0.008	0.010	0.15	**0.20**	0.25
C	0.004	-	0.008	0.09	-	0.20
c1	0.004	-	0.006	0.09	-	0.16
D	0.630 BSC			16.00 BSC		
D1	0.551 BSC			14.00 BSC		
E	0.630 BSC			16.00 BSC		
E1	0.551 BSC			14.00 BSC		
e	0.020 BSC			0.50 BSC		
L	0.016	0.024	0.031	0.40	0.60	0.80
L1	0.039 REF			1.00 REF		
θ	0°	3.5°	9°	0°	3.5°	9°
θ 1	0°	-	-	0°	-	-
θ 2	12°TYP			12°TYP		
θ 3	12°TYP			12°TYP		

Note:
1.To be determined at seating plane -c-
2.Dimensions D1 and E1 do not include mold protrusion.
D1 and E1 are maximum plastic body size dimensions

including mold mismatch.
3.Dimension b does not include dambar protrusion.
Dambar can not be located on the lower radius of the foot.
4.Exact shape of each corner is optional.
5.These dimensions apply to the flat section of the lead
between 0.10 mm and 0.25 mm from the lead tip.
6. A1 is defined as the distance from the seating plane
to the lowest point of the package body.
7.Controlling dimension: millimeter.
8. Reference document: JEDEC MS-026 , BED.

TITLE: 100LD LQFP (14x14x1.4mm) PACKAGE OUTLINE DRAWING , FOOTPRINT 2.0mm			
LEADFRAME MATERIAL:			
APPROVE		DOC. NO.	
		VERSION	1
		PAGE	OF
CHECK		DWG NO.	LQ100 - P1
		DATE	
REALTEK SEMICONDUCTOR CORP.			

15. Ordering Information

Table 75. Ordering Information

Part No.	Package	Status
RTL8101L	100-pin LQFP	MP
RTL8101L-LF	RTL8101L with Lead (Pb)-Free package	MP
RTL8101L-GR	RTL8101L with Green package	MP

Note: See page 5 for package identification.

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