DDR3 AND DDR4 SYNCHRONOUS BUCK CONTVERTER WITH 1.5A LDO

Features

Buck Controller (VDDQ)

- **High Input Voltages Range from 4.5V to 26V Input Power**
- **Provide Adjustable Output Voltage from 0.75V to 3.3V**
- **Integrated MOSFET Drivers and Bootstrap Forward P-CH MOSFET**
- **Low Quiescent Current (200uA)**
- **Excellent Load Transient Responses**
- **PFM Mode for Increased Light Load Efficiency**
- **Constant On-Time Controller Scheme**
  - Switching Frequency Compensation for PWM Mode
  - Adjustable Switching Frequency from 400kHz to 550kHz in PWM Mode with DC Output Current
- **S3 and S5 Pins Control The Device in S0, S3 or S4/S5 State**
- **Power Good Monitoring**
- **70% Under-Voltage Protection (UVP)**
- **125% Over-Voltage Protection (OVP)**
- **Adjustable Current-Limit Protection**
  - Using Sense Low-Side MOSFET's RDS(ON)
- **TQFN-32 4mmx4mm Thin package**
- **Lead Free Available (RoHS Compliant)**

±1.5A LDO Section (VTT)

- **Sourcing and Sinking Current up to 1.5A**
- **Fast Transient Response for Output Voltage**
- **Output Ceramic Capacitors Support at least 10㎷ MLCC**
- **VTT and VTTREF Track at Half the VDDQSNS by internal divider**
- **±20mV Accuracy for VTT and VTTREF**
- **Independent Over-Current Limit (OCL)**
- **Thermal Shutdown Protection**

General Description

The APW8861 integrates a synchronous buck PWM converter to generate VDDQ, a sourcing and sinking LDO linear regulator to generate VTT. It offers the lowest total solution cost in system where space is at a premium.

The APW8861 provides excellent transient response and accurate DC voltage output in either PFM or PWM Mode. In Pulse Frequency Mode (PFM), the APW8861 provides very high efficiency over light to heavy loads with loading-modulated switching frequencies. On TQFN-32 Package, the Forced PWM Mode works nearly at constant frequency for low-noise requirements.

The APW8861 is equipped with accurate current-limit, output under-voltage, and output over-voltage protections. A Power-On- Reset function monitors the voltage on VCC prevents wrong operation during power on.

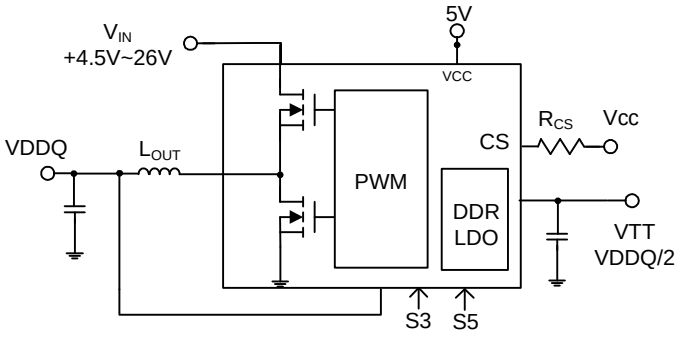
The LDO is designed to provide a regulated voltage with bi-directional output current for DDR-SDRAM termination. The device integrates two power transistors to source and sink current up to 1.5A. It also incorporates current-limit and thermal shutdown protection.

The output voltage of LDO tracks the voltage at VREF pin. An internal resistor divider is used to provide a half voltage of VREF for VTTREF and VTT Voltage. The VTT output voltage is only requiring 20μF of ceramic output capacitance for stability and fast transient response. The S3 and S5 pins provide the sleep state for VTT (S3 state) and suspend state (S4/S5 state) for device, when S5 and S3 are both pulled low the device provides the soft-off for VTT and VTTREF.

Applications

- **DDR3 and DDR4 Memory Power Supplies**
- **SSTL-2 SSTL-18 and HSTL Termination**

Simplified Application Circuit



Ordering and Marking Information

APW8861 □□ – □□□

Lead Free Code
Handling Code
Temperature Range
Package Code

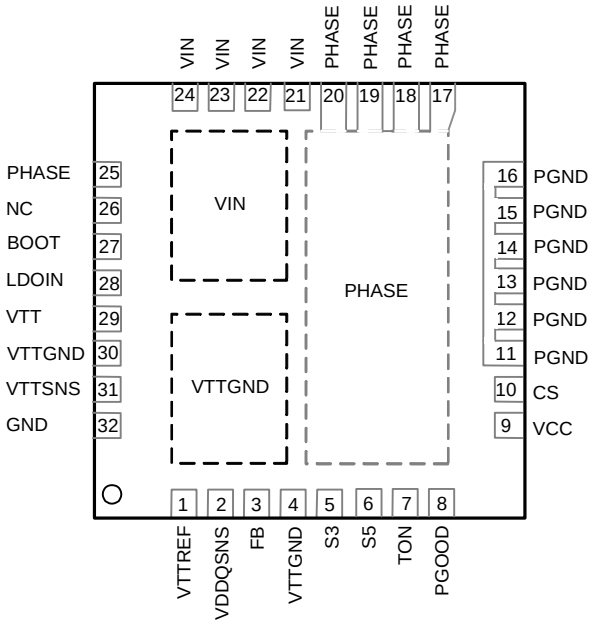
Package Code
QB : TQFN4x4-32
Operating Ambient Temperature Range
I : -40 to 85°C
Handling Code
TR : Tape & Reel
Lead Free Code
G : Halogen and Lead Free Device

APW8861 QB :

XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Pin Configuration



Absolute Maximum Ratings (Note 1.2)

Symbol	Parameter	Rating	Unit
V_{CC}	VCC Supply Voltage (VCC to GND)	-0.3 ~ 7	V
V_{BOOT}	BOOT Supply Voltage (BOOT to PHASE)	-0.3 ~ 7	V
$V_{BOOT-GND}$	BOOT Supply Voltage (BOOT to GND)	-0.3 ~ 35	V
	PHASE Voltage (PHASE to GND) <100ns pulse width >100ns pulse width	 -5 ~ 35 -0.3 ~ 28	V
	PGND, VTTGND and CS_GND to GND Voltage	-0.3 ~ 0.3	V
	All Other Pins (CS, S3, S5, VTTSNS, VDDQSNS, VLDOIN, FB, PGOOD, VTT, VTTREF GND)	-0.3 ~ 7	V
T_j	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Soldering Temperature, 10 Seconds	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Note 2: The device is ESD sensitive. Handling precautions are recommended

Thermal Characteristics(Note 3)

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Thermal Resistance -Junction to Ambient	48	°C/W
θ_{JC}	Thermal Resistance -Junction to Case	7	°C/W

Note3: θ_{JA} and θ_{JC} are measured with the component mounted on a high effective the thermal conductivity test board in free air. The exposed pad of package is soldered directly on the PCB.

Recommended Operating Conditions

Symbol	Parameter	Range	Unit
V_{CC}	VCC Supply Voltage	4.5 ~ 5.5	V
V_{IN}	Converter Input Voltage	4.5 ~ 26	V
V_{VDDQ}	Converter Output Voltage	0.75 ~3.3V	V
V_{VTT}	LDO Output Voltage	0.375 ~ 1.65	V
I_{OUT}	Converter Output Current	0 ~ 8	A
I_{VTT}	LDO Output Current	-1.5 ~ +1.5	A
C_{VCC}	VCC Capacitance	1~	µF
C_{VTT}	VTT Output Capacitance	20~50	µF
C_{VTTREF}	VTTREF Output Capacitance	0.033~0.1	µF
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Electrical Characteristics

Refer to the typical application circuits. These specifications apply over V_{VCC}=V_{BOOT}=5V, V_{IN}=12V and T_A= -40 ~ 85°C, unless otherwise specified. Typical values are at TA=25°C.

Symbol	Parameter	Test Conditions		APW8861			Unit
				Min	Typ	Max	
SUPPLY CURRENT							
I_{VCC}	VCC Supply Current	T_A = 25°C, V_{S3} = V_{S5} = 5V, no load, VCC Current		-	160	280	µA
I_{VCCSTB}	VCC Standby Current	T_A = 25°C, V_{S3} = 0V, V_{S5} = 5V, no load, VCC Current		-	120	175	µA
I_{VCCSDN}	VCC Shutdown Current	T_A =25°C, V_{S3} = V_{S5} = 0V, no load		-	0.1	1	µA
I_{LDOIN}	LDOIN Supply Current	T_A = 25°C, V_{S3} = V_{S5} = 5V, no load		-	1	10	µA
$I_{LDOINSTB}$	LDOIN Standby Current	T_A = 25°C, V_{S3} = 0V, V_{S5} = 5V, no load,		-	0.1	10	
$I_{LDOINSDN}$	LDOIN Shutdown Current	T_A = 25°C, V_{S3} = V_{S5} = 0V, no load		-	0.1	1	
POWER-ON-RESET							
	VCC POR Threshold	VCC Rising		3.95	4.1	4.4	V
	VCC POR Hysteresis			-	0.1	-	V
VTT OUTPUT							
V_{VTT}	VTT Output Voltage	V_{LDOIN} = $V_{VDDQSNS}$ = 1.5V		-	0.75		V
		V_{LDOIN} = $V_{VDDQSNS}$ = 1.35V		-	0.675	-	
		V_{LDOIN} = $V_{VDDQSNS}$ = 1.2V		-	0.6	-	
V_{VTT}	VTT Output Tolerance	V_{LDOIN} = $V_{VDDQSNS}$ = 1.5V, $V_{VDDQSNS}$/2 - V_{VTT}, I_{VTT} = 0A		-20	-	20	mV
		V_{LDOIN} = $V_{VDDQSNS}$ = 1.5V, $V_{VDDQSNS}$/2 - V_{VTT}, I_{VTT} = 1A		-30	-	30	
		V_{LDOIN} = $V_{VDDQSNS}$ = 1.35V, $V_{VDDQSNS}$/2 - V_{VTT}, I_{VTT} = 0A		-20	-	20	
		V_{LDOIN} = $V_{VDDQSNS}$ = 1.35V, $V_{VDDQSNS}$/2 - V_{VTT}, I_{VTT} = 1A		-30	-	30	
		V_{LDOIN} = $V_{VDDQSNS}$ = 1.2V, $V_{VDDQSNS}$/2 - V_{VTT}, I_{VTT} = 0A		-20	-	20	
		V_{LDOIN} = $V_{VDDQSNS}$ = 1.2V, $V_{VDDQSNS}$/2 - V_{VTT}, I_{VTT} = 1A		-30	-	30	
T_{SSVTT}	VTT Soft Start time	S3 is go high to 0.95*VTT Regulation		25	30	35	us
I_{LIM}	Current-Limit	Sourcing Current (V_{LDOIN}=1.5V)	T_J=25°C	1.5	1.8	2.6	A
			T_J=125°C	1.1	-	-	
		Sinking Current (V_{LDOIN}=1.5V)	T_J=25°C	-1.6	-1.8	-2.6	
			T_J=125°C	-1.1	-	-	
		Sourcing Current (V_{LDOIN}=1.35V)	T_J=25°C	1.35	1.8	2.6	
			T_J=125°C	1.1	-	-	
		Sinking Current (V_{LDOIN}=1.35V)	T_J=25°C	-1.45	-1.8	-2.6	
			T_J=125°C	-1.1	-	-	

Electrical Characteristics

Refer to the typical application circuits. These specifications apply over V_{VCC}=V_{BOOT}=5V, V_{IN}=12V and T_A= -40 ~ 85°C, unless otherwise specified. Typical values are at TA=25°C.

Symbol	Parameter	Test Conditions		APW8861			Unit
				Min	Typ	Max	
VTT OUTPUT							
I_{LIM}	Current-Limit	Sourcing Current (V_{LDOIN}=1.2V)	T_J=25°C	1.15	1.8	2.6	A
			T_J=125°C	1.1	-	-	
		Sinking Current (V_{LDOIN}=1.2V)	T_J=25°C	-1.3	-1.8	-2.6	
			T_J=125°C	-1.1	-	-	
$R_{DS(ON)}$	VTT Power MOSFETs $R_{DS(ON)}$	Upper MOSFET		-	350	500	mΩ
		Lower MOSFET		-	350	500	
I_{VTTLK}	VTT Leakage Current	V_{VTT} = 1.25V, V_{S3} = 0V, V_{S5} = 5V, T_A = 25°C		-1.0	-	1.0	µA
$I_{VTTSNSLK}$	VTTSNS Leakage Current	V_{VTT} = 1.25V, T_A = 25°C		-1.00	0.01	1.00	µA
I_{VTTDIS}	VTT Discharge Current	V_{VTT} = 0.5V, V_{S3} = V_{S5} = 0V, T_A = 25°C V_{VREF} = 0V		15	25	-	mA
VTTREF OUTPUT							
V_{VTTREF}	VTTREF Output Voltage	V_{LDOIN} = $V_{VDDQSNS}$ = 1.5V, $V_{VDDQSNS}$/2		-	0.75	-	V
		V_{LDOIN} = $V_{VDDQSNS}$ = 1.35V, $V_{VDDQSNS}$/2		-	0.675	-	
		V_{LDOIN} = $V_{VDDQSNS}$ = 1.2V, $V_{VDDQSNS}$/2		-	0.6	-	
	VTTREF Tolerance	-10mA < I_{VTTREF} < 10mA, $V_{VDDQSNS}$/2 - V_{VTTREF} V_{LDOIN} = V_{VTTREF} =1.5V		--20	-	20	mV
		-10mA < I_{VTTREF} < 10mA, $V_{VDDQSNS}$/2 - V_{VTTREF} V_{LDOIN} = $V_{VDDQSNS}$ = 1.35V		-20	-	20	
		-10mA < I_{VTTREF} < 10mA, $V_{VDDQSNS}$/2 - V_{VTTREF} V_{LDOIN} = $V_{VDDQSNS}$ = 1.2V		-20	-	20	
I_{VTTREF}	VTTREF Source Current	V_{VTTREF} = 0V		-10	-20	-50	mA
I_{VTTREF}	VTTREF Sink Current	V_{VTTREF} = 1.5V		10	20	60	mA
VDDQ OUTPUT							
V_{FB}	FB Regulation Voltage	T_A = 25°C		0.745	0.75	0.757	V
		T_A = -40°C to 85°C		0.7425	0.75	0.7595	V
		T_A = 25°C, V_{VCC} = 4.5V to 5.5V, V_{IN} = 3V to 28V		-0.1	-	+0.1	%
		T_A = 25°C, Load = 0 to 10A, V_{VCC} = 4.5V to 5.5V		-1	-	+1	%
	FB Input Current	V_{FB}= 0.78V		-0.1		+0.1	µA
	VDDQ Discharge Current	V_{S3} = V_{S5} = 0V, $V_{VDDQSNS}$ = 0.5V,		15	25	-	mA

Electrical Characteristics

Refer to the typical application circuits. These specifications apply over V_{VCC}=V_{BOOT}=5V, V_{IN}=12V and T_A= -40 ~ 85°C, unless otherwise specified. Typical values are at TA=25°C.

Symbol	Parameter	Test Conditions	APW8861			Unit
			Min	Typ	Max	
PWM CONTROLLERS						
F_{SW}	Operating Frequency	Adjustable Frequency	400	-	550	KHz
T_{SS}	Internal Soft Start Time	S5 is High to 0.9*V_{OUT} Regulation	0.77	1.1	1.4	ms
T_{ONF}	Fast on time	V_{PHASE} =19V, V_{OUT}=1.5V, R_{TON} =620KΩ	175	205	235	ns
$T_{OFF(MIN)}$	Minimum off time		-	300	-	ns
$T_{ON(MIN)}$	Slow on time		80	110	140	ns
	Zero-Crossing Threshold		-9.5	0.5	10.5	mV
VDDQ PROTECTIONS						
	CS Pin Sink Current	T_A = 25°C	15	16	17	µA
		Temperature Coefficient, On The Basis of 25°C	-	4500	-	ppm/°C
	OCP Comparator Offset	(V_{VCC} – V_{CS}) – (V_{PHASE} – PGND), V_{VCC} – V_{CS} = 60mV	-18	0	+18	mV
	VDDQ Current Limit Setting Range	V_{VCC}-V_{CS}	30	-	200	mV
VDDQ PROTECTIONS						
	VDDQ OVP Trip Threshold	V_{VDDQ} Rising	120	125	130	%
	VDDQ OVP Debounce Delay	V_{FB} Rising, DV=10mV	-	1.5	-	µs
	VDDQ UVP Trip Threshold	V_{VDDQ} Falling	60	70	80	%
	VDDQ UVP Debounce		-	10	-	µs
PGOOD						
V_{PGOOD}	PGOOD Threshold	PGOOD in from Lower (PGOOD Goes High)	87	90	93	%
		PGOOD in from Higher (PGOOD Goes High)	120	125	130	%
I_{PGOOD}	PGOOD Leakage Current	V_{PGOOD}=5V	-	0.1	1.0	µA
	PGOOD Sink Current	V_{PGOOD}=0.3V	2.5	7.5	-	mA
	PGOOD Debounce Time		-	63	-	µs
T_{SSPOK}	POK Soft Start time	S5 is High to POK Ready	1.4	2	2.6	ms
GATE DRIVERS						
$R_{ON(H)}$	High Side N-MOSFET $R_{DS(ON)}$		-	15	17	mΩ
$R_{ON(L)}$	Low Side N-MOSFET $R_{DS(ON)}$		-	8	11	mΩ
T_D	Dead Time	(Note 4)	-	20	-	ns

Electrical Characteristics

Refer to the typical application circuits. These specifications apply over V_{VCC}=V_{BOOT}=5V, V_{IN}=12V and T_A= -40 ~ 85°C, unless otherwise specified. Typical values are at TA=25°C.

Symbol	Parameter	Test Conditions	APW8861			Unit
			Min	Typ	Max	
BOOTSTRAP DIODE						
	Forward Voltage	V_{VCC} – V_{BOOT}, I_F = 10mA, T_A = 25°C	-	0.3	0.5	V
	Reverse Leakage	V_{BOOT} = 30V, V_{PHASE} = 25V, V_{VCC}=5V, T_A = 25°C	-	-	0.5	µA
LOGIC THRESHOLD						
V_{IH}	S3, S5 High Threshold Voltage	S3, S5 Rising	2	-	-	V
V_{IL}	S3, S5 Low Threshold Voltage	S3, S5 Falling	-	-	0.8	V
I_{ILEAK}	Logic Input Leakage Current	V_{S3} = V_{S5} = 5V, T_A =25°C	-1	-	1	µA
THERMAL SHUTDOWN						
TSD	Thermal Shutdown Temperature	T_J Rising	-	160	-	°C
	Thermal Shutdown Hysteresis		-	25	-	°C

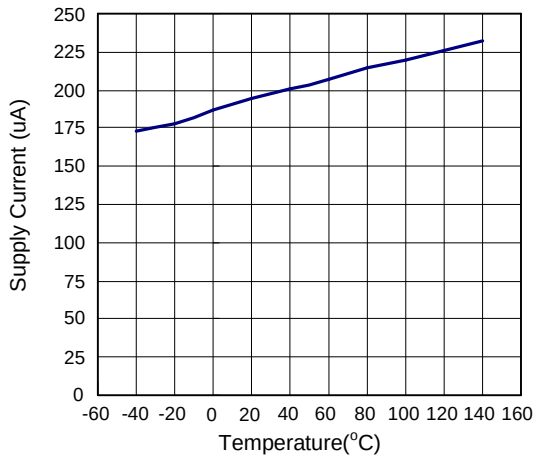
Note 4: Guaranteed by design.

Pin Description

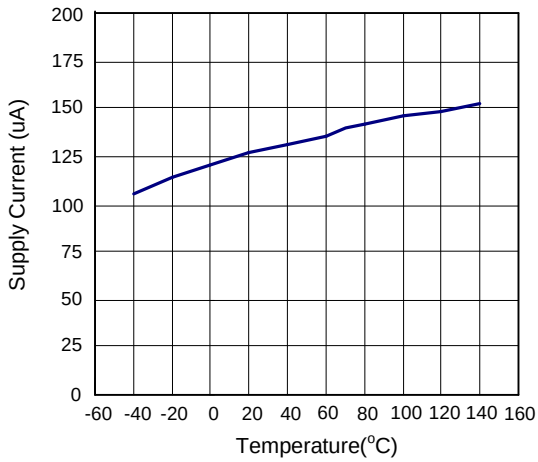
NO.	NAME	FUNCTION
1	VTTREF	VTTREF buffered reference output.
2	VDDQSNS	VDDQ reference input for VTT and VTTREF. Power supply for the VTTREF. Discharge current sinking terminal for VDDQ non-tracking discharge.
3	FB	VDDQ output voltage setting pin.
4	VTTGND	Power ground output for the VTT LDO.
5	S3	S3 signal input.
6	S5	S5 signal input.
7	TON	This Pin is Allowed to Adjust The Switching Frequency. Connect a resistor R_{TON} = 100KΩ ~ 600KΩ from TON pin to PHASE pin.
8	PGOOD	Power-good output pin. PGOOD is an open drain output used to Indicate the status of the output voltage. When VDDQ output voltage is within the target range, it is in high state.
9	VCC	5V power supply voltage input pin for both internal control circuitry and low-side MOSFET gate driver.
10	CS	Over-current trip voltage setting input for $R_{DS(ON)}$ current sense scheme if connected to VCC through the voltage setting resistor.
11~16	PGND	Power ground of the low-side MOSFET driver. Connect the pin to the Source of the low-side MOSFET.
17~20, 25	PHASE	Junction point of the high-side MOSFET Source, output filter inductor and the low-side MOSFET Drain. Connect this pin to the Source of the high-side MOSFET. PHASE serves as the lower supply rail for the high-side gate driver.
21~24	VIN	The pin is supply input, its supplies current to VDDQSNS.
26	NC	-
27	BOOT	Supply Input for the High-Side Gate Driver and an internal level-shift circuit. Connect to an external capacitor and diode to create a boosted voltage suitable to drive a logic-level N-channel MOSFET.
28	LDOIN	Supply voltage input for the VTT LDO.
29	VTT	Power output for the VTT LDO.
30	VTTGND	Power ground output for the VTT LDO.
31	VTTSNS	Voltage sense input for the VTT LDO. Connect to plus terminal of the VTT LDO output capacitor.
32	GND	Signal Ground.

Typical Operating Characteristics

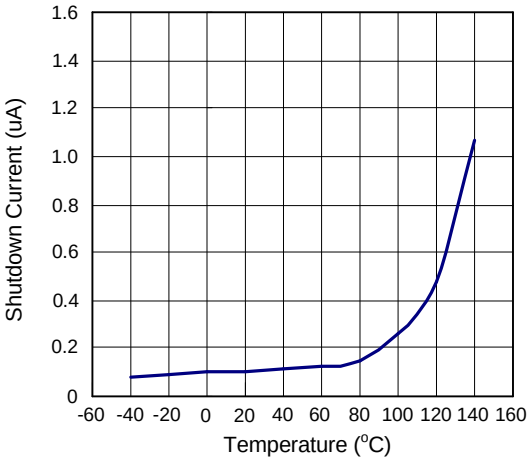
Supply Current In S0 VS Temperature



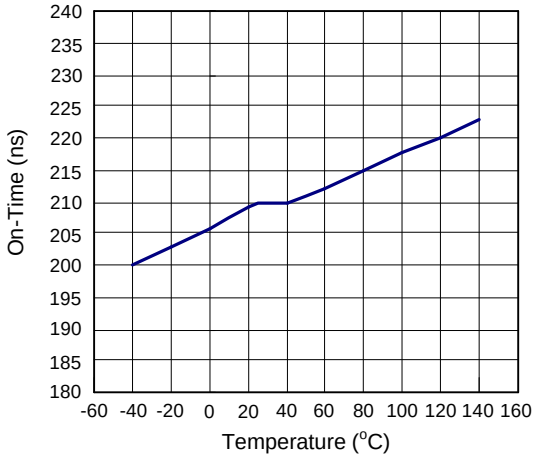
Supply Current In S3 VS Temperature



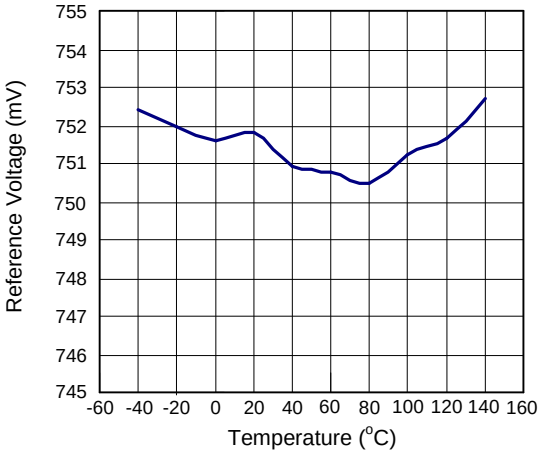
Shutdown Current VS Temperature



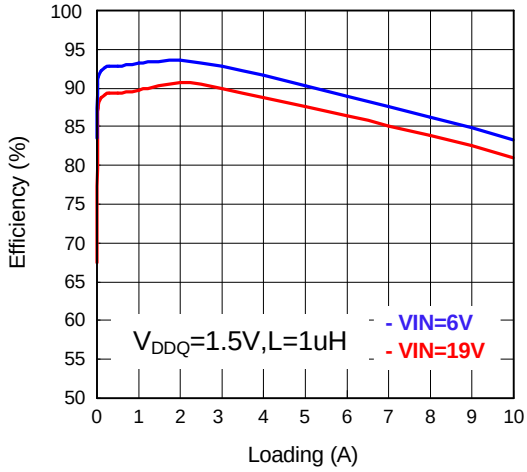
On-Time VS Temperature



Reference Voltage VS Temperature

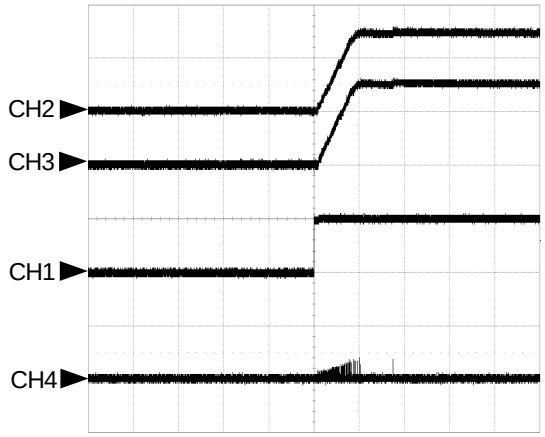


Efficiency VS Loading



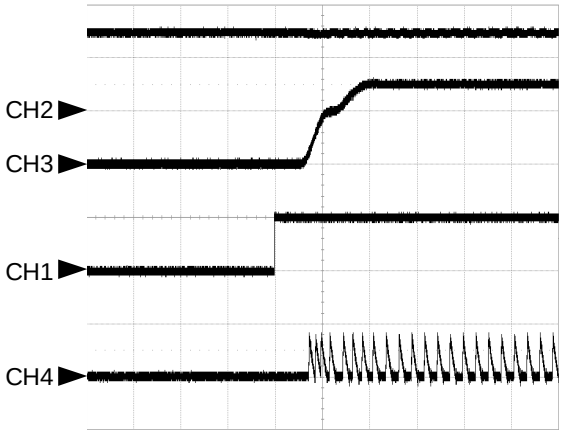
Operating Waveforms

Enable VCC - No Load



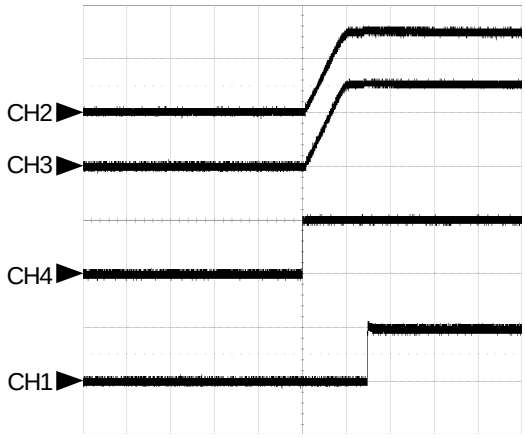
CH1:V_{CC}-5V/div
CH2:V_{DDQ}-1V/div
CH3:V_{TT}-500mV/div
CH4:I_L-10A/div
Time:1ms/div

Enable S3 – No Load



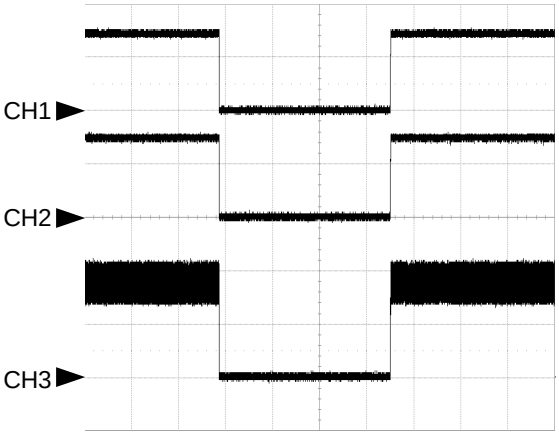
CH1:V_{S3}-5V/div
CH2:V_{DDQ}-1V/div
CH3:V_{TT}-500mV/div
CH4:I_L-5A/div
Time:20us/div

POK- Enable S3/S5



CH1:POK-5V/div
CH2:V_{DDQ}-1V/div
CH3:V_{TT}-500mV/div
CH4:$V_{S3/S5}$-5V/div
Time:1ms/div

OTP



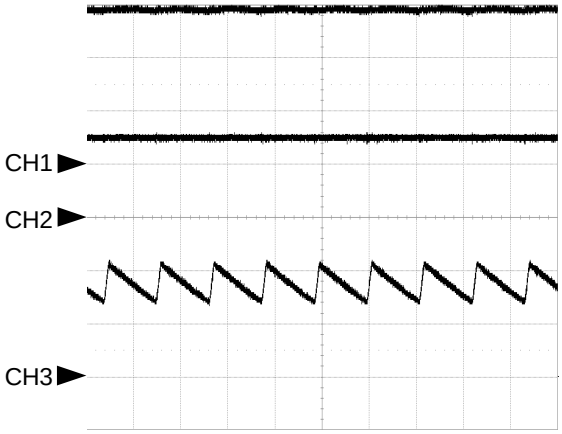
CH1:V_{DDQ}-1V/div
CH2:V_{TT}-500mV/div
CH3:I_L-5A/div
Time:200ms/div

Operating Waveforms (Cont.)

UVP

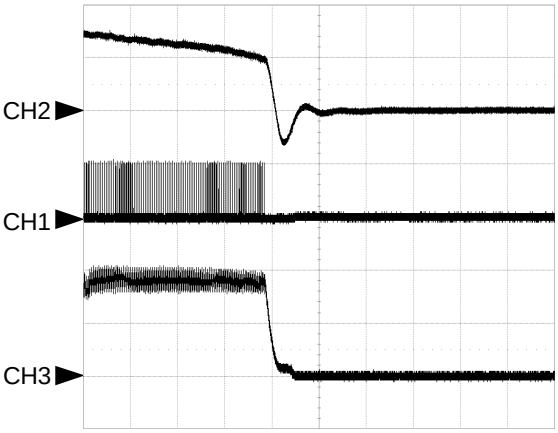
CH1:POK-5V/div
CH2:V_{DDQ}-1V/div
CH3:V_{TT}-500mV/div
CH4:I_L-10A/div
Time:50us/div

Normal Operaion



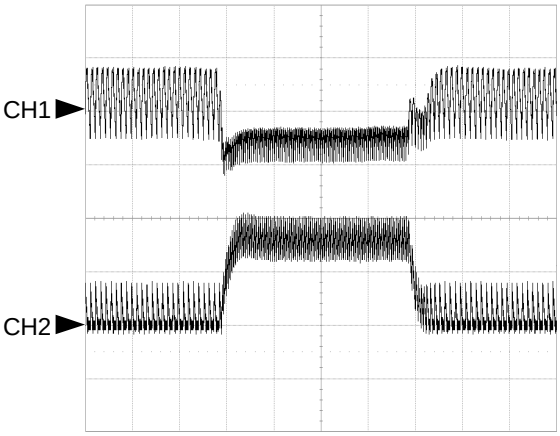
CH1:V_{DDQ}-500mV/div
CH2:V_{TT}-500mV/div
CH3:I_L-5A/div
Time:2us/div

OCP



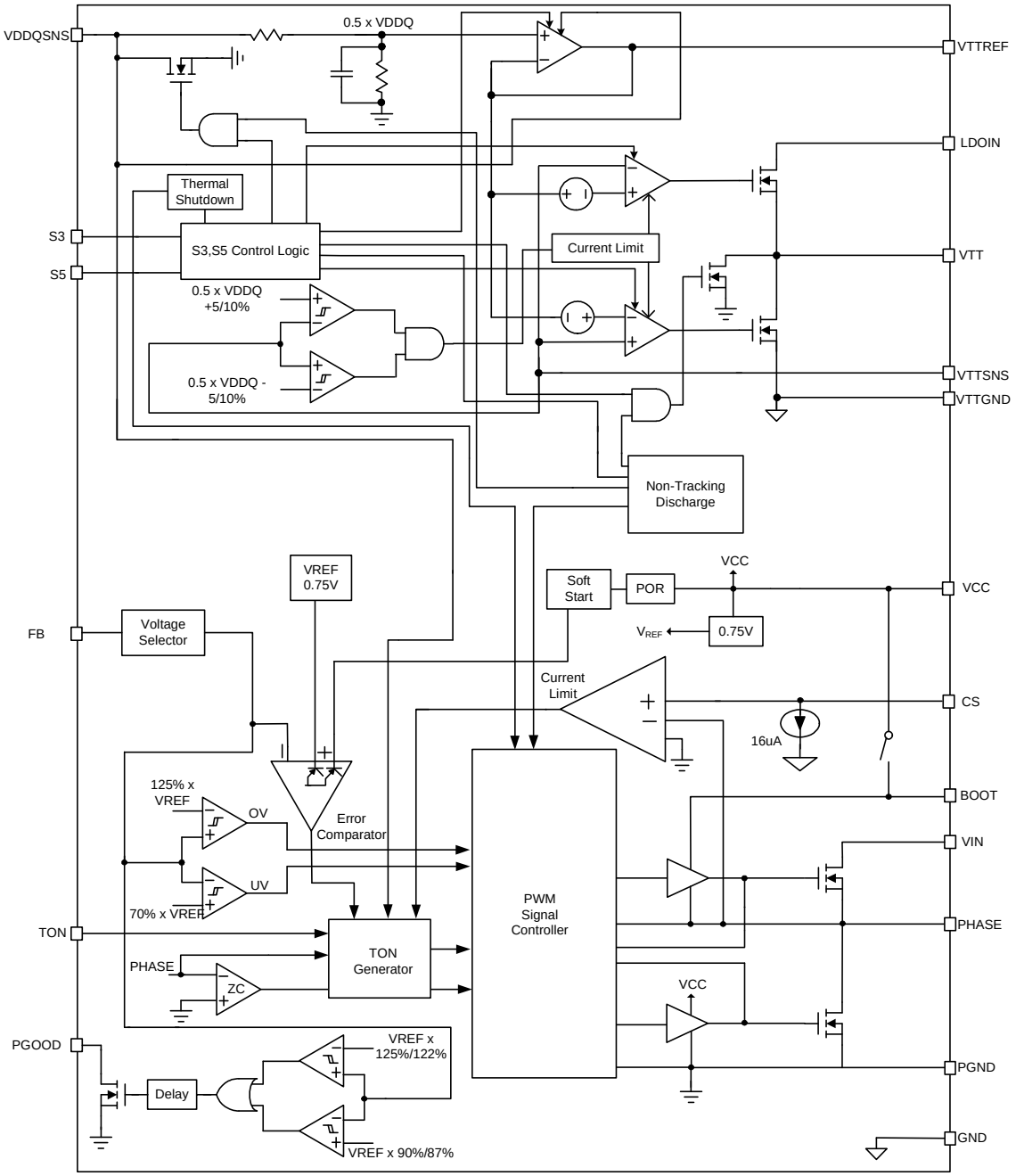
CH1:Phase-20V/div
CH2:V_{DDQ}-1V/div
CH3:I_L-10A/div
Time:50us/div

Load Transient-Load=0.8A<-->8A

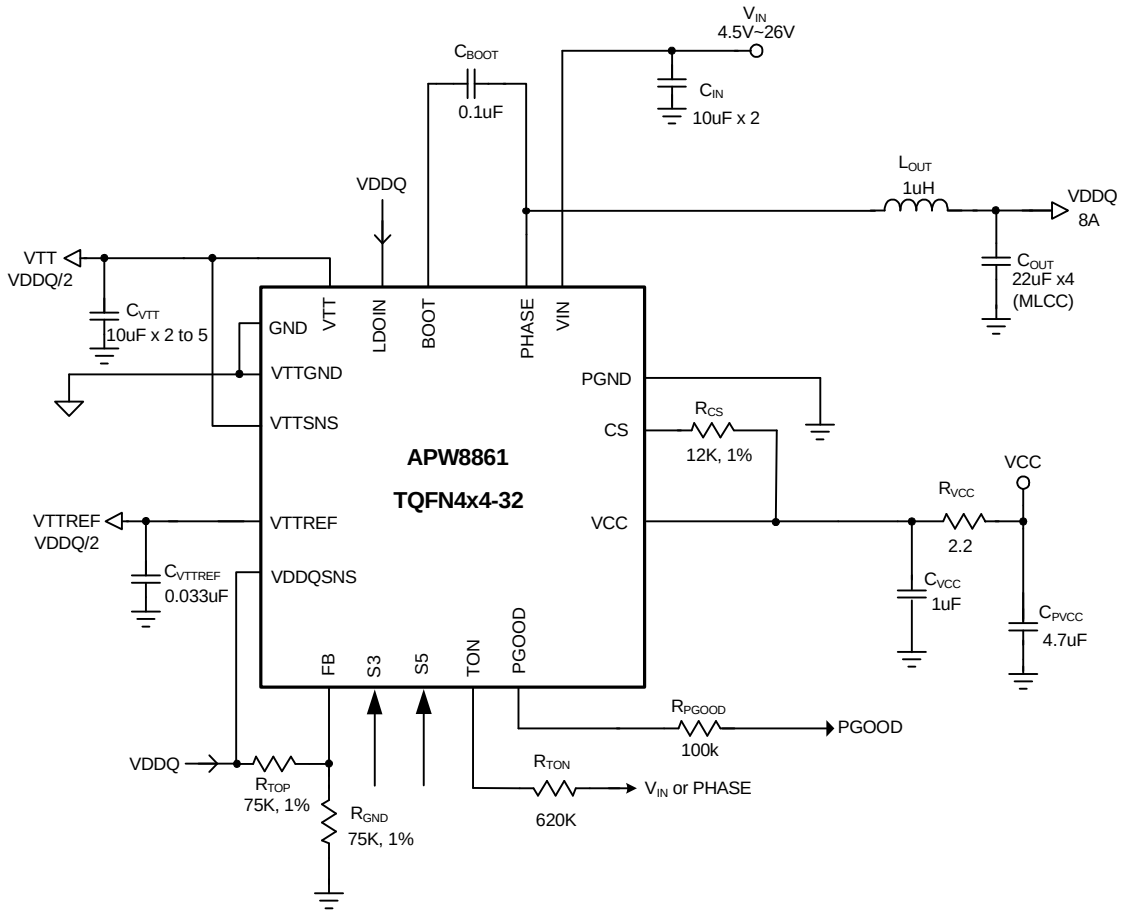


CH1:V_{DDQ}-50mV/div
CH2:I_L-5A/div
Time:50us/div

Block Diagram



Typical Application Circuit



Note 5: The VTT output ceramic capacitors is just recommend.

Adjustable Output Voltage Regulator for VDDQ

Function Description

The APW8861 integrates a synchronous buck PWM controller to generate VDDQ, a sourcing and sinking LDO linear regulator to generate VTT. It provides a complete power supply for DDR3 and DDR4 memory system in a 32-pin TQFN package. User defined output voltage is also possible and can be adjustable from 0.75V to 3.3V. Input voltage range of the PWM converter is 4.5V to 26V. The converter runs an adaptive on-time PWM operation at high-load condition and automatically reduces frequency to keep excellent efficiency down to several mA. The VTT LDO can source and sink up to 1.5A peak current with only 10µF ceramic output capacitor. VTTREF tracks VDDQ/2 within 1% of VDDQ. VTT output tracks VTTREF within 20 mV at no load condition while 40 mV at full load. The LDO input can be separated from VDDQ and optionally connected to a lower voltage by using VLDOIN pin. This helps reducing power dissipation in sourcing phase. The APW8861 is fully compatible to JEDEC DDR3/DDR4 specifications at S3/S5 sleep state (see Table 1). When both VTT and VDDQ are disabled, the non-tracking discharge mode discharges outputs using internal discharge MOSFETs that are connected to VDDQSNS and VTT.

Constant-On-Time PWM Controller with Input Feed-Forward

The constant on-time control architecture is a pseudo-fixed frequency with input voltage feed-forward. This architecture relies on the output filter capacitor's effective series resistance (ESR) to act as a current-sense resistor, so the output ripple voltage provides the PWM ramp signal. In PFM operation, the high-side switch on-time controlled by the on-time generator is determined solely by a one-shot whose pulse width is inversely proportional to input voltage and directly proportional to output voltage. In PWM operation, the high-side switch on-time is determined by a switching frequency control circuit in the on-time generator block. The switching frequency control circuit senses the switching frequency of the high-side switch and keeps regulating it at a constant frequency in PWM mode. The design improves the frequency variation and be more outstanding than a conventional constant on-time controller which has large switching frequency variation over input voltage, output current and temperature. Both in PFM and PWM, the on-time generator, which senses input voltage on PHASE pin, provides very fast on-time response to input line transients.

Another one-shot sets a minimum off-time (typical: 300ns). The on-time one-shot is triggered if the error comparator is high, the low-side switch current is below the current-limit threshold, and the minimum off-time one-shot has timed out.

Power-On-Reset

A Power-On-Reset (POR) function is designed to prevent wrong logic controls when the VCC voltage is low. The POR function continually monitors the bias supply voltage on the VCC pin if at least one of the enable pins is set high. When the rising VCC voltage reaches the rising POR voltage threshold (4.1V typical), the POR signal goes high and the chip initiates soft-start operations. Should this voltage drop lower than 4V (typical), the POR disables the chip.

Soft- Start

The APW8861 integrates digital soft-start circuits to ramp up the output voltage of the converter to the programmed regulation set point at a predictable slew rate. The slew rate of output voltage is internally controlled to limit the inrush current through the output capacitors during softstart process. In addition, the VTT LDO provides a softstart function, using the current limit method to charge the output capacitor that gives a rapid output voltage rise. The figure 1 shows VDDQ soft-start sequence. When the S5 pin is pulled above the rising S5 threshold voltage, the device initiates a soft-start process to ramp up the output voltage. The soft-start interval is 1.2ms (typical) and independent of the PHASE switching frequency.

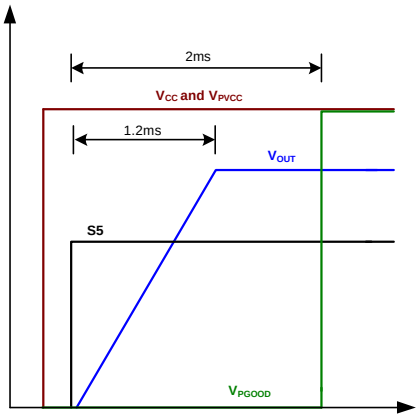


Figure 1. Soft-Start Sequence.

Function Description (Cont.)

During soft-start stage before the PGOOD pin is ready, the under voltage protection is prohibited. The over voltage and current limit protection functions are enabled. If the output capacitor has residue voltage before startup, both low-side and high-side MOSFETs are in off-state until the internal digital soft start voltage equal the internal feedback voltage. This will ensure the output voltage starts from its existing voltage level.

The VTT LDO part monitors the output current, both sourcing and sinking current, and limits the maximum output current to prevent damages during current overload or short circuit (shorted from VTT to GND or VLDOIN) conditions.

The VTT LDO provides a soft-start function, using the constant current to charge the output capacitor that gives a rapid and linear output voltage rise. If the load current is above the current limit start-up, the VTT cannot start successfully.

APW8861 has an independent counter for each output, but the PGOOD signal indicates only the status of VDDQ and does not indicate VTT power good externally.

Power-Good Output (PGOOD)

PGOOD is an open-drain output and the PGOOD comparator continuously monitors the output voltage. PGOOD is actively held low in shutdown, and standby. When PWM converter's output voltage is greater than 95% of its target value, the internal open-drain device will be pulled low. After 63µs debounce time, the PGOOD goes high. The PGOOD goes low if V_{VDDQ} output is 10% below or above its nominal regulation point.

Under Voltage Protection

In the process of operation, if a short-circuit occurs, the output voltage will drop quickly. When load current is bigger than current limit threshold value, the output voltage will fall out of the required regulation range. The under-voltage continually monitors the setting output voltage after 2ms of PWM operations to ensure startup. If a load step is strong enough to pull the output voltage lower than the under voltage threshold (70% of normal output voltage), APW8861 shuts down the output gradually and latches off both high and low side MOSFETs.

Over Voltage Protection (OVP)

The feedback voltage should increase over 125% of the reference voltage due to the high-side MOSFET failure or for other reasons, and the over voltage protection comparator designed with a 1.5ms noise filter will force the low-side MOSFET gate driver to be high. This action actively pulls down the output voltage and eventually attempts to blow the battery fuse.

When the OVP occurs, the PGOOD pin will pull down and latch-off the converter. This OVP scheme only clamps the voltage overshoot, and does not invert the output voltage when otherwise activated with a continuously high output from low-side MOSFET driver. It's a common problem for OVP schemes with a latch. Once an over-voltage fault condition is set, toggling VCC power-on-reset signal can only reset it.

PWM Converter Current Limit

The current-limit circuit employs a unique "valley" current sensing algorithm (Figure 2). CS pin should be connected to VCC through the trip voltage-setting resistor, R_{CS}. CS terminal sinks 16µA current, I_{CS}, and the current limit threshold is set to the voltage across the R_{CS}. The voltage between or CS_GND pin and PHASE pin monitors the inductor current so that PHASE pin should be connected to the drain terminal of the low side MOSFET. PGND is used as the positive current sensing node so that PGND should be connected to the proper current sensing device, i.e. the sense resistor or the source terminal of the low side MOSFET.

If the magnitude of the current-sense signal is above the current-limit threshold, the PWM is not allowed to initiate a new cycle. The actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current- limit characteristic and maximum load capability are a function of the sense resistance, inductor value, and input voltage. The equation for the current limit threshold is as follows:

$$I_{LIMIT} = \frac{R_{CS} \times 16\mu A}{R_{DS(ON)}} + \frac{(V_{IN} - V_{VDDQ})}{2 \times L \times f_{SW}} \times \frac{V_{VDDQ}}{V_{IN}}$$

Function Description (Cont.)

Where ILIMIT is the desired current limit threshold, R_{CS} is the value of the current sense resistor connected to CS and VCC pins V_{CS} is the voltage across the R_{CS} resistor I_{RIPPLE} is inductor peak to peak current F_{SW} is the PWM switching frequency

In a current limit condition, the current to the load exceeds the current to the output capacitor thus the output voltage tends to fall down. If the output voltage becomes less than power good level, the V_{CS} is cut into half and the output voltage tends to be even lower. Eventually, it crosses the under voltage protection threshold and shutdown.

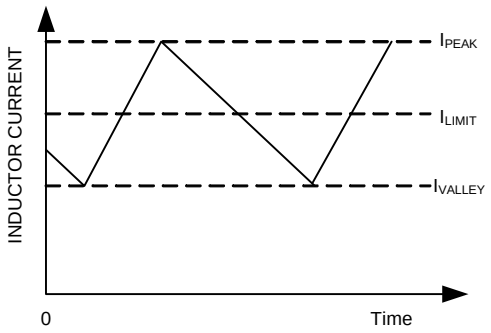


Figure 2. Current Limit Algorithm.

VTT Sink/Source Regulator

The output voltage at VTT pin tracks the reference voltage applied at VTTREF pin. Two internal N-channel MOSFETs controlled by separate high bandwidth error amplifiers regulate the output voltage by sourcing current from VLDOIN pin or sinking current to GND pin. To prevent two pass transistors from shoot-through, a small voltage offset is created between the positive inputs of the two error amplifiers. The VTT with fast response feedback loop keeps tracking to the VTTREF within ±40 mV at all conditions including fast load transient.

S3, S5 Control

In the DDR3/DDR4 memory applications, it is important to keep VDDQ always higher than VTT/VTTREF including both start-up and shutdown. The S3 and S5 signals control the VDDQ, VTT, VTTREF states and these pins should be connected to SLP_S3 and SLP_S5 signals respectively. The table1 shows the truth table of the S3 and S5 pins. When both S3 and S5 are above the logic threshold voltage, the VDDQ, VTT and VTTREF are turned on at S0 state. When S3 is low and S5 is high, the VDDQ and VTTREF are kept on while the VTT voltage is disabled and left high impedance in S3 state. When both S3 and S5 are low, the VDDQ, VTT and VTTREF are turned off and discharged to the ground.

Table1. The Truth Table of S3 and S5 pins

STATE	S3	S5	VDDQ	VTTREF	VTT
S0	H	H	1	1	1
S3	L	H	1	1	0 (high-Z)
S4/5	L	L	0 (discharge)	0 (discharge)	0 (discharge)

Thermal Shutdown

A thermal shutdown circuit limits the junction temperature of APW8861. When the junction temperature exceeds +160°C, PWM converter, VTTLDO and VTTREF are shut off, allowing the device to cool down. The regulator regulates the output again through initiation of a new soft-start cycle after the junction temperature cools by 25°C, resulting in a pulsed output during continuous thermal overload conditions. The thermal shutdown designed with a 25°C hysteresis lowers the average junction temperature during continuous thermal overload conditions, extending life time of the device. For normal operation, device power dissipation should be externally limited so that junction temperatures will not exceed +125°C

Programming the On-Time Control and PWM Switching Frequency

The APW8861 does not use a clock signal to produce PWM. The device uses the constant on-time control architecture to produce pseudo-fixed frequency with input voltage feed-forward. The on-time pulse width is proportional to output voltage VDDQ and inverse proportional to input voltage VIN. In PWM, the on-time calculation is written as below equation.

$$T_{ON} = 6.3 \times 10^{-12} \times R_{TON} \left[\frac{\frac{2}{3} \times V_{VDDQ}}{V_{IN}} \right]$$

Function Description (Cont.)

Where:

R_{TON} is the resistor connected from TON pin to PHASE pin. Furthermore, The approximate PWM switching frequency is written as:

$$T_{ON} = \frac{D}{F_{SW}} = F_{SW} = \frac{V_{OUT} / V_{IN}}{T_{ON}}$$

Where:

F_{SW} is the PWM switching frequency APW8861 doesn't have VIN pin to calculate on-time pulse width. Therefore, monitoring V_{PHASE} voltage as input voltage to calculate on-time when the high-side MOSFET is turned on. And then, use the relationship between on-time and duty cycle to obtain the switching frequency.

Application Information

Output Voltage Selection

PWM can be also adjusted from 0.75V to 3.3V with a resistor-driver at FB between VDDQSNS and GND. Using 1% or better resistors for the resistive divider is recommended. The FB pin is the inverter input of the error amplifier, and the reference voltage is 0.75V. Take the example, the output voltage of PWM is determined by:

$$V_{OUT} = 0.75 \times \left[1 + \frac{R_{TOP}}{R_{GND}}\right]$$

Where R_{TOP} is the resistor connected from V_{OUT} to FB and R_{GND} is the resistor connected from FB to GND.

Output Inductor Selection

The duty cycle of a buck converter is the function of the input voltage and output voltage. Once an output voltage is fixed, it can be written as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

The inductor value determines the inductor ripple current and affects the load transient response. Higher inductor value reduces the inductor's ripple current and induces lower output ripple voltage. The ripple current and ripple voltage can be approximated by:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{F_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}}$$

Where FSW is the switching frequency of the regulator. Although increase the inductor value and frequency reduce the ripple current and voltage, there is a tradeoff between the inductor's ripple current and the regulator load transient response time.

A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current. Increasing the switching frequency (FSW) also reduces the ripple current and voltage, but it will increase the switching loss of the MOSFETs and the power dissipation of the converter. The maximum ripple current occurs at the maximum input voltage. A good starting point is to choose the ripple current to be approximately 30% of the maximum output current. Once the inductance value has been chosen, selecting an inductor is capable of carrying the required peak current without going into saturation. In some types of inductors, especially core that is made of ferrite, the ripple current will increase abruptly whenit saturates. This will be result in a larger output ripple voltage.

Output Capacitor Selection

Output voltage ripple and the transient voltage deviation are factors that have to be taken into consideration when selecting an output capacitor. Higher capacitor value and lower ESR reduce the output ripple and the load transient drop. Therefore, selecting high performance low ESR capacitors is intended for switching regulator applications. In addition to high frequency noise related MOSFET turn-on and turn-off, the output voltage ripple includes the capacitance voltage drop and ESR voltage drop caused by the AC peak-to-peak current. These two voltages can be represented by:

$$\Delta V_{COUT} = \frac{I_{RIPPLE}}{8 C_{OUT} F_{SW}}$$

$$\Delta V_{ESR} = I_{RIPPLE} \times R_{ESR}$$

These two components constitute a large portion of the total output voltage ripple. In some applications, multiple capacitors have to be paralleled to achieve the desired ESR value. If the output of the converter has to support another load with high pulsating current, more capacitors are needed in order to reduce the equivalent ESR and suppress the voltage ripple to a tolerable level. A small decoupling capacitor in parallel for bypassing the noise is also recommended, and the voltage rating of the output capacitors must also be considered.

To support a load transient that is faster than the switching frequency, more capacitors have to be used to reduce the voltage excursion during load step change. Another aspect of the capacitor selection is that the total AC current going through the capacitors has to be less than the rated RMS current specified on the capacitors to prevent the capacitor from over-heating.

Application Information (Cont.)

Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, select the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage. The maximum RMS current rating requirement is approximately $I_{OUT}/2$, where I_{OUT} is the load current. During power up, the input capacitors have to handle large amount of surge current. In low-duty notebook applications, ceramic capacitors are recommended. The capacitors must be connected between the drain of high-side MOSFET and the source of low-side MOSFET with very low-impedance PCB layout.

Layout Consideration

In any high switching frequency converter, a correct layout is important to ensure proper operation of the regulator. With power devices switching at higher frequency, the resulting current transient will cause voltage spike across the interconnecting impedance and parasitic circuit elements. As an example, consider the turn-off transition of the PWM MOSFET. Before turn-off condition, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is freewheeling by the lower MOSFET and parasitic diode. Any parasitic inductance of the circuit generates a large voltage spike during the switching interval. In general, using short and wide printed circuit traces should minimize interconnecting impedances and the magnitude of voltage spike. And signal and power grounds are to be kept separating and finally combined to use the ground plane construction or single point grounding. The best tie-point between the signal ground and the power ground is at the negative side of the output capacitor on each channel, where there is less noise. Noisy traces beneath the IC are not recommended. Below is a checklist for your layout:

- Keep the switching nodes (BOOT, and PHASE) away from sensitive small signal nodes(FB, VTTREF, and CS) since these nodes are fast moving signals. Therefore, keep traces to these nodes as short as possible and there should be no other weak signal traces in parallel with theses traces on any layer.
- The LDOIN is closed to VDDQ output, the connect LDOIN and VDDQ output is short and wide trace. If other power is used as LDOIN, the ceramic decoupling capacitor is closed to LDOIN.
- Decoupling capacitor, the resistor dividers, boot capacitors, and current limit stetting resistor should be close their pins. (For example, place the decoupling ceramic capacitor near the drain of the high-side MOSFET as close as possible. The bulk capacitors are also placed near the drain).
- The high quality ceramic decoupling capacitor can be put close to the VCC and GND pins; the VTTREF decoupling capacitor should be close to the VTTREF pin and GND; the VDDQ and VTT output capacitors should be located right across their output pin as close as possible to the part to minimize parasitic. The input capacitor GND should be close to the output capacitor GND.
- It (VIN and PHASE nodes) should be a large plane for heat sinking.
- The APW8861 used ripple mode control. Build the resistor divider close to the FB pin so that the high impedance trace is shorter. And the FB pin and V_{OUT} feedback traces can't be close to or cross under the switching signal traces (BOOT, and PHASE).

It is recommended to place the switching signal traces on the top layer and the GND plane under the IC on the inner1 layer to shield the switching signal traces noise.

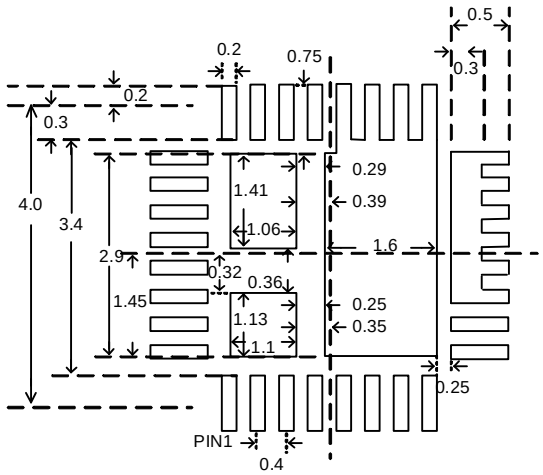
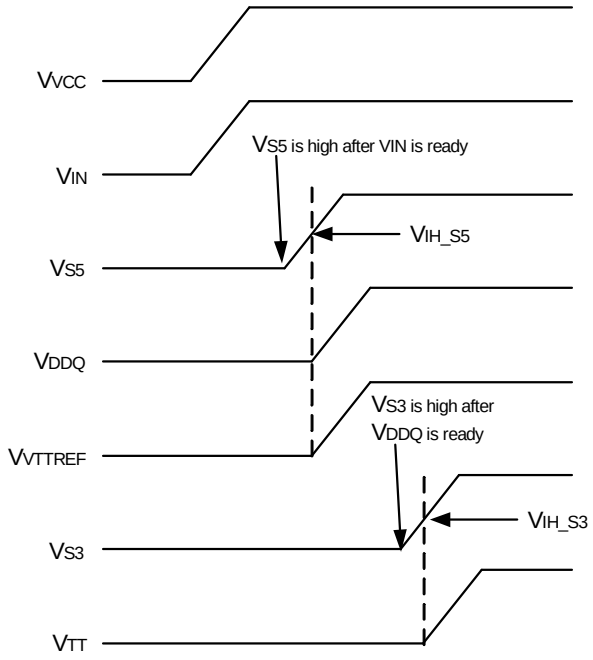


Figure 3. Recommended Minimum Footprint.

Application Information (Cont.)

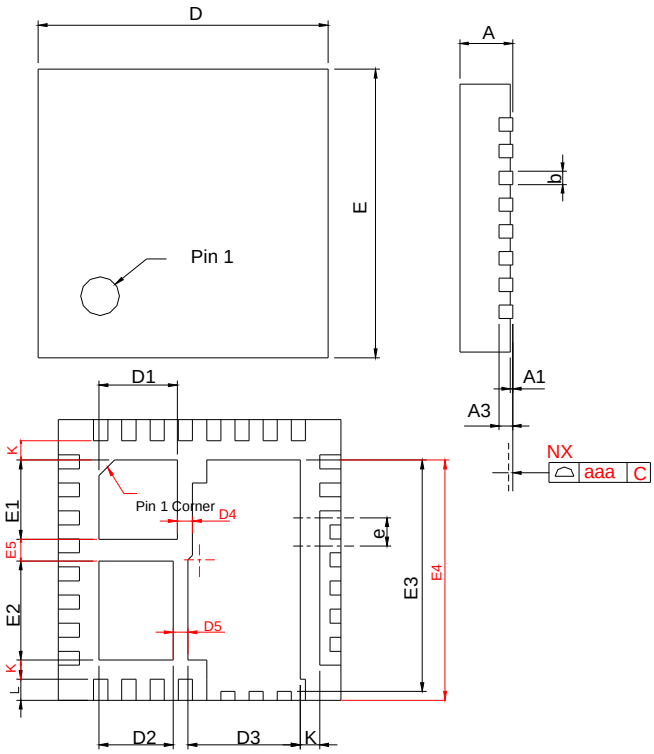
Power-on Sequencing

The DDR memory applications should have a standard power-up sequence to avoid system errors at startup. It is recommended to provide the S3 and S5 signals after all power inputs are ready. The recommended power-on sequencing is shown in below figure.



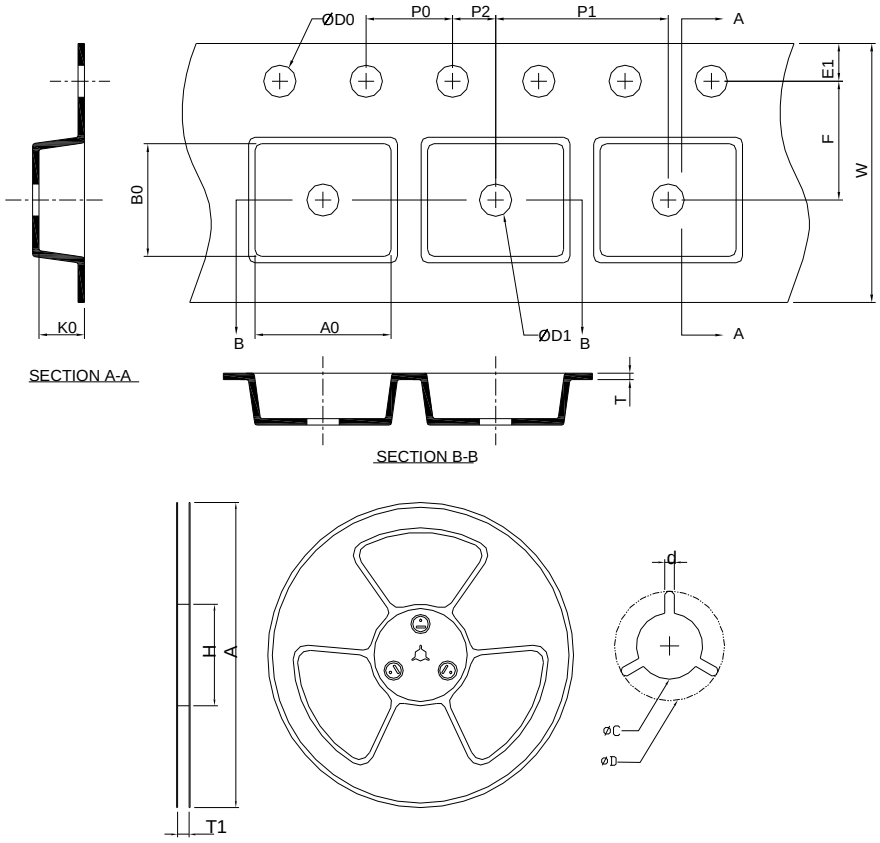
Package Information

TQFN4x4-32



SYMBOL	TQFN4*4-32			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.15	0.25	0.006	0.010
D	3.90	4.10	0.154	0.161
D1	1.01	1.21	0.040	0.048
D2	0.95	1.15	0.037	0.045
D3	1.49	1.69	0.059	0.067
D4	0.25 REF		0.010 REF	
D5	0.26 REF		0.010 REF	
E	3.90	4.10	0.154	0.161
E1	1.03	1.23	0.041	0.048
E2	1.31	1.51	0.052	0.059
E3	3.20	3.40	0.126	0.134
E4	3.45 REF		0.136 REF	
E5	0.36 REF		0.014 REF	
e	0.4 BSC		0.016 BSC	
L	0.25	0.35	0.010	0.014
K	0.24	0.26	0.009	0.010
aaa	0.08		0.003	

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TQFN4x4	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	4.30±0.20	4.30±0.20	1.00±0.20

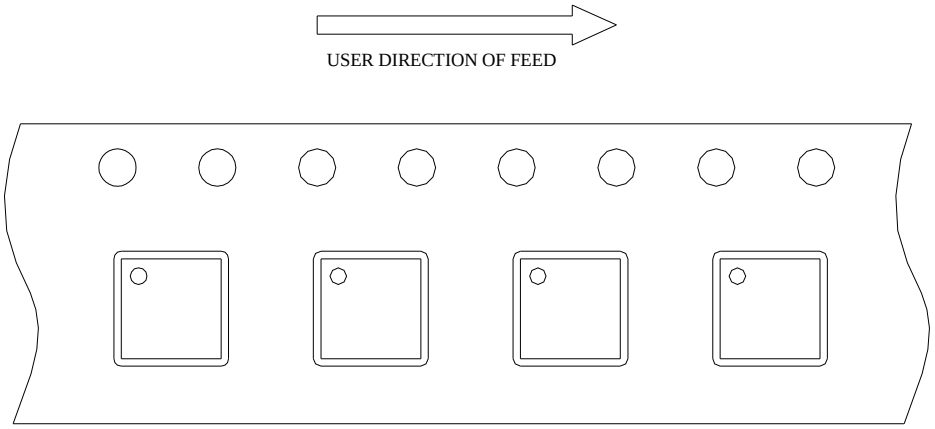
(mm)

Devices Per Unit

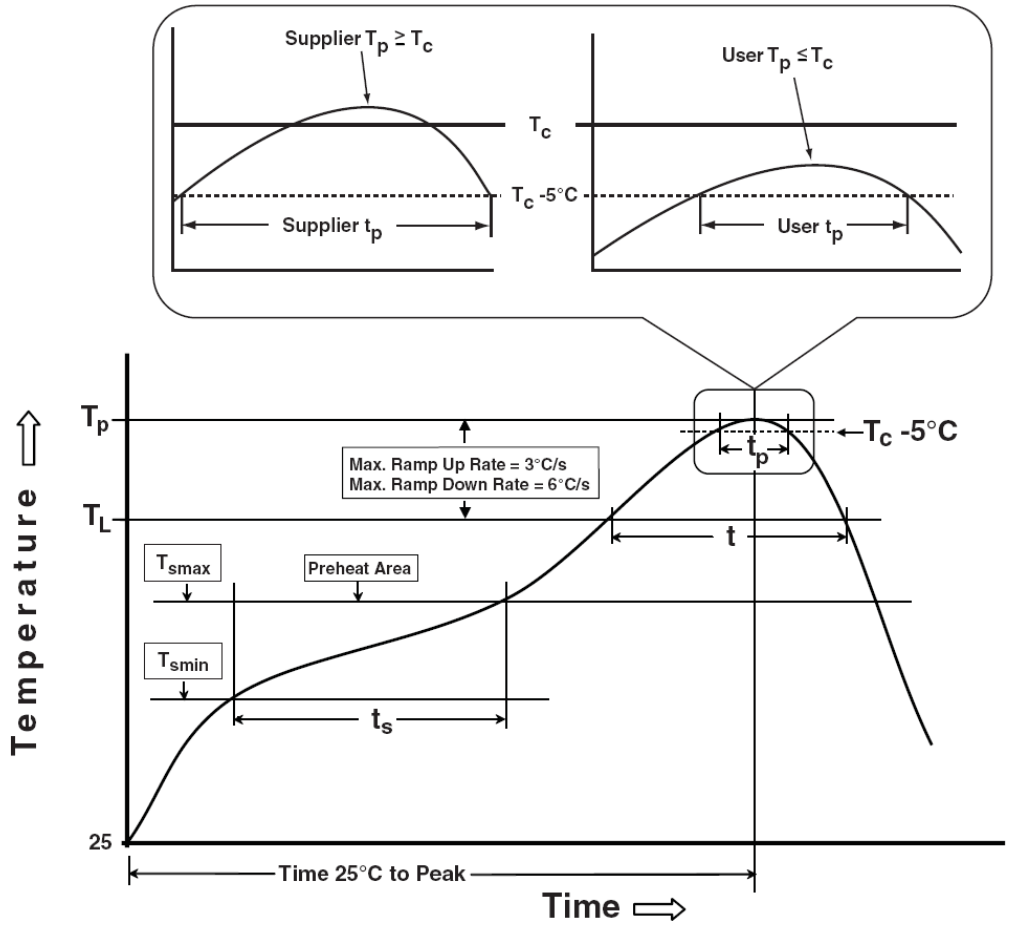
Package Type	Unit	Quantity
TQFN4x4	Tape & Reel	3000

Taping Direction Information

TQFN4x4-32



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.

* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum.
** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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