TDA8950

2 × 150 W class-D power amplifier

Rev. 01 — 9 September 2008 Preliminary data sheet

1. General description

The TDA8950 is a high efficiency class-D audio power amplifier. The typical output power is 2 × 150 W with a speaker load impedance of 4 Ω.

The TDA8950 is available in the HSOP24 power package and DBS23P power package. The amplifier operates over a wide supply voltage range from ±12.5 V to ±40 V and consumes a low quiescent current.

2. Features

- Pin compatible with TDA8920B for both HSOP24 and DBS23P packages
- Symmetrical high operating supply voltage range from ±12.5 V to ±40 V
- Stereo full differential inputs, usable as stereo Single-Ended (SE) or mono Bridge-Tied Load (BTL) amplifier
- High output power at typical applications:
  - SE 2 × 150 W, R_L = 4 Ω (V_P = ±37 V)
  - SE 2 × 170 W, R_L = 4 Ω (V_P = ±39 V)
  - SE 2 × 100 W, R_L = 6 Ω (V_P = ±37 V)
  - BTL 1 × 300 W, R_L = 8 Ω (V_P = ±37 V)
- Low noise in BTL due to BD-modulation
- Smooth pop noise-free start-up and switch down
- Zero dead time Pulse Width Modulation (PWM) output switching
- Fixed frequency
- Internal or external clock switching frequency
- High efficiency
- Low quiescent current
- Advanced protection strategy: voltage protection and output current limiting
- Thermal foldback
- Fixed gain of 30 dB in SE and 36 dB in BTL
- Full short-circuit proof across load

3. Applications

- DVD
- Mini and micro receiver
- Home Theater In A Box (HTIAB) system
- High power speaker system

4. Quick reference data

Table 1. Quick reference data

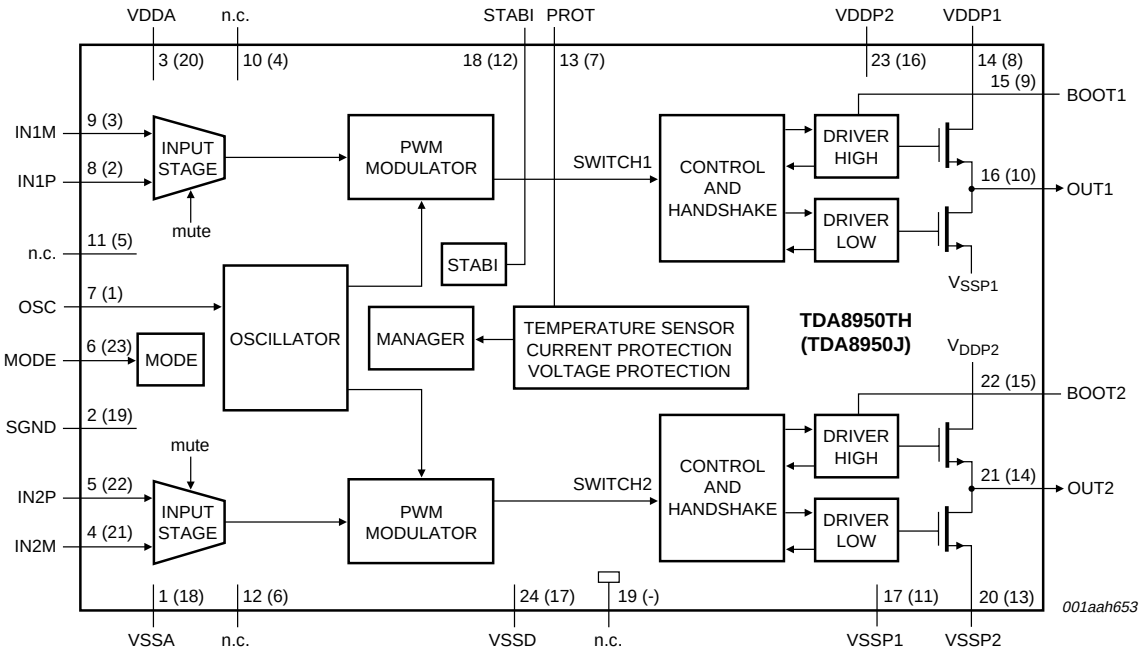
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
General, V_P = ±35 V						
V_P	supply voltage		±12.5	±35	±40	V
$V_{P(ovp)}$	overvoltage protection supply voltage	non-operating; $V_{DD} - V_{SS}$	85	-	90	V
$I_{q(tot)}$	total quiescent current	Operating mode; no load; no filter; no RC-snubber network connected	-	50	75	mA
Stereo single-ended configuration						
P_o	output power	R_L = 4 Ω; THD = 10 %; V_P = ±39 V	-	170	-	W
		R_L = 4 Ω; THD = 10 %; V_P = ±37 V	-	150	-	W
		R_L = 6 Ω; THD = 10 %; V_P = ±37 V	-	100	-	W
Mono bridge-tied load configuration						
P_o	output power	R_L = 8 Ω; THD = 10 %; V_P = ±37 V	-	300	-	W

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TDA8950J	DBS23P	plastic DIL-bent-SIL power package; 23 leads (straight lead length 3.2 mm)	SOT411-1
TDA8950TH	HSOP24	plastic, heatsink small outline package; 24 leads; low stand-off height	SOT566-3

6. Block diagram



The pin numbers in parenthesis refer to type number TDA8950J.

Fig 1. Block diagram

7. Pinning information

7.1 Pinning

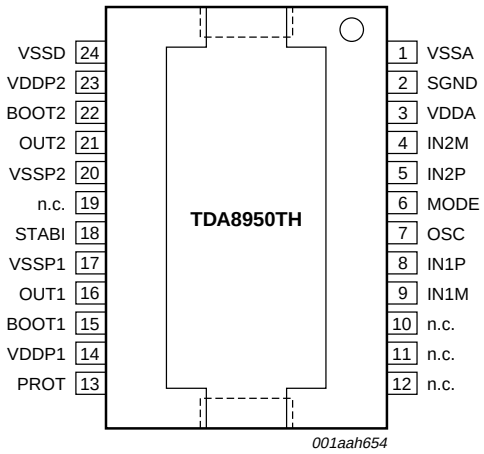


Fig 2. Pin configuration TDA8950TH

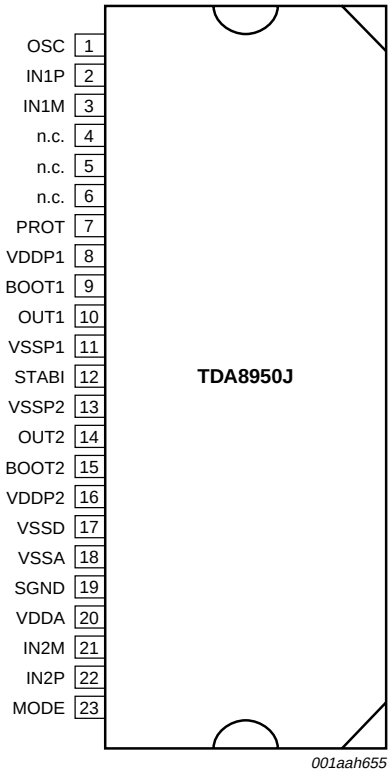


Fig 3. Pin configuration TDA8950J

7.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	TDA8950TH	TDA8950J	
VSSA	1	18	negative analog supply voltage
SGND	2	19	signal ground
VDDA	3	20	positive analog supply voltage
IN2M	4	21	negative audio input for channel 2
IN2P	5	22	positive audio input for channel 2
MODE	6	23	mode selection input: Standby, Mute or Operating mode
OSC	7	1	oscillator frequency adjustment or tracking input
IN1P	8	2	positive audio input for channel 1
IN1M	9	3	negative audio input for channel 1
n.c.	10	4	not connected
n.c.	11	5	not connected
n.c.	12	6	not connected
PROT	13	7	decoupling capacitor for protection (OCP)
VDDP1	14	8	positive power supply voltage for channel 1
BOOT1	15	9	bootstrap capacitor for channel 1
OUT1	16	10	PWM output from channel 1
VSSP1	17	11	negative power supply voltage for channel 1
STABI	18	12	decoupling of internal stabilizer for logic supply
n.c.	19	-	not connected
VSSP2	20	13	negative power supply voltage for channel 2
OUT2	21	14	PWM output from channel 2
BOOT2	22	15	bootstrap capacitor for channel 2
VDDP2	23	16	positive power supply voltage for channel 2
VSSD	24	17	negative digital supply voltage

8. Functional description

8.1 General

The TDA8950 is a two-channel audio power amplifier using class-D technology.

The audio input signal is converted into a digital pulse width modulated signal via an analog input stage and PWM modulator, see Figure 1. To enable the output power transistors to be driven, this digital PWM signal is applied to a control and handshake block and driver circuits for both the high side and low side. In this way a level shift is performed from the low power digital PWM signal (at logic levels) to a high power PWM signal that switches between the main supply lines.

A 2nd-order low-pass filter converts the PWM signal to an analog audio signal across the loudspeakers.

The TDA8950 one-chip class-D amplifier contains high power switches, drivers, timing and handshaking between the power switches and some control logic. Also an advanced protection strategy is implemented which contains several voltage protections, temperature protections and a maximum current protection to secure maximum system robustness.

The two audio channels of the TDA8950 each contain a PWM modulator, an analog feedback loop and a differential input stage. It also contains circuits common to both channels such as the oscillator, all reference sources, the mode interface and a digital timing manager.

The TDA8950 contains two independent amplifier channels with high output power, high efficiency, low distortion and low quiescent current. The amplifier channels can be connected in the following configurations:

- Mono Bridge-Tied Load (BTL) amplifier
- Stereo Single-Ended (SE) amplifiers

The amplifier system can be switched to one of three operating modes by pin MODE:

- Standby mode; with a very low supply current
- Mute mode; the amplifiers are operational, but the audio signal at the output is suppressed by disabling the VI-converter input stages
- Operating mode; the amplifiers are fully operational

To ensure pop noise-free start-up, the DC output offset voltage is applied gradually to the output at a level between Mute mode and Operating mode levels. The bias current setting of the VI converters is related to the voltage on pin MODE; in Mute mode the bias current setting of the VI converters is zero (VI converters disabled) and in Operating mode the bias current is at maximum. The time constant required to apply the DC output offset voltage gradually between Mute and Operating mode levels can be generated via an RC-network on pin MODE. An example of a switching circuit for driving pin MODE is illustrated in Figure 4. If the capacitor C is left out of the application, the voltage on pin MODE will be applied with a much smaller time-constant, which might result in audible pop noises during start-up (depending on DC output offset voltage and loudspeaker used).

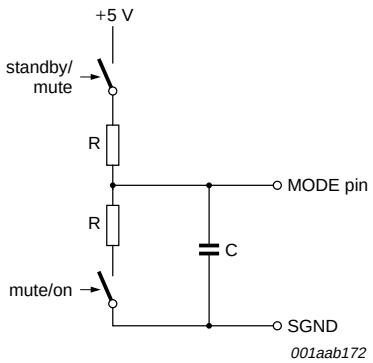
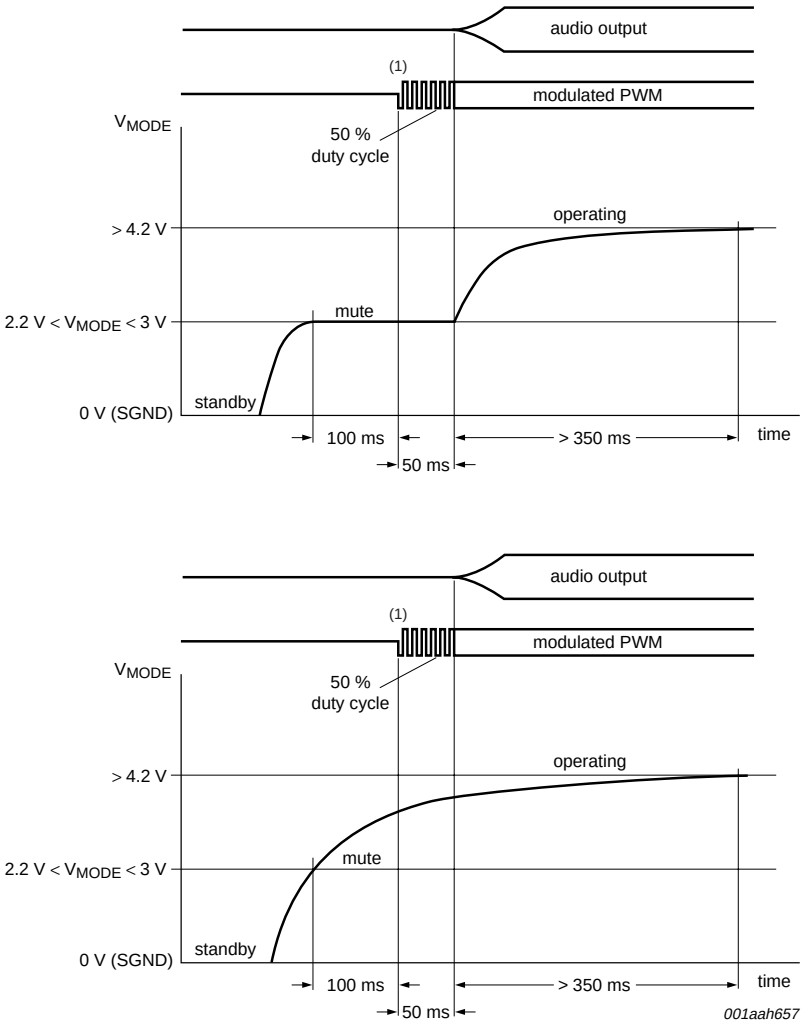


Fig 4. Example of mode selection circuit

In order to fully charge the coupling capacitors at the inputs, the amplifier will remain automatically in the Mute mode before switching to the Operating mode. A complete overview of the start-up timing is given in Figure 5.



(1) First 1/4 pulse down.

Upper diagram: When switching from standby to mute, there is a delay of approximately 100 ms before the output starts switching. The audio signal is available after V_{MODE} has been set to operating, but not earlier than 150 ms after switching to mute. For pop noise-free start-up it is recommended that the time constant applied to pin MODE is at least 350 ms for the transition between mute and operating.

Lower diagram: When switching directly from standby to operating, there is a first delay of 100 ms before the outputs starts switching. The audio signal is available after a second delay of 50 ms. For pop noise-free start-up it is recommended that the time constant applied to pin MODE is at least 500 ms for the transition between standby and operating.

Fig 5. Timing on mode selection input

8.2 Pulse width modulation frequency

The output signal of the amplifier is a PWM signal with a carrier frequency that typically lies between 300 kHz and 400 kHz. Using a 2nd-order LC demodulation filter in the application results in an analog audio signal across the loudspeaker. The carrier frequency is determined by an external resistor R_{OSC}, connected between pin OSC and pin VSSA. An optimal setting for the carrier frequency is between 300 kHz and 400 kHz.

Using an external resistor of 30 kΩ on pin OSC, the carrier frequency is set to 345 kHz. For more details see Table 8.

If two or more class-D amplifiers are used in the same audio application, it is recommended that all devices operate at the same switching frequency by using an external clock circuit.

Due to an internal clock divider:

- The external applied clock frequency must have the double frequency of the output PWM frequency.
- The duty cycle of the external clock is not critical for product performance.

8.3 Protections

The following protections are included in TDA8950:

- Thermal protections:
  - Thermal FoldBack (TFB)
  - OverTemperature Protection (OTP)
- OverCurrent Protection (OCP, diagnostic via pin PROT)
- Window Protection (WP)
- Supply voltage protections:
  - UnderVoltage Protection (UVP)
  - OverVoltage Protection (OVP)
  - UnBalance Protection (UBP)

The reaction of the device to the different fault conditions differs per protection.

8.3.1 Thermal protection

In the TDA8950 an advanced thermal protection strategy is implemented. It consists of a TFB function that gradually reduces the out put power within a certain temperature range. When temperature is still rising an OTP is implemented which shuts down the device completely.

8.3.1.1 Thermal FoldBack (TFB)

If the junction temperature T_j exceeds a defined threshold value, the gain is gradually reduced. This will result in a smaller output signal and less dissipation. Eventually the temperature will stabilize.

TFB is specified at the temperature value $T_{act(th\_fold)}$ where the closed loop voltage gain is reduced with 6 dB. The range of the TFB is:

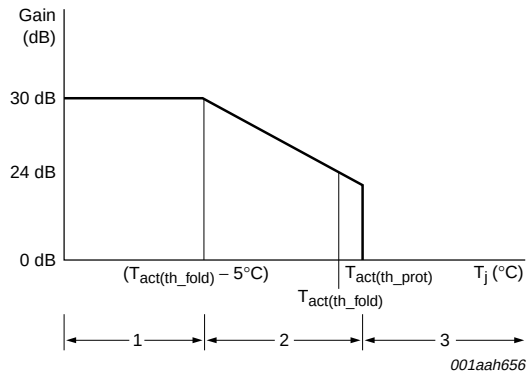
$T_{act(th\_fold)} - 5\ °C < T_{act(th\_fold)} < T_{act(th\_prot)}$.

For the TDA8950 the value of $T_{act(th\_fold)}$ is about +153 °C. For more details see: Table 7.

8.3.1.2 OverTemperature Protection (OTP)

If, despite the TFB function, the junction temperature T_j of the TDA8950 continues rising and exceeds the threshold $T_{act(th\_prot)}$ the amplifier will shutdown immediately. The amplifier resumes switching approximately 100 ms after the temperature drops below $T_{act(th\_prot)}$.

In Figure 6 the thermal behavior is visualized.



(1) Duty cycle of PWM output modulated according audio input signal.

(2) Duty cycle of PWM output reduced due to TFB.

(3) Amplifier is switched off due to OTP.

Fig 6. Behavior of TFB and OTP

8.3.2 OverCurrent Protection (OCP)

If a short-circuit is applied to one of the demodulated outputs of the amplifier, the OCP will detect this. If the output current exceeds the maximum of 9.2 A, it is automatically limited to its maximum value by the OCP protection circuit. The amplifier outputs remain switching (the amplifier is NOT shut-down completely). If the active current limiting continues longer than time τ, the TDA8950 shuts down. Activation of current limiting and the triggering of the OCP are observed at pin PROT.

The amplifier can distinguish between an impedance drop of the loudspeaker and a low-ohmic short-circuit across the load. In the TDA8950 the impedance threshold (Z_{th}) depends on the supply voltage used.

When a short-circuit is made across the load, causing the impedance to drop below the threshold level ($<Z_{th}$), the amplifier is switched off completely and, after a time of 100 ms, it will try to restart. If the short-circuit condition is still present after this time, the cycle will be repeated. The average dissipation will be low because of this low duty cycle.

Should there be an impedance drop (e.g. due to dynamic behavior of the loudspeaker) the same protection will be activated. The maximum output current will again be limited to 9.2 A, but the amplifier will not switch-off completely (thus preventing audio holes from occurring).

The result will be a clipping output signal.

See Section 13.7 for more information on this maximum output current limiting feature.

8.3.3 Window Protection (WP)

The WP checks the conditions at the output terminals of the power stage and is activated:

- During the start-up sequence, when pin MODE is switched from standby to mute. In the event of a short-circuit at one of the output terminals to pin VDDPn or pin VSSPn the start-up procedure is interrupted and the TDA8950 waits until the short-circuit to the supply lines has been removed. Because the test is done before enabling the power stages, no large currents will flow in an event of short-circuit.
- When the amplifier is completely shut-down due to activation of the OCP because a short-circuit to one of the supply lines is made, then during restart (after 100 ms) the WP will be activated. As a result the amplifier will not start-up until the short-circuit to the supply lines is removed.

8.3.4 Supply voltage protections

If the supply voltage drops below minimum supply voltage, the UVP circuit is activated and the system will shutdown correctly. If the internal clock is used, this switch-off will be silent and without pop noise. When the supply voltage rises above the threshold level, the system is restarted again after 100 ms.

If the supply voltage exceeds maximum supply voltage, the OVP circuit is activated and the power stages will shutdown. When the supply voltage drops below the threshold level, the system is restarted again after 100 ms.

An additional UBP circuit compares the positive analog (voltage on pin VDDA) and the negative analog (voltage on pin VSSA) supply voltage and is triggered if the voltage difference exceeds a factor of two.

When the supply voltage difference drops below the threshold level, the system is restarted again after 100 ms.

Example: With a symmetrical supply of ±30 V, the protection circuit will be triggered if the unbalance exceeds approximately 15 V. See Section 13.7.

In Table 4 an overview is given of all protections and their respective effects on the output signal.

Table 4. Overview of TDA8950 protections

Protection name	Complete shutdown	Restart directly	Restart after 100 ms	Pin PROT detection
TFB[1]	N	N	N	N
OTP	Y	N	Y	N
OCP	Y[2]	N[2]	Y[2]	Y
WP	N[3]	Y	N	N
UVP	Y	N	Y	N
OVP	Y	N	Y	N
UBP	Y	N	Y	N

[1] Amplifier gain will depend on junction temperature and heatsink size.

[2] Only complete shutdown of amplifier if short-circuit impedance is below threshold of 1 Ω. In all other cases current limiting results in clipping of the output signal.

[3] Fault condition detected during (every) transition between standby-to-mute and during restart after activation of OCP (short-circuit to one of the supply lines).

8.4 Differential audio inputs

For a high common mode rejection ratio and a maximum of flexibility in the application, the audio inputs are fully differential.

There are two possibilities:

- For stereo operation it is advised to use the inputs in anti phase and also to connect the speakers in anti phase (to avoid acoustical phase differences). This construction has several advantages:
  - The peak current in the power supply is minimized
  - The supply pumping effect is minimized, especially at low audio frequencies
- For mono BTL operation it is required that the inputs are connected in anti parallel. The output of one of the channels is inverted and the speaker load is now connected between the two outputs of the TDA8950. In principle the output power to the speaker can be significantly boosted to two times the output power in single ended stereo.

  The input configuration for a mono BTL application is illustrated in Figure 7.

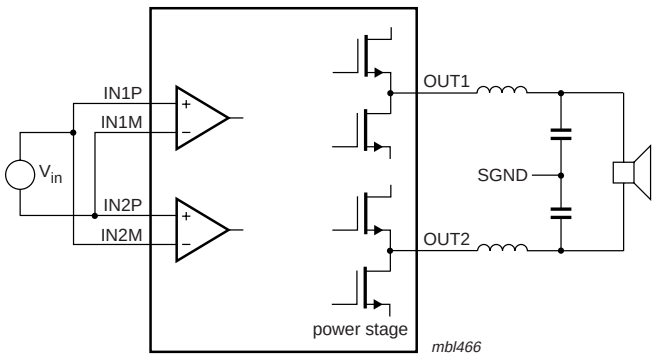


Fig 7. Input configuration for mono BTL application

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_P	supply voltage	non-operating mode; $V_{DD} - V_{SS}$	-	90	V
I_{ORM}	repetitive peak output current	maximum output current limiting	9.2	-	A
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–40	+85	°C
T_j	junction temperature		-	150	°C
V_{MODE}	voltage on pin MODE	referenced to SGND	0	6	V
V_{OSC}	voltage on pin OSC		0	SGND + 6	V
V_I	input voltage	referenced to SGND; pin IN1P; IN1M; IN2P and IN2M	–5	+5	V
V_{PROT}	voltage on pin PROT	referenced to voltage on pin VSSD	0	12	V
V_{esd}	electrostatic discharge voltage	Human Body Model (HBM); pin VSSP1 with respect to other pins	–1800	+1800	V
		HBM; all other pins	–2000	+2000	V
		Machine Model (MM); all pins	–200	+200	V
		Charged Device Model (CDM)	–500	+500	V
$I_{q(tot)}$	total quiescent current	Operating mode; no load; no filter; no RC-snubber network connected	-	75	mA

10. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	40	K/W
$R_{th(j-c)}$	thermal resistance from junction to case		1.1	K/W

11. Static characteristics

Table 7. Static characteristics

V_P = ±35 V; f_{osc} = 345 kHz; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply							
V_P	supply voltage		[1]	±12.5	±35	±40	V
$V_{P(ovp)}$	overvoltage protection supply voltage	non-operating; $V_{DD} - V_{SS}$		85	-	90	V
$V_{P(uvp)}$	undervoltage protection supply voltage	$V_{DD} - V_{SS}$		20	-	25	V
$I_{q(tot)}$	total quiescent current	Operating mode; no load; no filter; no RC-snubber network connected		-	50	75	mA
I_{stb}	standby current			-	480	600	µA
Mode select input; pin MODE							
V_{MODE}	voltage on pin MODE	referenced to SGND	[2]	0	-	6.0	V
		Standby mode	[2][3]	0	-	0.8	V
		Mute mode	[2][3]	2.2	-	3.0	V
		Operating mode	[2][3]	4.2	-	6.0	V
I_I	input current	V_I = 5.5 V		-	110	150	µA
Audio inputs; pins IN1M, IN1P, IN2P and IN2M							
V_I	input voltage	DC input	[2]	-	0	-	V
Amplifier outputs; pins OUT1 and OUT2							
$V_{O(offset)}$	output offset voltage	SE; mute		-	-	±15	mV
		SE; operating	[4]	-	-	±150	mV
		BTL; mute		-	-	±21	mV
		BTL; operating	[4]	-	-	±210	mV
Stabilizer output; pin STABI							
$V_{O(STABI)}$	output voltage on pin STABI	mute and operating; with respect to VSSP1		9.3	9.8	10.3	V
Temperature protection							
$T_{act(th\_prot)}$	thermal protection activation temperature			-	154	-	°C
$T_{act(th\_fold)}$	thermal foldback activation temperature	closed loop SE voltage gain reduced with 6 dB	[5]	-	153	-	°C

[1] The circuit is DC adjusted at V_P = ±12.5 V to ±42.5 V.

[2] With respect to SGND (0 V).

[3] The transition between Standby and Mute mode has hysteresis, while the slope of the transition between Mute and Operating mode is determined by the time-constant of the RC-network on pin MODE; see Figure 8.

[4] DC output offset voltage is gradually applied to the output during the transition between the Mute and Operating modes. The slope caused by any DC output offset is determined by the time-constant of the RC-network on pin MODE.

[5] At a junction temperature of approximately $T_{act(th\_fold)}$ − 5 °C the gain reduction will commence and at a junction temperature of approximately $T_{act(th\_prot)}$ the amplifier switches off.

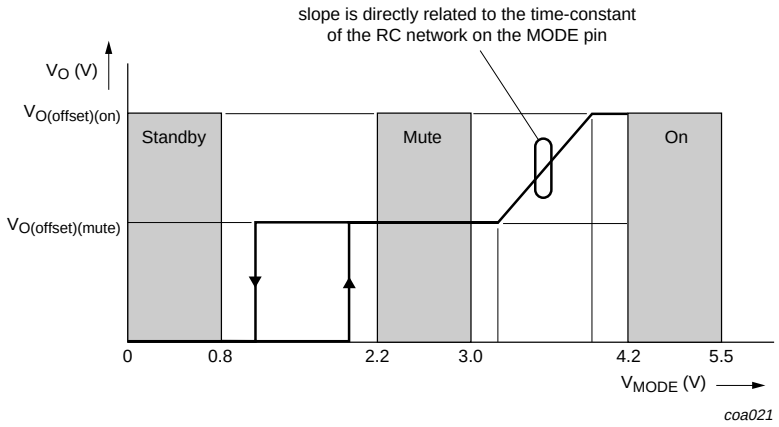


Fig 8. Behavior of mode selection pin MODE

12. Dynamic characteristics

12.1 Switching characteristics

Table 8. Dynamic characteristics

V_P = ±35 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Internal oscillator						
$f_{osc(typ)}$	typical oscillator frequency	R_{OSC} = 30.0 kΩ	325	345	365	kHz
f_{osc}	oscillator frequency		250	-	450	kHz
External oscillator or frequency tracking						
V_{OSC}	voltage on pin OSC		SGND + 4.5	SGND + 5	SGND + 6	V
$V_{trip(OSC)}$	trip voltage on pin OSC		-	SGND + 2.5	-	V
f_{track}	tracking frequency	[1]	250	-	450	kHz

[1] When using an external oscillator, the $f_{osc(ext)}$ frequency (500 kHz minimum, 900 kHz maximum) will result in a PWM frequency f_{track} (250 kHz minimum, 450 kHz maximum) due to the internal clock divider. See Section 8.2.

12.2 Stereo and dual SE application characteristics

Table 9. Dynamic characteristics

V_P = ±35 V; R_L = 4 Ω; f_i = 1 kHz; f_{osc} = 345 kHz; R_{sL} < 0.1 Ω[1]; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
P_o	output power	L = 22 µH; C = 680 nF; T_j = 85 °C	[2]				
		R_L = 4 Ω; THD = 0.5 %; V_P = ±37 V		-	100	-	W
		R_L = 4 Ω; THD = 10 %; V_P = ±37 V		-	150	-	W
		R_L = 6 Ω; THD = 10 %; V_P = ±37 V		-	100	-	W
		R_L = 4 Ω; THD = 10 %; V_P = ±39 V		-	170	-	W
THD	total harmonic distortion	P_o = 1 W; f_i = 1 kHz	[3]	-	0.05	-	%
		P_o = 1 W; f_i = 6 kHz	[3]	-	0.05	-	%
$G_{v(cl)}$	closed-loop voltage gain			29	30	31	dB
SVRR	supply voltage ripple rejection	between pin VDDPn and SGND					
		operating; f_i = 100 Hz	[4]	-	90	-	dB
		operating; f_i = 1 kHz	[4]	-	70	-	dB
		mute; f_i = 100 Hz	[4]	-	75	-	dB
		standby; f_i = 100 Hz	[4]	-	120	-	dB
		between pin VSSPn and SGND					
		operating; f_i = 100 Hz	[4]	-	80	-	dB
		operating; f_i = 1 kHz	[4]	-	60	-	dB
		mute; f_i = 100 Hz	[4]	-	80	-	dB
		standby; f_i = 100 Hz	[4]	-	115	-	dB
Z_i	input impedance	between the input pins and SGND		45	63	-	kΩ
$V_{n(o)}$	output noise voltage	operating; R_s = 0 Ω	[5]	-	160	-	µV
		mute	[6]	-	85	-	µV
α_{cs}	channel separation		[7]	-	70	-	dB
$\lvert\Delta G_v\rvert$	voltage gain difference			-	-	1	dB
α_{mute}	mute attenuation	f_i = 1 kHz; V_i = 2 V (RMS)	[8]	-	75	-	dB
CMRR	common mode rejection ratio	$V_{i(CM)}$ = 1 V (RMS)		-	75	-	dB
η_{po}	output power efficiency	SE, R_L = 4 Ω		-	88	-	%
		SE, R_L = 6 Ω		-	90	-	
		BTL, R_L = 8 Ω		-	88	-	%
$R_{DSon(hs)}$	high-side drain-source on-state resistance		[9]	-	200	-	mΩ
$R_{DSon(ls)}$	low-side drain-source on-state resistance		[9]	-	190	-	mΩ

[1] R_{sL} is the series resistance of inductor of low-pass LC filter in the application.

[2] Output power is measured indirectly; based on R_{DSon} measurement. See also Section 13.3.

[3] THD is measured in a bandwidth of 22 Hz to 20 kHz, using AES17 20 kHz brickwall filter. Maximum limit is not guaranteed100 % tested.

[4] V_{ripple} = $V_{ripple(max)}$ = 2 V (p-p); R_s = 0 Ω. Measured independently between VDDPn and SGND and between VSSPn and SGND.

[5] B = 22 Hz to 20 kHz, using AES17 20 kHz brickwall filter.

[6] B = 22 Hz to 22 kHz, using AES17 20 kHz brickwall filter; independent of R_s.

[7] P_o = 1 W; R_s = 0 Ω; f_i = 1 kHz.

[8] V_i = $V_{i(max)}$ = 1 V (RMS); f_i = 1 kHz.

[9] Leads and bond wires included.

12.3 Mono BTL application characteristics

Table 10. Dynamic characteristics

V_P = ±35 V; R_L = 8 Ω; f_i = 1 kHz; f_{osc} = 345 kHz; R_{sL} < 0.1 Ω [1]; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
P_o	output power	L = 22 µH; C = 680 nF; T_j = 85 °C; R_L = 8 Ω	[2]				
		THD = 10 %; V_P = ±39 V		-	340	-	W
		THD = 10 %; V_P = ±37 V		-	300	-	W
		THD = 0.5 %; V_P = ±37 V		-	200	-	W
THD	total harmonic distortion	P_o = 1 W; f_i = 1 kHz	[3]	-	0.05	-	%
		P_o = 1 W; f_i = 6 kHz	[3]	-	0.05	-	%
$G_{v(cl)}$	closed-loop voltage gain			-	36	-	dB
SVRR	supply voltage ripple rejection	between pin VDDPn and SGND					
		operating; f_i = 100 Hz	[4]	-	80	-	dB
		operating; f_i = 1 kHz	[4]	-	80	-	dB
		mute; f_i = 100 Hz	[4]	-	95	-	dB
		standby; f_i = 100 Hz	[4]	-	120	-	dB
		between pin VSSPn and SGND					
		operating; f_i = 100 Hz	[4]	-	75	-	dB
		operating; f_i = 1 kHz	[4]	-	75	-	dB
		mute; f_i = 100 Hz	[4]	-	90	-	dB
		standby; f_i = 100 Hz	[4]	-	130	-	dB
Z_i	input impedance	measured between the input pins and SGND		45	63	-	kΩ
$V_{n(o)}$	output noise voltage	operating; R_s = 0 Ω	[5]	-	190	-	µV
		mute	[6]	-	45	-	µV
α_{mute}	mute attenuation	f_i = 1 kHz; V_i = 2 V (RMS)	[7]	-	82	-	dB
CMRR	common mode rejection ratio	$V_{i(CM)}$ = 1 V (RMS)		-	75	-	dB

[1] R_{sL} is the series resistance of inductor of low-pass LC filter in the application.

[2] Output power is measured indirectly; based on R_{DSon} measurement. See also Section 13.3.

[3] Total harmonic distortion is measured in a bandwidth of 22 Hz to 20 kHz, using an AES17 20 kHz brickwall filter. Maximum limit is guaranteed but may not be 100 % tested.

[4] $V_{ripple} = V_{ripple(max)}$ = 2 V (p-p); R_s = 0 Ω.

[5] B = 22 Hz to 20 kHz, using an AES17 20 kHz brickwall filter. Low noise due to BD modulation.

[6] B = 22 Hz to 20 kHz, using an AES17 20 kHz brickwall filter; independent of R_s.

[7] $V_i = V_{i(max)}$ = 1 V (RMS); f_i = 1 kHz.

13. Application information

13.1 Mono BTL application

When using the power amplifier in a mono BTL application the inputs of both channels must be connected in parallel and the phase of one of the inputs must be inverted (see Figure 7). In principle the loudspeaker can be connected between the outputs of the two single-ended demodulation filters.

13.2 Pin MODE

For pop noise-free start-up, an RC time-constant must be applied on pin MODE. The bias-current setting of the VI-converter input is directly related to the voltage on pin MODE. In turn the bias-current setting of the VI converters is directly related to the DC output offset voltage. Thus a slow dV/dt on pin MODE results in a slow dV/dt for the DC output offset voltage, resulting in pop noise-free start-up. A time-constant of 500 ms is sufficient to guarantee pop noise-free start-up (see also Figure 4, 5 and 8).

13.3 Output power estimation

13.3.1 SE

Maximum output power:

$$P_{o(0.5\%)} = \frac{\left[\frac{R_L}{R_L + R_{DSon(hs)} + R_{sL}} \times V_P \times (1 - t_{min} \times 0.5 f_{osc})\right]^2}{2R_L} \quad (1)$$

Maximum current internally limited to 9.2 A:

$$I_{o(peak)} = \frac{V_P \times (1 - t_{min} \times 0.5 f_{osc})}{R_L + R_{DSon(hs)} + R_{sL}} \quad (2)$$

Variables:

- R_L: load impedance
- R_{sL}: series impedance of the filter coil
- $R_{DSon(hs)}$: high-side R_{DSon} of power stage output DMOS (temperature dependent)
- f_{osc}: oscillator frequency
- t_{min}: minimum pulse width (typical 150 ns, temp. dependent)
- V_P: single-sided supply voltage (or $0.5 \times (V_{DD} + |V_{SS}|)$)
- $P_{o(0.5\ \%)}$: output power at the onset of clipping

Note that $I_{o(peak)}$ should be below 9.2 A (Section 8.3.2). $I_{o(peak)M}$ is the sum of the current through the load and the ripple current. The value of the ripple current is dependent on the coil inductance and voltage drop over the coil.

13.3.2 Bridge-Tied Load (BTL)

Maximum output power:

$$P_{o(0.5\%)} = \frac{\left[\frac{R_L}{R_L + R_{DSon(hs)} + R_{dson(ls)}} \times 2V_P \times (1 - t_{min} \times 0.5 f_{osc})\right]^2}{2R_L} \quad (3)$$

Maximum current internally limited to 9.2 A:

$$I_{o(peak)} = \frac{2V_P \times (1 - t_{min} \times 0.5 f_{osc})}{R_L + (R_{DSon(hs)} + R_{DSon(ls)}) + 2R_{sL}} \quad (4)$$

Variables:

- R_L: load impedance
- R_{sL}: series impedance of the filter coil
- $R_{DSon(hs)}$: high-side R_{DSon} of power stage output DMOS (temperature dependent)
- $R_{DSon(ls)}$: low-side R_{DSson} of power stage output DMOS (temperature. dependent)
- f_{osc}: oscillator frequency
- t_{min}: minimum pulse width (typical 150 ns, temp. dependent)
- V_P: single-sided supply voltage (or $0.5 \times (V_{DD} + |V_{SS}|)$)
- $P_{o(0.5\ \%)}$: output power at the onset of clipping

Note that $I_{o(peak)M}$ should be below 9.2 A (Section 8.3.2). $I_{o(peak)}$ is the sum of the current through the load and the ripple current. The value of the ripple current is dependent on the coil inductance and voltage drop over the coil.

13.4 External clock

For duty cycle independent operation of the device, the external clock input frequency is internally divided by two. This implies that the frequency of the external clock is as twice as high as the internal clock (typical 2 × 345 kHz = 690 kHz).

If two or more class-D amplifiers are used it is recommended that all devices run at the same switching frequency. This can be realized by connecting all OCS pins together and feeding them from an external oscillator. When applying an external oscillator, it is necessary to force pin OSC to a DC level above SGND. The internal oscillator is disabled and the PWM modulator will switch with half the externally applied frequency.

The internal oscillator requires an external resistor $R_{ext(OSC)}$ and capacitor C_{OSC} between pin OSC and PIN VSSA.

The noise contribution of the internal oscillator is supply voltage dependent. An external low noise oscillator is recommended for low noise applications running at high supply voltage.

13.5 Noise

Noise should be measured using a high order low-pass filter with a cut-off frequency of 20 kHz. The standard audio band pass filters, used in audio analyzers, do not suppress the residue of the carrier frequency sufficiently to ensure a reliable measurement of the audible noise. Noise measurements should preferably be carried out using AES 17 ('brickwall') filters or an audio precision AUX 0025 filter, which was designed specifically for measuring class-D switching amplifiers.

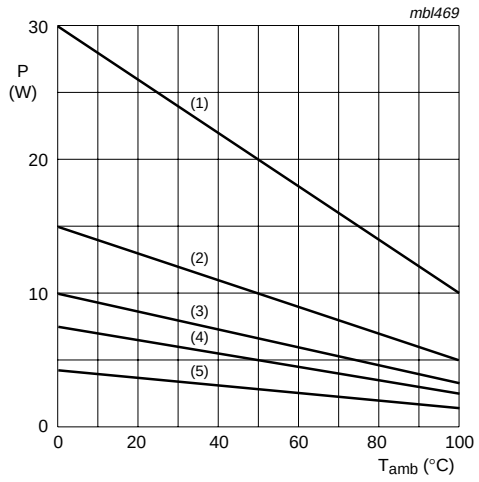
13.6 Heatsink requirements

In many applications it may be necessary to connect an external heatsink to the TDA8950.

Equation 5 shows the relationship between the maximum power dissipation, before activation of the TFB, and the total thermal resistance from junction to ambient

$$R_{th(j-a)} = \frac{T_j - T_{amb}}{P_{diss}} \quad (5)$$

Power dissipation (P_{diss}) is determined by the efficiency of the TDA8950. The efficiency measured as a function of output power is given in Figure 21. The power dissipation can be derived as a function of output power (Figure 20).



(1) $R_{th(j-a)}$ = 5 K/W.
(2) $R_{th(j-a)}$ = 10 K/W.
(3) $R_{th(j-a)}$ = 15 K/W.
(4) $R_{th(j-a)}$ = 20 K/W.
(5) $R_{th(j-a)}$ = 35 K/W.

Fig 9. De-rating curves for power dissipation as a function of maximum ambient temperature

In the following example, a heatsink calculation is made for an 8 Ω BTL application with a ±35 V supply:

The audio signal has a crest factor of 10 (the ratio between peak power and average power (20 dB)), this means that the average output power is $\frac{1}{10}$ of the peak power.

In this case, the peak RMS output power level would be the 0.5 % THD level, i.e. 220 W.

The average power would then be $\frac{1}{10} \times 220$ W = 22 W.

The dissipated power at an output power of 22 W is approximately 5 W.

When the maximum expected ambient temperature is 85 °C, the total $R_{th(j-a)}$ would then become $\frac{(140-85)}{5} = 11$ K/W

$R_{th(j-a)} = R_{th(j-c)} + R_{th(c-h)} + R_{th(h-a)}$

$R_{th(j-c)}$ = 1.1 K/W

$R_{th(c-h)}$ = 0.5 K/W to 1 K/W (dependent on mounting)

So the thermal resistance between heatsink and ambient temperature is:

$R_{th(h-a)} = 11 - (1.1 + 1) = 8.9$ K/W

The de-rating curves (given for several values of $R_{th(j-a)}$) are illustrated in Figure 9. A maximum junction temperature T_j = 150 °C is taken into account. From Figure 9 the maximum allowable power dissipation for a given heatsink size can be derived or the required heatsink size can be determined at a required dissipation level.

13.7 Output current limiting

To guarantee the robustness of the TDA8950, the maximum output current that can be delivered by the output stage is limited. An advanced OverCurrent Protection (OCP) is included for each output power switch.

When the current flowing through any of the power switches exceeds the defined internal threshold current of 9.2 A (e.g. in case of a short-circuit to the supply lines or a short-circuit across the load), the maximum output current of the amplifier will be regulated to 9.2 A.

The TDA8950 amplifier can distinguish between a low-ohmic short-circuit condition and other over current conditions like dynamic impedance drops of the loudspeakers used. The impedance threshold (Z_{th}) depends on the supply voltage used.

Depending on the impedance of the short-circuit, the amplifier will react as follows:

- Short-circuit impedance > Z_{th}: The maximum output current of the amplifier is regulated to 9.2 A, but the amplifier will not shut-down its PWM outputs. Effectively this results in a clipping output signal across the load (behavior is very similar to voltage clipping).
- Short-circuit impedance < Z_{th}: The amplifier will limit the maximum output current to 9.2 A and at the same time the capacitor on pin PROT is discharged. When the voltage across this capacitor drops below an internal threshold voltage, the amplifier will shutdown completely and an internal timer will be started.

A typical value for the capacitor on pin PROT is 220 pF. After a fixed time of 100 ms the amplifier is switched on again. If the requested output current is still too high, the amplifier will switch-off again. Thus the amplifier will try to switch to the Operating mode every

100 ms. The average dissipation will be low in this situation because of this low duty cycle. If the over current condition is removed the amplifier will remain in Operating mode after being restarted. In this way the TDA8950 amplifier is fully protected against short-circuit conditions while at the same time so-called audio holes, as a result of loudspeaker impedance drops, are eliminated.

13.8 Pumping effects

In a typical stereo half-bridge SE application the TDA8950 is supplied by a symmetrical voltage (e.g. V_{DD} = +35 V and V_{SS} = −35 V). When the amplifier is used in an SE configuration, a 'pumping effect' can occur. During one switching interval, energy is taken from one supply (e.g. V_{DD}), while a part of that energy is returned to the other supply line (e.g. V_{SS}) and vice versa. When the voltage supply source cannot sink energy, the voltage across the output capacitors of that voltage supply source will increase and the supply voltage is pumped to higher levels. The voltage increase caused by the pumping effect depends on:

- Speaker impedance
- Supply voltage
- Audio signal frequency
- Value of decoupling capacitors on supply lines
- Source and sink currents of other channels

When applying the TDA8950, measures must be taken within the application to minimize the pumping effect and prevent malfunctions of either the audio amplifier and/or the voltage supply source. Amplifier malfunction due to the pumping effect can cause triggering of the UVP, OVP or UBP.

The best remedy against pumping effects is to use the TDA8950 in a mono full-bridge application or, in the case of stereo half-bridge applications, adapt the power supply (e.g. increase supply decoupling capacitors).

13.9 Application schematics

Notes for the application schematic:

- A solid ground plane connected to V_{SS} around the switching amplifier is necessary to prevent emission.
- 100 nF capacitors must be placed as close as possible to the power supply pins of the TDA8950.
- The internal heat spreader of the TDA8950 is internally connected to V_{SS}.
- The external heatsink must be connected to the ground plane.
- Use a thermally conductive, electrically non-conductive, Sil-Pad between the backside of the TDA8950 and a small external heatsink.
- The differential inputs enable the best system level audio performance with unbalanced signal sources. In case of hum, due to floating inputs, connect the shielding or source ground to the amplifier ground. Jumpers J1 and J2 are open on set level and are closed on the stand-alone demo board.
- Minimum total required capacitance per power supply line is 3300 µF.

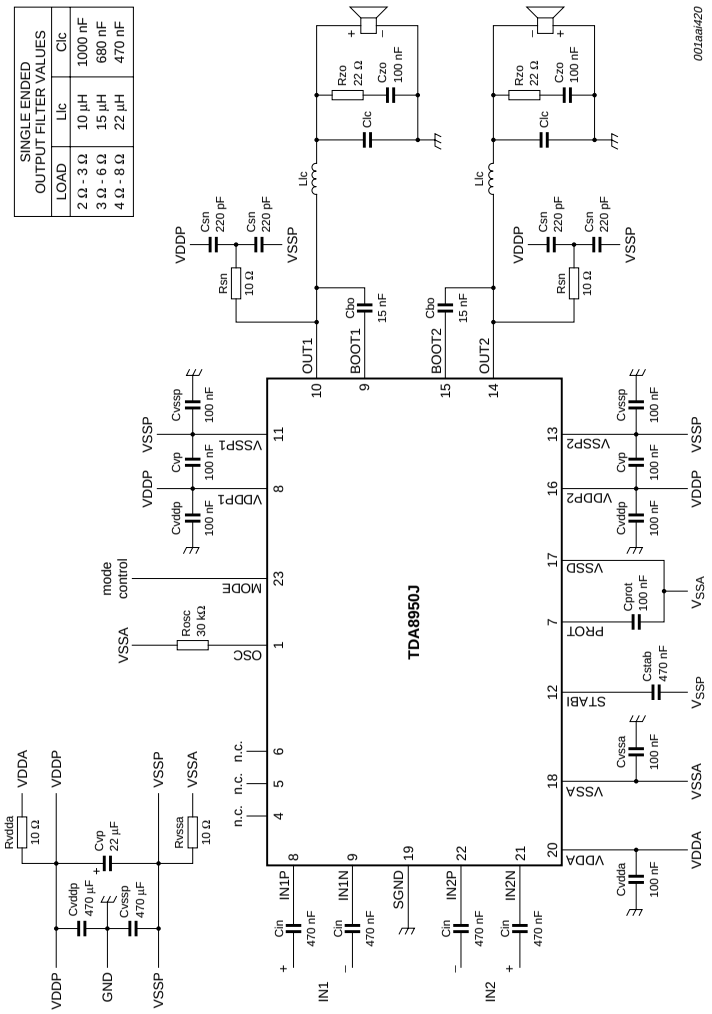


Fig 10. Simplified application diagram

13.10 Layout and grounding

To obtain a high-level system performance, certain grounding techniques are essential. The input reference grounds have to be tied with their respective source grounds and must have separate tracks from the power ground tracks. This will prevent the large (output) signal currents from interfering with the small AC input signals. The small-signal ground tracks should be physically located as far as possible from the power ground tracks. Supply and output tracks should be as wide as possible for delivering maximum output power.

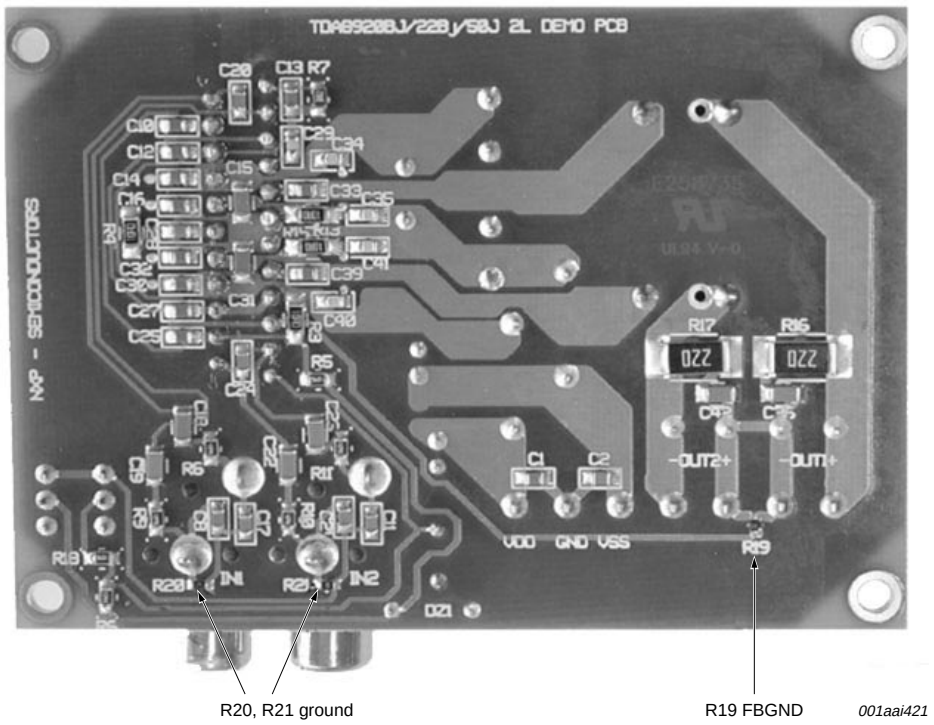
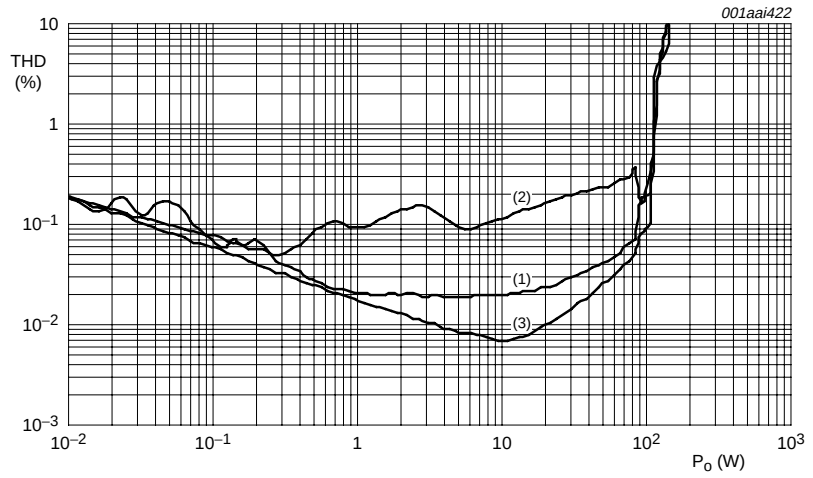


Fig 11. Printed-circuit board layout (quasi-single-sided); components view

13.11 Curves measured in reference design



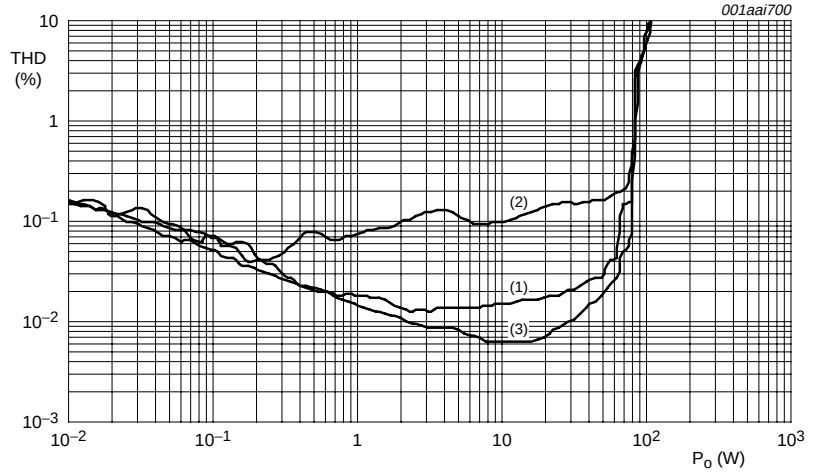
V_P = ±35 V, 2 × 4 Ω SE configuration.

(1) OUT2, f_i = 6 kHz

(2) OUT2, f_i = 1 kHz

(3) OUT2, f_i = 100 Hz

Fig 12. THD as a function of output power, SE configuration with 2 × 4 Ω load



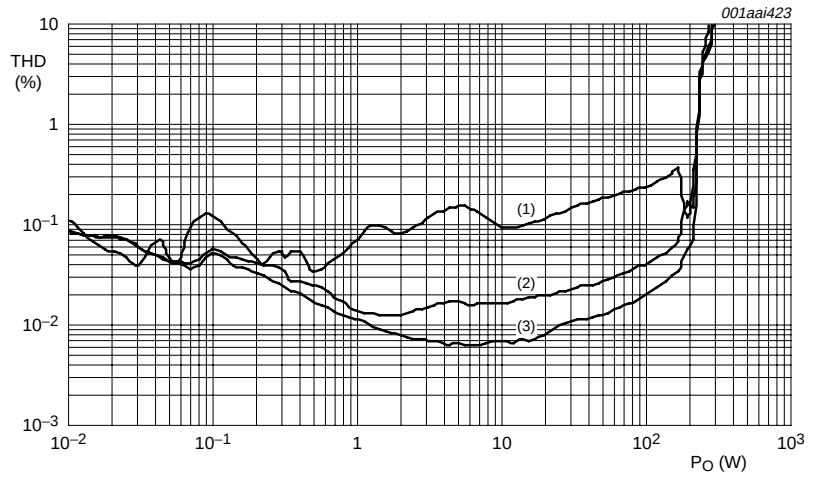
V_P = ±35 V, 2 × 6 Ω SE configuration.

(1) OUT2, f_i = 6 kHz

(2) OUT2, f_i = 1 kHz

(3) OUT2, f_i = 100 Hz

Fig 13. THD as a function of output power, SE configuration with 2 × 6 Ω load



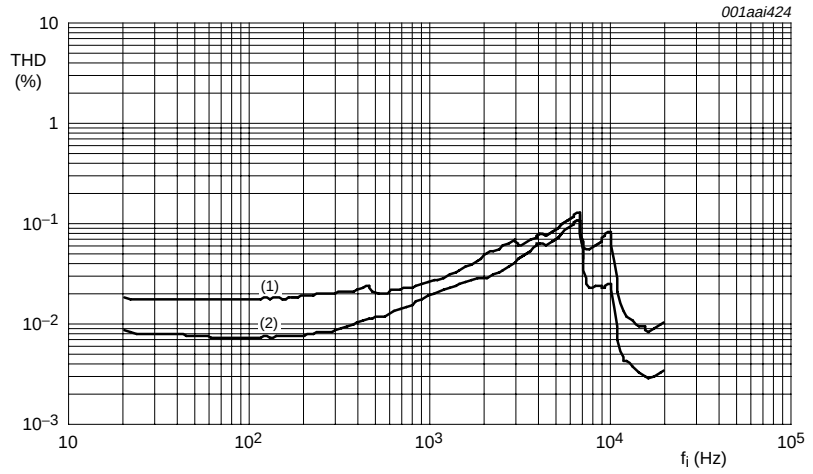
V_P = ±35 V, f_{osc} = 350 kHz, 1 × 8 Ω BTL configuration.

(1) f_i = 6 kHz

(2) f_i = 1 kHz

(3) f_i = 100 Hz

Fig 14. THD as a function of output power, BTL configuration with 1 × 8 Ω load

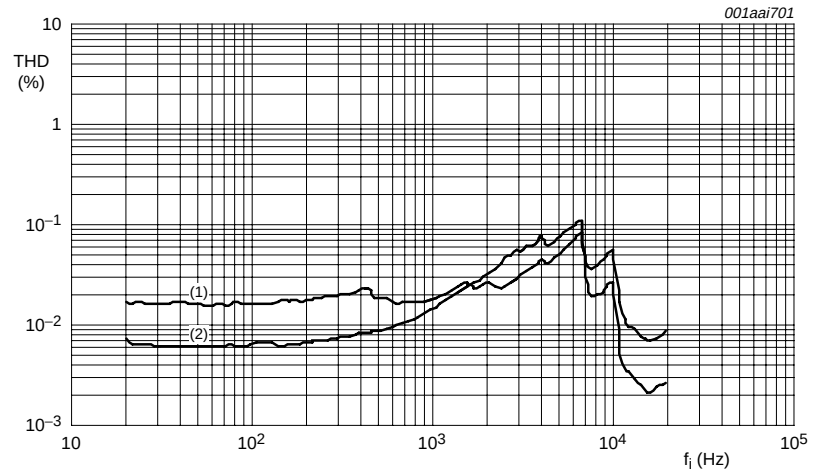


V_P = ±35 V, 2 × 4 Ω SE configuration.

(1) OUT2, P_O = 1 W

(2) OUT2, P_O = 10 W

Fig 15. THD as a function of frequency, SE configuration with 2 × 4 Ω load

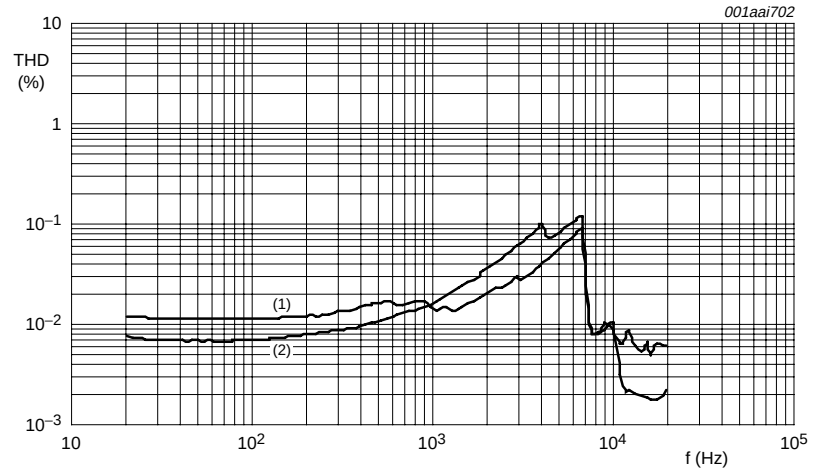


V_P = ±35 V, 2 × 6 Ω SE configuration.

(1) OUT2, P_o = 1 W

(2) OUT2, P_o = 10 W

Fig 16. THD as a function of frequency, SE configuration with 2 × 6 Ω load

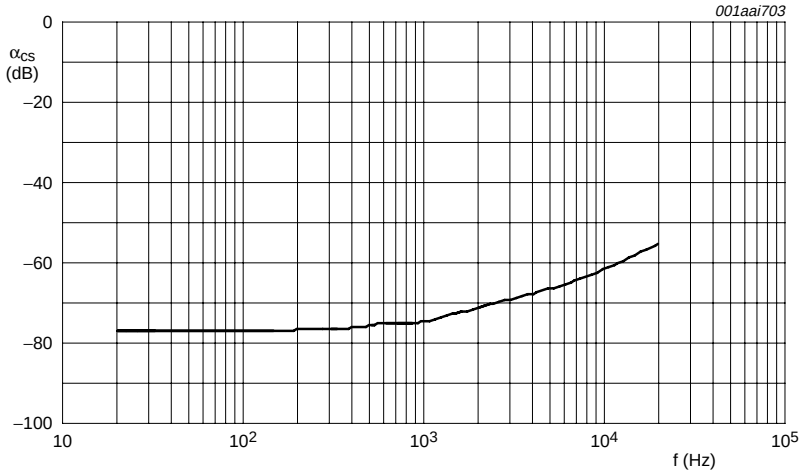


V_P = ±35 V, 1 × 8 Ω BTL configuration

(1) P_o = 1 W

(2) P_o = 10 W

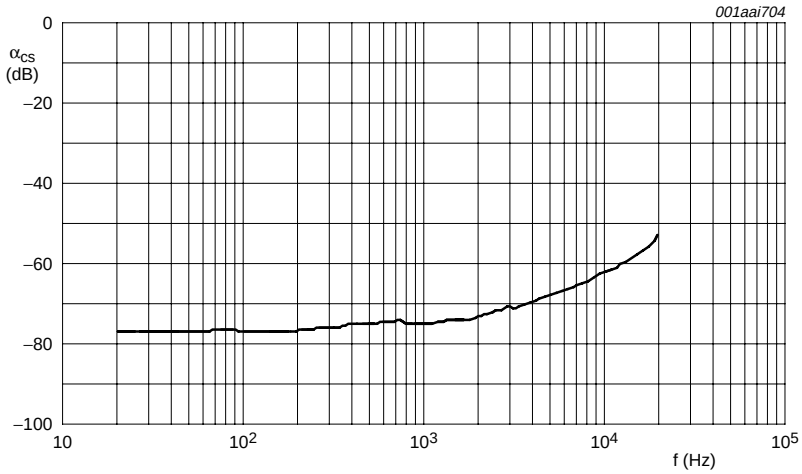
Fig 17. THD as a function of frequency, BTL configuration with 1 × 8 Ω load



V_P = ±35 V, 2 × 4 Ω SE configuration

For OUT1 and OUT2 for both 1 W and 10 W.

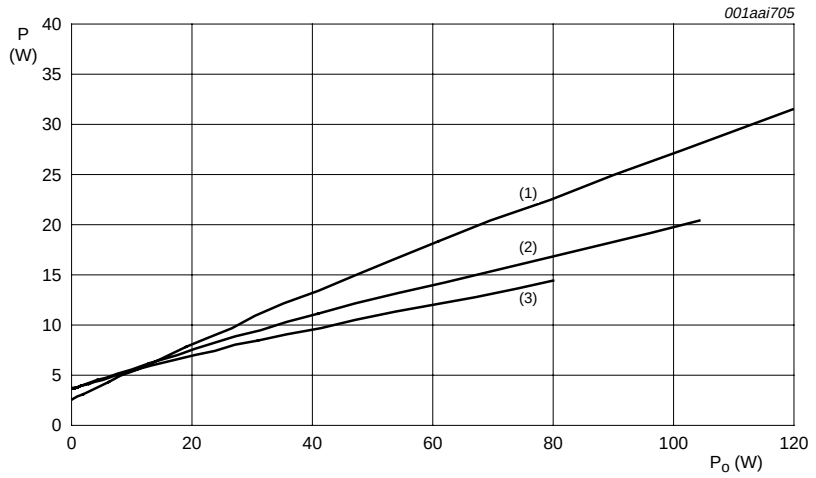
Fig 18. Channel separation as a function of frequency, SE configuration with 2 × 4 Ω load



V_P = ±35 V, 2 × 6 Ω SE configuration

For OUT1 and OUT2 for both 1 W and 10 W.

Fig 19. Channel separation as a function of frequency, SE configuration with 2 × 6 Ω load



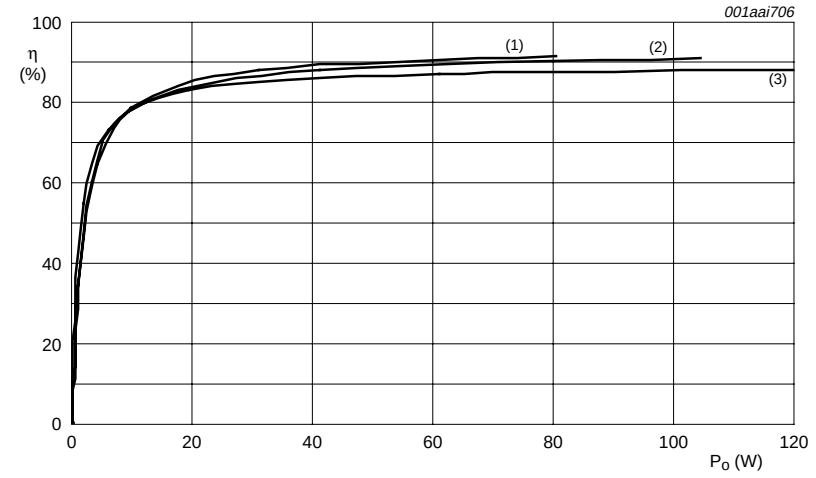
V_P = ±35 V, f_i = 1 kHz, f_{osc} = 325 kHz

(1) 2 × 4 Ω SE configuration

(2) 2 × 6 Ω SE configuration

(3) 2 × 8 Ω SE configuration

Fig 20. Power dissipation as function of output power per channel



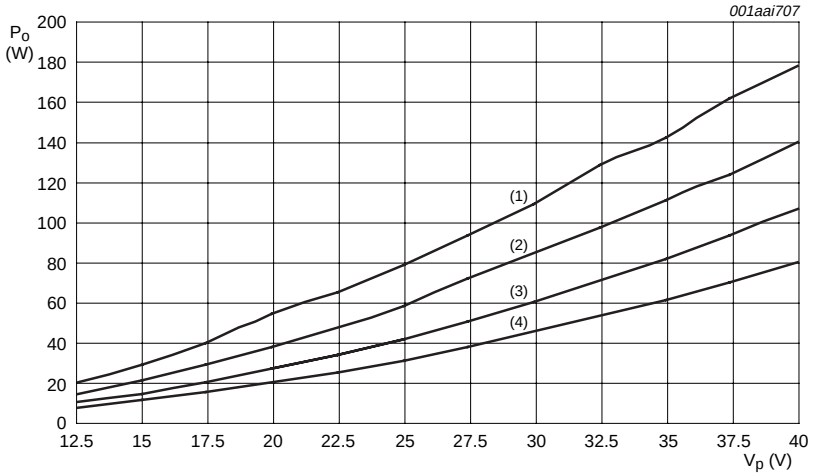
V_P = ±35 V, f_i = 1 kHz, f_{osc} = 325 kHz

(1) 2 × 4 Ω SE configuration

(2) 2 × 6 Ω SE configuration

(3) 2 × 8 Ω SE configuration

Fig 21. Efficiency as function of output power per channel



f_i = 1 kHz, f_{osc} = 325 kHz

Note: infinite heat sink used.

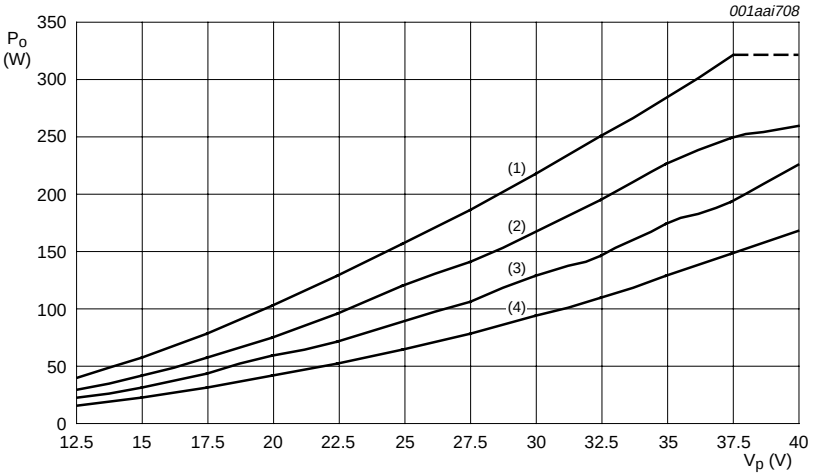
(1) THD = 10 %, 4 Ω

(2) THD = 0.5 %, 4 Ω; THD = 10 %, 6 Ω

(3) THD = 0.5 %, 6 Ω; THD = 10 %, 8 Ω

(4) THD = 0.5 %, 8 Ω

Fig 22. Output power as a function of supply voltage, SE configuration



f_i = 1 kHz, f_{osc} = 325 kHz

Note: infinite heat sink used.

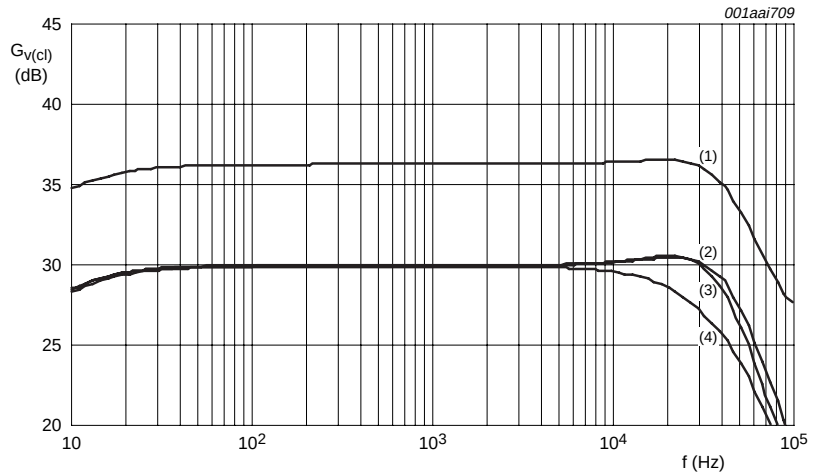
(1) THD = 10 %, 8 Ω

(2) THD = 0.5 %, 8 Ω

(3) THD = 10 %, 16 Ω

(4) THD = 0.5 %, 16 Ω

Fig 23. Output power as function of supply voltage, BTL configuration



V_P = ±35 V, V_i = 100 mV, R_s = 0 Ω, C_i = 330 pF.

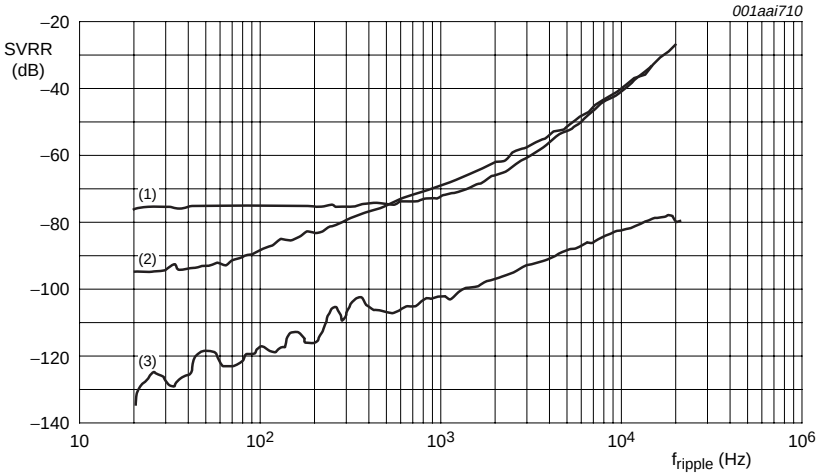
(1) 1 × 8 Ω BTL configuration

(2) 2 × 4 Ω SE configuration

(3) 2 × 6 Ω SE configuration

(4) 2 × 8 Ω SE configuration

Fig 24. Gain as function of frequency, R_s = 0 Ω, C_i = 330 pF



Ripple on V_{DD}, short on input pins.

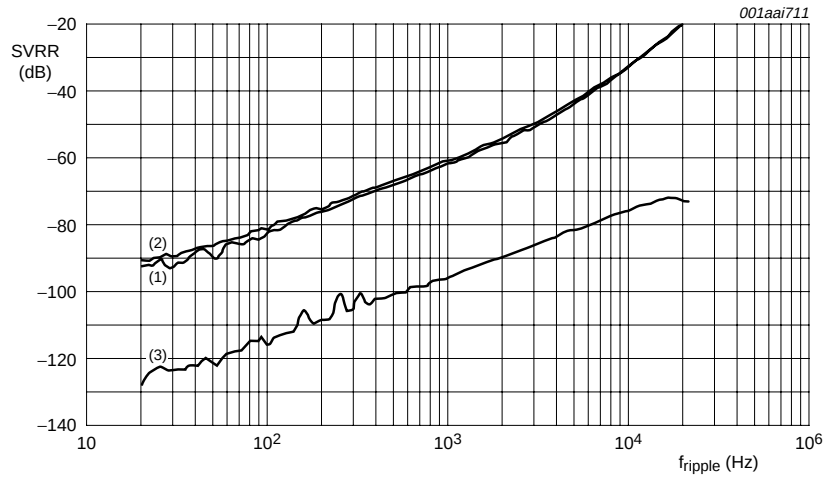
V_P = ±35 V, R_L = 4 Ω, V_{ripple} = 2 V (p-p).

(1) OUT2, mute

(2) OUT2, on

(3) OUT2, standby

Fig 25. SVRR as function of ripple frequency



Ripple on V_{SS}, short on input pins.

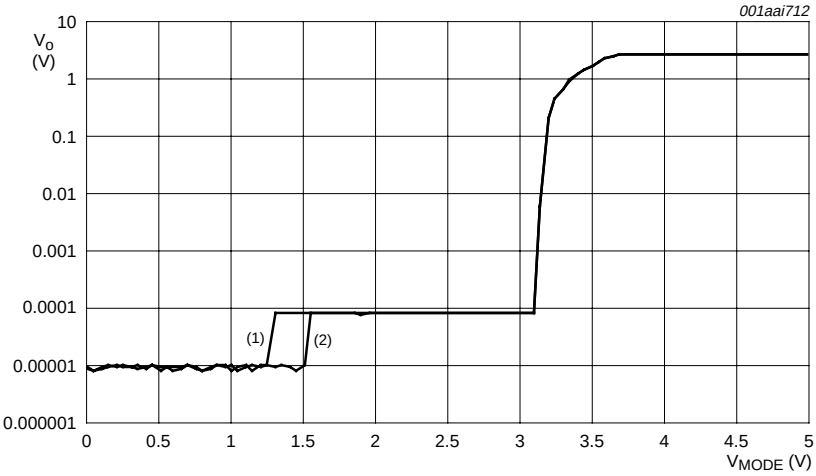
V_P = ±35 V, R_L = 4 Ω, V_{ripple} = 2 V (p-p).

(1) OUT2, mute

(2) OUT2, on

(3) OUT2, standby

Fig 26. SVRR as function of ripple frequency

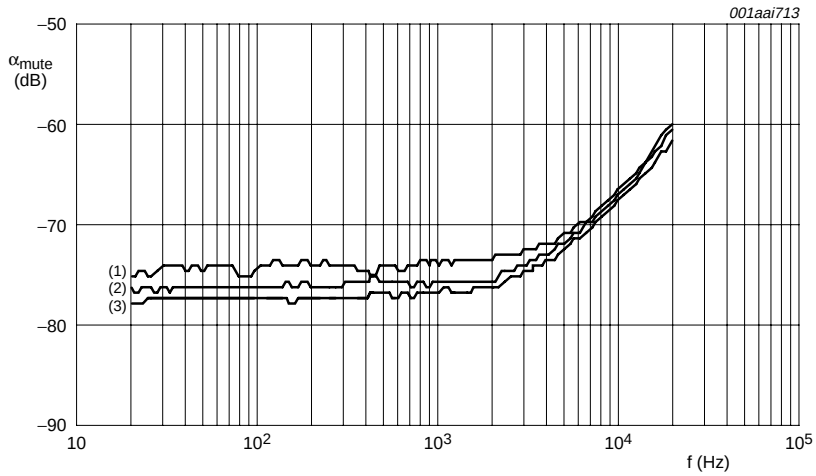


V_P = ±35 V

(1) Out1, down

(2) Out1, up

Fig 27. Output voltage as function of mode voltage



V_P = ±35 V, V_i = 2 V (rms), f_{osc} = 325 kHz

(1) OUT2, 8 Ω

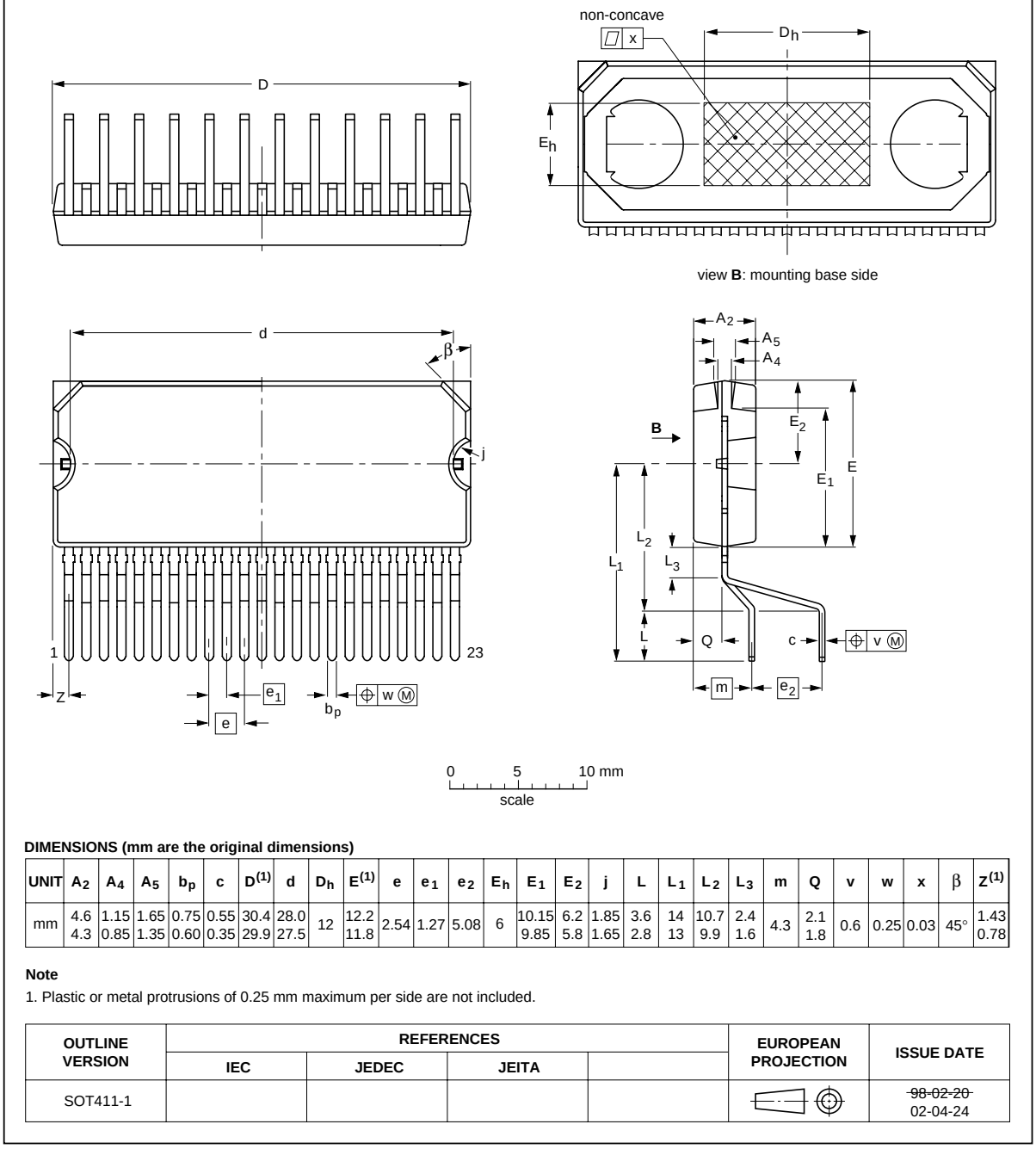
(2) OUT2, 6 Ω

(3) OUT2, 4 Ω

Fig 28. Mute attenuation as function of frequency

14. Package outline

DBS23P: plastic DIL-bent-SIL power package; 23 leads (straight lead length 3.2 mm) **SOT411-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A_2	A_4	A_5	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	e_1	e_2	E_h	E_1	E_2	j	L	L_1	L_2	L_3	m	Q	v	w	x	β	$Z^{(1)}$
mm	4.6 4.3	1.15 0.85	1.65 1.35	0.75 0.60	0.55 0.35	30.4 29.9	28.0 27.5	12	12.2 11.8	2.54	1.27	5.08	6	10.15 9.85	6.2 5.8	1.85 1.65	3.6 2.8	14 13	10.7 9.9	2.4 1.6	4.3	2.1 1.8	0.6	0.25	0.03	45°	1.43 0.78

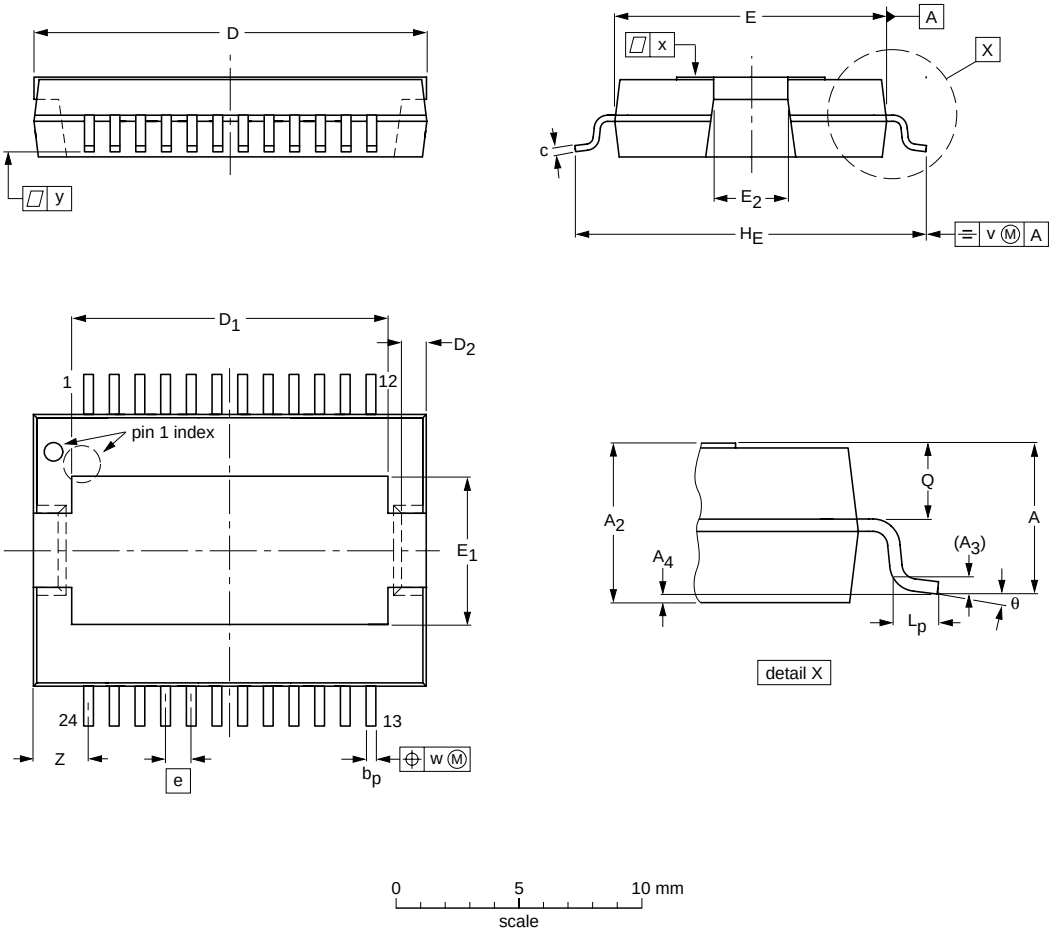
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT411-1						~~98-02-20~~ 02-04-24

Fig 29. Package outline SOT411-1 (DBS23P)

HSOP24: plastic, heatsink small outline package; 24 leads; low stand-off height **SOT566-3**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_2	A_3	A_4[1]	b_p	c	D[2]	D_1	D_2	E[2]	E_1	E_2	e	H_E	L_p	Q	v	w	x	y	Z	θ
mm	3.5	3.5 3.2	0.35	+0.08 −0.04	0.53 0.40	0.32 0.23	16.0 15.8	13.0 12.6	1.1 0.9	11.1 10.9	6.2 5.8	2.9 2.5	1	14.5 13.9	1.1 0.8	1.7 1.5	0.25	0.25	0.03	0.07	2.7 2.2	8° 0°

Notes

1. Limits per individual lead.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT566-3						~~03-02-18~~ 03-07-23

Fig 30. Package outline SOT566-3 (HSOP24)

15. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 31) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 11 and 12

Table 11. SnPb eutectic process (from J-STD-020C)

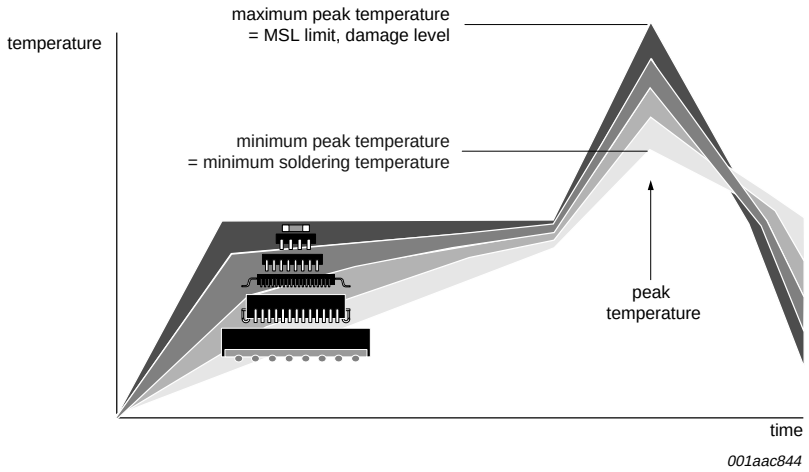
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 12. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 31.



MSL: Moisture Sensitivity Level

Fig 31. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

16. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDA8950_1	20080909	Preliminary data sheet	-	-

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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