FAIRCHILD SEMICONDUCTOR®

May 2008

FDMC8884

N-Channel Power Trench® MOSFET

30V, 15A, 19mΩ

Features

- Max $r_{DS(on)}$ = 19mΩ at V_{GS} = 10V, I_D = 9.0A
- Max $r_{DS(on)}$ = 30mΩ at V_{GS} = 4.5V, I_D = 7.2A
- High performance trchnology for extremely low $r_{DS(on)}$
- Termination is Lead-free and RoHS Compliant

General Description

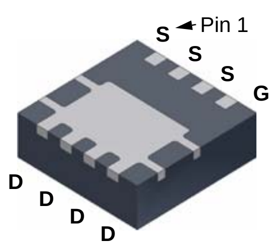
This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench® process that has been especially tailored to minimize the on-state resistance. This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.

Application

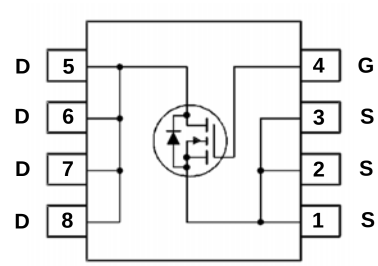
- High side in DC - DC Buck Converters
- Notebook battery power management
- Load switch in Notebook

Top

Bottom



Power 33



MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current -Continuous (Package limited) T_C = 25°C	15	A
	-Continuous (Silicon limited) T_C = 25°C	24	
	-Continuous T_A = 25°C (Note 1a)	9.0	
	-Pulsed	40	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	24	mJ
P_D	Power Dissipation T_C = 25°C	18	W
	Power Dissipation T_A = 25°C (Note 1a)	2.3	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	6.6	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC8884	FDMC8884	Power 33	13''	12mm	3000 units

Electrical Characteristics T_J = 25°C unless otherwise noted

Off Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250μA, referenced to 25°C		22		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24V, V_{GS} = 0V			1	μA
		T_J = 125°C			250	
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V, V_{DS} = 0V			±100	nA

On Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	1.2	1.9	2.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250μA, referenced to 25°C		-6		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10V, I_D = 9.0A		16	19	mΩ
		V_{GS} = 4.5V, I_D = 7.2A		22	30	
		V_{GS} = 10V, I_D = 9.0A, T_J = 125°C		22	30	
g_{FS}	Forward Transconductance	V_{DD} = 5V, I_D = 9.0A		24		S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
C_{iss}	Input Capacitance	V_{DS} = 15V, V_{GS} = 0V, f = 1MHz		513	685	pF
C_{oss}	Output Capacitance			110	150	pF
C_{rss}	Reverse Transfer Capacitance			76	115	pF
R_g	Gate Resistance	f = 1MHz		1.4	2.1	Ω

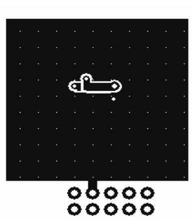
Switching Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 15V, I_D = 9.0A, V_{GS} = 10V, R_{GEN} = 6Ω		6	12	ns
t_r	Rise Time			2	10	ns
$t_{d(off)}$	Turn-Off Delay Time			15	27	ns
t_f	Fall Time			2	10	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0V to 10V; V_{DD} = 15V, I_D = 9.0A		10	14	nC
	Total Gate Charge	V_{GS} = 0V to 4.5V; V_{DD} = 15V, I_D = 9.0A		5.0	7.0	nC
Q_{gs}	Total Gate Charge	V_{DD} = 15V, I_D = 9.0A		1.8		nC
Q_{gd}	Gate to Drain “Miller” Charge			2.2		nC

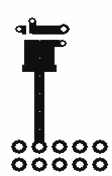
Drain-Source Diode Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0V, I_S = 9.0A (Note 2)		0.86	1.2	V
		V_{GS} = 0V, I_S = 1.6A (Note 2)		0.76	1.2	
t_{rr}	Reverse Recovery Time	I_F = 9.0A, di/dt = 100A/μs		13	18	ns
Q_{rr}	Reverse Recovery Charge			3	10	nC

NOTES:
1. $R_{\theta JA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 53°C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 125°C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300μs, Duty cycle < 2.0%.
3. Starting T_J = 25^{o}C; N-ch: L = 1mH, I_{AS} = 7A, V_{DD} = 30V, V_{GS} = 10V.

Typical Characteristics T_J = 25°C unless otherwise noted

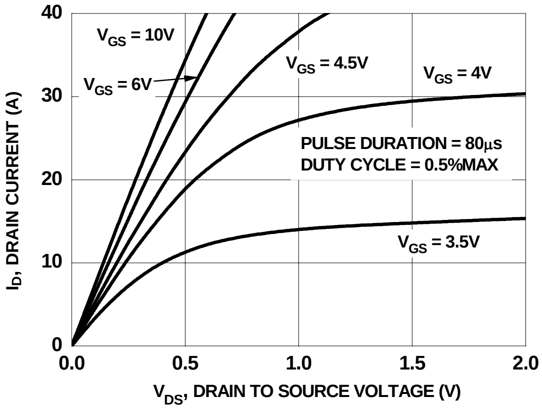


Figure 1. On-Region Characteristics

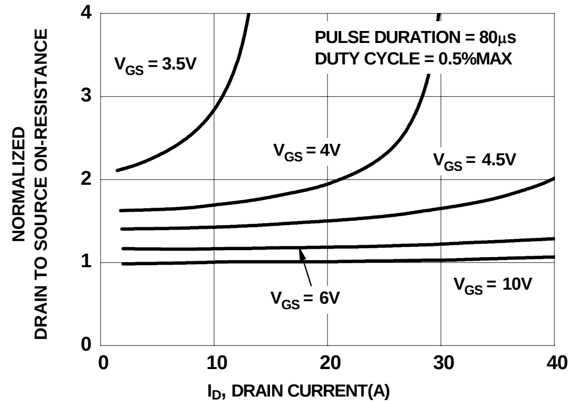


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

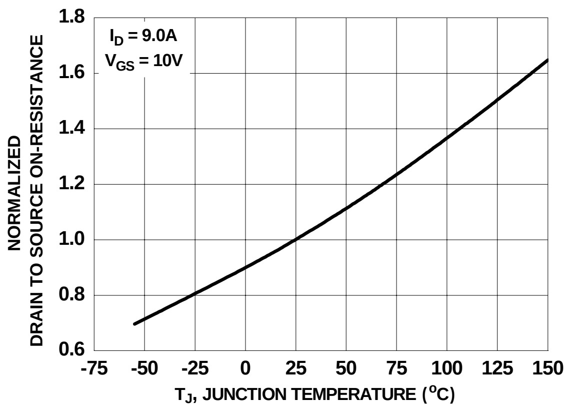


Figure 3. Normalized On-Resistance vs Junction Temperature

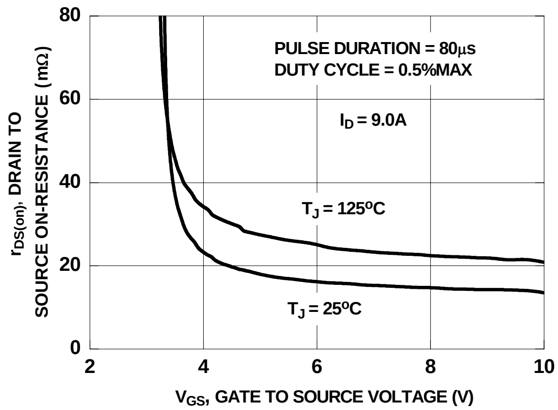


Figure 4. On-Resistance vs Gate to Source Voltage

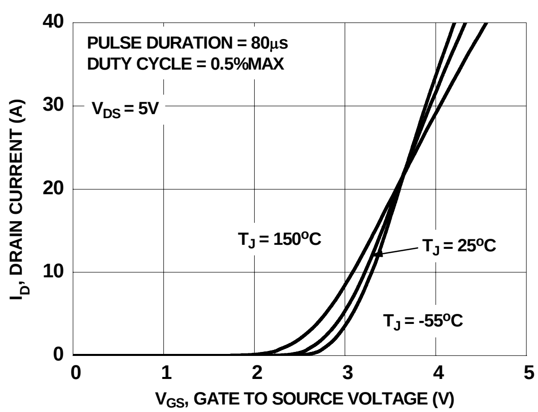


Figure 5. Transfer Characteristics

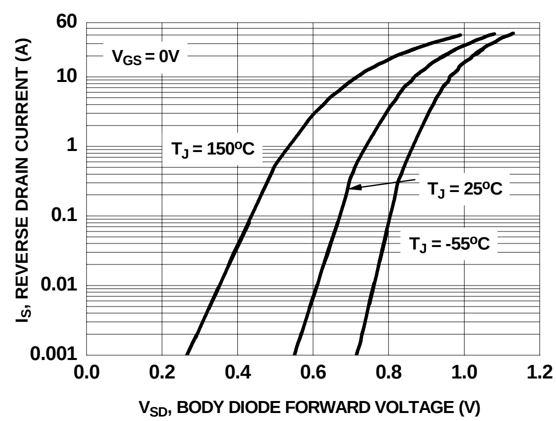


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25°C unless otherwise noted

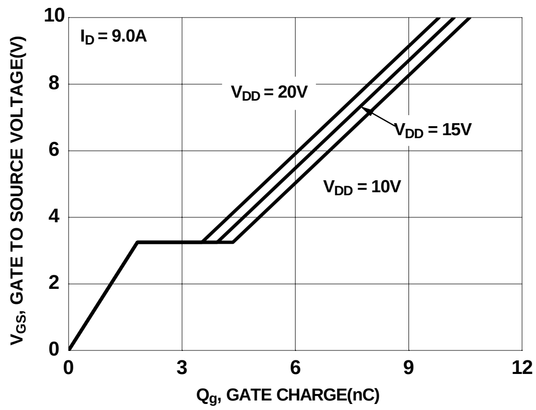


Figure 7. Gate Charge Characteristics

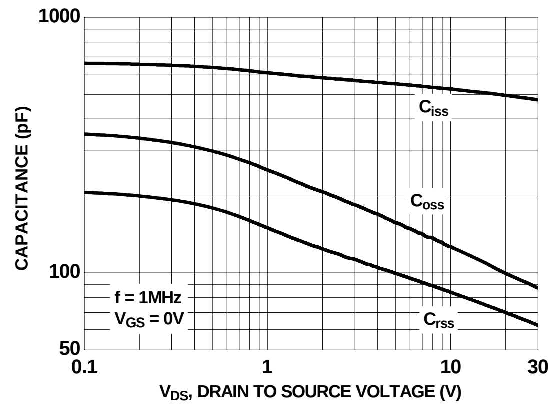


Figure 8. Capacitance vs Drain to Source Voltage

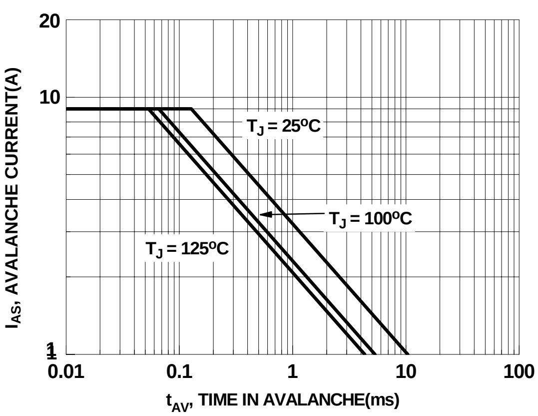


Figure 9. Unclamped Inductive Switching Capability

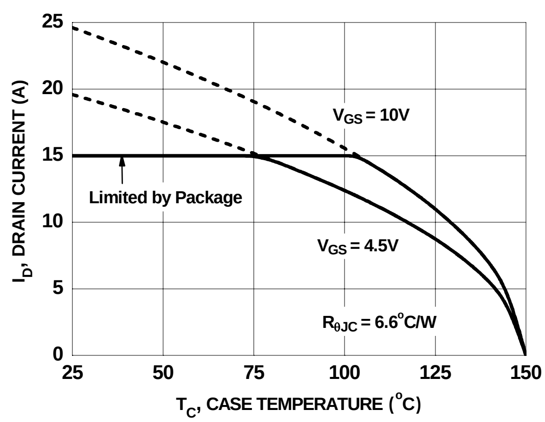


Figure 10. Maximum Continuous Drain Current vs Case Temperature

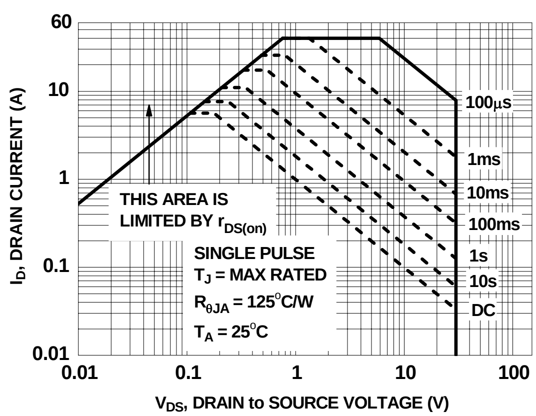


Figure 11. Forward Bias Safe Operating Area

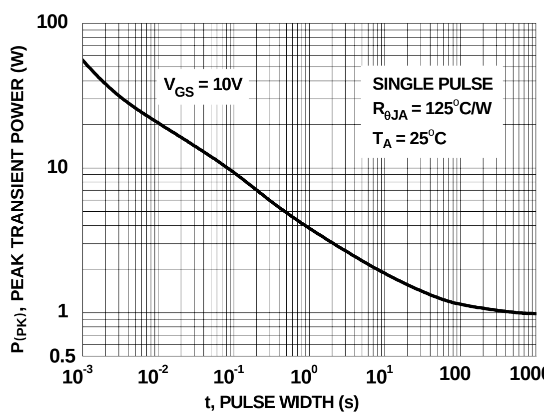


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25°C unless otherwise noted

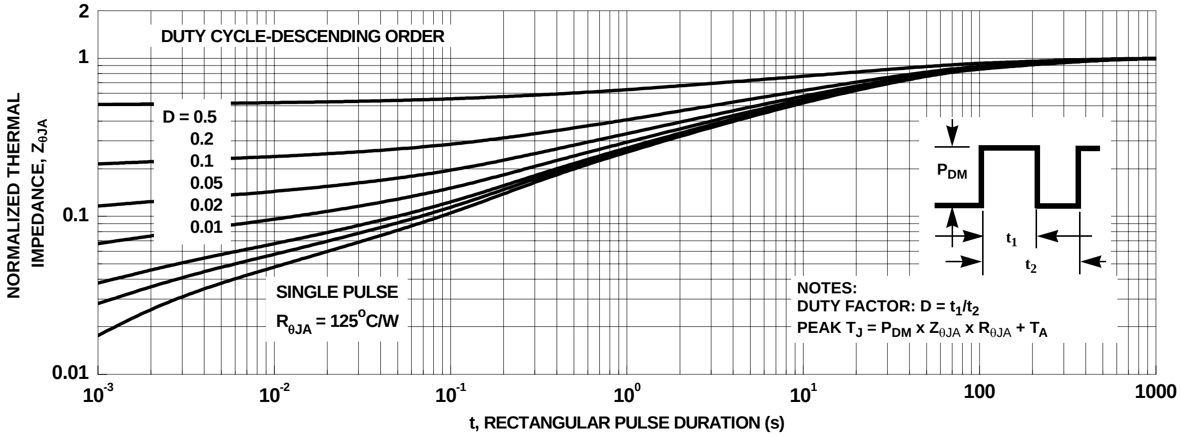
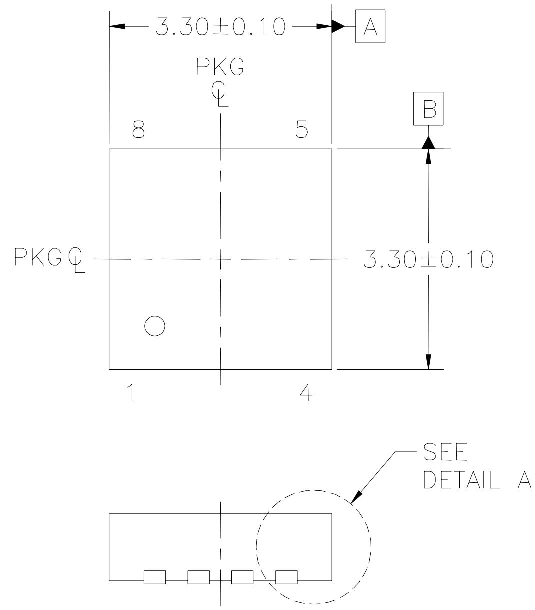
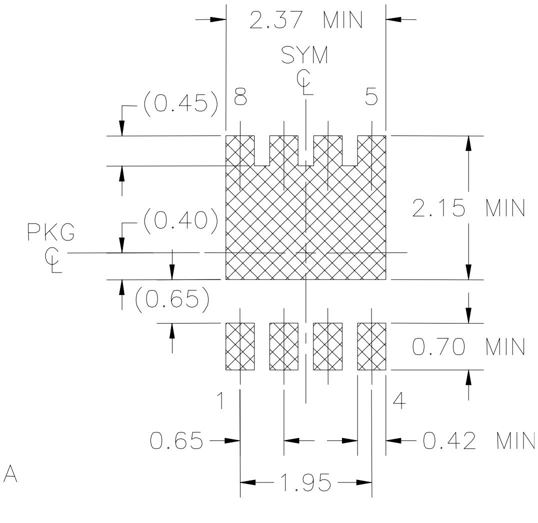


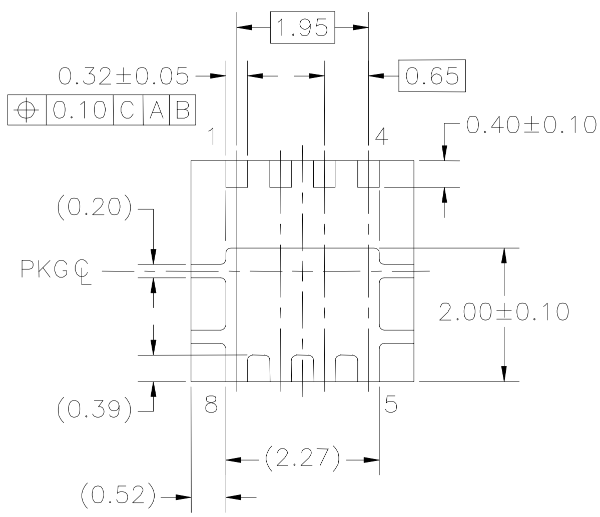
Figure 13. Transient Thermal Response Curve

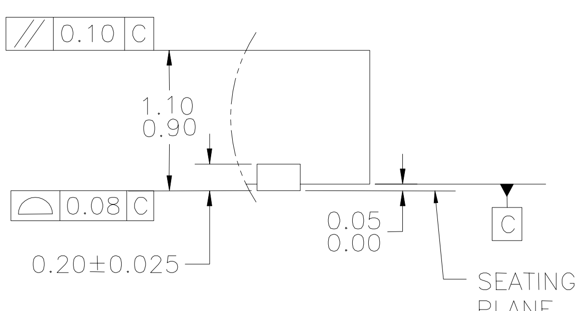
Dimensional Outline and Pad Layout





LAND PATTERN
RECOMMENDATION





DETAIL A
SCALE: 2X

NOTES: UNLESS OTHERWISE SPECIFIED

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OR MOLD FLASH. MOLD FLASH OR
BURRS DOES NOT EXCEED 0.10MM.
D) DIMENSIONING AND TOLERANCING PER
ASME Y14.5M-1994.
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Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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