High Efficiency, Main Power Supply Controller for Notebook Computers

General Description

The RT8206L/M dual step-down, Switch-Mode Power-Supply (SMPS) controller generates logic-supply voltages in battery-powered systems. The RT8206L/M includes two Pulse-Width Modulation (PWM) controllers fixed at 5V/3.3V or adjustable from 2V to 5.5V. An optional external charge pump can be monitored through SECFB (RT8206L). This device also features a linear regulator providing a fixed 5V output. The linear regulator provides up to 70mA output current with automatic linear regulator bootstrapping to the BYP input. The RT8206L/M includes on-board power-up sequencing, the power good outputs, internal soft-start, and internal soft-discharge output that prevents negative voltages on shutdown.

A constant on-time PWM control scheme operates without sense resistors and provides 100ns response to load transients while maintaining a relatively constant switching frequency. The unique ultrasonic mode maintains the switching frequency above 25kHz, which eliminates noise in audio applications. Other features include Diode-Emulation Mode (DEM), which maximizes efficiency in light-load applications, and fixed frequency PWM mode, which reduces RF interference in sensitive application.

The RT8206L/M is available in a WQFN-32L 5x5 package.

Ordering Information

RT8206□□□

- Package Type
  - QW : WQFN-32L 5x5 (W-Type)
- Lead Plating System
  - G : Green (Halogen Free and Pb Free)
  - Z : ECO (Ecological Element with Halogen Free and Pb free)
- L : With SECFB
- M : Without SECFB

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

- **Wide Input Voltage Range 6V to 25V**
- **Dual Fixed 5V/3.3V Outputs or Adjustable from 2V to 5.5V, 1.5% Accuracy**
- **Secondary Feedback Input Maintains Charge Pump Voltage (RT8206L)**
- **Independent Enable and Power Good**
- **5V Fixed LDO Output : 70mA**
- **2V Reference Voltage ±1% : 50μA**
- **Constant ON-Time Control with 100ns Load Step Response**
- **Frequency Selectable via TON Setting**
- **$R_{DS(ON)}$ Current Sensing and Programmable Current Limit**
- **4700ppm/°C $R_{DS(ON)}$ Current Sensing**
- **Selectable PWM, DEM or Ultrasonic Mode**
- **Internal Soft-Start with Current Limiting and Soft-Discharge**
- **High Efficiency Up to 97%**
- **5mW Quiescent Power Dissipation**
- **Thermal Shutdown**
- **RoHS Compliant and Halogen Free**

Applications

- Notebook and Sub-Notebook Computers
- 3-Cell and 4-Cell Li+ Battery-Powered Devices

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Marking Information

RT8206LGQW

RT8206LGQW : Product Number
YMDNN : Date Code

RT8206MGQW

RT8206MGQW : Product Number
YMDNN : Date Code

RT8206LZQW

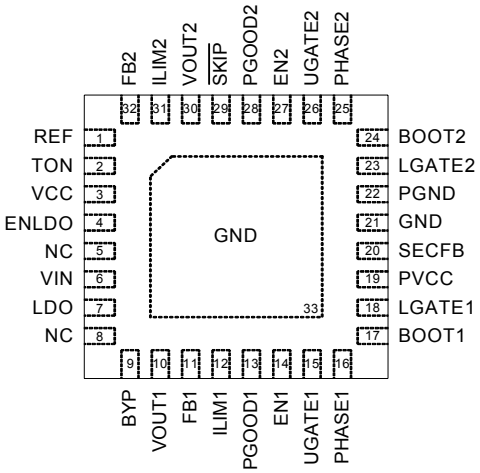
RT8206LZQW : Product Number
YMDNN : Date Code

RT8206MZQW

RT8206MZQW : Product Number
YMDNN : Date Code

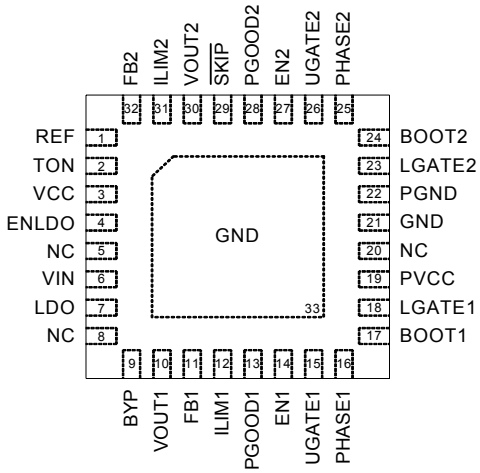
Pin Configurations

(TOP VIEW)



WQFN-32L 5x5

RT8206L



WQFN-32L 5x5

RT8206M

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Typical Application Circuit

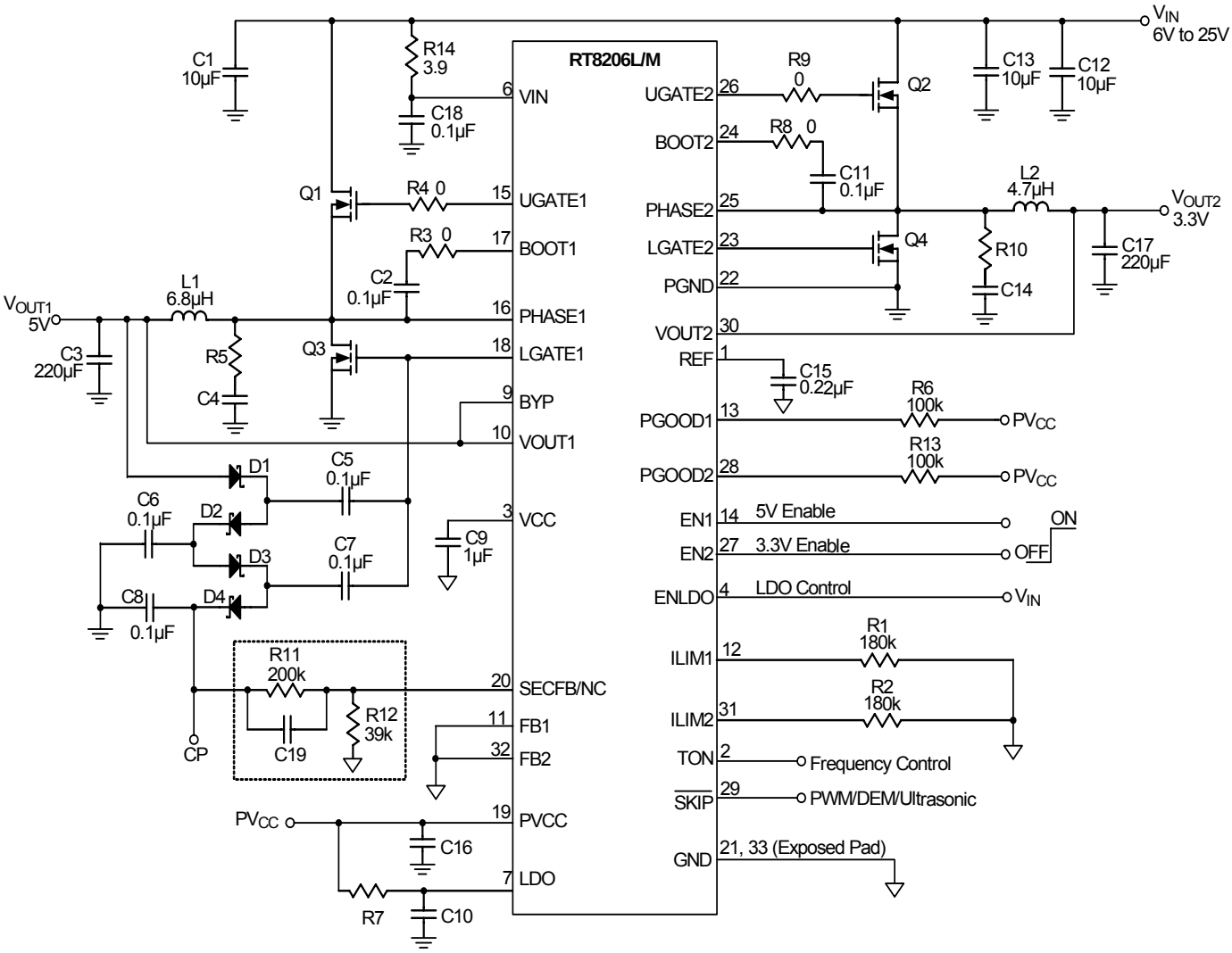

Figure 1. Fixed Voltage Regulator

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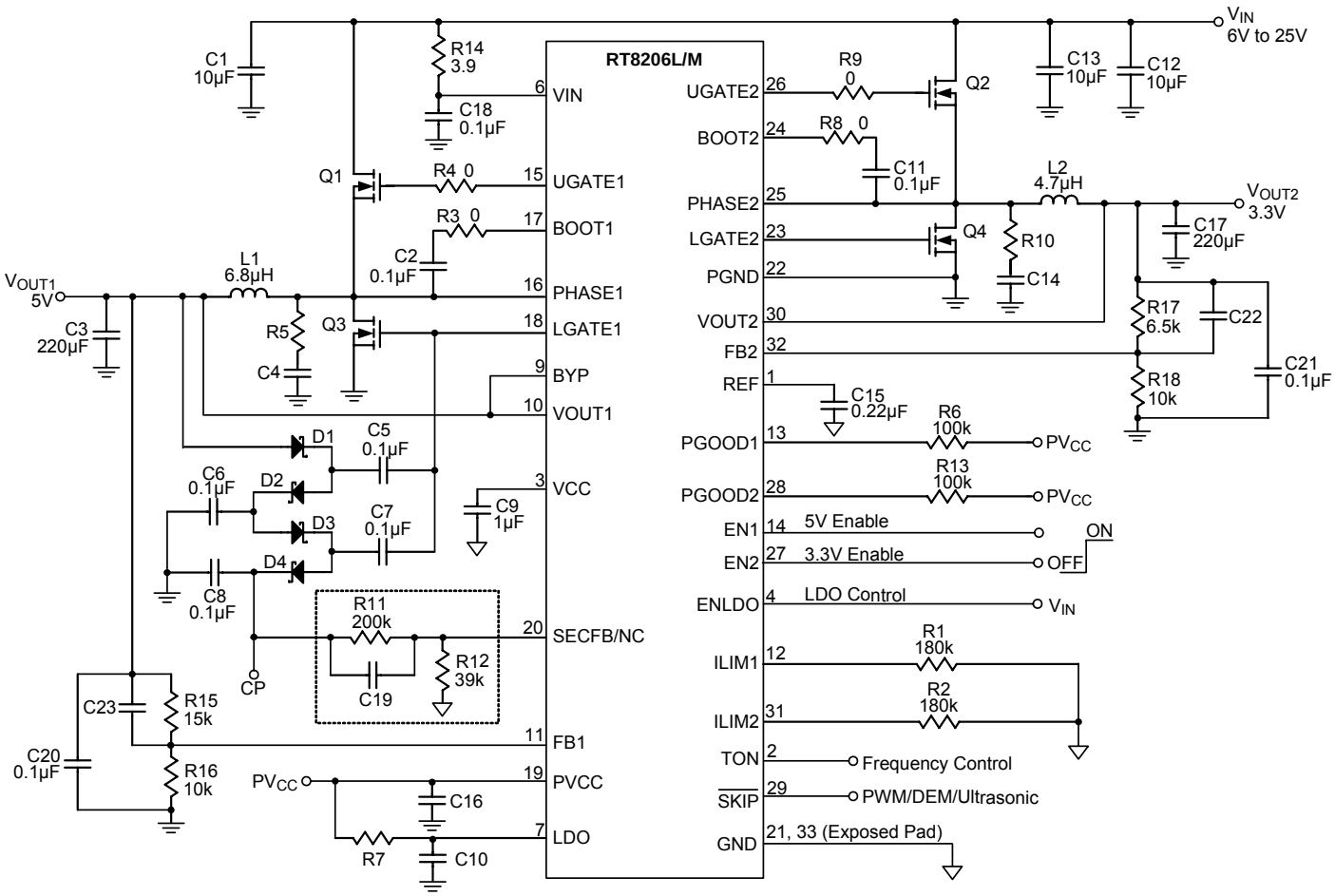

Figure 2. Adjustable Voltage Regulator

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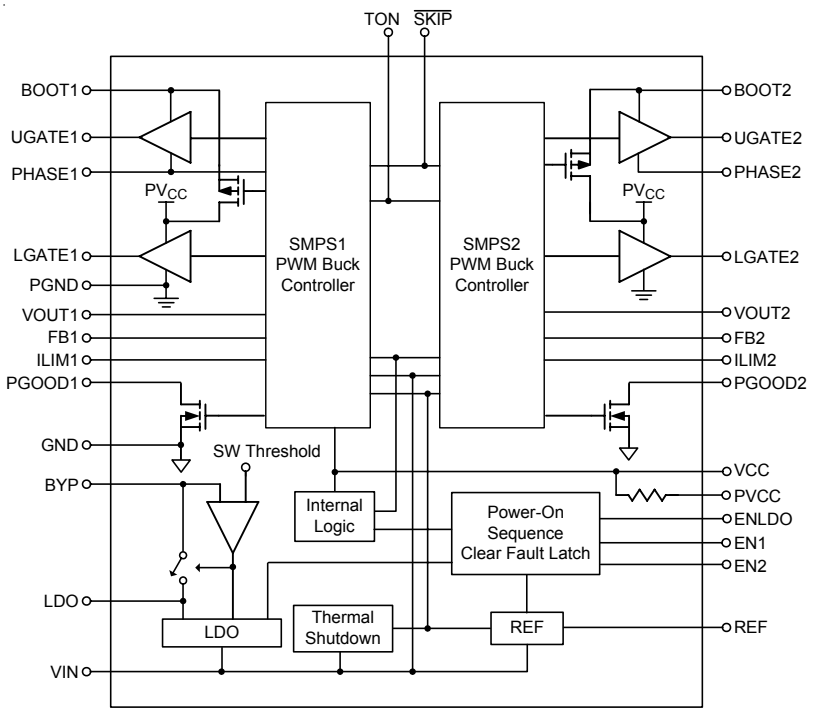
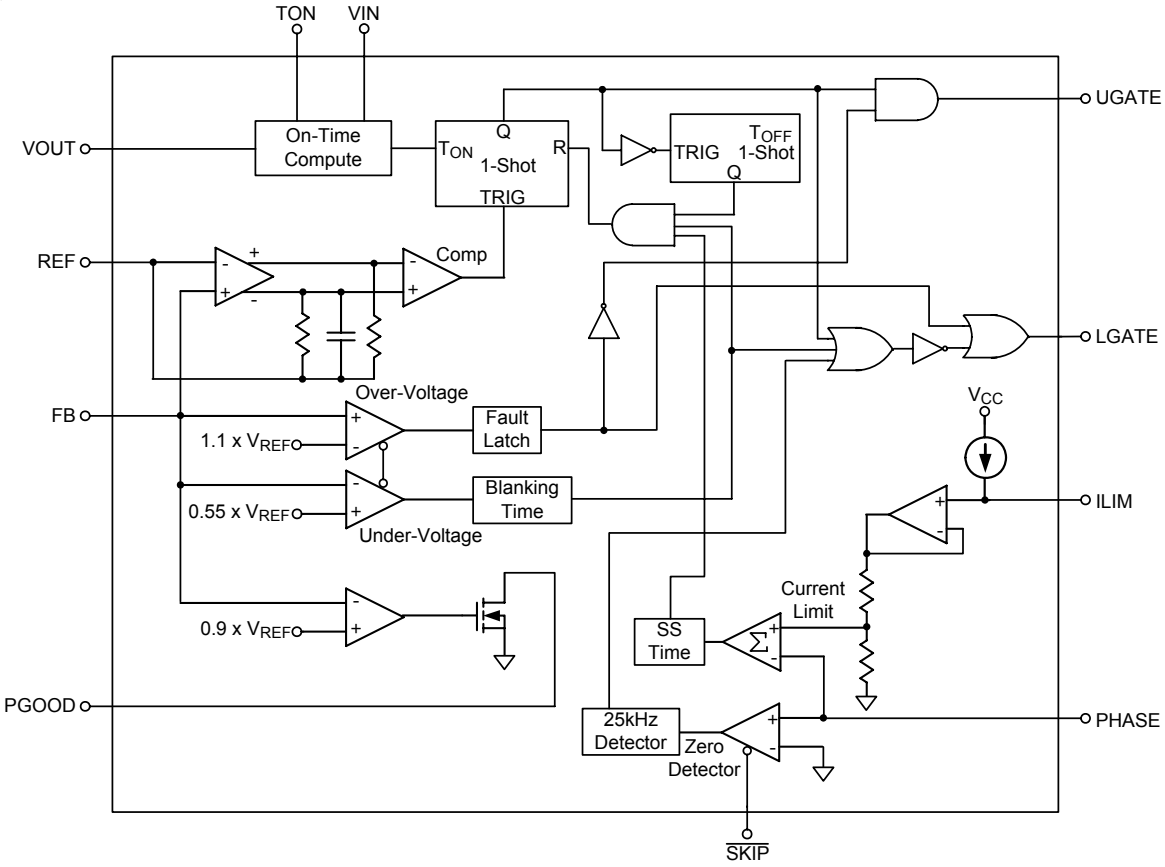
Function Block Diagram



Function Block Diagram



PWM Controller (One Side)

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Functional Pin Description

REF (Pin 1)

2V Reference Output. Bypass to GND with a 0.22μF capacitor. REF can source up to 50μA for external loads. Loading REF degrades FBx and output accuracy according to the REF load-regulation error.

TON (Pin 2)

Frequency Select Input. (VOUT1/VOUT2 switching frequency, respectively) :

TON = VCC, (200kHz / 300kHz)

TON = REF, (300kHz / 400kHz)

TON = GND, (400kHz / 500kHz)

VCC (Pin 3)

Analog Supply Voltage Input for the PWM Core. Bypass to GND with a 1μF ceramic capacitor

ENLDO (Pin 4)

LDO Enable Input. REF and LDO are enabled if ENLDO is within logic high level and disabled if ENLDO is less than the logic low level.

NC (Pin 5, 8)

No Internal Connection.

VIN (Pin 6)

Power Supply Input. VIN is used for the constant on-time PWM one shot circuits. VIN is also used to power the linear regulators. The linear regulators are powered by SMPS1 if VOUT1 is set greater than 4.66V and BYP is tied to VOUT1. Connect VIN to the battery input and bypass with a 1μF capacitor.

LDO (Pin 7)

Linear-Regulator Output. LDO can provide a total of 70mA external loads. The LDO regulates a fixed 5V output. When the BYP is within 5V switchover threshold, the internal regulator shuts down and the LDO output pin connects to BYP through a 1.5Ω switch. Bypass LDO output with a minimum of 4.7μF ceramic.

BYP (Pin 9)

Switchover Source Voltage Input for LDO.

VOUT1 (Pin 10)

SMPS1 Output Voltage Sense Input. Connect this pin to the SMPS1 output. VOUT1 is an input to the constant on-time-PWM one-shot circuit. It also serves as the SMPS1 feedback input in fixed-voltage mode.

FB1 (Pin 11)

SMPS1 Feedback Input. Connect FB1 to VCC or GND for fixed 5V operation. Connect FB1 to a resistive voltage-divider from VOUT1 to GND to adjust output from 2V to 5.5V.

ILIM1 (Pin 12)

SMPS1 Current Limit Adjustment. The GND – PHASE1 current-limit threshold is 1/10th the voltage seen at ILIM1 over a 0.5V to 2.5V range. There is an internal 5μA current source from VCC to ILIM1. The logic current limit threshold defaults to 100mV if ILIM1 is higher than (VCC – 1V).

PGOOD1 (Pin 13)

SMPS1 Power Good Open-Drain Output. PGOOD1 is low when the SMPS1 output voltage is more than 10% below the normal regulation point or during soft-start. PGOOD1 is in high impedance when the output is in regulation and the soft-start circuit has terminated. PGOOD1 is low in shutdown.

EN1 (Pin 14)

SMPS1 Enable Input. The SMPS1 will be enabled if EN1 is greater than the logic high level and disabled if EN1 is less than the logic low level. If EN1 is connected to REF, SMPS1 starts after SMPS2 reaches regulation (delay start). Drive EN1 below 0.8V to clear fault level and reset the fault latches.

UGATE1 (Pin 15)

High Side MOSFET Floating Gate-Driver Output for SMPS1. UGATE1 swings between PHASE1 and BOOT1.

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PHASE1 (Pin 16)

Inductor Connection for SMPS1. PHASE1 is the internal lower supply rail for the UGATE1 high side gate driver. PHASE1 is the current-sense input for the SMPS1.

BOOT1 (Pin 17)

Boost Flying Capacitor Connection for SMPS1. Connect to an external capacitor according to the typical application circuits.

LGATE1 (Pin 18)

SMPS1 Synchronous-Rectifier Gate-drive Output. LGATE1 swings between PGND and PVCC.

PVCC (Pin 19)

Supply Voltage for Low Side MOSFET driver LGATEx. Connect a 5V power source to the PVCC pin (bypass with 1μF MLCC capacitor to PGND if necessary). There is an internal 10Ω connecting from PVCC to VCC. Make sure that both VCC and PVCC are bypassed with 1μF MLCC capacitors.

SECFB (Pin 20) (RT8206L)

Charge Pump Feedback Input. The SECFB is used to monitor the optional external charge pump. Connect a resistive voltage-divider from the charge pump output to GND to detect the output. If SECFB drops below the threshold voltage, an ultrasonic pulse occurs to refresh the external charge pump driven by LGATE1 or LGATE2

NC (Pin 20) (RT8206M)

No Internal Connection.

GND [Pin 21, 33 (Exposed Pad)]

Analog Ground for both SMPS and LDO. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

PGND (Pin 22)

Power Ground for SMPS Controller. Connect PGND externally to the underside of the exposed pad.

LGATE2 (Pin 23)

SMPS2 Synchronous-Rectifier Gate-drive Output. LGATE2 swings between PGND and PVCC.

BOOT2 (Pin 24)

Boost Flying Capacitor Connection for SMPS2. Connect this pin to an external capacitor according to the typical application circuits.

PHASE2 (Pin 25)

Inductor Connection for SMPS2. PHASE2 is the internal lower supply rail for the UGATE2 high side gate driver. PHASE2 is the current sense input for the SMPS2.

UGATE2 (Pin 26)

High Side MOSFET Floating Gate-Driver Output for SMPS2. UGATE2 swings between PHASE2 and BOOT2.

EN2 (Pin 27)

SMPS2 Enable Input. The SMPS2 will be enabled if EN2 is greater than the logic high level and be disabled if EN2 is less than the logic low level. If EN2 is connected to REF, the SMPS2 starts after the SMPS1 reaches regulation (delay start). Drive EN2 below 0.8V to clear fault level and reset the fault latches.

PGOOD2 (Pin 28)

SMPS2 Power Good Open-Drain Output. PGOOD2 is low when the SMPS2 output voltage is more than 10% below the normal regulation point or during soft-start. PGOOD2 is high impedance when the output is in regulation and the soft-start circuit has terminated. PGOOD2 is low in shutdown.

$\overline{\text{SKIP}}$ (Pin 29)

SMPS Operation Mode Control.

$\overline{\text{SKIP}}$ = GND : DEM Mode operation

$\overline{\text{SKIP}}$ = REF : Ultrasonic Mode operation

$\overline{\text{SKIP}}$ = VCC : PWM Mode operation.

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VOUT2 (Pin 30)

SMPS2 Output Voltage Sense Input. Connect this pin to the SMPS2 output. VOUT2 is an input to the constant on-time-PWM one-shot circuit. It also serves as the SMPS2 feedback input in fixed-voltage mode.

ILIM2 (Pin 31)

SMPS2 Current-Limit Adjustment. The GND – PHASE2 current limit threshold is 1/10th the voltage seen at ILIM2 over a 0.5V to 2.5V range. There is an internal 5μA current source from VCC to ILIM2. The logic current limit threshold is default to 100mV value if ILIM2 is higher than (VCC – 1V).

FB2 (Pin 32)

SMPS2 Feedback Input. Connect FB2 to VCC or GND for fixed 3.3V operation. Connect FB2 to a resistive voltage-divider from VOUT2 to GND to adjust output from 2V to 5.5V.

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Absolute Maximum Ratings (Note 1)

- VIN, ENLDO to GND ---------- –0.3V to 30V
- PHASEx to GND
  - DC ---------- –0.3V to 30V
  - <20ns ---------- –8V to 38V
- BOOTx to PHASEx ---------- –0.3V to 6V
- VCC, ENx, $\overline{SKIP}$, TON, PVCC, PGOODx, to GND ---------- –0.3V to 6V
- LDO, FBx, VOUTx, SECFB, REF, ILIMx to GND ---------- –0.3V to (V_{CC} + 0.3V)
- UGATEx to PHASEx
  - DC ---------- –0.3V to (PV_{CC} + 0.3V)
  - <20ns ---------- –5V to 7.5V
- LGATEx, BYP to GND
  - DC ---------- –0.3V to (PV_{CC} + 0.3V)
  - <20ns ---------- –2.5V to 7.5V
- PGND to GND ---------- –0.3V to 0.3V
- Power Dissipation, P_D @ T_A = 25°C
  - WQFN-32L 5x5 ---------- 2.778W
- Package Thermal Resistance (Note 2)
  - WQFN-32L 5x5, θ_{JA} ---------- 36°C/W
  - WQFN-32L 5x5, θ_{JC} ---------- 6°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Input Voltage, VIN ---------- 6V to 25V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

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Electrical Characteristics

(V_{IN} = 12V, V_{EN1} = V_{EN2} = V_{CC} = 5V, V_{BYP} = 5V, PV_{CC} = 5V, V_{ENLDO} = 5V, No Load on LDO, VOUT1, VOUT2 and REF, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Input Supply							
VIN Standby Supply Current	I_{VIN_SBY}	V_{IN} = 6V to 25V, Both SMPS Off, V_{ENLDO} = 5V		--	180	250	μA
VIN Shutdown Supply Current	I_{VIN_SHDH}	V_{IN} = 6V to 25V, ENx = ENLDO = GND		--	20	40	μA
Quiescent Power Consumption	I_Q	Both SMPSs On, FB1 = $\overline{SKIP}$ = GND, FB2 = V_{CC}, V_{OUT1} = V_{BYP} = 5.3V, V_{OUT2} = 3.5V (Note 5)		--	5	7	mW
SMPS Output and FB Voltage							
VOUT1 Output Voltage in Fixed Mode	V_{OUT1}	V_{IN} = 6V to 25V, FB1= GND, $V_{\overline{SKIP}}$ = 5V		4.975	5.05	5.125	V
VOUT2 Output Voltage in Fixed Mode	V_{OUT2}	V_{IN} = 6V to 25V, FB2 = V_{CC}, $V_{\overline{SKIP}}$ = 5V		3.285	3.33	3.375	V
SECFB Voltage	V_{SECFB}	V_{IN} = 6V to 25V (RT8206L)		1.92	2	2.08	V
Output Voltage Adjust Range		SMPS1, SMPS2		2	--	5.5	V
FBx Adjustable Mode Threshold Voltage		Fixed or Adj-Mode comparator threshold		0.2	0.4	0.55	V
FBx in Output Adjustable Mode	V_{LOAD}	Either SMPS, $\overline{SKIP}$ = V_{CC}		1.975	2	2.025	V
		Either SMPS, $\overline{SKIP}$ = REF		--	2.012	--	V
		Either SMPS, $\overline{SKIP}$ = GND		--	2.012	--	V
Line Regulation	V_{LINE}	Either SMPS, V_{IN} = 6V to 25V		--	0.005	--	%/V
On-Time							
On-Time Pulse Width	t_{ON}	TON = V_{CC}	SMPS1 = 5.05V (200kHz)	1895	2105	2315	ns
			SMPS2 = 3.33V (300kHz)	832.5	925	1018	
		TON = REF	SMPS1 = 5.05V (300kHz)	1227	1403	1579	
			SMPS2 = 3.33V (400kHz)	606	694	782	
		TON = GND	SMPS1 = 5.05V (400kHz)	895	1052	1209	
			SMPS2 = 3.33V (500kHz)	475	555	635	
Minimum Off-Time	$t_{OFF\ (MIN)}$			200	300	400	ns
Ultrasonic Mode Frequency		$\overline{SKIP}$ = REF		25	33	--	kHz
Soft-Start							
Soft-Start Time	t_{SSx}	Zero to 200mV current limit threshold from ENx enable		--	2	--	ms
Current Sense							
Current Limit Threshold (Default)		V_{ILIMx} = V_{CC}, GND – PHASEx		85	100	115	mV
Current Limit Current Source	I_{LIMX}			4.75	5	5.25	μA

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Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
I_{LIM} Current Temperature Coefficient		On the basis of 25°C		--	4700	--	ppm/°C
I_{LIM} Adjustment Range		$V_{ILIMx} = I_{LIMx} \times R_{ILIMx}$		0.5	--	2	V
Current-Limit Threshold		GND – PHASEx	V_{ILIMx} = 0.5V	40	50	60	mV
			V_{ILIMx} = 1V	85	100	115	
			V_{ILIMx} = 2V	180	200	220	
Zero-Current Threshold		$\overline{SKIP}$ = GND or REF, GND – PHASEx		--	3	--	mV
Internal Regulator and Reference							
LDO Output Voltage	V_{LDO}	BYP = GND, 6V < V_{IN} < 25V, 0 < I_{LDO} < 70mA		4.9	5	5.1	V
LDO Output Current	I_{LDO}	BYP = GND, V_{IN} = 6V to 25V		70	--	--	mA
LDO Short-Circuit Current		LDO = GND, BYP = GND		--	200	300	mA
LDO 5V Switchover Threshold to BYP	V_{BYP}	Falling Edge, Rising Edge with FB1 Regulation Point		4.53	4.66	4.79	V
LDO Switchover Equivalent Resistance	R_{SW}	LDO to BYP, 10mA		--	1.5	3	Ω
REF Output Voltage	V_{REF}	No External Load		1.98	2	2.02	V
REF Load Regulation		I_{REF} = 0 to 50μA		--	10	--	mV
REF Sink Current		REF in Regulation		10	--	--	μA
UVLO							
PVCC UVLO Threshold	V_{UVLO}	Rising Edge		--	4.35	4.5	V
		Falling Edge		3.9	4.05	4.2	
Power Good							
PGOODx Threshold		PGOOD Detect, FBx Falling edge		86	90	94	%
PGOODx Hysteresis		Rising Edge with Soft-Start Delay Time		--	3	--	%
PGOODx Propagation Delay		Falling Edge		--	10	--	μs
PGOODx Leakage Current		High State, Forced to 5.5V		--	--	1	μA
PGOODx Output Low Voltage		I_{SINK} = 4mA		--	--	0.3	V
Fault Detection							
OVP Trip Threshold	V_{FB_OVP}	OVP Detect, FBx Rising edge		108	112	116	%
OVP Propagation Delay		FBx with 50mV Overdrive		--	10	--	μs
UVP Trip Threshold		UVP Detect, FBx Falling edge		50	55	60	%
UVP Shutdown Blanking Time	t_{SHDN_UVP}	From ENx Enable		--	5	--	ms
Thermal Shutdown							
Thermal Shutdown	T_{SHDN}			--	150	--	°C
Thermal Shutdown Hysteresis	ΔT_{SHDN}			--	10	--	°C

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Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Logic Input							
FB1/FB2 Input Voltage	Low-Level		Internal Fixed V_{OUTx}	--	--	0.2	V
	High-Level		Internal Fixed V_{OUTx}	V_{CC} – 1	--	--	
$\overline{SKIP}$ Input Voltage			Low Level (DEM Mode)	--	--	0.8	V
			REF Level (Ultrasonic Mode)	1.8	--	2.3	
			High Level (PWM Mode)	2.5	--	--	
TON Setting Voltage			V_{OUT1} / V_{OUT2} (400kHz / 500kHz)	--	--	0.8	V
			V_{OUT1} / V_{OUT2} (300kHz / 400kHz)	1.8	--	2.3	
			V_{OUT1} / V_{OUT2} (200kHz / 300kHz)	2.5	--	--	
ENx Input Voltage			Clear Fault Level / SMPS Off Level	--	--	0.8	V
			Delay Start	1.8	--	2.3	
			SMPS On Level	2.5	--	--	
ENLDO Input Voltage		V_{ENLDO}	Rising Edge	1.2	1.6	2.0	V
			Falling Edge	0.94	1	1.06	
Input Leakage Current			V_{ENLDO} = 0V or 25V	–1	--	3	μA
			V_{ENx} = 0V or 5V	–1	--	1	
			V_{TON}, $V_{\overline{SKIP}}$ = 0V or 5V	–1	--	1	
			V_{FBx} = 0V or 5V	–1	--	1	
			V_{SECFB} = 0V or 5V (RT8206L)	–1	--	1	
Internal BOOT Switch							
Internal Boost Charging Switch On-Resistance			PVCC to BOOTx	--	40	80	Ω
Power MOSFET Drivers							
UGATEx On-Resistance			BOOTx to PHASEx Forced to 5V, High State	--	2.5	4	Ω
			BOOTx to PHASEx Forced to 5V, Low State	--	1.5	3	
LGATEx On-Resistance			LGATEx, High State	--	2.2	5	Ω
			LGATEx, Low State	--	0.6	1.5	
Dead Time			LGATE Rising	--	30	--	ns
			UGATE Rising	--	40	--	

Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. P_{VIN} + P_{PVCC}

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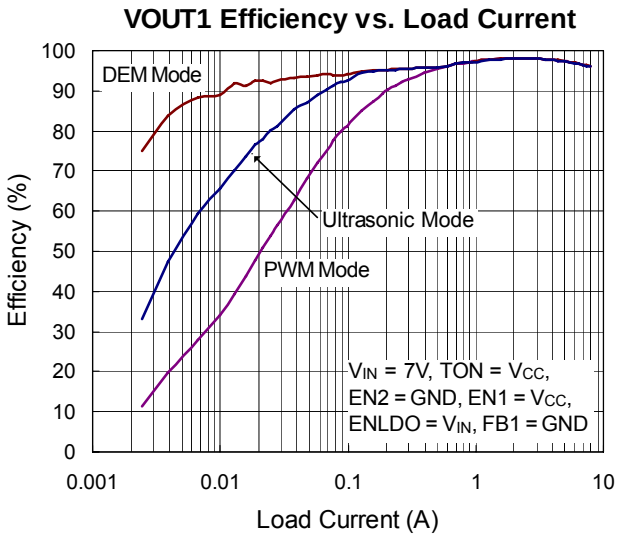
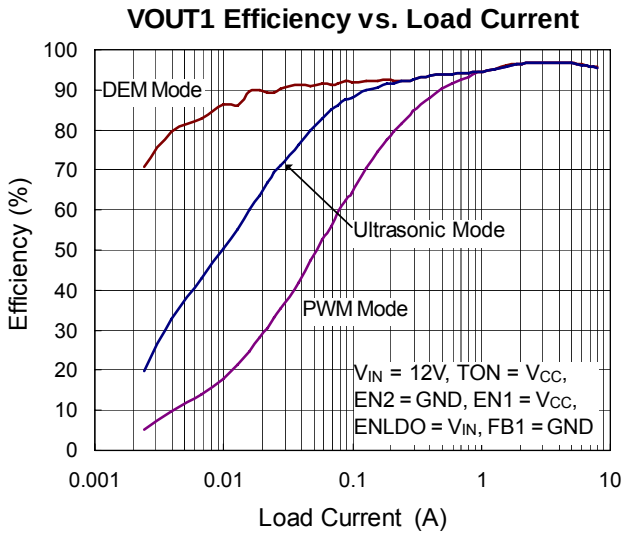
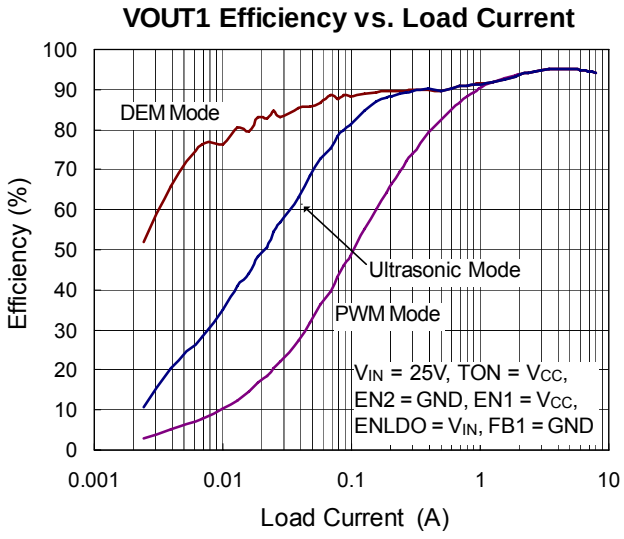
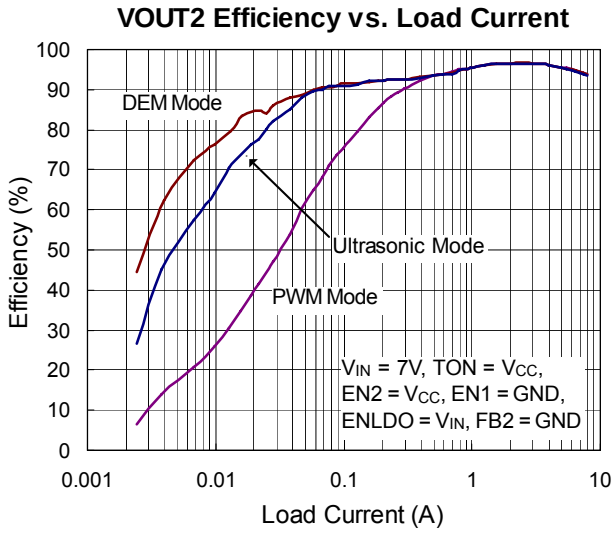
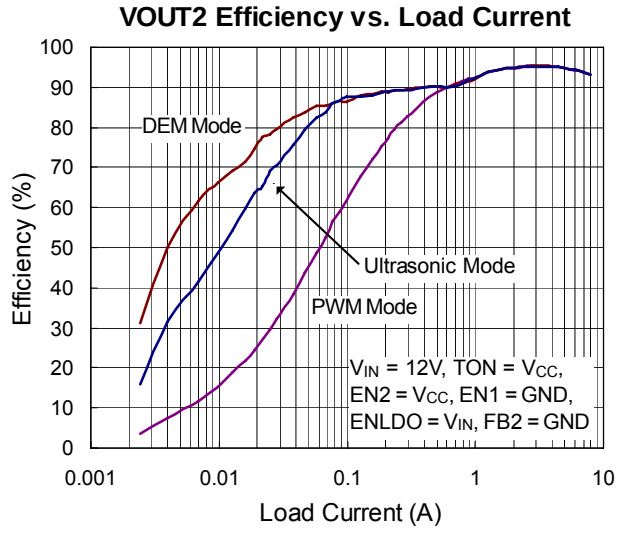
Typical Operating Characteristics

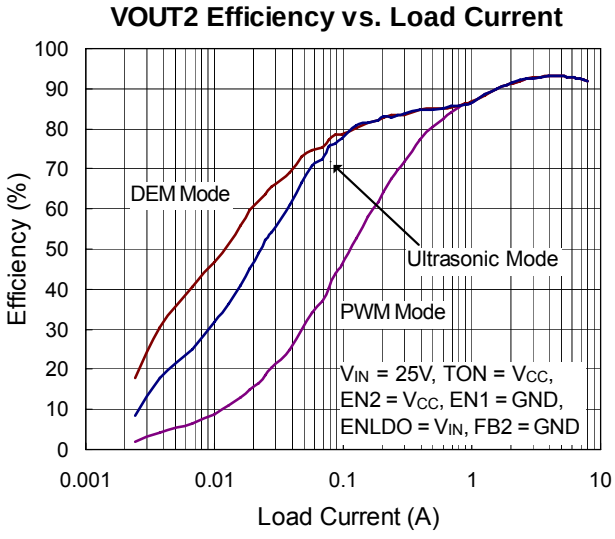












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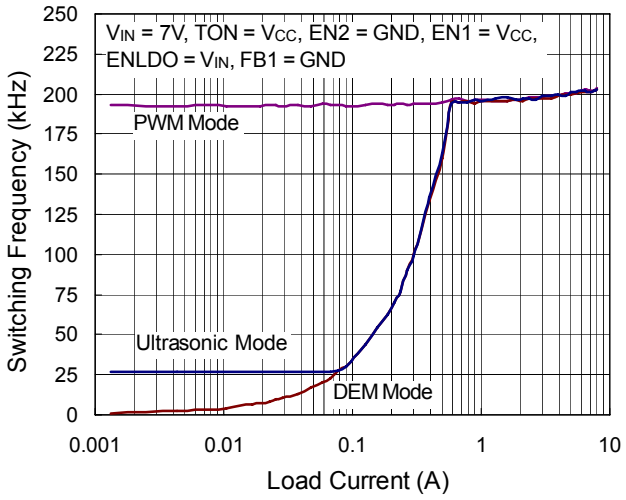
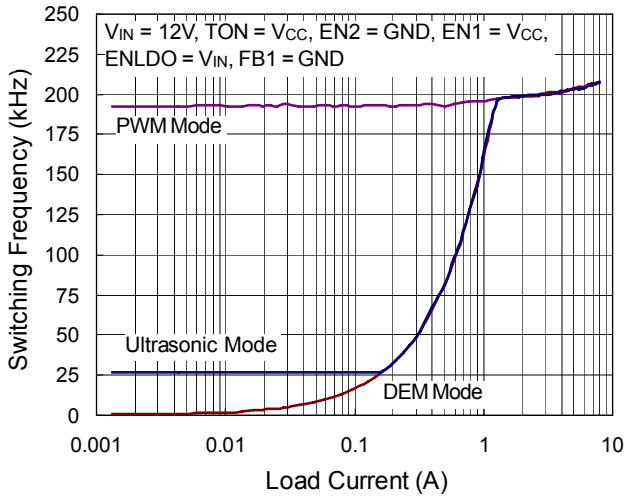
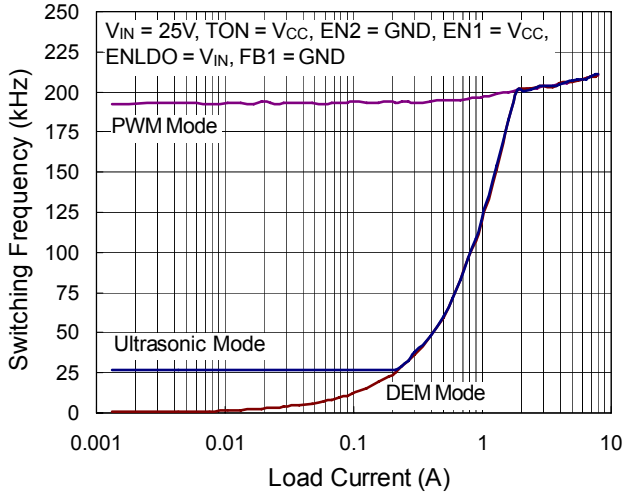
VOUT1 Switching Frequency vs. Load Current



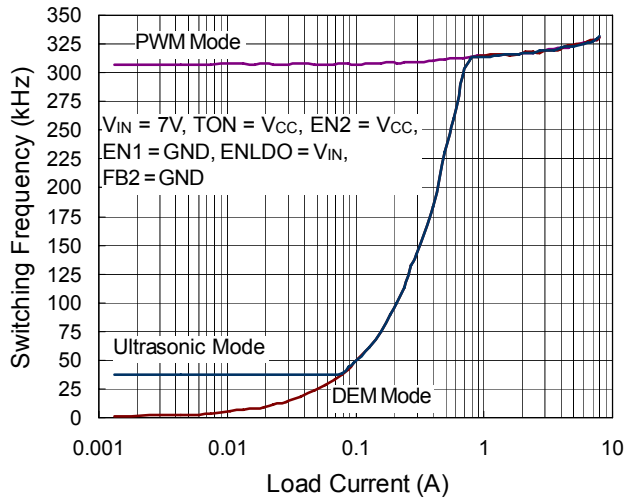
VOUT1 Switching Frequency vs. Load Current



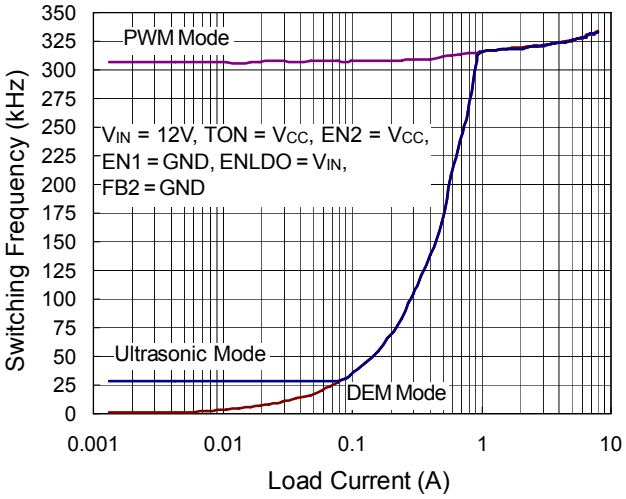
VOUT1 Switching Frequency vs. Load Current



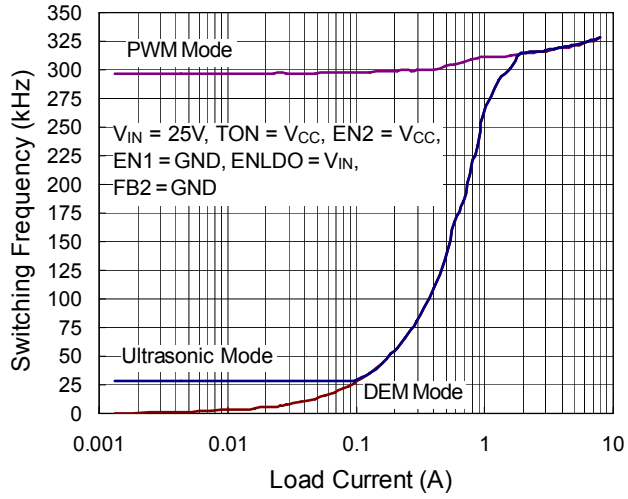
VOUT2 Switching Frequency vs. Load Current



VOUT2 Switching Frequency vs. Load Current



VOUT2 Switching Frequency vs. Load Current



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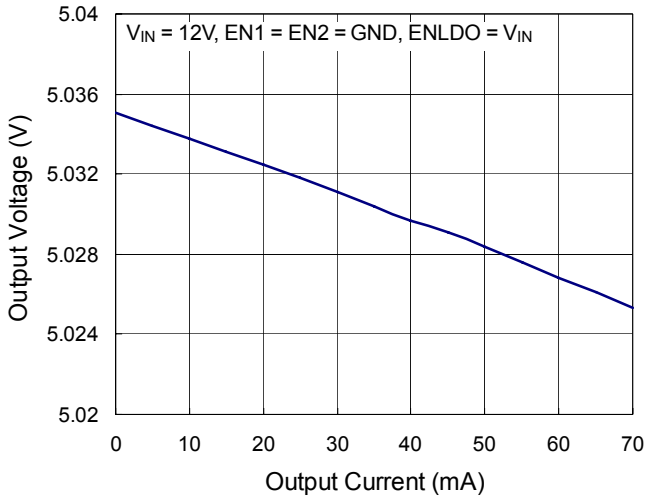
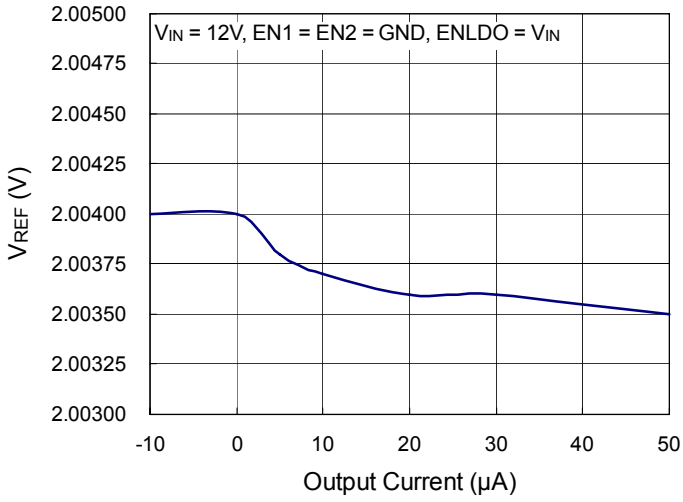
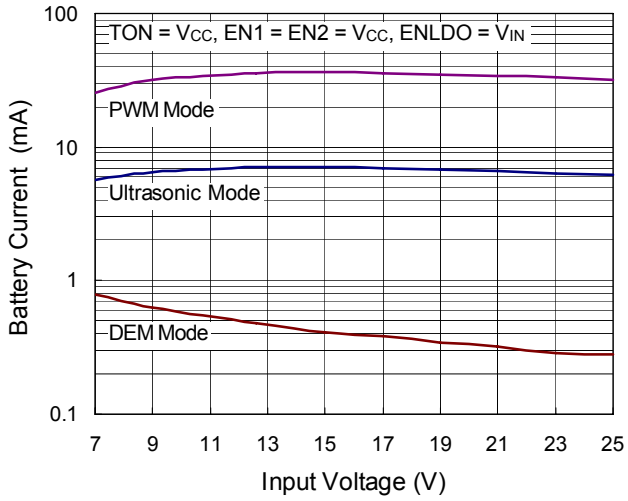
LDO Output Voltage vs. Output Current



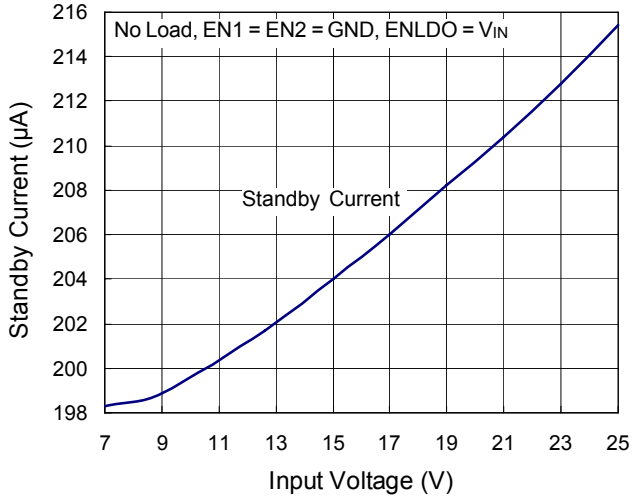
V_{REF} vs. Output Current



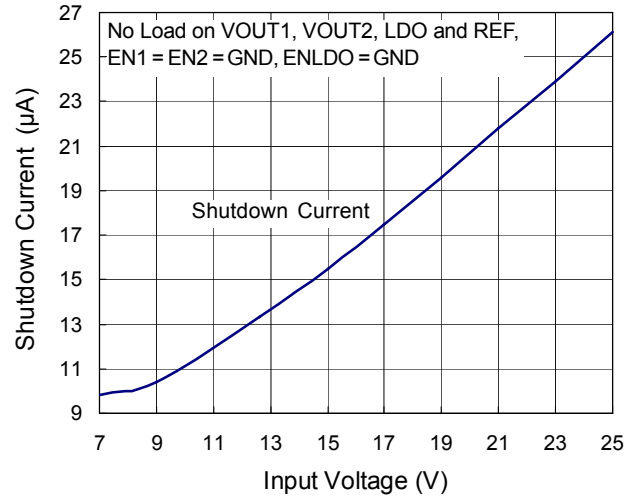
No Load Battery Current vs. Input Voltage



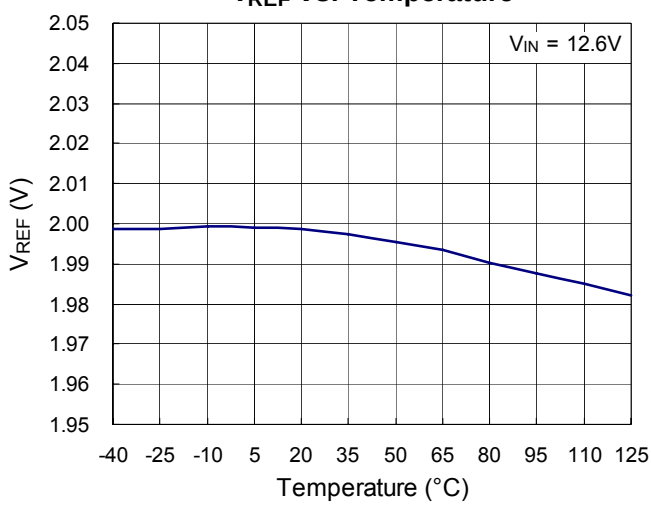
Standby Current vs. Input Voltage



Shutdown Current vs. Input Voltage



V_{REF} vs. Temperature



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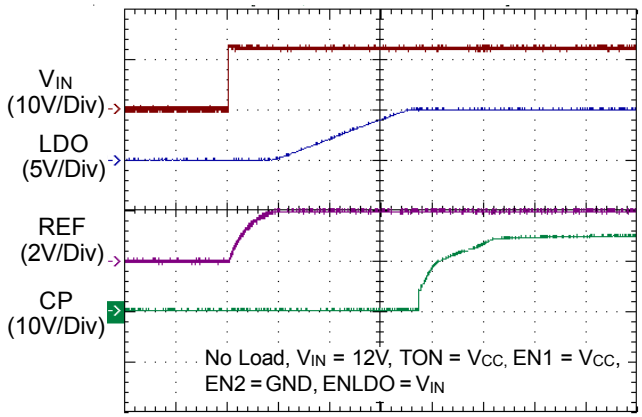
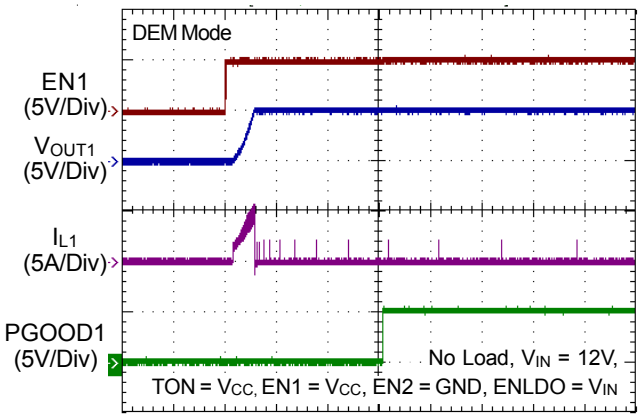
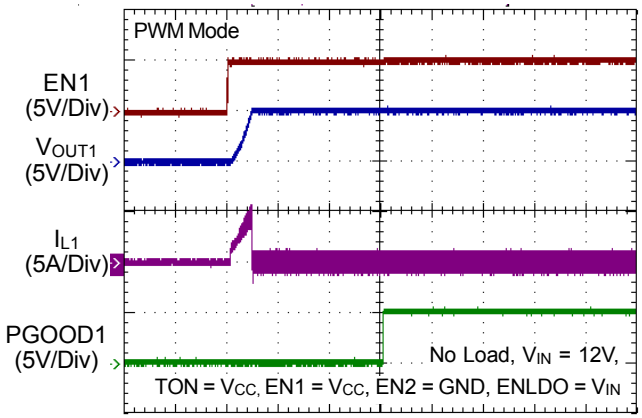
Power On from VIN



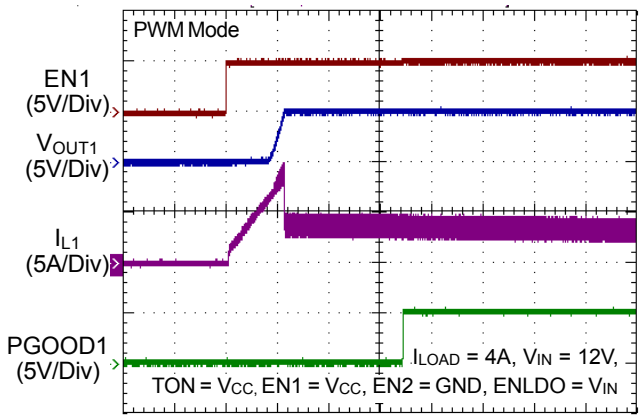
Power On from EN1



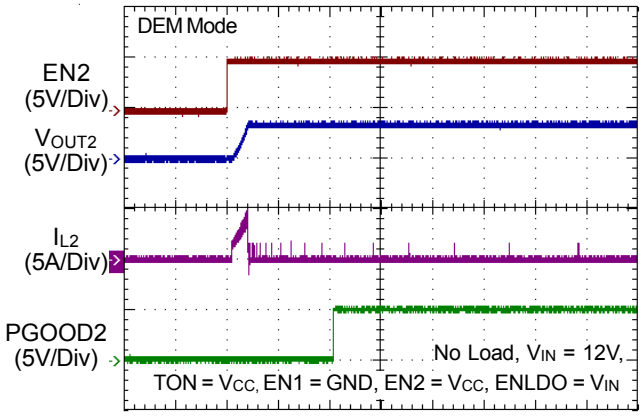
Power On from EN1



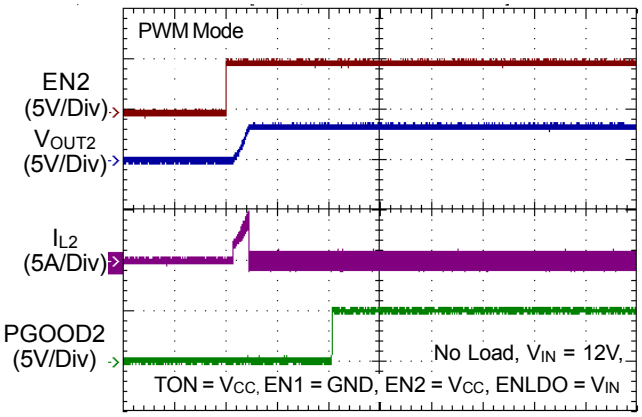
Power On from EN1



Power On from EN2



Power On from EN2



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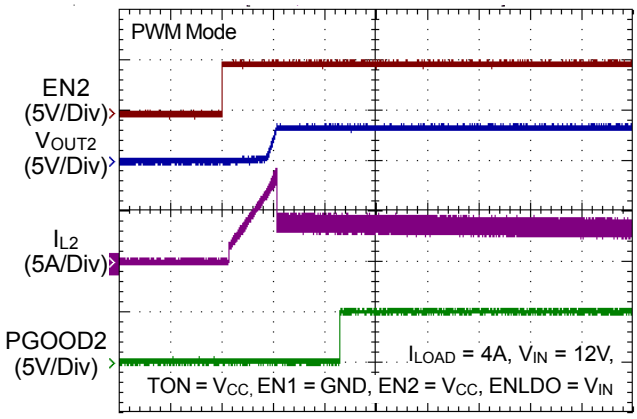
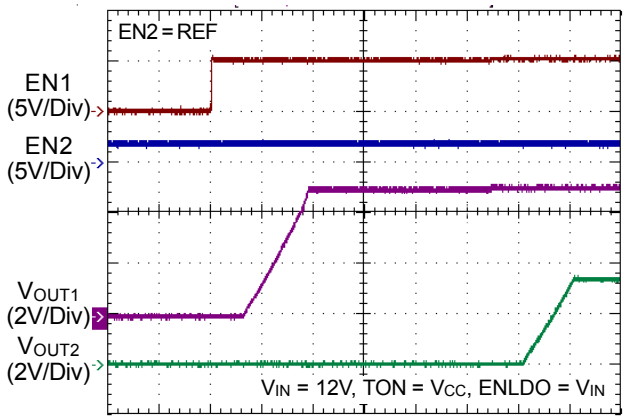
Power On from EN2



Power On from EN1 (Delay Start)



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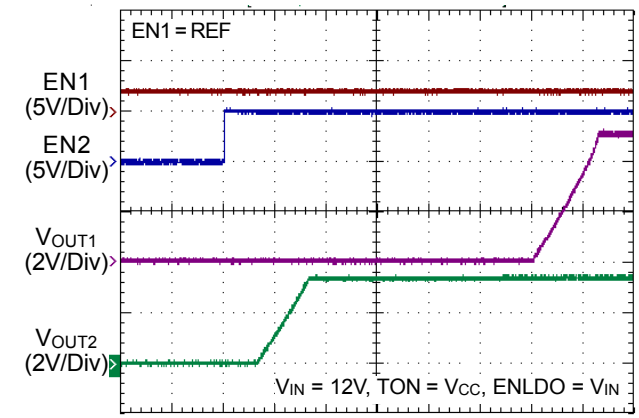
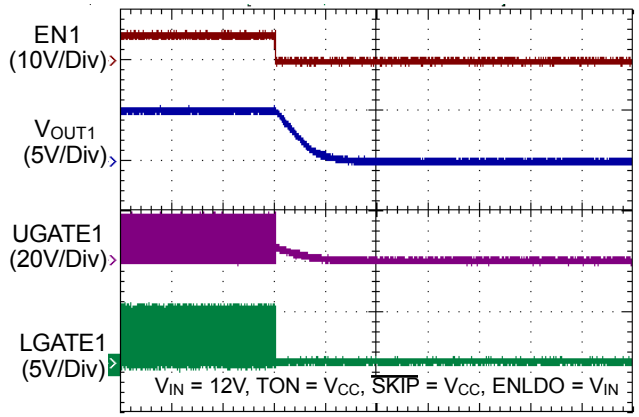
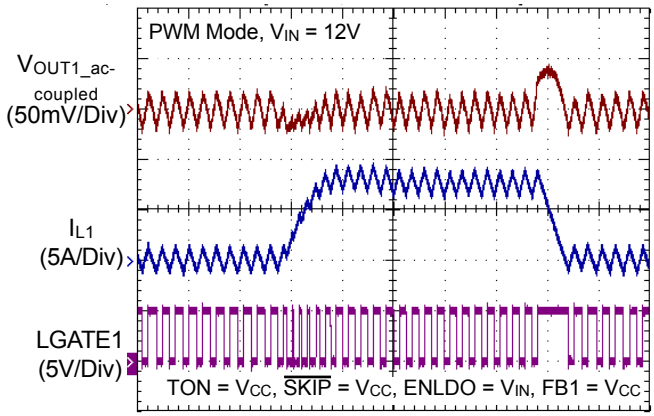


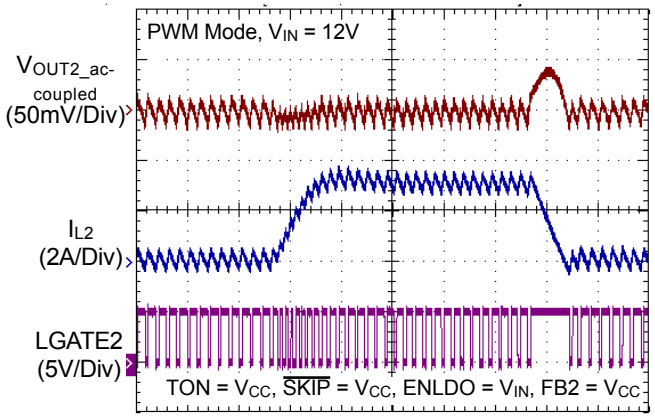
Power Off from EN1



VOUT1 Load Transient Response



VOUT2 Load Transient Response



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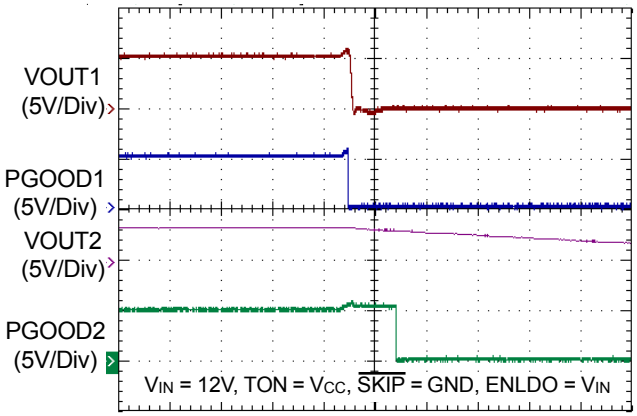
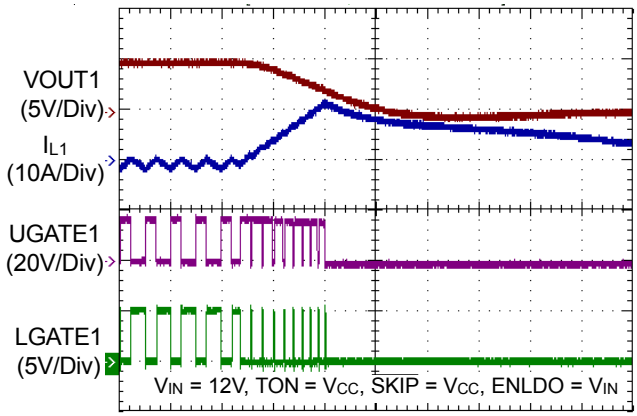
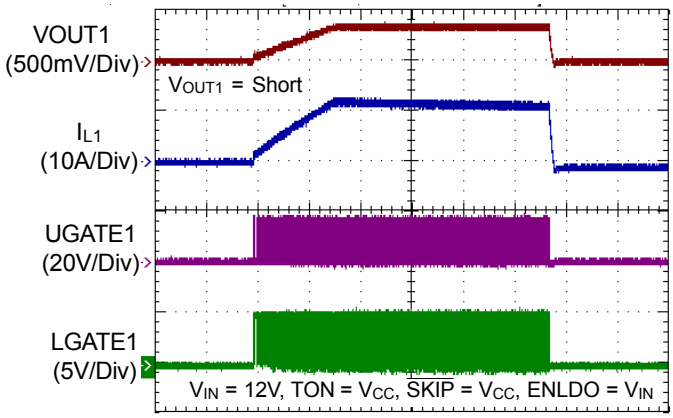
OVP



UVP



Power On in Short Circuit



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Application Information

The RT8206L/M is a dual, high efficiency, Mach Response™ DRV™ dual ramp valley mode synchronous buck controller. The controller is designed for low voltage power supplies for notebook computers. Richtek Mach Response™ technology is specifically designed for providing 100ns "instant-on" response to load steps while maintaining a relatively constant operating frequency and inductor operating point over a wide range of input voltages. The DRV™ mode PWM modulator is specifically designed to have better noise immunity for such a dual output application. The RT8206L/M achieves high efficiency at a reduced cost by eliminating the current-sense resistor found in traditional current-mode PWMs. Efficiency is further enhanced by its ability to drive very large synchronous rectifier MOSFETs. The RT8206L/M includes 5V (LDO) linear regulator which can step down the battery voltage to supply both internal circuitry and gate drivers. When V_{OUT1} voltage is above 4.66V, an automatic circuit turns off the linear regulator and powers the device from V_{OUT1} through the BYP pin connected to V_{OUT1}.

PWM Operation

The Mach Response™ DRV™ mode controller relies on the output filter capacitor's Effective Series Resistance (ESR) to act as a current-sense resistor, so the output ripple voltage provides the PWM ramp signal. Refer to the function block diagram, the UGATE driver will be turned on at the beginning of each cycle. After the internal one-shot timer expires, the UGATE driver will be turned off. The pulse width of this one shot is determined by the converter's input voltage and the output voltage to keep the frequency fairly constant over the input voltage range. Another one-shot sets a minimum off-time (300ns typ.). The on-time one-shot is triggered if the error comparator is high, the low-side switch current is below the current-limit threshold, and the minimum off-time one-shot has timed out.

PWM Frequency and On-Time Control

The Mach Response™ control architecture runs with pseudo-constant frequency by feed-forwarding the input and output voltage into the on-time one-shot timer. The high-side switch on-time is inversely proportional to the input voltage as measured by the V_{IN}, and proportional to the output voltage. The on-time is given by :

On-Time= K (V_{OUT} / V_{IN})

Where "K" is set by the TON pin-strap connector (Table 1). One-shot timing error increases for the shorter on-time setting due to fixed propagation delays that is approximately ±15% at high frequency and the ±10% at low frequency. The on-time guaranteed in the Electrical Characteristics tables is influenced by switching delays in the external high side power MOSFET. Two external factors that influence switching-frequency accuracy are resistive drops in the two conduction loops (including inductor and PC board resistance) and the dead-time effect. These effects are the largest contributors to the change of frequency with changing load current. The dead-time effect increases the effective on-time, reducing the switching frequency as one or both dead times. It occurs only in PWM mode ($\overline{SKIP}$ = high) when the inductor current reverses at light or negative load currents. With reversed inductor current, the inductor's EMF causes $PHASE_X$ to go high earlier than normal, extending the on-time by a period equal to the low-to-high dead time. For loads above the critical conduction point, the actual switching frequency is :

$f_S = (V_{OUT} + V_{DROP1}) / t_{ON} \times (V_{IN} + V_{DROP1} - V_{DROP2})$

V_{DROP1} is the sum of the parasitic voltage drops in the inductor discharge path, including synchronous rectifier, inductor, and PC board resistances; V_{DROP2} is the sum of the resistances in the charging path; and t_{ON} is the on-time calculated by the RT8206L/M.

Table 1. TON Setting and PWM Frequency Table

TON	TON = VCC	TON = REF	TON = GND
V_{OUT1} K-Factor	5µs	3.33µs	2.5µs
V_{OUT1} Frequency	200kHz	300kHz	400kHz
V_{OUT2} K-Factor	4µs	2.67µs	2µs
V_{OUT2} Frequency	300kHz	400kHz	500kHz
Approximate K-Factor Error	±10%	±12.5%	±15%

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Operation Mode Selection

The RT8206L/M supports three operation modes: Diode-Emulation Mode, Ultrasonic Mode, and Forced-CCM Mode. Users can set operation mode by $\overline{SKIP}$ pin. All of the three operation modes will be introduced as follows.

Diode-Emulation Mode ($\overline{SKIP}$ = GND)

In Diode-Emulation mode, the RT8206L/M automatically reduces switching frequency at light-load conditions to maintain high efficiency. This reduction of frequency is achieved smoothly and without the increase of V_{OUTx} ripple or load regulation. As the output current decreases from heavy-load condition, the inductor current is also reduced, and eventually comes to the point that its valley touches zero current, which is the boundary between continuous conduction and discontinuous conduction modes. By emulating the behavior of diodes, the low side MOSFET allows only partial negative current when the inductor free-wheeling current becomes negative. As the load current further decreases, it takes longer and longer to discharge the output capacitor to the level that requires for the next "ON" cycle. The on-time is kept the same as that in the heavy-load condition. In reverse, when the output current increases from light load to heavy load, the switching frequency increases to the preset value as the inductor current reaches the continuous conduction. The transition load point to the light-load operation can be calculated as the following equation.

$$I_{LOAD} \approx \frac{(V_{IN} - V_{OUT})}{2L} \times t_{ON}$$

where t_{ON} is the given On-time.

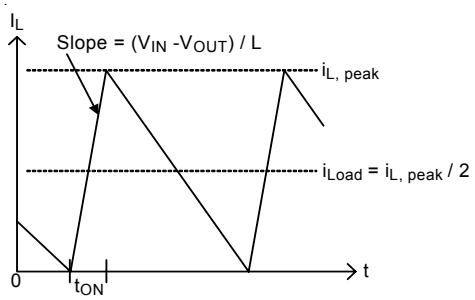

Figure 3. Boundary Condition of CCM/DEM

The switching waveforms may appear noisy and asynchronous when light loading causes Diode-Emulation operation, but this is a normal operating condition that results in high light-load efficiency. Trade-offs in PFM noise vs. light-load efficiency is made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full-load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. Penalties for using higher inductor values include larger physical size and degraded load-transient response (especially at low input-voltage levels).

Ultrasonic Mode ($\overline{SKIP}$ = REF)

Connecting $\overline{SKIP}$ to REF activates a unique Diode-Emulation mode with a minimum switching frequency above 25kHz. This ultrasonic mode eliminates audio-frequency modulation that would otherwise be present when a lightly loaded controller automatically skips pulses. In ultrasonic mode, the low side switch gate-driver signal is ORed with an internal oscillator (>25kHz). Once the internal oscillator is triggered, the ultrasonic controller forces the LGATEx high, turning on the low side MOSFET to induce a negative inductor current. At the point that the output voltage is higher than that of REF, the controller turns off the low side MOSFET (LGATEx pulled low) and triggers a constant on-time (UGATEx driven high). When the on-time has expired, the controller re-enables the low-side MOSFET until the controller detects that the inductor current has dropped below the zero-crossing threshold.

Forced-CCM Mode ($\overline{SKIP}$ = V_{CC})

The low noise, forced-CCM mode ($\overline{SKIP}$ = V_{CC}) disables the zero-crossing comparator, which controls the low side switch on-time. This causes the low side gate-driver waveform to become the complement of the high side gate-driver waveform. This in turn causes the inductor current to reverse at light loads as the PWM loop strives to maintain a duty ratio of V_{OUT}/V_{IN}. The benefit of the forced-CCM mode is to keep the switching frequency fairly constant, but it comes at a cost : The no-load battery current can be from 10mA to 40mA, depending on the external MOSFETs.

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Reference and Linear Regulator (REF, LDO and 14V Charge Pump)

The 2V reference (REF) is accurate within ±1% over the entire temperature range, making REF useful as a precision system reference. Bypass REF to GND with as 0.22μF(MIN) capacitor. REF can supply up to 50μA for external loads. Loading REF degrades FBx and output accuracy according to the REF load-regulation error.

An internal regulator produces a fixed output voltage 5V. The LDO regulator can supply up to 70mA for external loads. Bypass LDO with a minimum 4.7μF ceramic capacitor. When the output voltage of the V_{OUT1} is higher than the switchover threshold, an internal 1.5Ω N-Channel MOSFET switch connects V_{OUT1} to LDO through BYP while simultaneously shutting down the internal linear regulator.

In typical application circuit, the external 14V charge pump is driven by LGATE1. When LGATE1 is low, D1 charges C5 sourced from V_{OUT1}. C5 voltage is equal to V_{OUT1} minus a diode drop. When LGATE1 transitions to high, the charge from C5 will transfer to C6 through D2 and charge it to V_{LGATE1} plus V_{C5}. As LGATE1 transients low on the next cycle, C6 will charge C7 to its voltage minus a diode drop through D3. Finally, C7 charges C8 through D4 when LGATE1 transitions to high. CP output voltage is :

$$V_{CP} = V_{OUT1} + 2 \times V_{LGATE1} - 4 \times V_D$$

where :

- V_{LGATE1} is the peak voltage of the LGATE1 driver
- V_D is the forward diode dropped across the Schottkys

SECFB (RT8206L) is used to monitor the charge pump via the resistive divider. In an event when SECFB drops below 2V the controller forces ultrasonic mode operation which keeps the switching frequency above 25kHz to maintain charge pump voltage.

Reducing the CP decoupling capacitor and placing a small ceramic capacitor C19 (10pF to 47pF) in parallel will the upper leg of the SECFB resistor feedback network, R11, will also increase the robustness of the charge pump.

Current Limit Setting (I_{LIMx})

The RT8206L/M has a cycle-by-cycle current limiting control. The current limit circuit employs a unique "valley" current sensing algorithm. If the magnitude of the current sense signal at PHASEx is above the current limit threshold, the PWM is not allowed to initiate a new cycle (Figure 4). The actual peak current is greater than the current limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current limit characteristic and maximum load capability are a function of the sense resistance, inductor value, battery voltage, and output voltage.

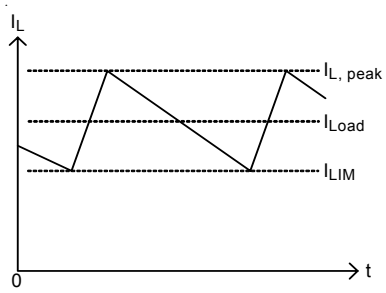

Figure 4. Valley Current Limit

The RT8206L/M uses the on-resistance of the synchronous rectifier as the current-sense element. Use the worse-case maximum value for $R_{DS(ON)}$ from the MOSFET datasheet, and add a margin of 0.5%/°C for the rise in $R_{DS(ON)}$ with temperature.

The current limit threshold is adjusted with an external resistor for the RT8206L/M at ILIMx. The current limit threshold adjustment range is from 50mV to 200mV. In the adjustment mode, the current limit threshold voltage is precise to 1/10 the voltage seen at ILIMx. The threshold defaults to 100mV when ILIMx is connected to VCC. The logic threshold for switchover to the 100mV default value is higher than VCC−1V.

Carefully observe the PC board layout guidelines to ensure that noise and DC errors do not corrupt the current sense signal at PHASEx and GND. Mount or place the IC close to the low side MOSFET.

MOSFET Gate Driver (UGATEx, LGATEx)

The high side driver is designed to drive high current, low $R_{DS(ON)}$ N-MOSFET(s). When configured as a floating driver the instantaneous drive current is supplied by the flying

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capacitor between BOOTx and PHASEx pins. A dead time to prevent shoot through is internally generated between high side MOSFET off to low side MOSFET on, and low side MOSFET off to high side MOSFET on.

The low side driver is designed to drive high current low $R_{DS(ON)}$ N-MOSFET(s). The internal pulldown transistor that drives LGATEx low is robust, with a 0.6Ω typical on-resistance. A 5V bias voltage is typically delivered from PVCC through LDO supply. The instantaneous drive current is supplied by an input capacitor connected between PVCC and GND.

For high current applications, some combinations of high and low side MOSFETs might be encountered that will cause excessive gate-drain coupling, which can lead to efficiency-killing, EMI-producing shoot-through currents. This is often remedied by adding a resistor in series with BOOTx, which increases the turn-on time of the high side MOSFET without degrading the turn-off time (Figure 5).

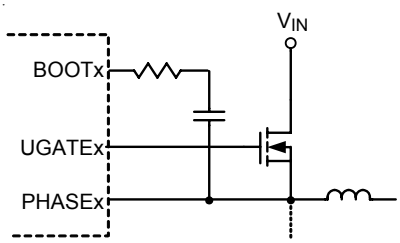

Figure 5. Reducing the UGATEx Rise Time

Soft-Start

The RT8206L/M provides an internal soft-start function to prevent large inrush current and output voltage overshoot when the converter starts up. The soft-start (SS) automatically begins once the chip is enabled. During soft-start period, the internal current limit circuit gradually ramps up the inductor current from zero. The maximum current limit value is set externally as described in previous section. The soft-star time is determined by the current limit and output capacitor value. The current limit threshold ramp up time is typically 2ms from zero to 200mV after ENx is enabled. A unique PWM duty limit control that prevents output over voltage during soft-start period is designed specifically for FBx floating.

POR and UVLO

Power On Reset (POR) occurs when VIN rises above approximately 5V (typ.), resetting the fault latches. PVCC Under Voltage Lockout (UVLO) circuitry inhibits switching by keeping UGATEx and LGATEx low when PVCC is below 4.05V. The PWM outputs begin to ramp up once PVCC exceeds its UVLO threshold and ENx is enabled.

Power Good Output (PGOODx)

The PGOODx is an open-drain type output. PGOODx is actively held low in soft-start, standby, and shutdown. It is released when the VOUTx voltage is above 90% of the nominal regulation point. The PGOODx goes low if it is 10% below its nominal regulator point.

Output Over Voltage Protection (OVP)

The output voltage can be continuously monitored for over voltage protection. When the output voltage of the VOUTx is 12% above the set voltage, over voltage protection will be enabled. If the output exceeds the over voltage threshold, over voltage fault protection will be triggered and the LGATEx low side gate drivers are forced high. This activates the low side MOSFET switch, which rapidly discharges the output capacitor and reduces the output voltage. Once an over voltage fault condition is set, it can only be reset by toggling ENLDO, ENx, or cycling VIN (POR.)

Output Under Voltage Protection (UVP)

The output voltage can be continuously monitored for under voltage protection. If the output is less than 55% of the error-amplifier trip voltage, under voltage protection will be triggered, and then both UGATEx and LGATEx gate drivers will be forced low. The UVP will be ignored for at least 5ms (typ.) after start-up or after a rising edge on ENx. Toggle ENx or cycle VIN (POR) to clear the under voltage fault latch and restart the controller. The UVP only applies to the PWM outputs.

Thermal Protection

The RT8206L/M has a thermal shutdown protection function to prevent it from overheating. Thermal shutdown occurs when the die temperature exceeds +150°C. All

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internal circuitry will be shut down during thermal shutdown. The RT8206L/M may trigger thermal shutdown if the LDO is not supplied from VOUTx, while input voltage on VIN and drawing current from the LDO are too high. Even if the LDO is supplied from VOUTx, overloading the LDO causes large power dissipation on automatic switches, which may result in thermal shutdown.

Discharge Mode

When standby or shutdown mode occurs, or the output under voltage fault latch is set, the output discharge mode is triggered. During discharge mode, the output capacitor will be discharged to GND through an internal 20Ω switch.

Shutdown Mode

The RT8206L/M SMPS1, SMPS2 and LDO have independent enabling control. Drive ENLDO, EN1 and EN2 below the precise input falling edge trip level to place the RT8206L/M in its low power shutdown state. The RT8206L/M consumes only 20μA of quiescent current while in shutdown. When shutdown mode is activated, the reference turns off. The accurate 1V falling-edge threshold on the ENLDO can be used to detect a specific analog voltage level and shutdown the device. Once in shutdown, the 1.6V rising edge threshold activates, providing sufficient hysteresis for most application.

Power Up Sequencing and On/Off Controls (ENx)

EN1 and EN2 control SMPS power-up sequencing. When the RT8206L/M applies in the single channel mode, EN1 or EN2 enables the respective outputs when ENx voltage rises above 2.5V, and disables the respective outputs when ENx voltage falls below 1.8V.

Connecting one ENx to VCC and the other to REF will force the latter one's output to start only after the former one regulates.

If both ENx are connected to REF, each output will wait for the regulation of the other one. However, in this situation, neither of the two ENx will be in regulation.

Output Voltage Setting (FBx)

Connect FB1 directly to GND or VCC for a fixed 5V output (VOUT1). Connect FB2 directly to GND or VCC for a fixed 3.3V output (VOUT2).

The output voltage can also be adjusted from 2V to 5.5V with a resistor-divider network (Figure 6). The following equation is for adjusting the output voltage. Choose R2 to be approximately 10kΩ, and solve for R1 using the following equation :

$$V_{OUTx} = V_{FBx} \times \left[1+\left(\frac{R1}{R2}\right)\right]$$

where V_{FBx} is 2V (typ.).

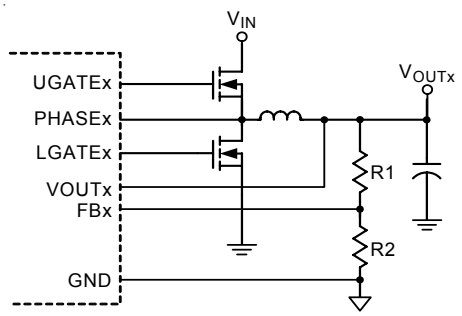

Figure 6. Setting VOUTx with a Resistor-Divider

Output Inductor Selection

The switching frequency (on-time) and operating point (% ripple or L_{IR}) determine the inductor value as follows :

$$L = \frac{t_{ON} \times (V_{IN} - V_{OUT})}{L_{IR} \times I_{LOAD(MAX)}}$$

where LIR is the ratio of the peak-to-peak ripple current to the average inductor current.

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, because the powdered iron is inexpensive and can work well at 200kHz. The core must be large enough to prevent it from saturating at the peak inductor current (I_{PEAK}) :

$$I_{PEAK} = I_{LOAD(MAX)} + [(L_{IR} / 2) \times I_{LOAD(MAX)}]$$

This inductor ripple current also impacts transient-response performance, especially at low $V_{IN} - V_{OUTx}$ differences. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter

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capacitors by a sudden load step. The peak amplitude of the output transient (V_{SAG}) is also a function of the maximum duty factor, which can be calculated from the on-time and minimum off-time :

$$V_{SAG} = \frac{(\Delta I_{LOAD})^2 \times L \times \left(K \frac{V_{OUTx}}{V_{IN}} + t_{OFF(MIN)} \right)}{2 \times C_{OUT} \times V_{OUTx} \times \left[K \left(\frac{V_{IN} - V_{OUTx}}{V_{IN}} \right) - t_{OFF(MIN)} \right]}$$

where minimum off-time ($t_{OFF(MIN)}$) = 300ns (typ.) and K is from Table 1.

Output Capacitor Selection

The output filter capacitor must have low enough equivalent series resistance (ESR) to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements. The output capacitance must also be high enough to absorb the inductor energy while transiting from full-load to no-load conditions without tripping the overvoltage fault latch.

Although Mach Response™ DRV™ dual ramp valley mode provides many advantages such as ease-of-use, minimum external component configuration, and extremely short response time, due to not employing an error amplifier in the loop, a sufficient feedback signal needs to be provided by an external circuit to reduce the jitter level. The required signal level is approximately 15mV at the comparing point. This generates V_{RIPPLE} = (V_{OUT} / 2) x 15mV at the output node. The output capacitor ESR should meet this requirement.

Output Capacitor Stability

Stability is determined by the value of the ESR zero relative to the switching frequency. The point of instability is given by the following equation :

$$f_{ESR} = \frac{1}{2 \times \pi \times ESR \times C_{OUT}} \leq \frac{f_{SW}}{4}$$

Do not put high value ceramic capacitors directly across the outputs without taking precautions to ensure stability. Large ceramic capacitors can have a high ESR zero frequency and cause erratic, unstable operation. However, it is easy to add enough series resistance by placing the capacitors a couple of inches downstream from the inductor and connecting VOUTx or the FBx divider close to the inductor.

There are two related but distinct factors, double-pulsing and feedback loop instability, for unstable operation.

Double-pulsing occurs due to noise on the output or because the ESR is so low that there is not enough voltage ramp in the output voltage signal. This “fools” the error comparator into triggering a new cycle immediately after the 300ns minimum off-time period has expired. Double-pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it may indicate the possible presence of loop instability, which is caused by insufficient ESR.

Loop instability can result in oscillations at the output after line or load perturbations that can trip the over-voltage protection latch or cause the output voltage to fall below the tolerance limit.

The easiest method for checking stability is to apply a very fast zero-to-max load transient and carefully observe the output-voltage-ripple envelope for overshoot and ringing. It helps to simultaneously monitor the inductor current with an AC current probe. Do not allow more than one cycle of ringing after the initial step-response under- or overshoot.

Thermal Considerations

For continuous operation, do not exceed absolute maximum operation junction temperature. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum operation junction temperature, T_A is the ambient temperature and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WQFN-32L 5x5 package, the thermal resistance, θ_{JA}, is 36°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

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$P_{D(MAX)}$ = (125°C – 25°C) / (36°C/W) = 2.778W for WQFN-32L 5x5 package

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. The derating curve in the Figure 7 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

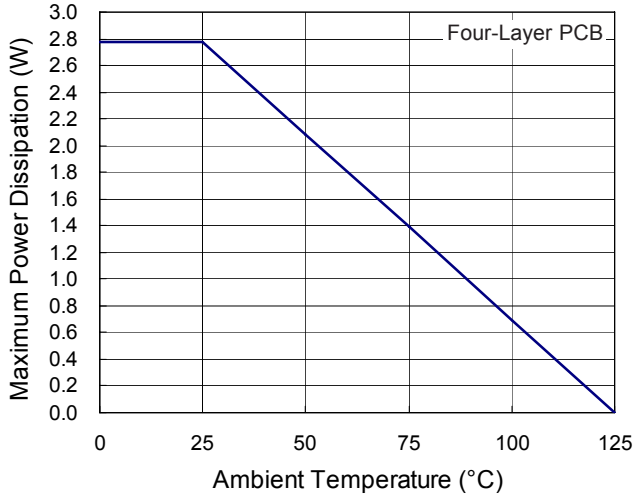

Figure 7. Derating Curve of Maximum Power Dissipation

Layout Considerations

Layout is very important in high frequency switching converter design. If the layout is designed improperly, the PCB could radiate excessive noise and contribute to the converter instability. The following guidelines must be strictly followed for a proper layout of RT8206L/M.

- Connect an RC low-pass filter from PVCC to VCC. The RC low-pass filter is composed of an external capacitor and an internal 10Ω resistor. It is recommended to bypass VCC to GND with a 1μF capacitor. Place the capacitor close to the IC, within 12mm (0.5 inch) if possible.
- Keep current limit setting network as close as possible to the IC. Routing of the network should avoid coupling to high-voltage switching node.
- Connections from the drivers to the respective gate of the high side or the low-side MOSFET should be as short as possible to reduce stray inductance. Use 0.65mm (25 mils) or wider trace.
- All sensitive analog traces and components such as VOUTx, FBx, GND, ENx, PGOODx, ILIMx, VCC, and TON should be placed away from high voltage switching nodes such as PHASEx, LGATEx, UGATEx or BOOTx nodes to avoid coupling. Use internal layer(s) as ground plane(s) and shield the feedback trace from power traces and components.
- Gather ground terminal of VIN capacitor(s), VOUTx capacitor(s), and source of low side MOSFETs as close as possible. PCB trace of the PHASEx node, which connects to source of high side MOSFET, drain of low side MOSFET and high voltage side of the inductor, should be as short and wide as possible.

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Table 2. Operation Mode Truth Table

Mode	Condition	Comment
Power Up	PVCC < UVLO threshold	Transitions to discharge mode after VIN POR and REF become valid. LDO and REF remain active.
RUN	ENLDO = high, EN1 or EN2 enabled	Normal Operation.
Over voltage Protection	Either output > 112% of nominal level.	LGATEx is forced high. LDO and REF active. Exited by VIN POR or by toggling ENLDO, ENx.
Under voltage Protection	Either output < 55% of nominal level after 3ms time-out expires and output is enabled.	Both UGATEx and LGATEx are forced low until discharge mode terminates. LDO and REF are active. Exited by VIN POR or by toggling ENLDO, EN1, or EN2.
Discharge	Either SMPS output is still high in either standby mode or shutdown mode.	During discharge mode, the output capacitor discharges to GND through an internal N-MOSFET switch.
Standby	ENx < startup threshold, ENLDO = high.	LGATEx stays low. LDO and REF active.
Shutdown	EN1, EN2, ENLDO=low	All circuitry off.
Thermal Shutdown	T_J > +150°C	All circuitry off. Exit by VIN POR or by toggling ENLDO, ENx.

Table 3. Power Up Sequencing

ENLDO (V)	V_{EN1} (V)	V_{EN2} (V)	LDO	5V SMPS1	3V SMPS2
Low	X	X	Off	Off	Off
“>2V” High	Low	Low	On (after REF powers up)	Off	Off
“>2V” High	Low	REF	On (after REF powers up)	Off	Off
“>2V” High	Low	High	On (after REF powers up)	Off	On
“>2V” High	REF	Low	On (after REF powers up)	Off	Off
“>2V” High	REF	REF	On (after REF powers up)	Off	Off
“>2V” High	REF	High	On (after REF powers up)	On (after SMPS2 on)	On
“>2V” High	High	Low	On (after REF powers up)	On	Off
“>2V” High	High	REF	On (after REF powers up)	On	On (after SMPS1 on)
“>2V” High	High	High	On (after REF powers up)	On	On

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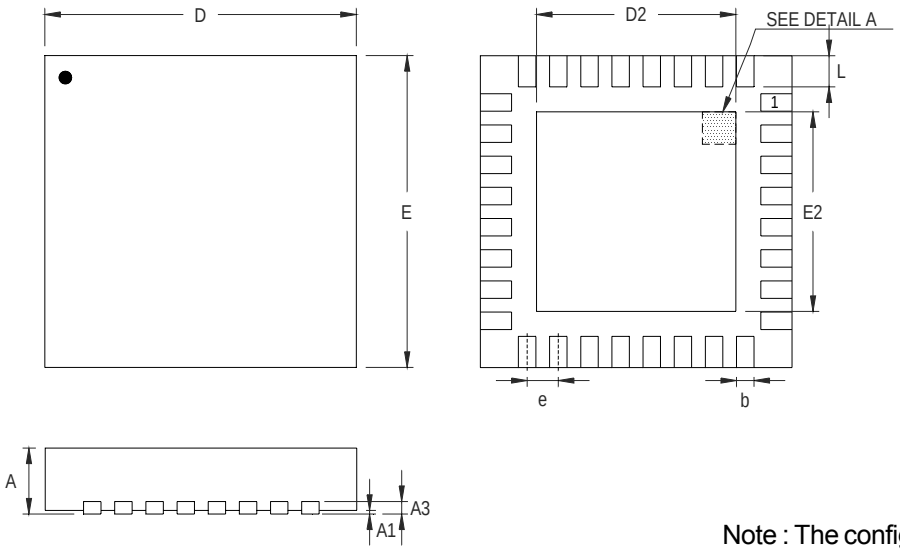
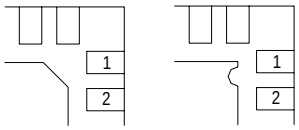
Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	4.950	5.050	0.195	0.199
D2	3.400	3.750	0.134	0.148
E	4.950	5.050	0.195	0.199
E2	3.400	3.750	0.134	0.148
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 32L QFN 5x5 Package

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