Dual Synchronous Buck Controller with 5V/3.3V 100mA LDOs for Notebook System Power

General Description

The uP1586 is a dual synchronous buck controller with 5V/3.3V 100mA LDOs for notebook system power supply solution.

The uP1586 supports high efficiency, fast transient response and provides a combined POK signal. The ultrasonic mode maintains the switching frequency above audio frequency, which eliminates noise in audio applications. The proprietary RCOT™ technology provides fast transient response and high noise immunity.

The uP1586 has internal soft-start to control the inrush current. Other features include overcurrent protection, overvoltage protection, power-up sequencing, power OK output, and thermal shutdown. The uP1586 is available in the space saving package VQFN4x4-24L, specified from -40°C to 85°C.

Applications

- **Notebook and Subnotebook System Power Supplies**
- **3-4 Cell Li-Ion Battery-Power Devices**
- **Dual Output Supplies for DSP, Memory, Logic and Microprocessor**

Features

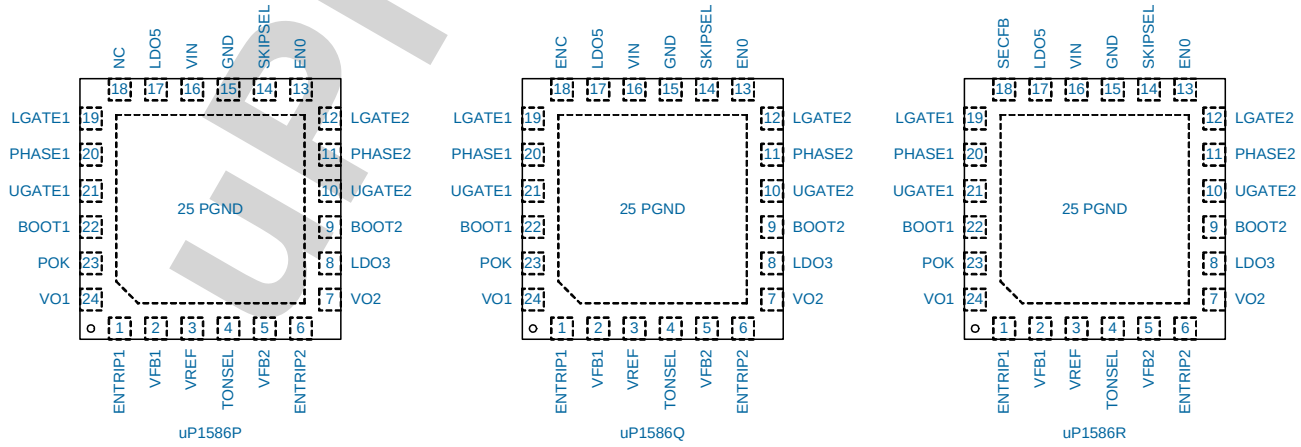
- **Wide Input Voltage Range: 6V to 26V**
- **Two Synchronous Buck Controllers**
  - **Dual Fixed 5V/3.3V Outputs or Adjustable from 2V to 5.5V**
  - **Selectable PWM, DEM and USM in Light Load**
  - **Internal Soft-start and Soft-Discharge**
  - **RCOT™ (Robust Constant On-Time) Control Architecture**
  - **4500ppm/°C $R_{DS(ON)}$ Current Sensing**
- **100mA 5V/3.3V LDO with Switches**
- **Secondary FB Input Maintains Charge Pump Voltage (uP1586R)**
- **2V ± 1% Reference Voltage Output**
- **Power OK Indicator**
- **OVP/UVP/OCP/OTP**
- **VQFN4x4-24L**
- **RoHS Compliant and Halogen Free**

Ordering Information

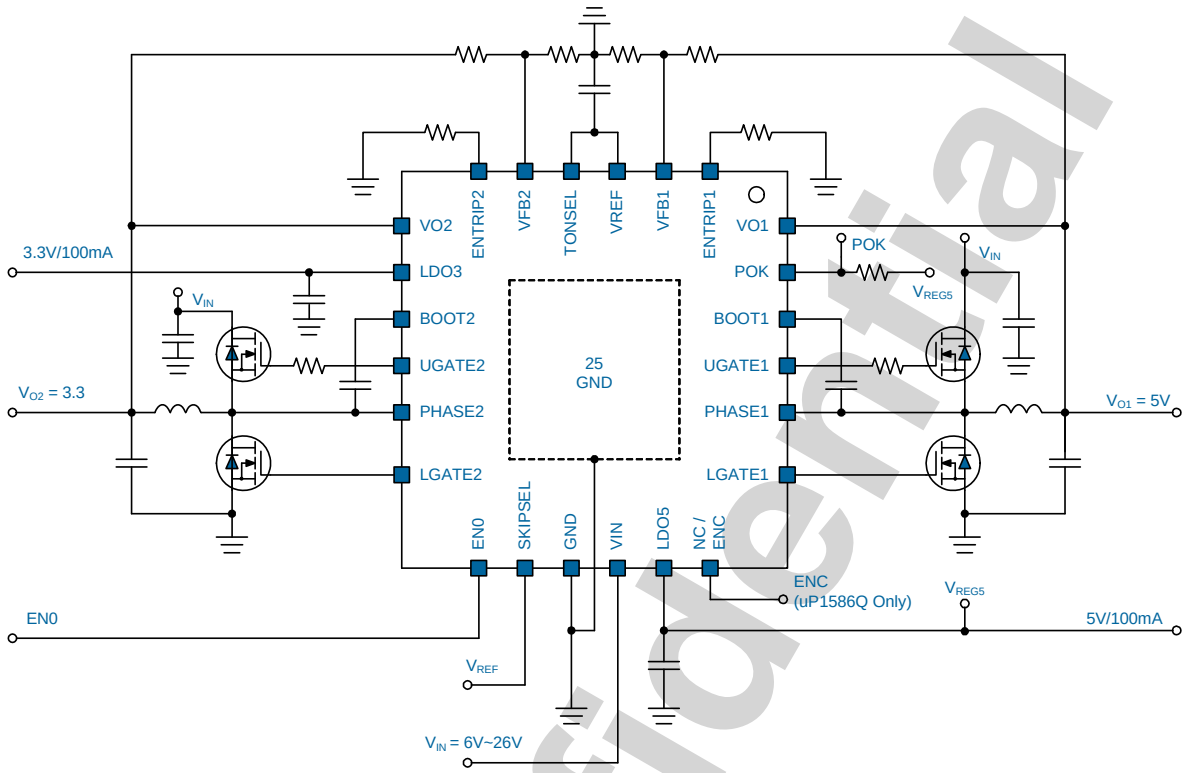
Order Number	Package Type	Remark	Top Marking
uP1586PQAG	VQFN4x4-24L	Pin 18: NC	uP1586P
uP1586QQAG	VQFN4x4-24L	Pin 18: ENC	uP1586Q
uP1586RQAG	VQFN4x4-24L	Pin 18: SECFB	uP1586R

Note: uPI products are compatible with the current IPC/JEDEC J-STD-020 requirements. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

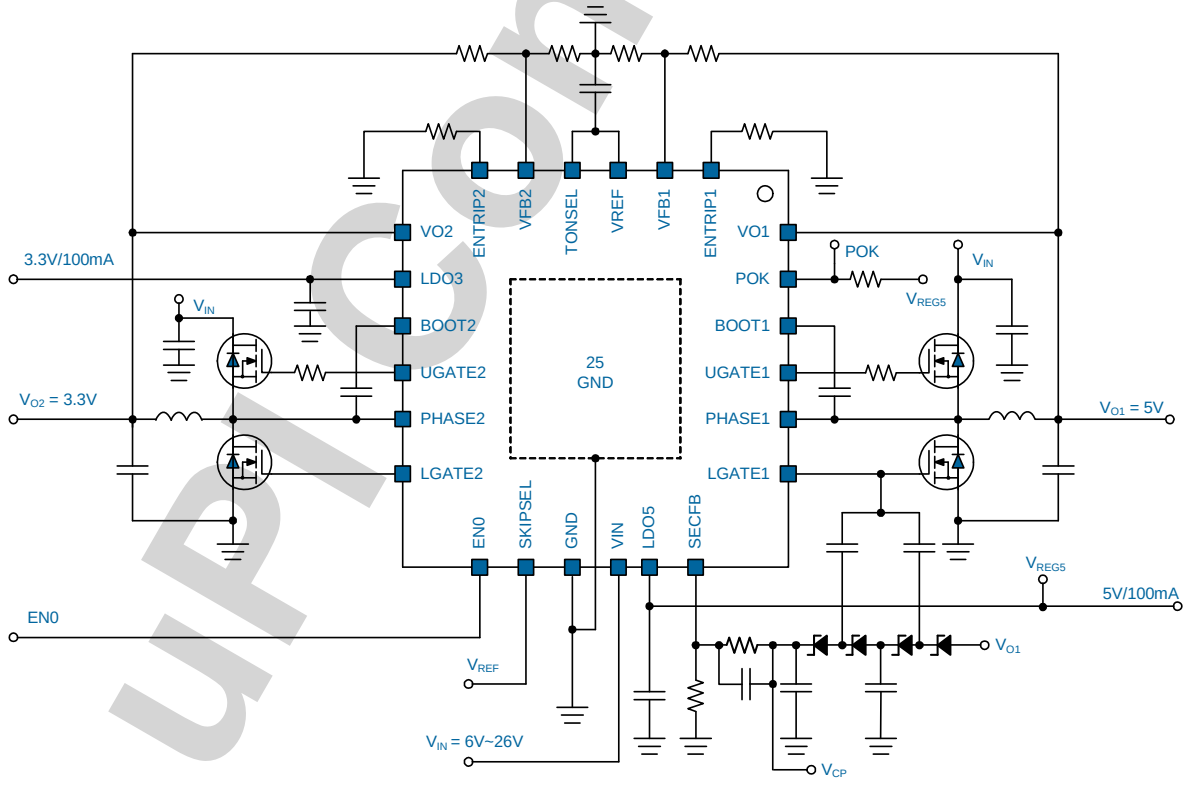
Pin Configuration



Typical Application Circuit



uP1586P/Q



uP1586R

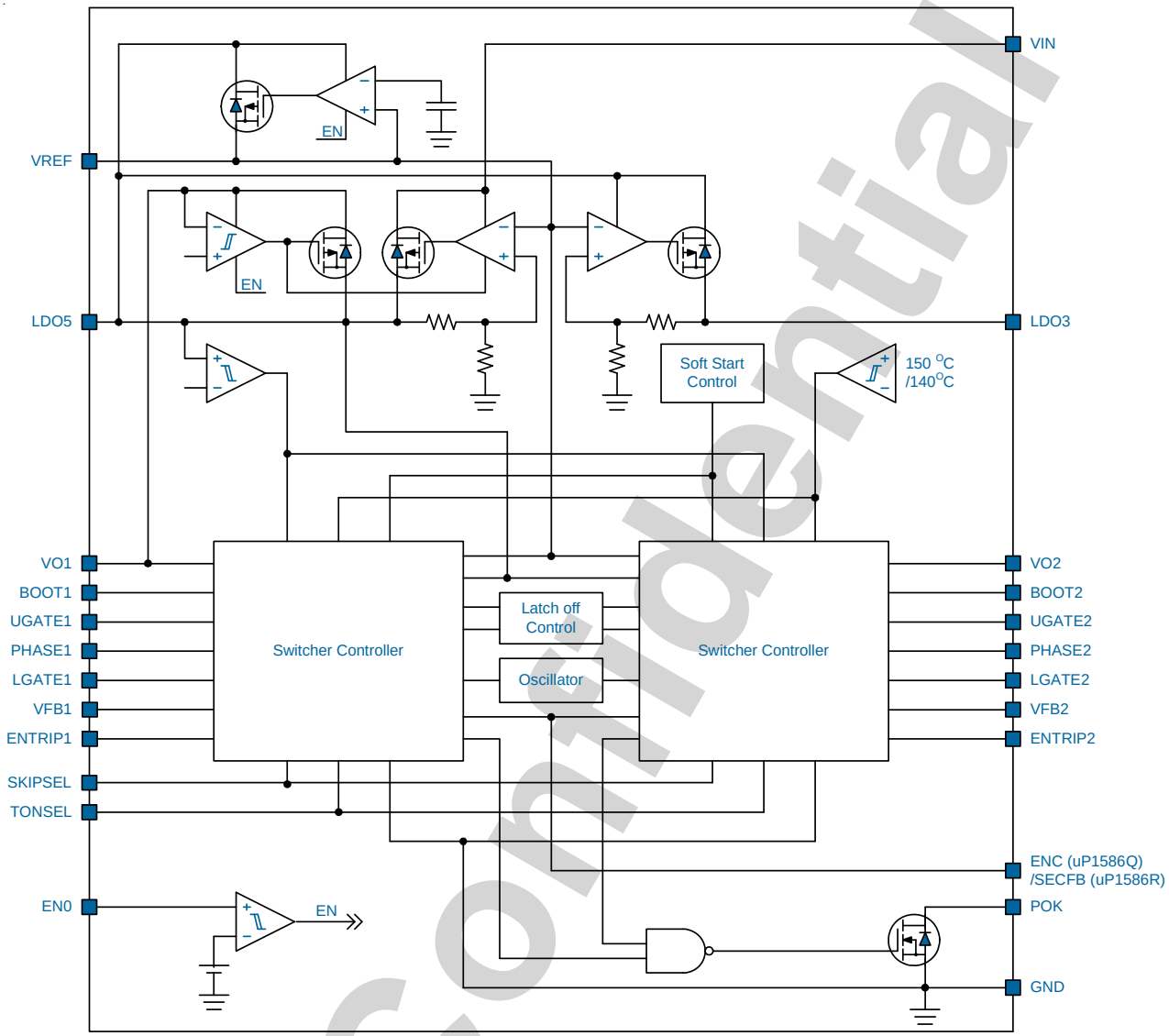
Functional Pin Description

No.	Name	Pin Function
1	ENTRIP1	**Buck 1 Enable and OCP Setting.** Connect resistor from this pin to GND to set threshold for synchronous buck 1 $R_{DS(ON)}$ OCP. Connect this pin to GND to shut down Buck 1.
2	VFB1	**Buck 1 Feedback Input.** This pin is the inverting input to the error amplifier. A resistor divider from output to GND is used to set regulator voltage.
3	VREF	**2V Reference Voltage Output.** Bypass this pin with a 0.22uF ceramic capacitor to GND. This pin is capable of sourcing up to 100uA current for external loads.
4	TONSEL	**On-Time Select Pin.** 400k/500k: Connect this pin to LDO5 or LDO3. 300k/375k: Floating this pin. 200k/250k: Connect this pin to GND.
5	VFB2	**Buck 2 Feedback Input.** This pin is the inverting input to the error amplifier. A resistor divider from output to GND is used to set regulator voltage.
6	ENTRIP2	**Buck 2 Enable and OCP Setting.** Connect resistor from this pin to GND to set threshold for synchronous buck 2 $R_{DS(ON)}$ OCP. Connect this pin to GND to shut down Buck 2.
7	VO2	**Output of Buck 2.** This pin works as fixed voltage feedback Input and output discharge inputs. VO2 also works as 3.3V switch over return power input respectively.
8	LDO3	**Output of Internal 3.3V LDO.** The LDO3 is capable of sourcing 100mA output current for external loads. Bypass this pin with a minimum 4.7uF.
9	BOOT2	**Bootstrap Supply for the Floating Upper MOSFET Gate Driver of Buck 2.** Connect the bootstrap capacitor C_{BOOT} (typ. 0.1uF to 0.47uF) between BOOT2 pin and the PHASE2 pin. Place the C_{BOOT} near the IC.
10	UGATE2	**Upper MOSFET Gate Driver Output for Buck 2.** Connect this pin to the gate of upper MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.
11	PHASE2	**Switch Node for Buck 2.** Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin is used as the sink for the UGATE2 driver. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off. A Schottky diode between this pin and ground is recommended to reduce negative transient voltage which is common in a power supply system.
12	LGATE2	**Lower MOSFET Gate Driver Output for Buck 2.** Connect this pin to the gate of lower side MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turned off.
13	EN0	**LDO Enable.** LDO3 or LDO5: Enable both LDOs and ready to turn on switcher channels. GND: Disable all circuit.
14	SKIPSEL (uP1586P/R)	**Operation Mode Selection Pin.** Ultrasonic Mode: Connect this pin to LDO3 or LDO5. Diode Emulation Mode: Floating this pin. PWM Only: Connect this pin to GND.
	SKIPSEL (uP1586Q)	**Operation Mode Selection Pin.** Ultrasonic Mode: Connect this pin to LDO3 or LDO5. Diode Emulation Mode: Connect this pin to GND. PWM Only: Floating this pin.
15	GND	**Signal Ground for the IC.** All voltages levels are measured with respect to this pin. Tie this pin to the ground island/plane through the lowest impedance connection available.

Functional Pin Description

No.	Name	Pin Function
16	VIN	**Supply Input.** This pin is the input of the internal 5V and 3.3V LDO regulators. Connect VIN to the battery or AC adapter output.
17	LDO5	**Output of Internal 5V LDO.** The LDO5 is capable of sourcing 100mA output current for external loads. Bypass this pin with a minimum 4.7uF.
18	NC(uP1586P)	**Not Internal Connection.**
	ENC(uP1586Q)	**Buckx Enable Input.** Pull this pin up to LDO3 or LDO5 to turn on both switcher channels. Connect this pin to GND to shutdown them.
	SECFB (uP1586R)	**Change Pump Feedback Pin.** The SECFB is used to monitor the optional external charge pump. Connect a resistive divider from the change pump output to GND to detect the output. If SECFB drops below its feedback threshold, an ultrasonic pulse occurs to refresh the charge pump driven by LGATE1 or LGATE2.
19	LGATE1	**Lower MOSFET Gate Driver Output for Buck 1.** Connect this pin to the gate of lower MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turned off.
20	PHASE1	**Switch Node for Buck 1.** Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin is used as the sink for the UGATE1 driver.This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off. A Schottky diode between this pin and GND is recommended to reduce negative transient voltage which is common in a power supply system.
21	UGATE1	**Upper MOSFET Gate Driver Output for Buck 1.** Connect this pin to the gate of upper MOSFET. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.
22	BOOT1	**Bootstrap Supply for the Floating Upper MOSFET Gate Driver of Buck 1**. Connect the bootstrap capacitor C_{BOOT} (typ. 0.1uF to 0.47uF) between BOOT1 pin and the PHASE1 pin. Place the C_{BOOT} is placed near the IC.
23	POK	**Open Drain Output for Power OK Indication.** This pin is set to high impedance with adequate time delay after soft-start cycle completes and both SMPSs outputs are above 95% of the nominal regulation voltages. It is pulled low immediately when either output is in soft-start, standby, shutdown or protection.
24	VO1	**Output of Buck 1.** This pin works as fixed voltage inputs and output discharge inputs. VO1 also works as 5V switch over return power input respectively.
25	Exposed Pad	**Ground.** The exposed pad dominates heat conduction path and should be well soldered to PCB for optimal thermal performance.

Functional Block Diagram



Functional Description

The uP1586 implements an unique RCOT™ control topology for both synchronous buck controllers. The uP1586 does not require the external compensator. The RCOT™ supports extremely low ESR output capacitors and makes the design easier and robust.

Enable and Soft Start

EN0 is the control pin of LDO5, LDO3 and VREF regulators. Connect this pin to GND disables three regulators. Float this pin will turn the three regulators on to standby mode. Two SMPSs become ready to enable at this standby mode. When ENC(uP1586Q) is higher than 2V, both SMPSs start up. The uP1586 has an internal 1.7ms output voltage soft-start for each channel. When the ENTRIPx pin becomes higher than its enable threshold, an internal SS begins ramping up the reference voltage of the two SMPSs. If ENTRIPx pin becomes higher than the enable threshold voltage while another channel is starting up, soft start is postponed until another channel soft-start has completed. If both of ENTRIP1 and ENTRIP2 become higher than the enable threshold voltage at the same time (within 60us), both channels start up at same time.

Table 1. Enabling State

EN0	ENTRIP1	ENTRIP2	VREF	LDO5	LDO3	CH1	CH2
GND	X	X	Off	Off	Off	Off	Off
LDO3/5	Off	Off	On	On	On	Off	Off
LDO3/5	On	Off	On	On	On	On	Off
LDO3/5	Off	On	On	On	On	Off	On
LDO3/5	On	On	On	On	On	On	On

On Time Control and PWM Frequency

The uP1586 runs with pseudo fixed frequency by feed-forwarding the input and output voltage into the on-time one-shot timer. The controlled on-time is proportional to VOUT/VIN so that the duty ratio will be kept as technically with the same cycle time. The frequencies are set by TONSEL pin as Table 2.

Table 2. TONSEL Connection and Switching Frequency

TONSEL Connection	Switching Frequency	
	CH1	CH2
GND	200KHz	250KHz
Floating	300KHz	375KHz
LDO5 or LDO3	400KHz	500KHz

Operation Modes

The uP1586 supports three operation modes: Force CCM, Diode Emulation and Ultrasonic mode. The operation mode is selected by SKIPSEL pin.

Diode Emulation Mode

In *Diode Emulation Mode,* the uP1586 automatically switches over to DEM at light load. As the output current decreases from heavy load condition, the inductor current is also reduced, and eventually comes to the point that its valley touches zero current, which is the boundary between continuous conduction and discontinuous conduction modes. The lower MOSFET is turned off if the negative inductor current is detected. As the load current is further decreased, it takes longer and longer to discharge the output capacitor to the level that requires the next on cycle. The frequency is reduced smoothly and hence the power losses are reduced at light load.

Ultrasonic Mode (SKIPSEL=LDO5 or LDO3)

Ultrasonic mode (USM) is a technique that keeps the switching frequency above audible frequencies while maintaining best of the high conversion efficiency. When the ultrasonic mode is selected, USM control circuit monitors both MOSFETs and forces to change into the next on state if both of MOSFETs are off for more than 32us. USM control circuit detects the over voltage condition and begins to modulate the on-time to keep the output voltage regulated.

LDO3/LDO5 Linear Regulators

The uP1586 has two sets of 100mA linear regulators which output 5V and 3.3V. The LDO5 provides the main power supply for the circuitry of the device and provides the current for gate drivers.The LDO3 is intended mainly for 3.3V supply for the notebook system during standby mode.

LDO5 Switcher

When VO1 finishes soft-start and the voltage is higher than its switchover threshold, an internal switch connects VO1 to LDO5 and shuts down the LDO5 simultaneously. When ENTRIP1 goes low, the LDO5 is activated immediately and then internal switch will be off. It decreases the power dissipation from battery.

Output Discharge Control

When ENTRIPx is low, the uP1586 discharges outputs using internal MOSFET which is connected to VOx. The current capability of these MOSFETs is limited to discharge slowly.

Power OK Indicator

The uP1586 has one POK output indicator. A pull-up resistor is needed for the open-drain output. The POK is actively held low in soft-start, standby, shutdown and protection. It is released when both VO1 and VO2 voltage rise above 95% of their nominal regulation voltage.

Functional Description

Over Current Protection

The uP1586 has cycle-by-cycle over current limit control. The inductor current is monitored during the off state and the controller keeps the off state when the inductor current is larger than the over current trip level.

In order to provide both good accuracy and cost effective solution, the uP1586 supports temperature compensated MOSFET $R_{DS(on)}$ sensing. ENTRIPx pin should be connected to GND through the trip voltage setting resistor, R_{TRIP}. ENTRIPx terminal sources I_{TRIP} current, which is 10uA typically at room temperature, and the trip level is set to the OCL trip voltage V_{TRIP} as below. Note that the V_{TRIP} is limited up to about 300mV(Max.) internally.

$$V_{TRIP}(mV) = \frac{R_{TRIP}(k\Omega) \times I_{TRIP}(uA)}{10} = I_{OCP} \times R_{DS(ON)}$$

$$R_{TRIP}(k\Omega) = \frac{I_{OCP} \times R_{DS(ON)} \times 10}{I_{TRIP}(uA)}$$

The voltage between GND pin and PHASEx pin monitors the inductor current so that PHASEx pin should be connected to the drain terminal of the lower MOSFET properly. I_{TRIP} has 4500 ppm/°C temperature slope to compensate the temperature dependency of the lower MOSFET $R_{DS(on)}$. GND is used as the positive current sensing node so that GND should be connected to the proper current sensing device, i.e. the source terminal of the lower MOSFET.

When the comparison is done during the off state, V_{TRIP} sets valley level of the inductor current. Therefore, the load current at over current threshold, I_{LIM}, can be calculated as follows:

$$I_{LIM} = \frac{V_{TRIP}}{R_{DSON}} + \frac{I_{RIPPLE}}{2}$$

$$= \frac{V_{TRIP}}{R_{DSON}} + \frac{1}{2 \times L \times f} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$

In an over current condition, the current to the load exceeds the current to the output capacitor. Thus the output voltage tends to fall down. Eventually, it ends up with crossing the under voltage protection threshold and shuts down both channels.

Over/Under Voltage Protection

The uP1586 monitors the feedback voltage to detect over and under voltage. When the feedback voltage becomes higher than 120% target voltage, the OVP circuit latches the upper MOSFET off and the lower MOSFET on. When the feedback voltage becomes lower than 60% target voltage, the UVP occurs after 30us UVP delay, the uP1586 latches off both side MOSFETs, and shuts off both drivers of another channel. This function is enabled after 3ms following ENTRIPx has become high.

UVLO Protection

The uP1586 has LDO5 under voltage lock out protection (UVLO). When the LDO5 voltage is lower than UVLO threshold voltage, both SMPS are turned off. This is a non-latch protection.

Over Temperature Protection

The uP1586 monitors the temperature of itself. If the temperature exceeds typical 150°C, the uP1586 is turned off excluding LDOs. This is a latch protection.

Charge Pump (SECFB)

As shown in the Figure1, the external charge pump is driven by LGATEx. The total charge pump voltage, V_{CP}, is

$$V_{CP} = VOx + 2 \times V_{LGATEx} - 4 \times V_D$$

where V_{LGATEx} is the peak voltage of the LGATEx driver which is equal to LDO5, V_D is the forward voltage dropped across the Schottky diode.

The SECFB pin in the uP1586R is used to monitor the charge pump via a resistive voltage divider to generate DC voltage and the clock driver uses VOx as its power supply. In the event where SECFB drops below its feedback threshold, an ultrasonic pulse will occur to refresh the charge pump driven by LGATEx. If there's an overload on the charge pump in which SECFB can not reach more than its feedback threshold, the controller will enter Ultrasonic Mode. Special care should be taken to ensure that enough normal ripple voltage is present on each cycle to prevent charge pump shutdown.

The robustness of the charge pump can be increased by reducing the charge pump decoupling capacitor and placing a small ceramic capacitor, C_p (47pF to 220pF), in parallel with the upper leg of the SECFB resistor feedback network, R_{CP1}, as shown below in Figure 1

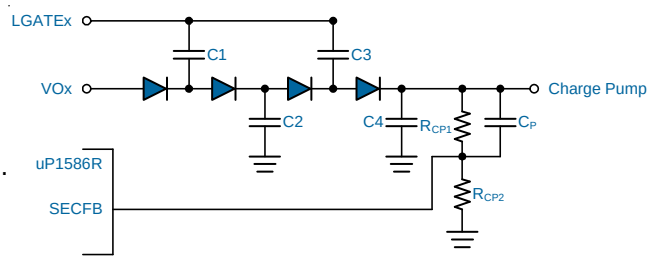


Figure 1.

Absolute Maximum Rating

(Note 1)

Supply Input Voltage, VIN ---------- -0.3V to +30V
BOOTx to PHASEx ---------- -0.3V to +6V
PHASEx to GND
DC ---------- -0.3V to +30V
< 200ns ---------- -5V to +38V
UGATEx to PHASEx
DC---------- -0.3V to +6V
<200ns ---------- -5V to +7V
LGATEx to GND
DC ---------- -0.3V to +6V
< 200ns ---------- -2V to +7V
Other Pins to GND ---------- -0.3V to +6V
Storage Temperature Range ---------- -65°C to +150°C
Junction Temperature ---------- 150°C
Lead Temperature Range(Soldering 10sec) ---------- 260°C
ESD Rating (Note 2)
HBM (Human Body Mode) ---------- 2kV
MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)
VQFN4x4 - 24L θ_{JA} ---------- 40°C/W
VQFN4x4 - 24L θ_{JC} ---------- 4°C/W
Power Dissipation, P_D @ TA = 25°C
VQFN4x4 - 24L ---------- 2.5W

Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range ---------- -40°C to +125°C
Operating Ambient Temperature Range ---------- -40°C to +85°C
Supply Input Voltage, VIN ---------- 6V to 26V

Electrical Characteristics

Electrical characteristics over recommended free-air temperature range, V_{IN}=12V, T_A= 25°C. (Unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
POR						
VIN Power On Reset	V_{IN_POR}	Rising	--	5.1	5.6	V
		Hysteresis	--	0.5	--	
LDO5 Power On Reset	V_{LDO5_POR}	Rising	--	4.3	4.8	V
		Hysteresis	--	0.2	--	
Supply Current						
VIN Supply Current	I_{VIN}	VIN current, No Load, VO1= 0V, VO2 = 0V, ENTRIPx = 2V, VFB1= VFB2 = 2.05V	--	0.55	1	mA

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
VIN Standby Current	$I_{VINSTBY}$	VIN current, No Load, EN0 = 1V, ENTRIPx = 0V	--	200	400	uA
VIN Shutdown Current	I_{SD}	VIN current, No Load, EN0 = ENTRIPx = 0V	--	--	30	uA
VREF Output						
VREF Output Voltage	V_{VREF}	I_{VREF} = 0A	1.98	2.00	2.02	V
		-5uA < I_{VREF} < 100uA	1.97	2.00	2.03	
LDO5 Output						
LDO5 Output Voltage	V_{LDO5}	ENC = GND, I_{LDO5} < 100mA	4.8	5.0	5.2	V
		ENC = GND, I_{LDO5} < 100mA, 7V < V_{IN} < 26V	4.75	5.0	5.25	
		ENC = GND, I_{LDO5} < 50mA, 6V < V_{IN} < 26V	4.75	5.0	5.25	
LDO5 Output Current	I_{LDO5}	ENC = GND, V_{LDO5} = 4.5V, I_{LDO3} = 0mA	--	150	--	mA
Switch Over Threshold	V_{TH5VSW}	Turns on	4.53	4.69	4.85	V
		Hysteresis	--	0.4	--	
5V Switch Over Ron	R_{5VSW}	VO1 = 5V, I_{LDO5} = 100mA	--	1.5	--	Ω
LDO3 Output						
LDO3 Output Voltage	V_{LDO3}	ENC = GND, I_{LDO3} < 100mA	3.20	3.3	3.46	V
		ENC = GND, I_{LDO3} < 100mA, 7V < V_{IN} < 26V	3.13	3.3	3.50	
		ENC = GND, I_{LDO3} < 50mA, 6V < V_{IN} < 26V	3.13	3.3	3.50	
LDO3 Output Current	I_{LDO3}	ENC = GND, V_{LDO3} = 3V, I_{LDO5} = 0mA	--	100	--	mA
Output						
Internal Reference Voltage	V_{VREF}	I_{VREF} = 0A, beginning of on state	1.98	2.00	2.02	V
VFB Regulation Voltage	V_{VFBx}	FB voltage, I_{VREF} = 0A, continuous conduction	--	2.00	--	V
VFB Input Current	I_{VFBx}	VFBx = 2.0 V	-20	--	20	nA
VOx Discharge Current	I_{Dischg}	ENTRIPx = 0V, VOx = 0.5V	10	33	--	mA
SECFB Voltage	V_{SECFB}	(uP1586R)	1.92	2.00	2.08	V
Output Drivers						
UGATE Resistance	R_{UGATEx}	Source, $V_{BOOTx-UGATEx}$ = 100mV	--	4.5	8	Ω
		Sink, $V_{UGATEx-PHASEx}$ = 100mV	--	1.8	3	
LGATE Resistance	R_{LGATEx}	Source, $V_{LDO5-LGATEx}$ = 100mV	--	4.5	8	Ω
		Sink, V_{LGATEx} = 100mV	--	1.2	3	
Dead Time	T_D	UGATEx < 1V to LGATEx > 1V	--	30	--	ns
		LGATEx < 1V to UGATEx > 1V	--	30	--	
Internal Bootstrap Switch						
Internal Boost Charging Switch On-Resistor	R_{BOOTX}	LDO5 to BOOTx, I_{BOOTx} = 10mA	--	80	--	Ω

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Duty and Frequency Control						
CH1 On-time 1	T_{ON11}	V_{IN}=12V, VO1=5V, 200kHz setting	--	2080	--	ns
CH1 On-time 2	T_{ON12}	V_{IN}=12V, VO1=5V, 300kHz setting	--	1390	--	ns
CH1 On-time 3	T_{ON13}	V_{IN}=12V, VO1=5V, 400kHz setting	--	1040	--	ns
CH2 On-time 1	T_{ON21}	V_{IN}=12V, VO2=3.3V, 250kHz setting	--	1100	--	ns
CH2 On-time 2	T_{ON22}	V_{IN}=12V, VO2=3.3V, 375kHz setting	--	730	--	ns
CH2 On-time 3	T_{ON23}	V_{IN}=12V, VO2=3.3V, 500kHz setting	--	550	--	ns
Minimum Off-time	T_{OFFMIN}		--	300	--	ns
Soft-start						
USM Frequency	F_{USM}	SMPS operating in USM	25	--	--	kHz
Internal SS Time	T_{SS}	Internal soft-start	--	1.7	--	ms
Power OK Indication						
POK Threshold	V_{THPOK}	Rising	87	90	93	%
		Hysteresis	--	5	--	
POK Sink Current	I_{POKMAX}	POK = 0.5V	5	12	--	mA
POK Delay	T_{POKDEL}	Delay from 90% of VFB to POK go high	--	500	--	us
Logic Threshold and Setting Conditions						
EN0 Voltage	V_{EN0}	Rising edge threshold	0.8	--	--	V
		Falling edge threshold	--	--	0.3	
ENTRIPx Input Voltage	$V_{ENTRIPx}$	Clear fault low level/SMPSx off level	--	--	0.4	V
		SMPSx on level	0.6	--	3	
		Clear fault high level/SMPSx off level	4.5	--	--	
TONSEL Logic Setting Voltage	V_{TON}	200kHz/250kHz	--	--	1.5	V
		300kHz/375kHz	1.9	--	2.1	
		400kHz/500kHz	2.7	--	--	
SKIPSEL Logic Setting Voltage	V_{SKIP}	PWM only	--	--	1.5	V
		DEM	1.9	--	2.1	
		USM	2.7	--	--	
ENTRIPx Source Current	$I_{ENTRIPx}$	$V_{ENTRIPx}$ = 1V	9.4	10	10.6	uA
ENTRIPx Current Temp. Coefficient	TC_{IEN}	On the basis of 25 ^{o}C	--	4500	--	ppm /^{o}C
ENC Threshold Voltage(uP1586Q)	V_{ENC}	Shutdown	--	--	0.8	V
		Enable	1.9	--	--	

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Protection: Current Sense						
OCP Comp. Offset	V_{OCLoff}	$V_{ENTRIPx}$ / 10	-8	0	8	mV
Maximum OCL Setting	V_{OCLmax}	$V_{ENTRIPx}$ = 2V	185	205	225	mV
Zero-Current Threshold	V_{ZC}	GND-PHASEx	--	3	--	mV
Protection: UVP & OVP						
OVP Trip Threshold	V_{OVP}	OVP detect	115	120	125	%
OVP Prop. Delay	T_{OVPDEL}		--	5	--	us
UVP Trip Threshold	V_{UVP}	UVP detect	55	60	65	%
UVP Prop. Delay	T_{UVPDEL}		--	10	--	us
UVP Enable Delay	T_{UVPEN}	From ENTRIPx enable	--	4	--	ms
Thermal Shutdown						
Thermal SDN Threshold	T_{SDN}	Shutdown temperature	--	150	--	°C

Note 1. Stresses listed as the above " Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

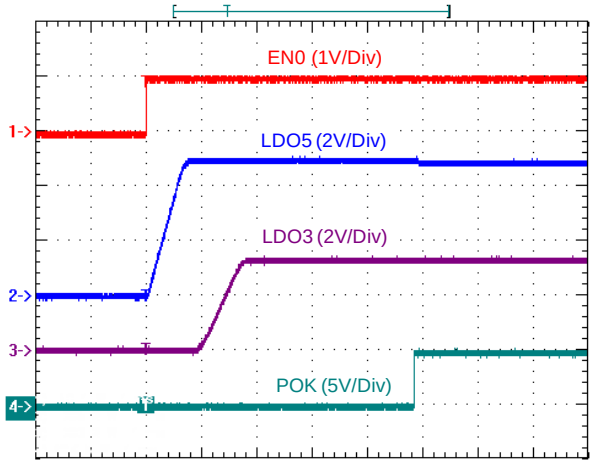
Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

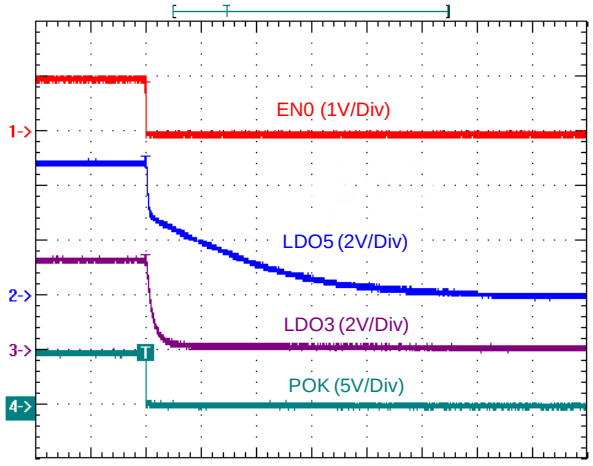
Typical Operation Characteristics

Power On from EN0



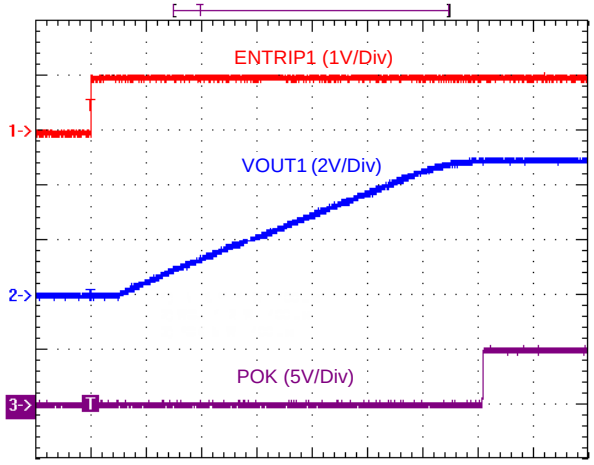
1ms/Div
I_{OUT1} = I_{OUT2} = 0A

Power Off from EN0



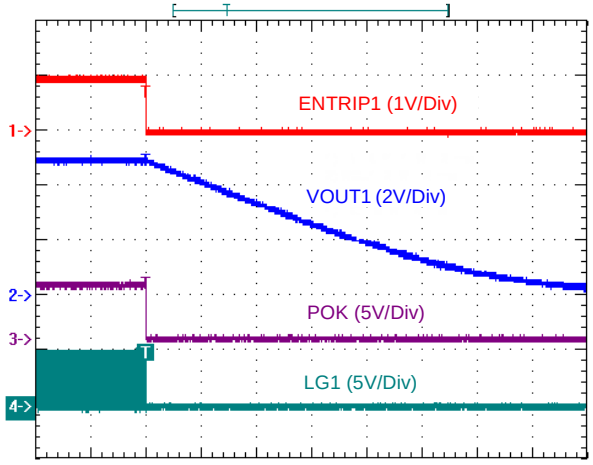
1ms/Div
I_{OUT1} = I_{OUT2} = 0A

Power On from ENTRIP1



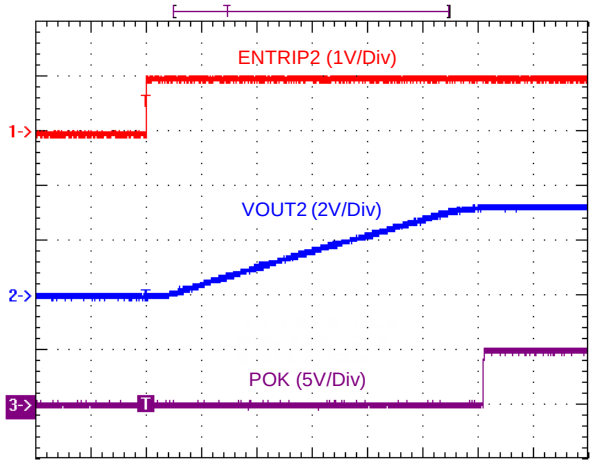
400us/Div
I_{OUT1} = 0A

Power Off from ENTRIP1



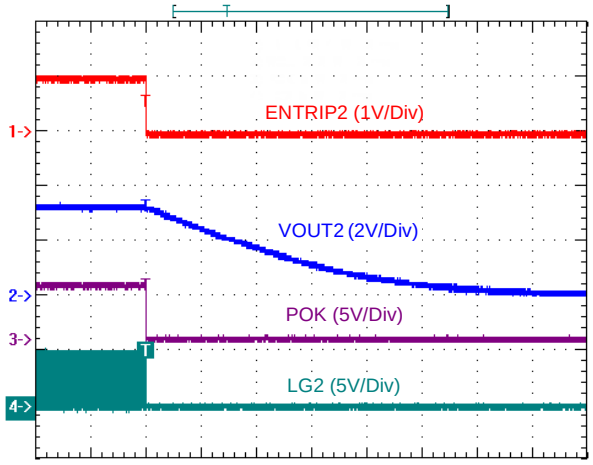
2ms/Div
I_{OUT1} = 0A

Power On from ENTRIP2



400us/Div
I_{OUT2} = 0A

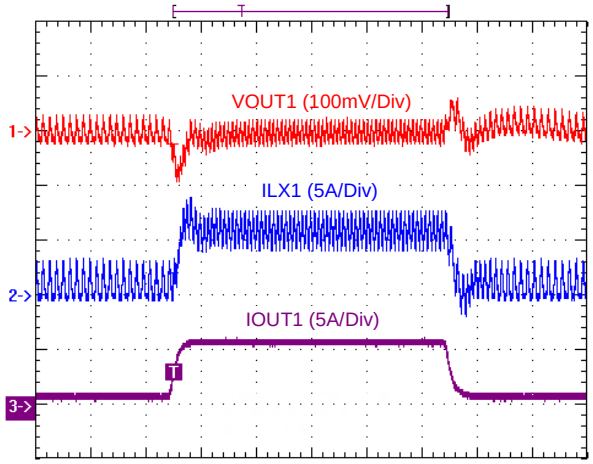
Power Off from ENTRIP2



2ms/Div
I_{OUT2} = 0A

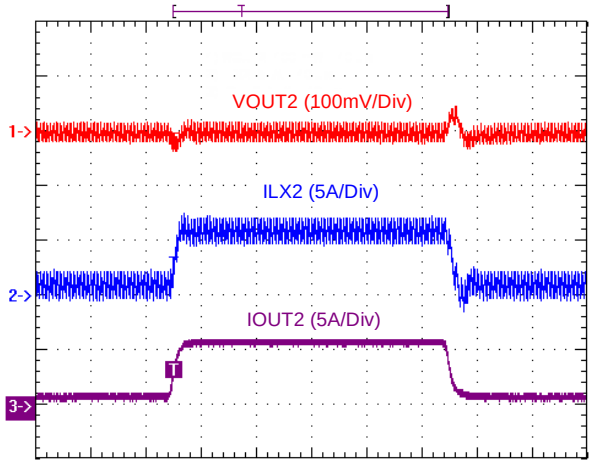
Typical Operation Characteristics

VO1 Load Transient ResponseC



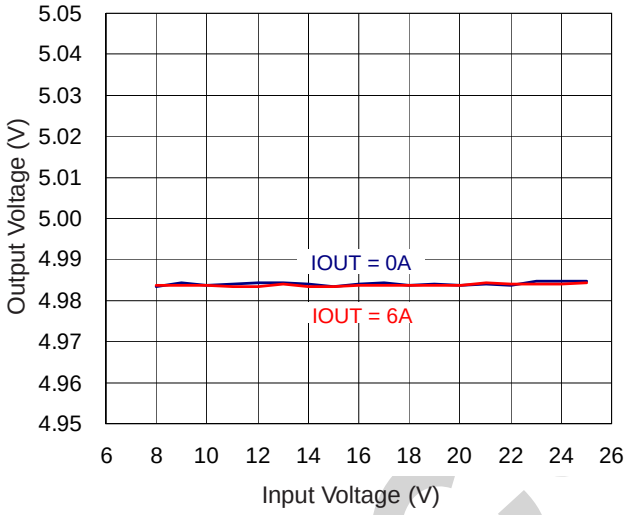
40us/Div
V_{IN} = 12V, I_{OUT1} = 1A to 6A

VO2 Load Transient ResponseC

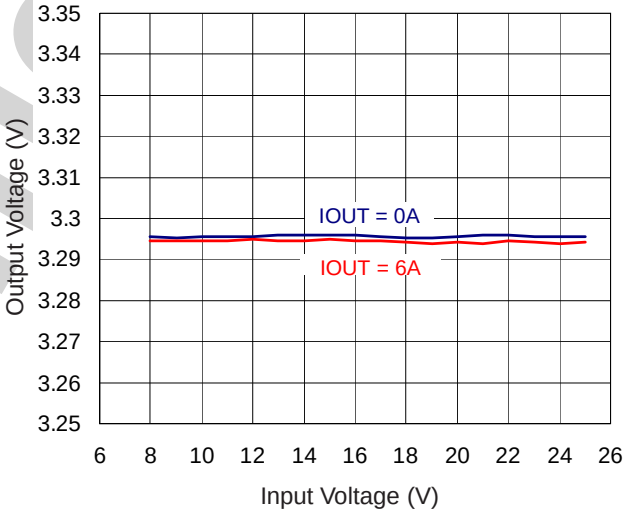


40us/Div
V_{IN} = 12V, I_{OUT2} = 1A to 6A

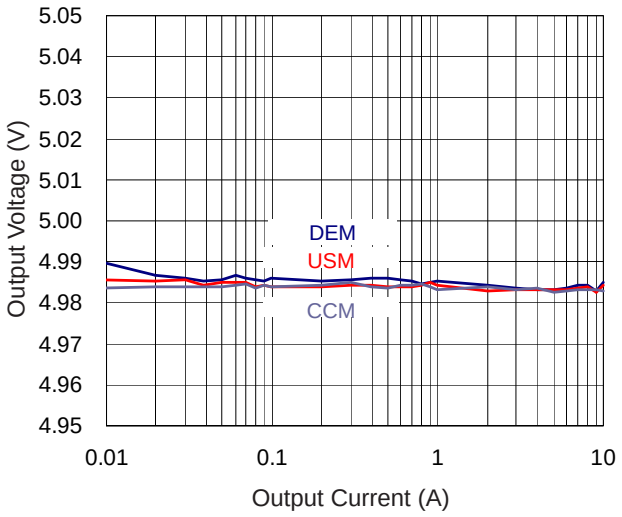
VO1 Line Regulation



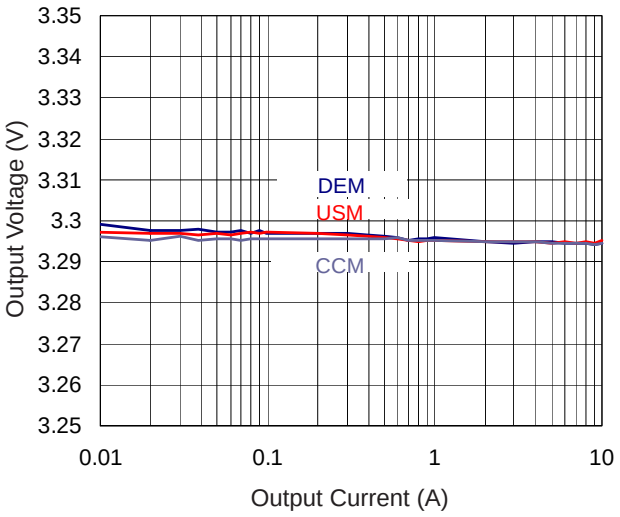
VO2 Line Regulation



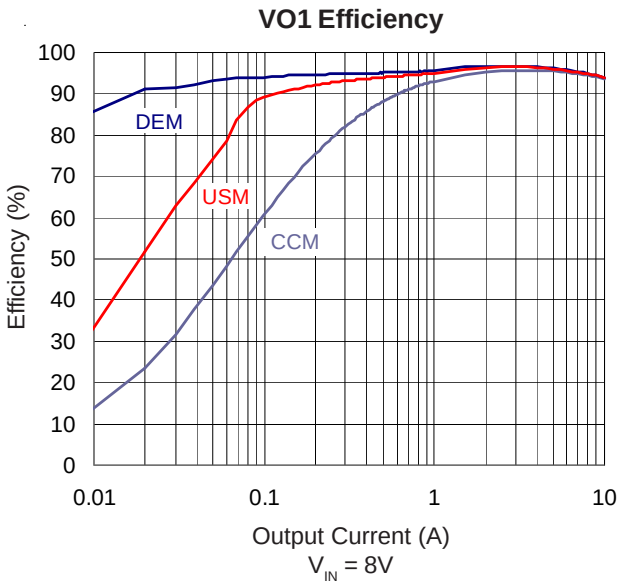
VO1 Load Regulation

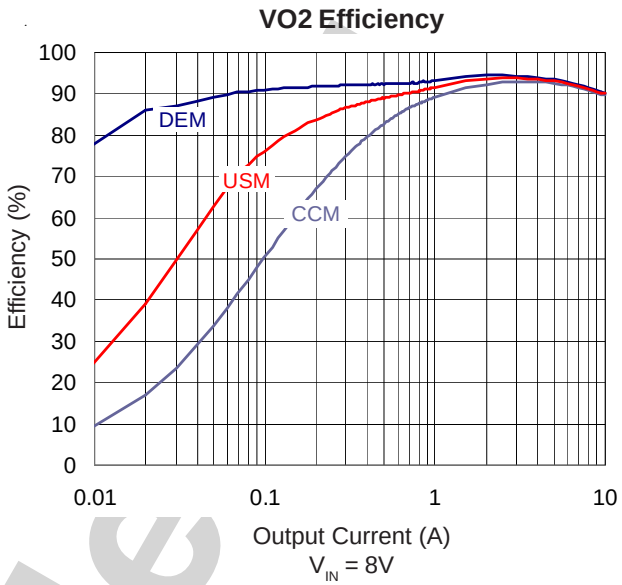


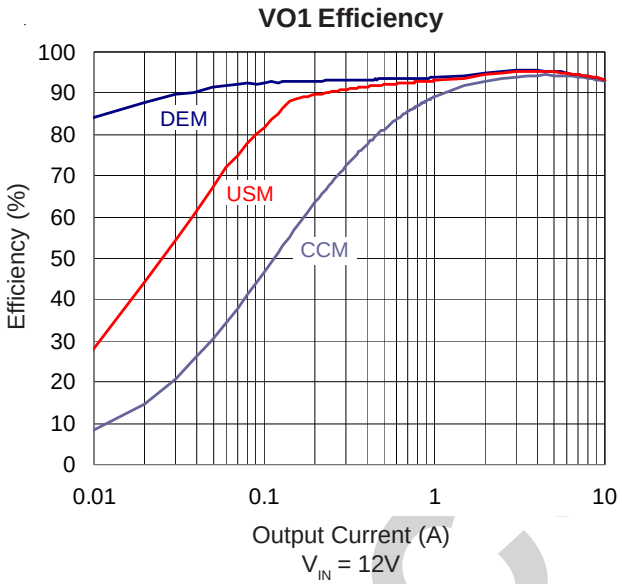
VO2 Load Regulation

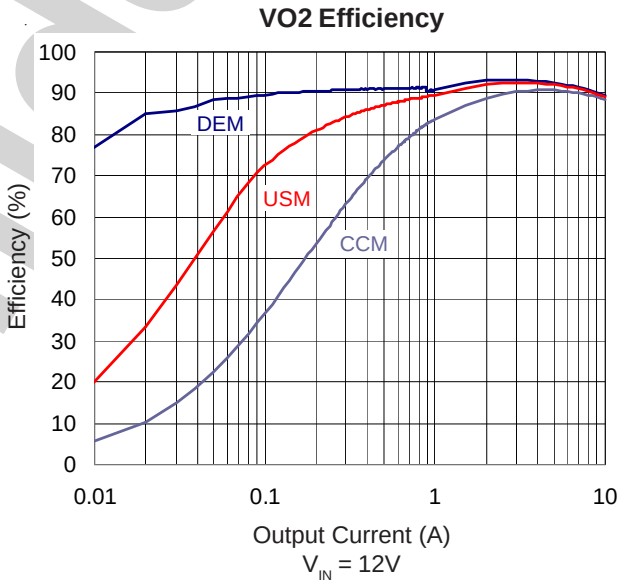


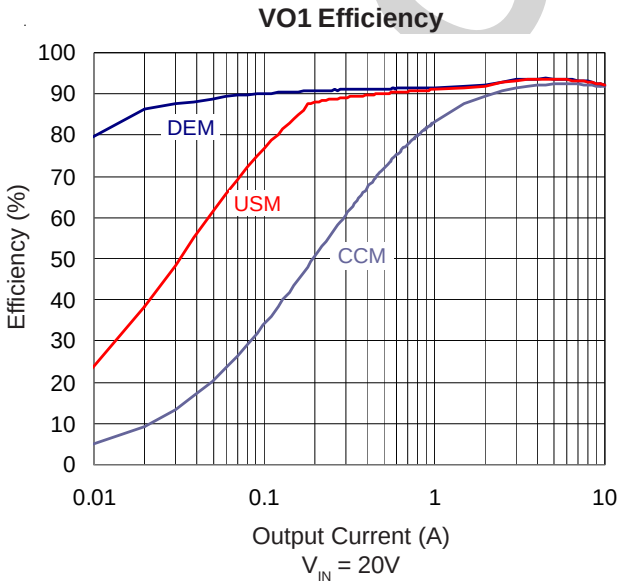
Typical Operation Characteristics

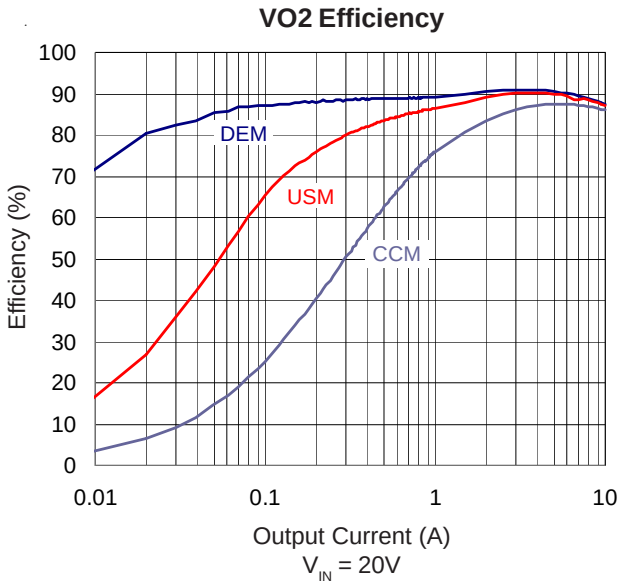












Application Information

Output Inductor Selection

The inductor plays an important role in step-down converters because it stores the energy from the input power rail and then releases the energy to the load. From the viewpoint of efficiency, the DC Resistance (DCR) of the inductor should be as small as possible to minimize the conduction loss. In addition, the inductor covers a significant proportion of the board space, so its size is also important. Low profile inductors can save board space especially when the height has a limitation. However, low DCR and low profile inductors usually cost ineffective.

Additionally, larger inductance results in lower ripple current, which translates into the lower power loss. However, the inductor current rising time increases with inductance value. This means the transient response will be slower. Therefore, the inductor design is a trade-off between performance, size and cost.

In general, the switching frequency (on-time) and operating point (% ripple or LIR) determine the inductor value as shown in the following equation:

$$L = \frac{t_{ON} \times (V_{IN} - VOx)}{LIR \times I_{LOAD(MAX)}}$$

where LIR is the ratio of the peak to peak ripple current to the average inductor current.

Find a low loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice because powdered iron is inexpensive and can work well at 200kHz. The core must be large enough to avoid saturating at the peak inductor current (I_{PEAK}):

$$I_{PEAK} = I_{LOAD(MAX)} + \frac{LIR}{2} \times I_{LOAD(MAX)}$$

The calculation above shall serve as a general reference. To further improve the transient response, the output inductance can be reduced even further. This needs to be considered along with the selection of the output capacitor.

Output Capacitor Selection

The capacitor value and ESR determine the amount of output voltage ripple and load transient response. Thus, the capacitor value must be greater than the largest value calculated from below equations:

$$V_{SOAR} = \frac{\Delta I_{LOAD}{}^2 \times L}{2 \times C_{OUT} \times VOx}$$

$$V_{P-P} = LIR \times I_{LOAD(MAX)} \times \left(ESR + \frac{1}{8 \times C_{OUT} \times f_{SW}} \right)$$

where V_{SOAR} are the allowable amount of undershoot voltage and overshoot voltage in the load transient, V_{P-P} is the output ripple voltage.

MOSFET Selection

The majority of power loss in the step-down power conveter is the loss in the power MOSFETs. For low voltage high current applications, the duty cycle of the upper MOSFET is small. Therefore, the switching loss of the upper MOSFET is of concern. Power MOSFETs with lower total gate charge are preferred in such kind of application. However, the small duty cycle means the lower MOSFET is on for most of the switching cycle. Therefore, the conduction loss tends to dominate the total power loss of the converter.

To improve the overall efficiency, MOSFETs with low $R_{DS(ON)}$ are preferred in the circuit design. In some cases, more than one MOSFET are connected in parallel to further decrease the on-state resistance. However, this depends on the MOSFET driver capability and the budget.

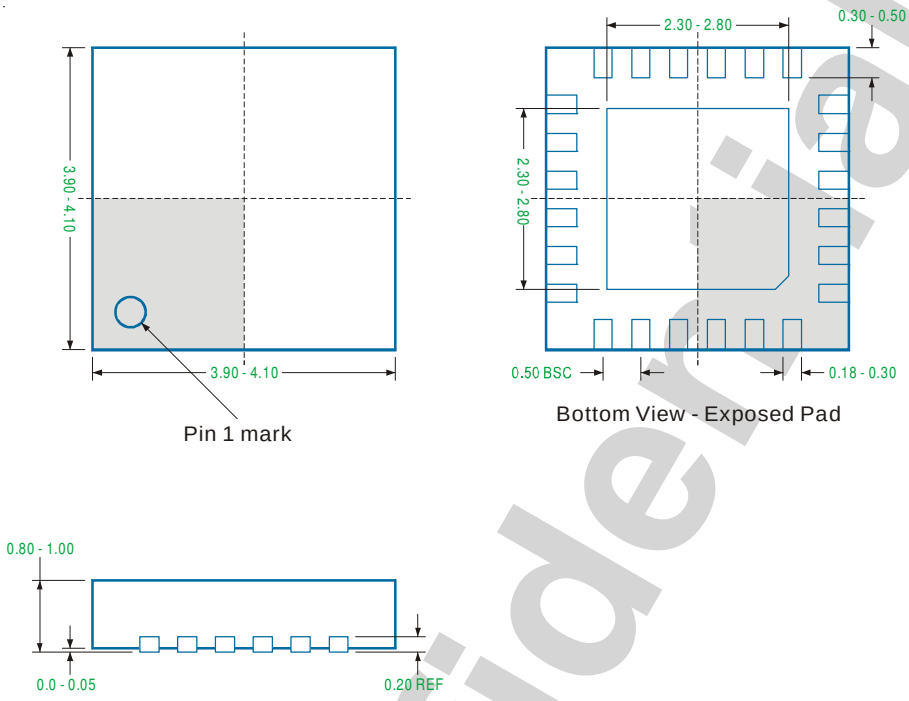
Layout Considerations

Layout is very important in high frequency switching converter designs, the PCB could radiate excessive noise and contribute to the converter instability with improper layout. Certain points must be considered before starting a layout.

- Place the filter capacitor close to the IC.
- Keep current limit setting network as close as possible to the IC. Routing of the network should avoid coupling to high voltage switching node.
- Connections from the drivers to the respective gate of both MOSFETs should be as short as possible to reduce stray inductance.
- All sensitive analog traces and components such as VOx, VFBx, GND, ENTRIPx, POK, and TONSEL should be placed away from high voltage switching nodes such as PHASEx, LGATEx, UGATEx, or BOOTx nodes to avoid coupling. Use internal layer(s) as ground plane(s) and shield the feedback trace from power traces and components.
- Place the ground terminals of VIN capacitor(s), VOx capacitor(s), and source of lower MOSFETs as close as possible. The PCB trace defined as PHASEx node, which connects to source of upper MOSFET, drain of lower MOSFET and high voltage side of the inductor, should be as short and wide as possible.

Package Information

VQFN4x4 - 24L



Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

Important Notice

uPI and its subsidiaries reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

uPI products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment. However, no responsibility is assumed by uPI or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of uPI or its subsidiaries.

uPI Semiconductor Corp.
Headquarter
9F.,No.5, Taiyuan 1st St. Zhubei City,
Hsinchu Taiwan, R.O.C.
TEL : 886.3.560.1666 FAX : 886.3.560.1888

Sales Branch Office
12F-5, No. 408, Ruiguang Rd. Neihu District,
Taipei Taiwan, R.O.C.
TEL : 886.2.8751.2062 FAX : 886.2.8751.5064