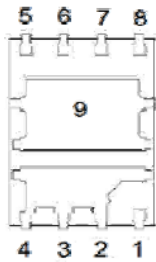
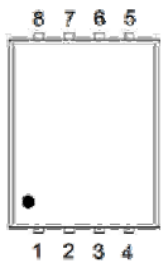


# PK650DY

## Dual N-Channel Enhancement Mode MOSFET

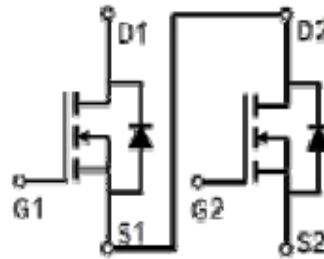
### PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	$I_D$	CH.
30V	2.8m $\Omega$ @ $V_{GS} = 10V$	83A	Q2
30V	11m $\Omega$ @ $V_{GS} = 10V$	36A	Q1



1 : G1  
2,3,4 : D1  
5,6,7 : S2  
8 : G2  
9 : S1/D2

PDFN 5\*6P



### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25\text{ }^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	CH.	LIMITS	UNITS
Drain-Source Voltage		$V_{DS}$	Q2	30	V
			Q1	30	
Gate-Source Voltage		$V_{GS}$	Q2	$\pm 20$	V
			Q1	$\pm 20$	
Continuous Drain Current <sup>3</sup>	$T_C = 25\text{ }^\circ\text{C}$	$I_D$	Q2	83	A
			Q1	36	
	$T_C = 100\text{ }^\circ\text{C}$		Q2	52	
			Q1	23	
Pulsed Drain Current <sup>1</sup>		$I_{DM}$	Q2	130	A
			Q1	55	
Continuous Drain Current	$T_A = 25\text{ }^\circ\text{C}$	$I_D$	Q2	21	A
			Q1	10	
	$T_A = 70\text{ }^\circ\text{C}$		Q2	17	
			Q1	8	
Avalanche Current		$I_{AS}$	Q2	52	A
			Q1	21	
Avalanche Energy	$L = 0.1\text{mH}$	$E_{AS}$	Q2	135	mJ
			Q1	22	
Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	$P_D$	Q2	36	W
			Q1	28	
	$T_C = 100\text{ }^\circ\text{C}$		Q2	14	
			Q1	11	

# PK650DY

## Dual N-Channel Enhancement Mode MOSFET

Power Dissipation	$T_A = 25\text{ }^\circ\text{C}$	$P_D$	Q2	2.4	W
			Q1	2	
	$T_A = 70\text{ }^\circ\text{C}$		Q2	1.5	
			Q1	1.3	
Operating Junction & Storage Temperature Range		$T_J, T_{STG}$	-55 to 150		$^\circ\text{C}$

### THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	CH.	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient <sup>2</sup>	$R_{\theta JA}$	Q2		51	$^\circ\text{C} / \text{W}$
		Q1		60	
Junction-to-Case	$R_{\theta JC}$	Q2		3.4	
		Q1		4.4	

<sup>1</sup>Pulse width limited by maximum junction temperature  $T_{J(\text{MAX})}=150^\circ\text{C}$ .

<sup>2</sup>The value of  $R_{\theta JA}$  is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A = 25^\circ\text{C}$ . The value in any given application depends on the user's specific board design.

<sup>3</sup>Package limitation current :Q1=29A,Q2=42A.

### ELECTRICAL CHARACTERISTICS ( $T_J = 25\text{ }^\circ\text{C}$ , Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	CH.	LIMITS			UNITS	
				MIN	TYP	MAX		
<b>STATIC</b>								
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu\text{A}$	Q2	30			V	
			Q1	30				
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	Q2	1.3	1.75	2.3	V	
			Q1	1.3	1.75	2.3		
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0V, V_{GS} = \pm 20V$	Q2			$\pm 100$	nA	
			Q1			$\pm 100$		
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 24V, V_{GS} = 0V$	Q2			1	$\mu\text{A}$	
			Q1			1		
		$V_{DS} = 20V, V_{GS} = 0V, T_J = 55\text{ }^\circ\text{C}$	Q2			10		
			Q1			10		
Drain-Source On-State Resistance <sup>1</sup>	$R_{DS(ON)}$	$V_{GS} = 4.5V, I_D = 16A$	Q2		2.1	3.8	m $\Omega$	
			Q1	$V_{GS} = 4.5V, I_D = 10A$		10		14
				$V_{GS} = 10V, I_D = 20A$	Q2			1.6
			Q1	$V_{GS} = 10V, I_D = 10A$		6.8		11
Forward Transconductance <sup>1</sup>	$g_{fs}$	$V_{DS} = 5V, I_D = 20A$	Q2		55		S	
		$V_{DS} = 5V, I_D = 10A$	Q1		40			

# PK650DY

## Dual N-Channel Enhancement Mode MOSFET

DYNAMIC							
Input Capacitance	$C_{iss}$	$V_{GS} = 0V,$ $V_{DS} = 15V, f = 1MHz$	Q2		3685	pF	
Output Capacitance	$C_{oss}$		Q1		531		
			Q2		615		
Reverse Transfer Capacitance	$C_{rss}$		Q1		147		
			Q2		388		
Gate Resistance	$R_g$		Q1		67		
		Q2		1			
Total Gate Charge <sup>2</sup>	$Q_g$	$V_{DS} = 15V, I_D = 20A$ Q2 $V_{DS} = 15V, I_D = 10A$ Q1	Q2		72	nC	
			Q1		10		
Gate-Source Charge <sup>2</sup>	$Q_{gs}$		Q2		37		
			Q1		5.6		
Gate-Drain Charge <sup>2</sup>	$Q_{gd}$		Q2		10		
			Q1		1.4		
Turn-On Delay Time <sup>2</sup>	$t_{d(on)}$		Q2		18		
			Q1		3		
Rise Time <sup>2</sup>	$t_r$		Q2		32		nS
			Q1		15		
Turn-Off Delay Time <sup>2</sup>	$t_{d(off)}$		Q2		16		
			Q1		13		
Fall Time <sup>2</sup>	$t_f$	Q2		72			
		Q1		21			
<b>SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (<math>T_J = 25^\circ C</math>)</b>							
Continuous Current <sup>3</sup>	$I_S$		Q2		36	A	
			Q1		23		
Forward Voltage <sup>1</sup>	$V_{SD}$	$I_F = 20A, V_{GS} = 0V$	Q2		1	V	
		$I_F = 10A, V_{GS} = 0V$	Q1		1.2		
Reverse Recovery Time	$t_{rr}$	Q2 $I_F = 20A, di_F/dt = 100A/\mu S$	Q2		28	nS	
			Q1		8.8		
Reverse Recovery Charge	$Q_{rr}$	Q1 $I_F = 10A, di_F/dt = 100A/\mu S$	Q2		13	nC	
			Q1		1.2		

<sup>1</sup>Pulse test : Pulse Width  $\leq 300 \mu sec$ , Duty Cycle  $\leq 2\%$ .

<sup>2</sup>Independent of operating temperature.

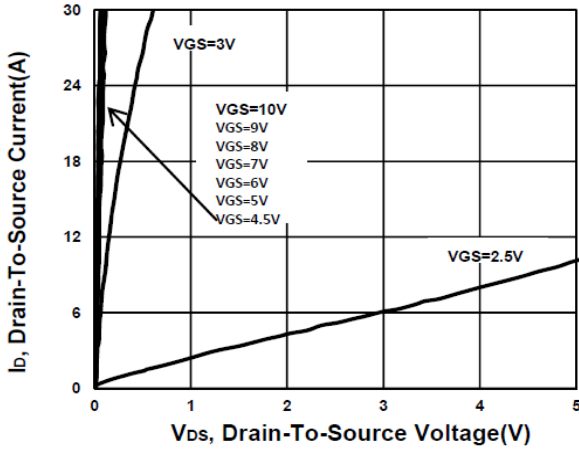
<sup>3</sup>Package limitation current : Q1=29A, Q2=42A.

# PK650DY

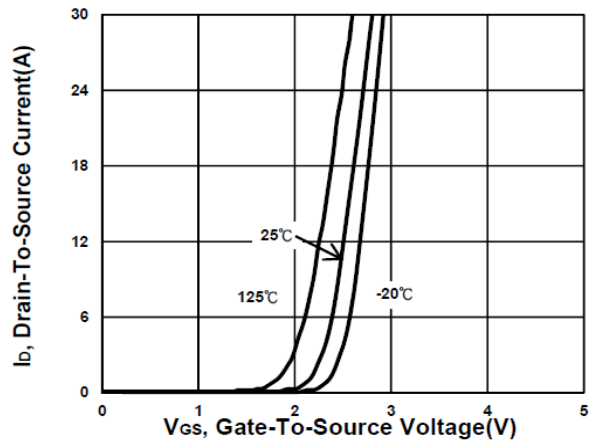
## Dual N-Channel Enhancement Mode MOSFET

Q2

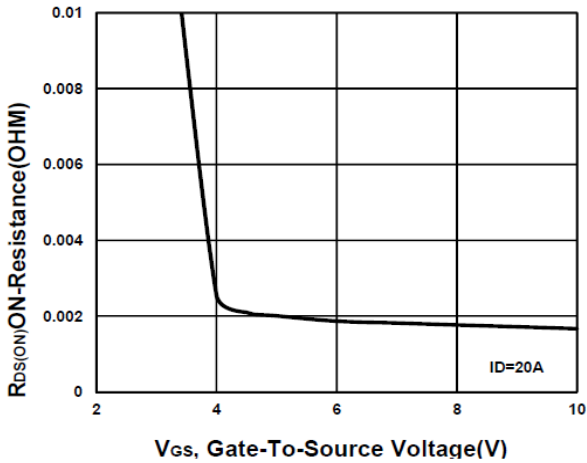
**Output Characteristics**



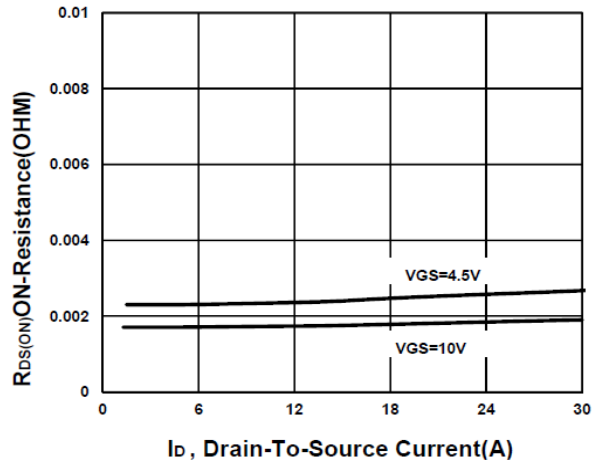
**Transfer Characteristics**



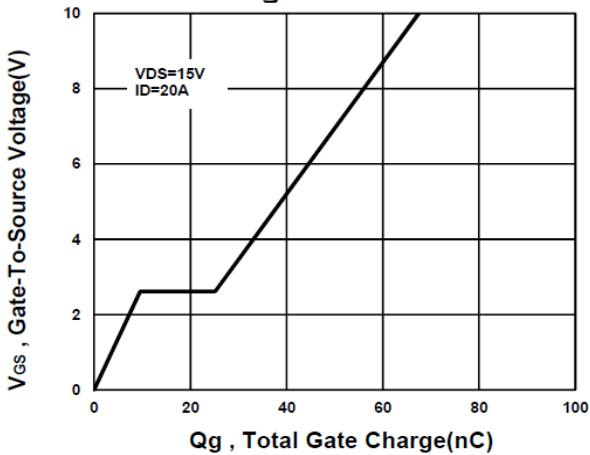
**On-Resistance VS Gate-To-Source**



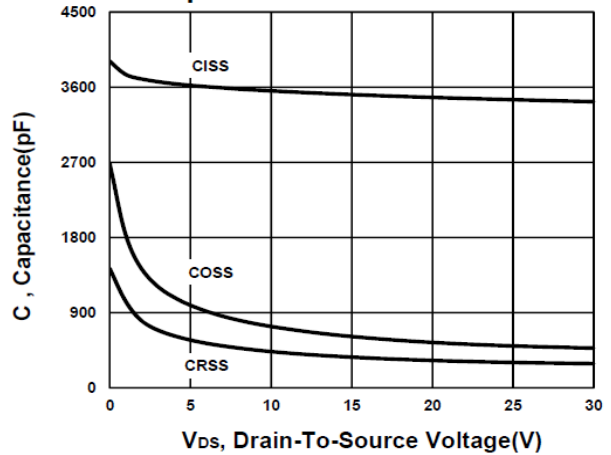
**On-Resistance VS Drain Current**



**Gate charge Characteristics**



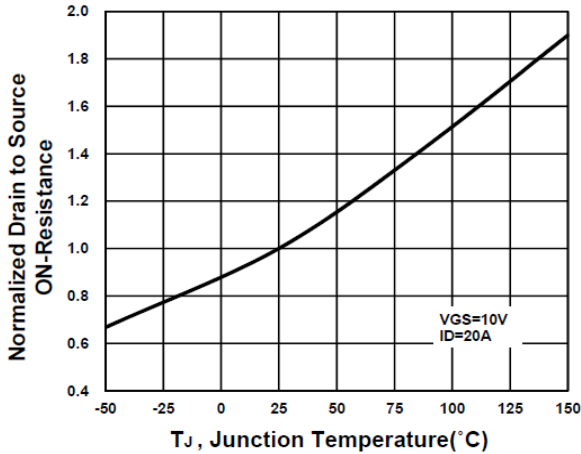
**Capacitance Characteristic**



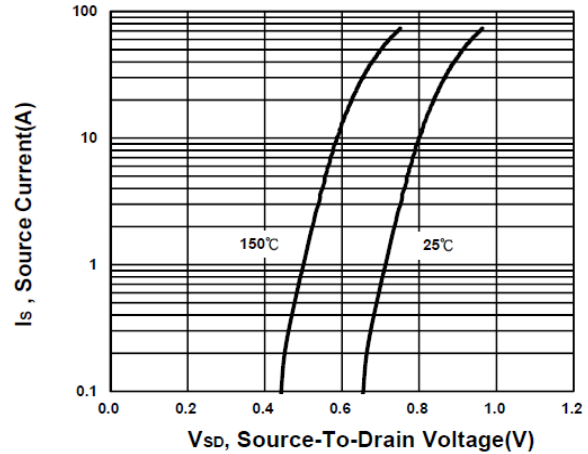
# PK650DY

## Dual N-Channel Enhancement Mode MOSFET

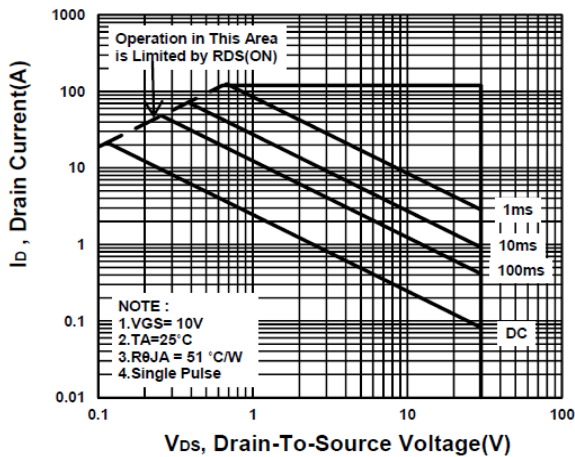
**On-Resistance VS Temperature**



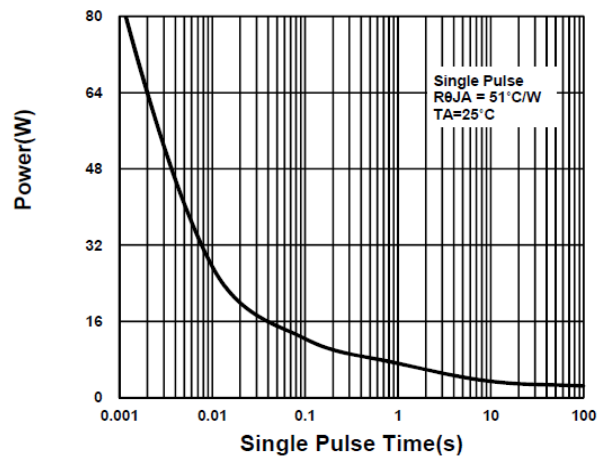
**Source-Drain Diode Forward Voltage**



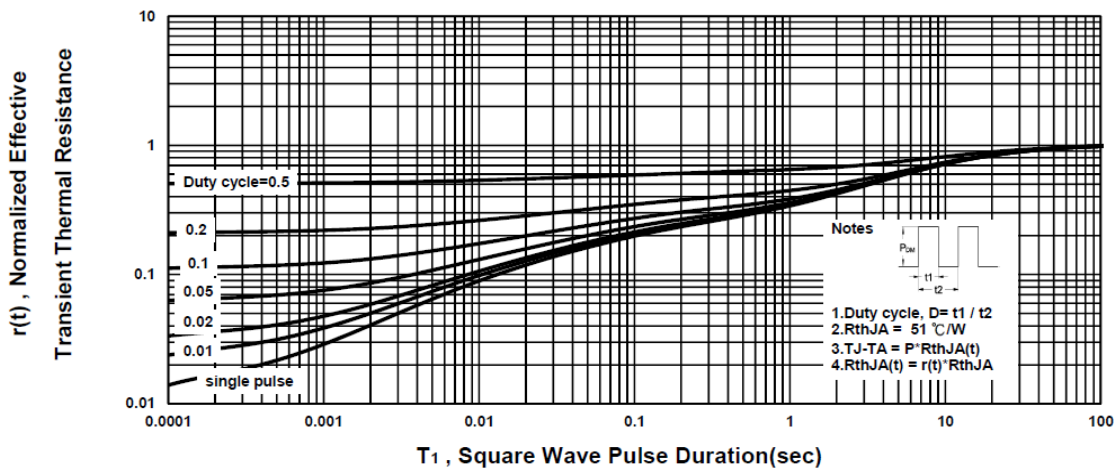
**Safe Operating Area**



**Single Pulse Maximum Power Dissipation**



**Transient Thermal Response Curve**

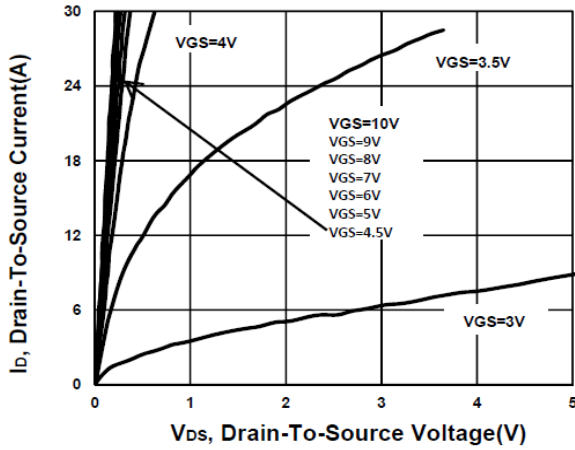


# PK650DY

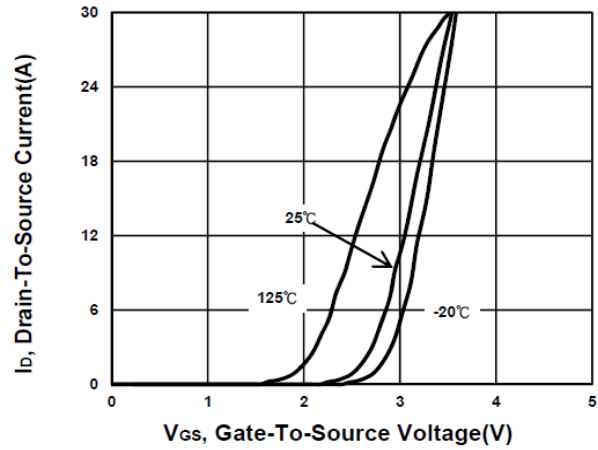
## Dual N-Channel Enhancement Mode MOSFET

Q1

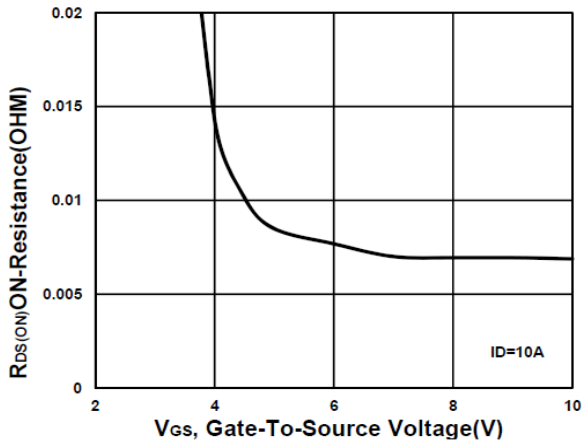
**Output Characteristics**



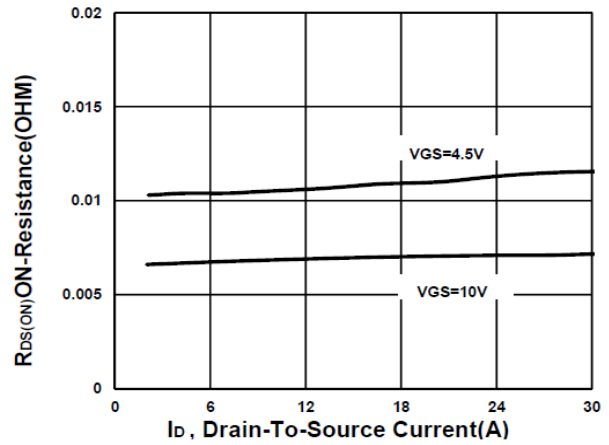
**Transfer Characteristics**



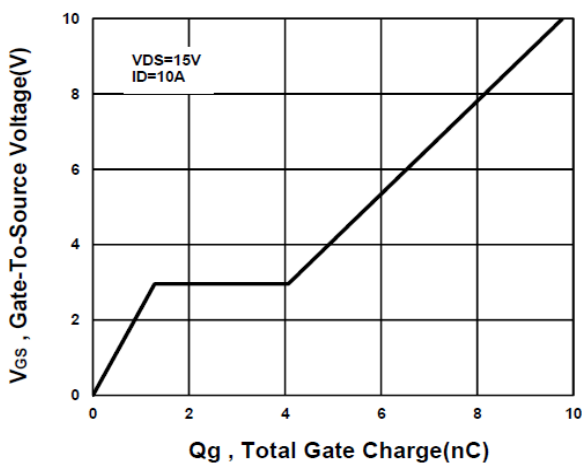
**On-Resistance VS Gate-To-Source**



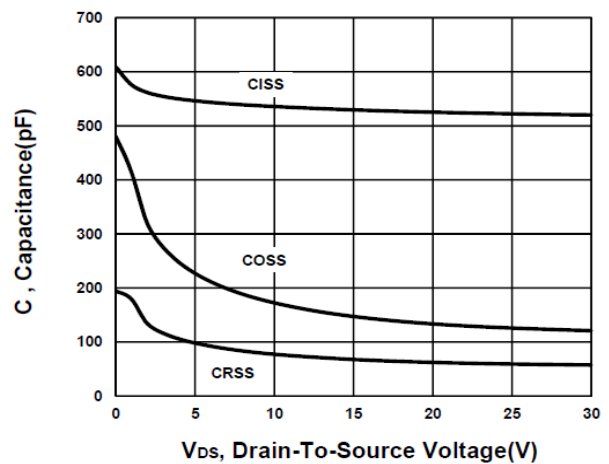
**On-Resistance VS Drain Current**



**Gate charge Characteristics**

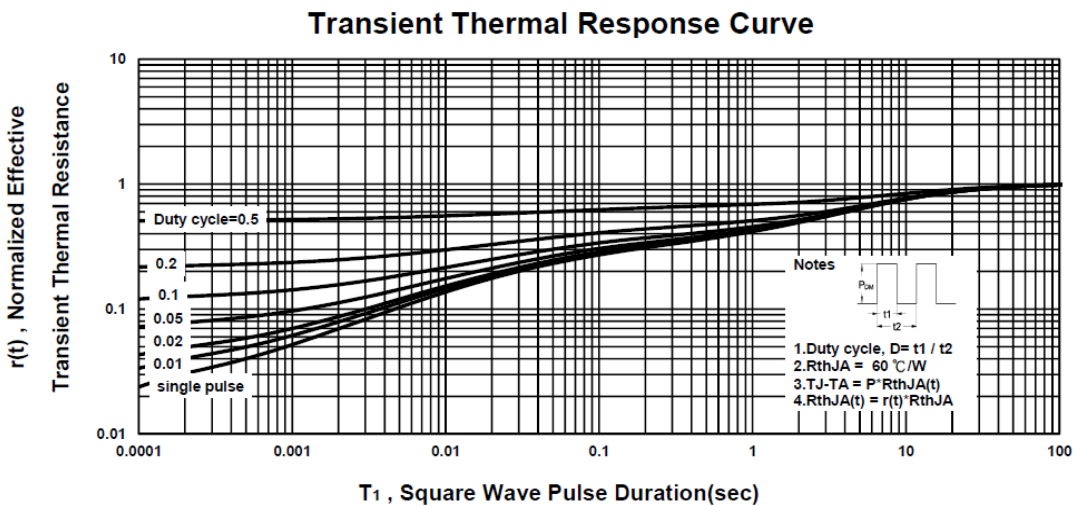
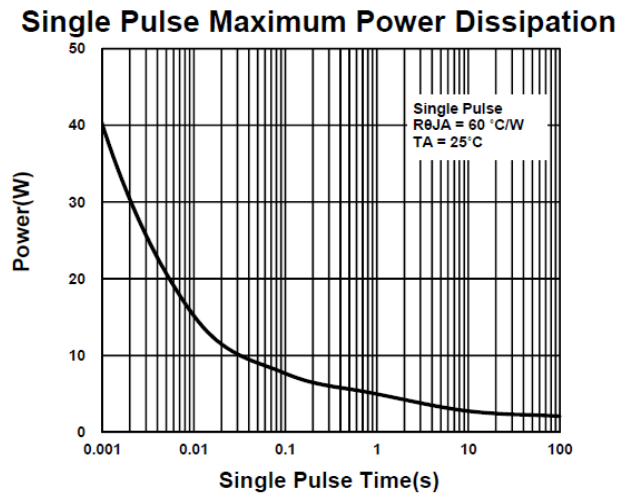
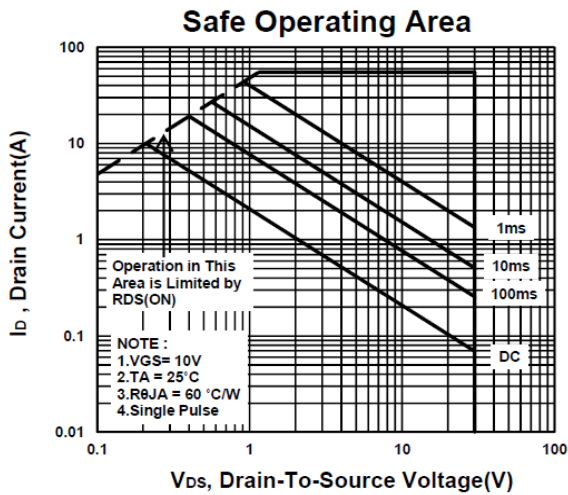
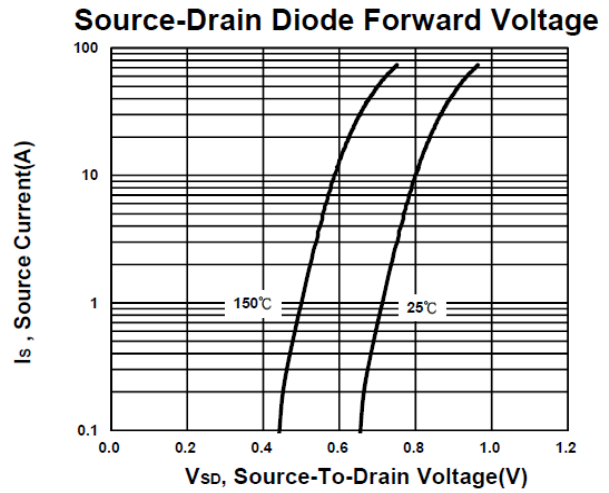
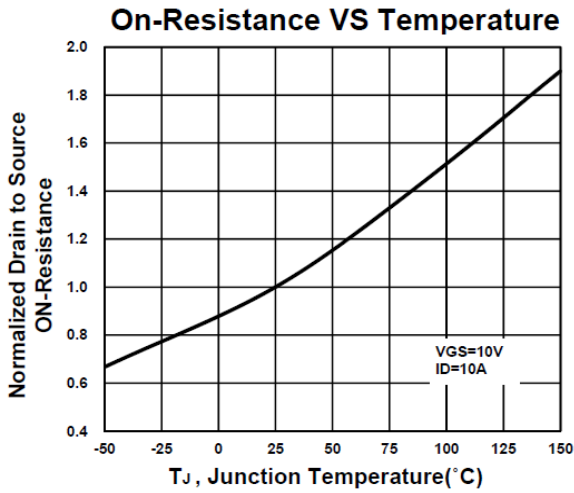


**Capacitance Characteristic**



# PK650DY

## Dual N-Channel Enhancement Mode MOSFET



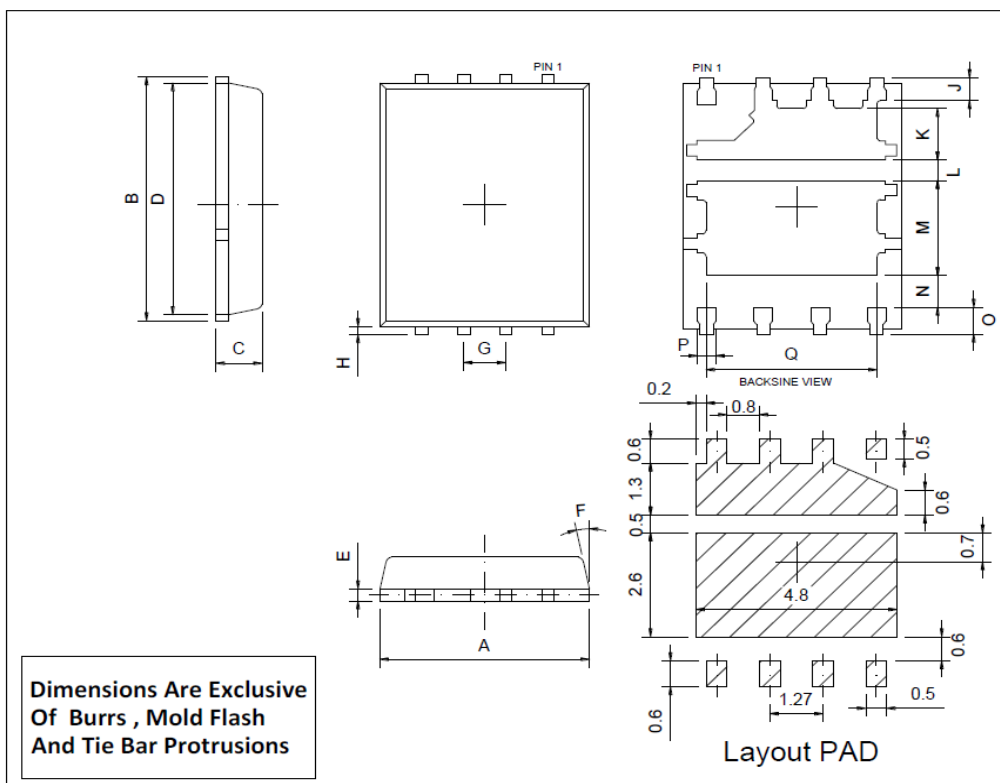
# PK650DY

## Dual N-Channel Enhancement Mode MOSFET

### Package Dimension

### PDFN 5x6P(上下 Dual) MECHANICAL DATA

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	4.8	5	5.4	K	0.82	1.06	1.3
B	5.9	6.15	6.35	L	0.4	0.5	0.6
C	0.9	1	1.18	M	2.0	2.21	2.42
D	5.42	5.59	5.85	N	0.5	1	
E	0.15	0.25	0.35	O	0.42	0.56	0.71
F	0°	6°	12°	P	0.3	0.4	0.51
G	1.17	1.27	1.37	Q	3.61	4.05	4.5
H	0.06	0.21	0.36				
J	0.41	0.55	0.7				



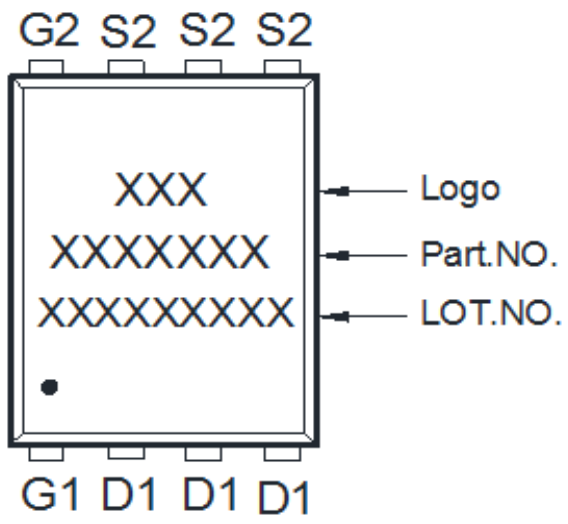
\* 散热片形状会因为封装厂框架不同而有所差异。



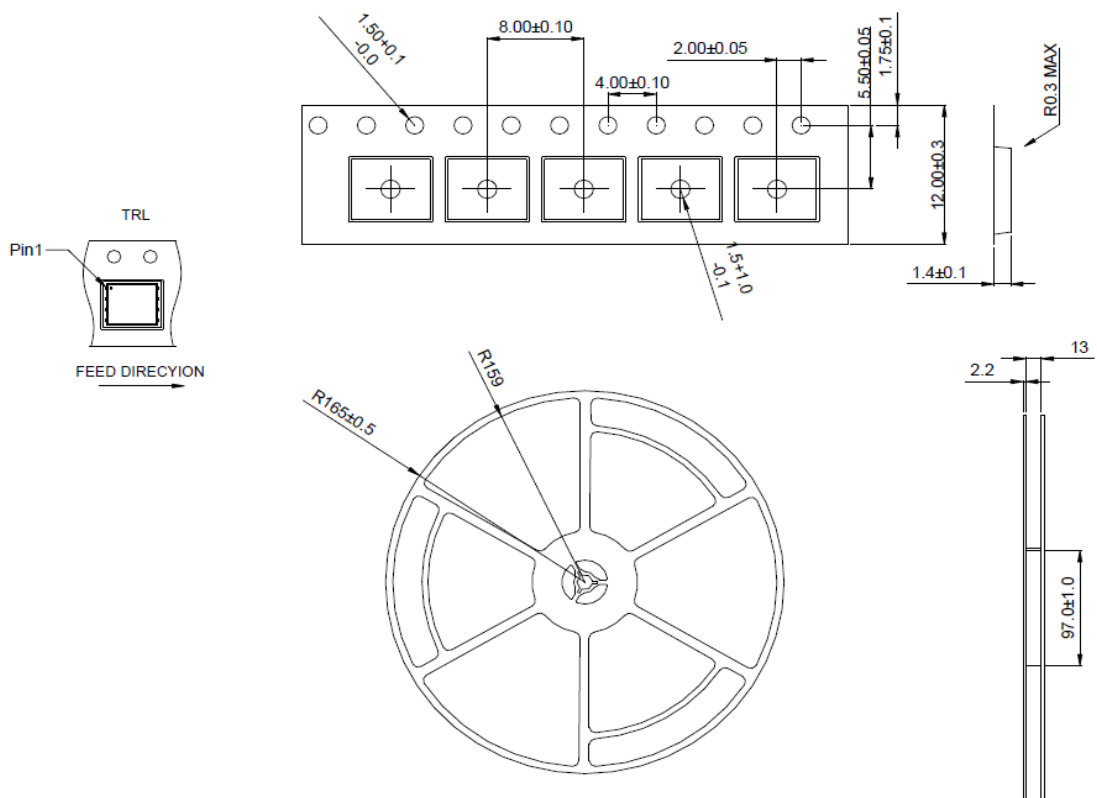
# PK650DY

## Dual N-Channel Enhancement Mode MOSFET

### A. Marking Information



### B. Tape & Reel Information: 3000pcs/Reel

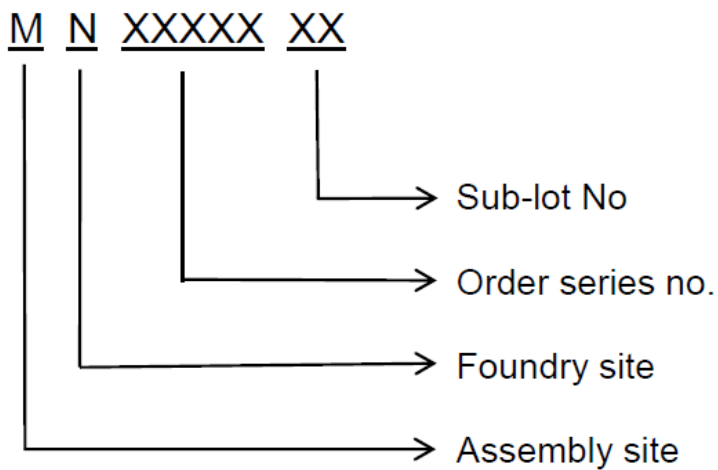


# PK650DY

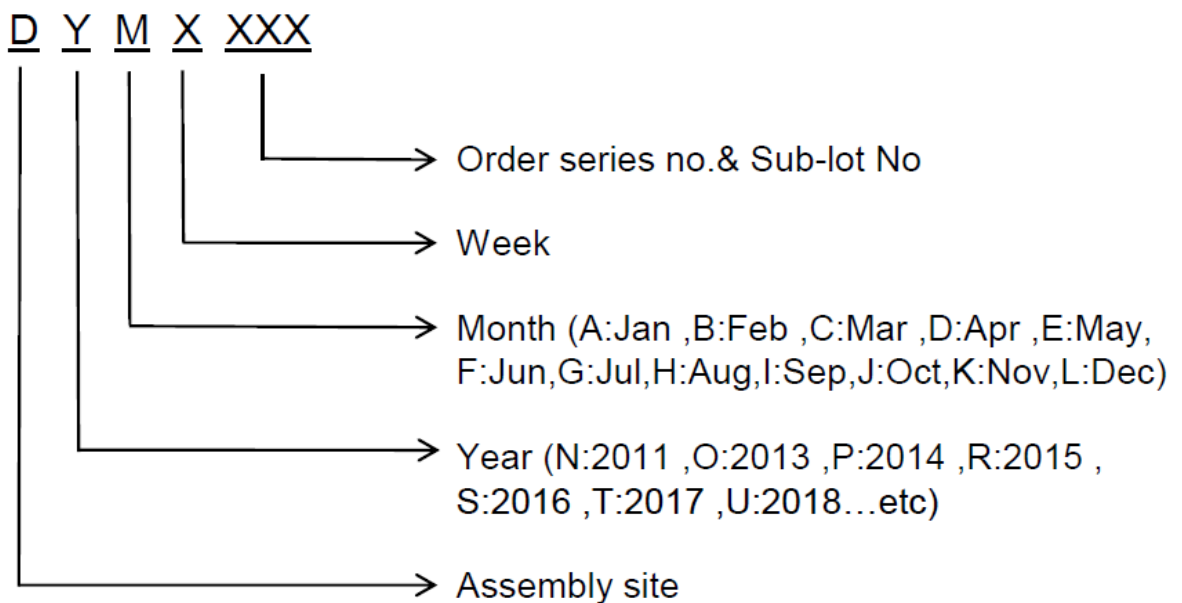
## Dual N-Channel Enhancement Mode MOSFET

### C. Lot No.&Date Code rule

#### 1.Lot No.



#### 2.Date Code





# PK650DY

## Dual N-Channel Enhancement Mode MOSFET

### D.Label rule

标签内容(Label content)



1	Label Size	30 * 90 mm
2	Font style	Times New Roman or Arial (或可区分英文”0”和数字”0”，”G和”Q”的字型即可)
3	U-NIKC	Height: 4 mm
4	Package	Height: 2 mm
5	Date	Height: 2 mm Shipping date: YYYY/MM/DD, ex. 2008/09/12
6	Device	Height: 3 mm (Max: 16 Digit)
7	Lot	Height: 3 mm (Max: 9 Digit) Sub lot
8	D/C	Height: 3 mm (Max: 7 Digit)
9	QTY	Height: 3 mm (Max: 6 Digit) Thousand mark is no needed
10	RoHS label	 long axis: 12 mm minor axis:6 mm bottom color: White Font color: Black Font style: Arial
11	Halogen Free label	 Diameter: 10 mm bottom color: Green Font color: Black Font style: Arial
12	Scan information	Device / Lot / D/C / QTY , Insert “ / “ between every parts. for example: P3055LDG/G12345601/GGG2301/2000 DPI (Dots per inch): Over 300 dpi Code : Code 128 Height: 6 mm at least