# APL6012

ANPEC

Low-Power, 8-bit, 15-Channel Analog to Digital Converters

Features

- **Supply Input Voltages Range: 2.8V to 5.5V**
- **100uA Low Support Current**
- **15-Ch Analog Voltage Input: AIN1, AIN2, AIN3,**
- **AIN4, AIN5, AIN6, AIN7, AIN8, AIN9, AIN10, AIN11, AIN12, AIN13, AIN14, AIN15.**
- **High Accuracy Nonlinearity: $\pm$1.5LSB**
- **High Accuracy A/D Resolution: 10mV**
- **High Accuracy A/D Full Scale Range: 1~3.56V**
- **Built-in Alert Flag Functions**
- **Built-in I²C Address Programming Functions**

Pin Configurations

APL6012

TQFN 3x3-20P
(Top View)

General Description

The APL6012 is a precision analog-to-digital converters (ADCs) with 8 bits of resolution, which designed with precision, low power and ease of implementation in mind. Data are transferred via an I²C-compatible serial interface. Three voltage sensing inputs are available for monitoring the temperature of the system. It measures voltage form the monitor place to GND by NTC resistor divider voltages. The sensed voltages are digitized and interfaced with microprocessor by I²C bus for advanced power management procedures.
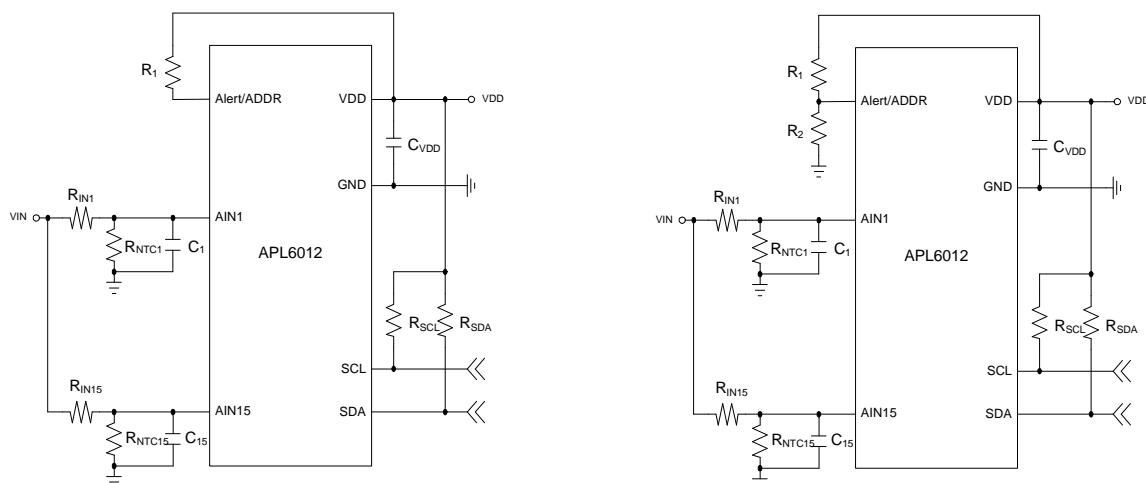
The APL6012 operates from a single power supply ranging from 2.8V to 5.5V.

This APL6012 is available in TQFN3x3-20P package.

Applications
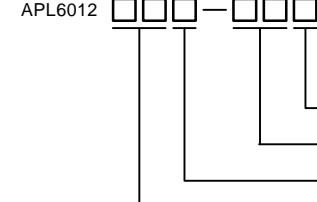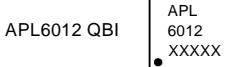
- **Phone & NB Application**
- **Temperature Measurement**
- **Portable Instrumentation**
- **Consumer Goods**

Simplified Application Circuit

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Ordering and Marking Information

APL6012 ☐☐☐ — ☐☐☐

- Assembly Material
- Handling Code
- Temperature Range
- Package Code

Package Code
   QB : TQFN 3x3-20P
Operating Ambient Temperature Range
   I : -40 to 85°C
Handling Code
   TR : Tape & Reel
Assembly Material
   G : Halogen and Lead Free Device

APL6012 QBI

APL
6012
XXXXX

X : Date Code

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant)and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter		Rating	Unit
VDD	VDD Supply Voltage, VDD to GND		-0.3 ~ 6.0	V
$V_{I/O}$	Input & Output or I/O (Alert/ADDR, SCL, SDA, AIN1, AIN2, AIN3,AIN4, AIN5, AIN6, AIN7, AIN8, AIN9, AIN10, AIN11, AIN12, AIN13, AIN14, AIN15.) voltages		-0.3 ~ VDD	V
PD	Power Dissipation		Internally Limited	W
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature		-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)		260	°C
V_{ESD}	Minimum ESD Rating	(Human Body Mode)	±2	kV
		(Machine Mode)	0.2	
		(Charged-Device Mode)	±1.5	

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2)	65	°C/W

Note 2 : θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

| Symbol	Parameter	Range	Unit
VDD	VDD Supply Voltage, VDD to GND	2.8 ~ 5.5	V
$V_{I/O}$	Input & Output pins (Alert/ADDR, SCL, SDA) voltage	0 ~ VDD	V
V_{AIN}	Input pins (AIN1, AIN2, AIN3,AIN4, AIN5, AIN6, AIN7, AIN8, AIN9, AIN10, AIN11, AIN12, AIN13, AIN14, AIN15.) voltage	1 ~ 3.56	V
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Electrical Characteristics
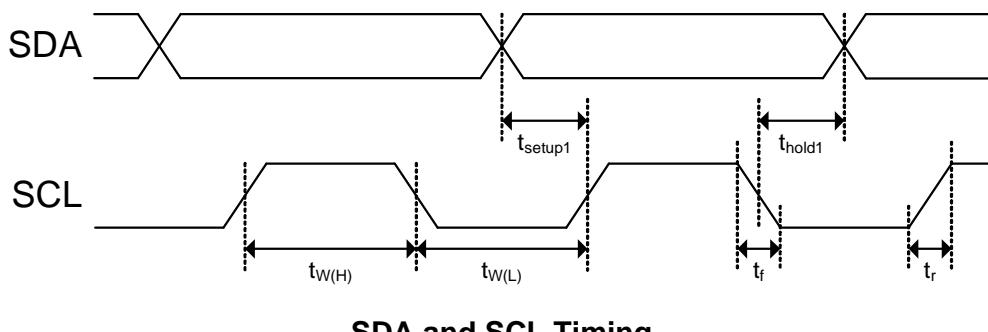
Unless otherwise specified, these specifications apply over V_{DD}=5V, and T_J= -40 to 85°C. Typical values are at T_J=25°C.

| Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
SUPPLY CURRENT						
I_{VDD}	VDD Input Current		-	80	100	uA
POWER-ON RESET (POR)						
V_{POR}	VDD POR Threshold Voltage	VDD Rising	2.35	2.5	2.6	V
V_{POR_Hys}	VDD POR Hysteresis Voltage	VDD Falling	-	0.3	-	V
Voltage Monitor						
A/D	A/D Resolution		-	10	-	mV/LSB
	A/D Full Scale Range		1	-	3.56	V
	Differential nonlinearity		-	-	1.5	LSB
	Differential nonlinearity	VDD=3.6V	-	-	2.5	LSB
	Integral nonlinearity		-	-	1.5	LSB
	Integral nonlinearity	VDD=3.6V	-	-	2.5	LSB
	Input Bias Current		-	-	10	nA
	AIN1, AIN2, AIN3, AIN4, AIN5, AIN6, AIN7, AIN8, AIN9, AIN10, AIN11, AIN12, AIN13, AIN14, AIN15. Monitor Time		0.48	0.6	0.72	ms
Address Setting and Alert Output						
ADDR	Address Latch Time		-	-	10	ms
	Address 1 Voltage Range	Address = 0x7E (Hex)	92	95	100	%VDD
	Address 2 Voltage Range	Address = 0x7C (Hex)	82	85	88	%VDD
	Address 3 Voltage Range	Address = 0x7A (Hex)	72	75	78	%VDD
	Address 4 Voltage Range	Address = 0x78 (Hex)	63	65	68	%VDD
	Address 5 Voltage Range	Address = 0x76 (Hex)	52	55	58	%VDD
	Address 6 Voltage Range	Address = 0x74 (Hex)	42	45	48	%VDD
	Address 7 Voltage Range	Address = 0x72 (Hex)	32	35	38	%VDD
	Address 8 Voltage Range	Address = 0x70 (Hex)	22	25	28	%VDD
Alert	Alert Output Low Voltage	When Alert/ADDR pin pull low, I_{ALT}=10mA	-	-	0.2	V
		When Alert/ADDR pin pull low, I_{ALT}=50mA	-	-	0.8	V
	Alert Pull Low Pulse Time	When Alert/ADDR pin Alert	40	50	60	us
	Alert Pull Low cycle Time	When Alert/ADDR pin Alert	-	2	-	s
	Alert/ADDR Leakage Current	$V_{Alert/ADDR}$=5V	-	-	100	nA
I²C Interface						
F_{I2C}	I²C Clock Rate Range		1	400	440	kHz
	I²C Input High Voltage		1.4	-	-	V
	I²C Input Low Voltage		-	-	0.4	V
	I²C Leakage Current	V_{SCL}=V_{SDA}=5V	-	-	100	nA
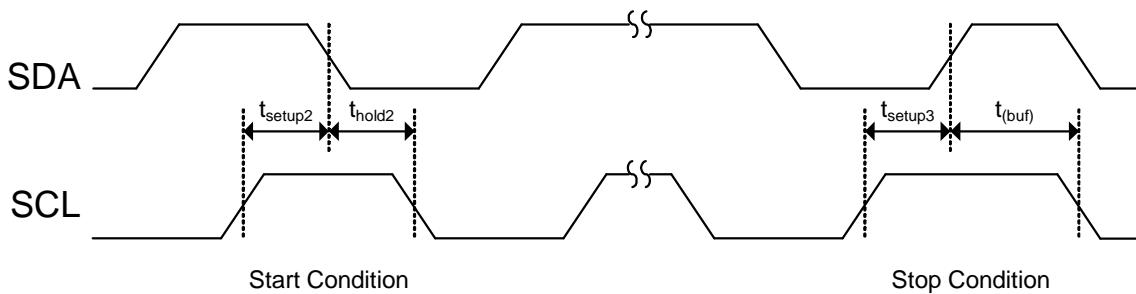
Electrical Characteristics (Cont.)

Timing characteristics for I²C Interface signals over recommended operating conditions (unless otherwise noted)

| Symbol	Parameter	Fast Speed		Unit
		Min.	Max.	
f_{SCL}	Frequency, SCL	-	400	kHz
$t_{W(H)}$	Pulse Duration, SCL High	600	-	ns
$t_{W(L)}$	Pulse Duration, SCL Low	1300	-	ns
t_r	Rise Time, SCL and SDA	20+0.1 C_L(pF)	300	ns
t_f	Fall Time, SCL and SDA	20+0.1 C_L(pF)	300	ns
t_{setup1}	Setup Time, SCL to SDA	100	-	ns
t_{hold1}	Hold Time, SCL to SDA	100	-	ns
$t_{(buf)}$	Bus Free Time Between Stop and Start Condition	1300	-	ns
t_{setup2}	Setup Time, SCL to Start Condition	600	-	ns
t_{hold2}	Hold Time, Start condition to SCL	600	-	ns
t_{setup3}	Setup Time, SCL to Stop Condition	600	-	ns
C_L	Load Capacitance for Each Bus Line	-	400	pF
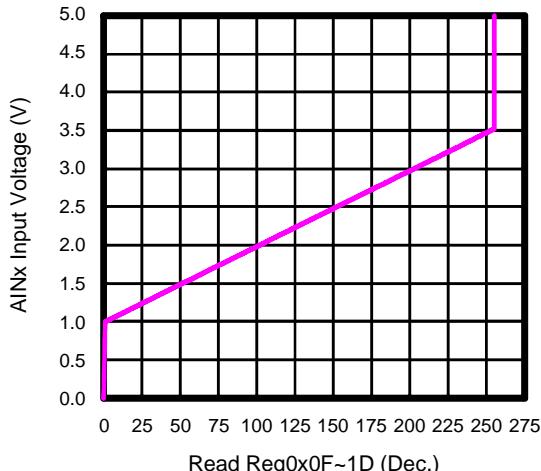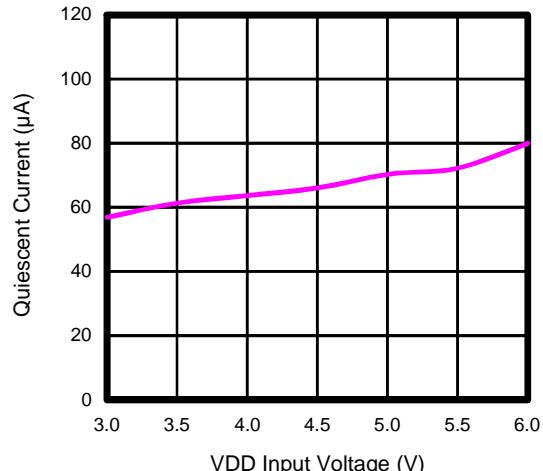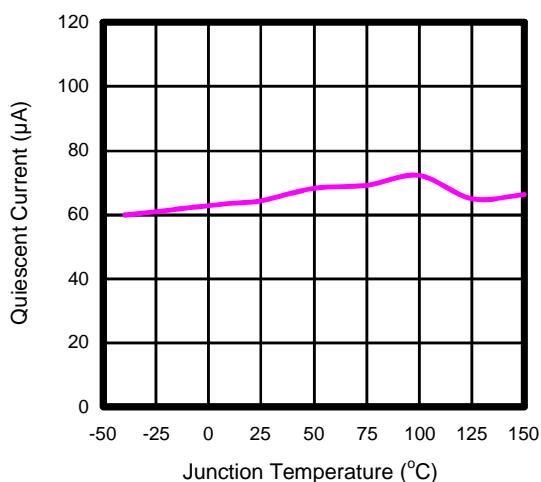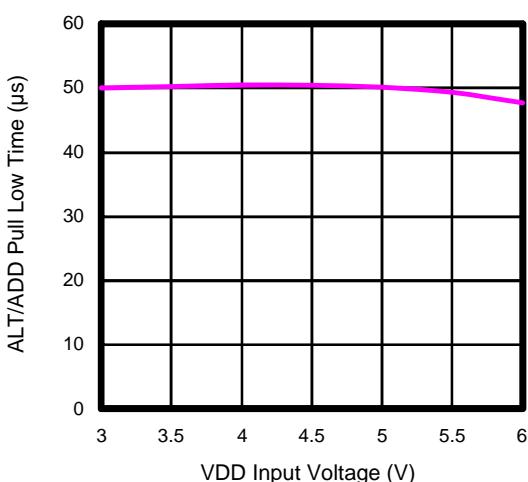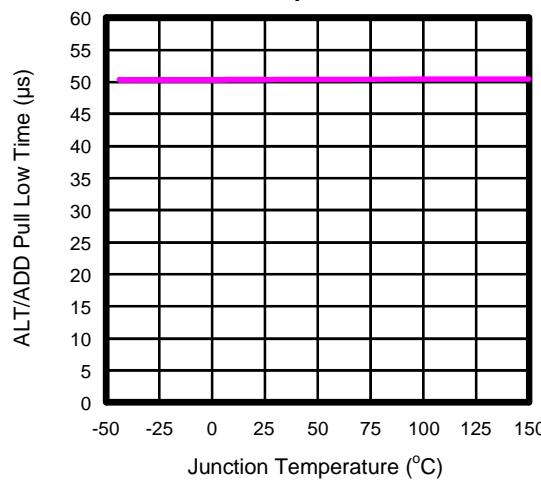
SDA and SCL Timing

Start and Stop Condition Timing
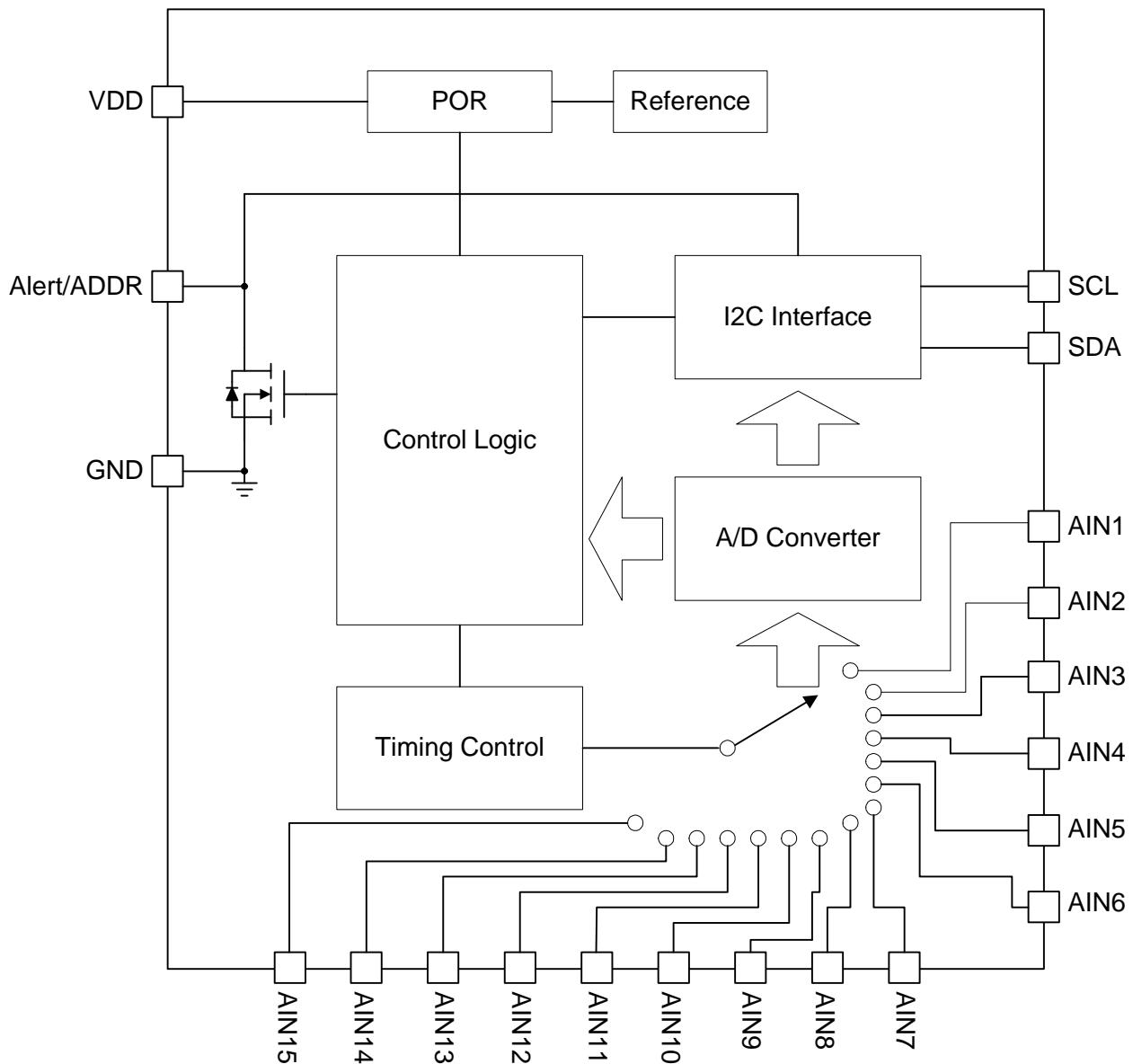
## Typical Operating Characteristics

**AIN1~15 vs. Reg0x0F~1D**

Quiescent Current vs. VDD

Quiescent Current vs. Temperature

Alert Low Pulse Time vs. VDD

**Alert Low Pulse Time vs. Temperature**

Pin Description
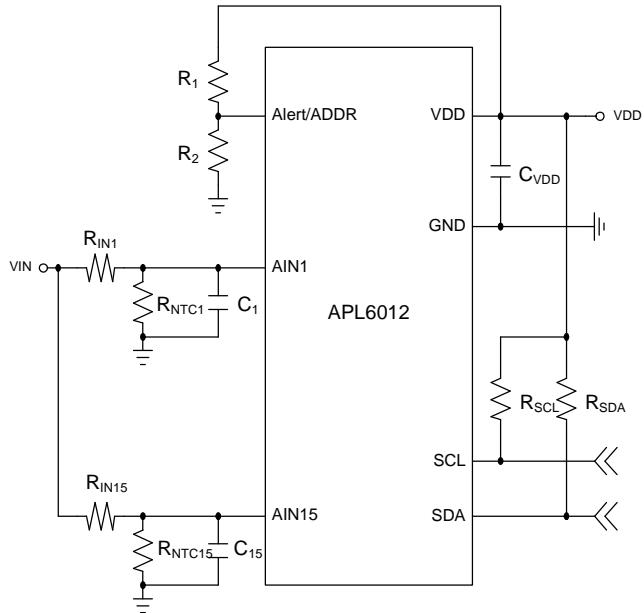
| PIN		FUNCTION
NO.	NAME	
1	SDA	I²C interface Data I/O pin. Connect this pin to I²C bus data signal.
2	SCL	I²C interface Clock I/O pin. Connect this pin to I²C bus clock signal.
3	VDD	Device power supply pin. Connect this pin with 0.1uF capacitor.
4	GND	Signal and Power Ground. All the voltage levels are measured by reference to this pin.
5	Alert/ADDR	Address Selection and Thermal Alert. Connect a voltage divider to select the APL6012 I²C address. When anyone of V_{AINx} is lower than setting voltage, it will pull low and send alert signal to the system. Connect this pin without any capacitor. **Do not leave NC(ADDR) pin floating.**
6	AIN1	Analog Voltage Input 1.
7	AIN2	Analog Voltage Input 2.
8	AIN3	Analog Voltage Input 3.
9	AIN4	Analog Voltage Input 4.
10	AIN5	Analog Voltage Input 5.
11	AIN6	Analog Voltage Input 6.
12	AIN7	Analog Voltage Input 7.
13	AIN8	Analog Voltage Input 8.
14	AIN9	Analog Voltage Input 9.
15	AIN10	Analog Voltage Input 10.
16	AIN11	Analog Voltage Input 11.
17	AIN12	Analog Voltage Input 12.
18	AIN13	Analog Voltage Input 13.
19	AIN14	Analog Voltage Input 14.
20	AIN15	Analog Voltage Input 15.

Block Diagram
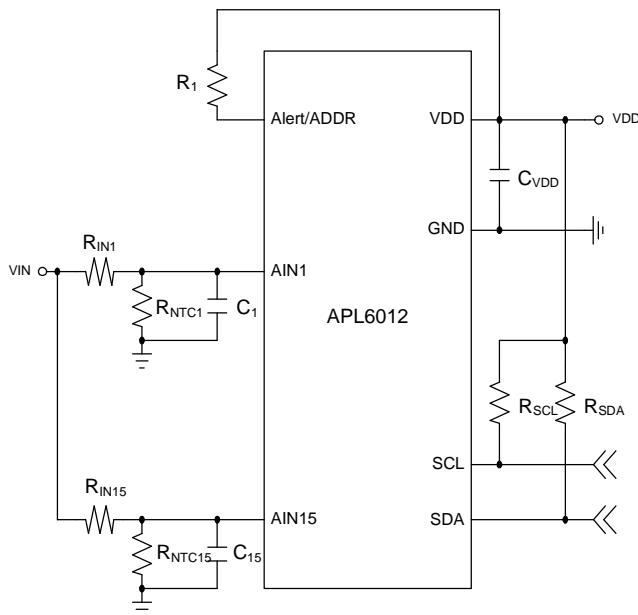
Typical Application Circuit

The I²C Address Programming and Alert Flag functions are used.

The I²C Address is used as default and Alert Flag function is unused.

V_{AINx} = 1~3.56V is recommended.

R_{INx} and R_{NTCx} = 10kΩ~10MΩ is recommended.

C_{VDD}, C_1, C_2 and $C_3 \geq$ 0.1uF is recommended.

R_{SCL} and R_{SDA} = 1kΩ~10kΩ is recommended.
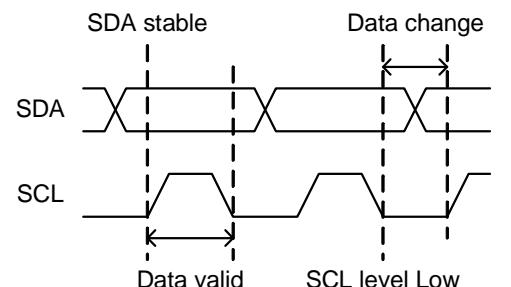
Function Description

Input Voltage and Power-On-Reset

The APL6012 can work normally and start monitoring the AINx voltage, when the supply voltage VDD is greater than the POR. The POR threshold is 2.5V typically when the VDD rising.
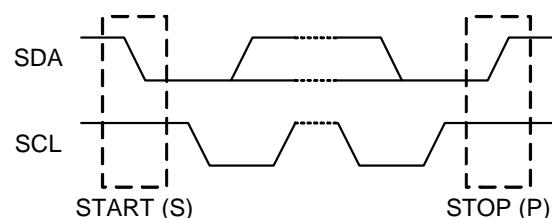
I²C Interface Data Validity

The SCL voltage level can only be changed to Low to High, when the SDA is stable unless the START and STOP status. The SDA can only be changed the voltage level when the SCL voltage is Low.
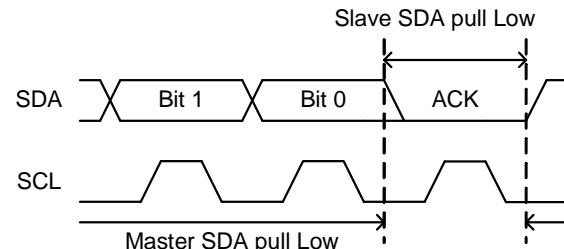
I²C Start and Stop Conditions

The START (S) condition is the SDA transient from High to Low, when SCL is High. The STOP (P) condition is the SDA transient from Low to High, when SCL is High. The STOP condition must send before each START condition.
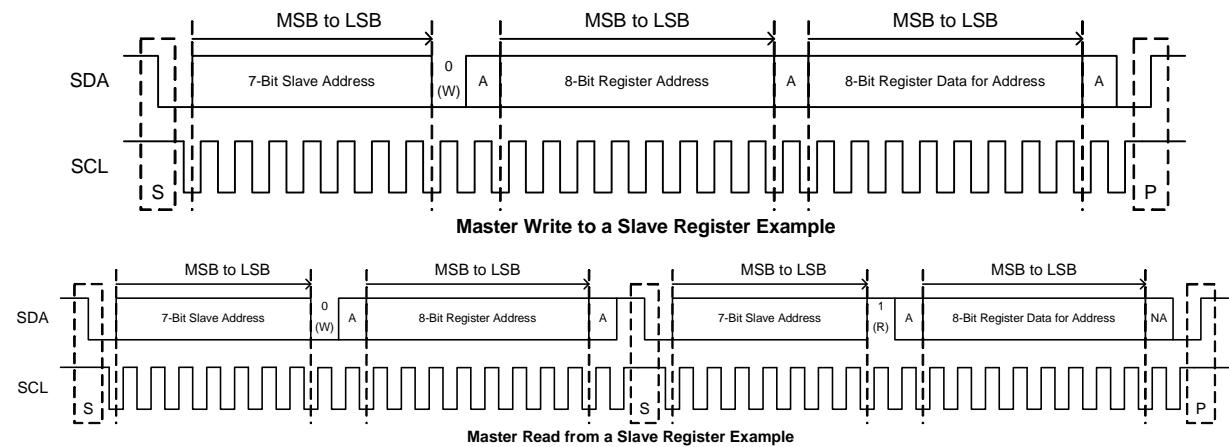
I²C Acknowledge

Each Address and Data are transmitted by using 8 clock pulses with 1 clock pulse Acknowledge (A). The Acknowledge is used for two purposes: one is the device that recognizes its own address. Another one is all of the master and slave to acknowledge receipt the register address or data. The SDA will pull Low to acknowledge.

Read and Write Protocol

Master Write to a Slave Register Example

Master Read from a Slave Register Example

(S=START, P=STOP, A=ACK from Slave, NA=Non-ACK)

Function Description (Cont.)

I²C Address Programming

The APL6012 I²C address is programmable, which can be selected from 0x70h to 0x7Eh by the 7-bit slave address with one R/W bit. The slave device compares the 7-bit slave address with its address and matches. The programmable address is selected by a voltage divider R1 and R2. The Alert/ADDR pin voltage is compared with 8 addresses available internal reference voltage for address programming.

Note: If the address programming function is not used, the Alert/ADDR pin must be connected to VDD via a resistor and the I²C address is used as default value 0x7Eh.

Voltage Monitoring and I²C Programming Interface

The AINx voltages are digitized directly by high precision A/D converter and interfaced to the I²C bus. The AINx voltages are sensed alternately and take 0.6ms every channel.

When the VDD supply voltage range from 2.8 to 5.5V, the A/D converter have 10mV of resolution, and 1 to 3.56V of full scale range. The A/D converter sensing results are stored in the internal register that shows as follow:

AIN1 A/D data store (TD1): Reg0x0F[7] (MSB) ~ Reg0x0F [0] (LSB)

AIN2 A/D data store (TD2): Reg0x10[7] (MSB) ~ Reg0x10 [0] (LSB)

....

AIN14 A/D data store (TD14): Reg0x1C[7] (MSB) ~ Reg0x1C[0] (LSB)

AIN15 A/D data store (TD15): Reg0x1D[7] (MSB) ~ Reg0x1D[0] (LSB)

Address	0x70	0x72	0x74	0x76	0x78	0x7A	0x7C	0x7E
R1 (kOhm)	6	5.1	4.3	3.9	3.6	2	1.5	10
R2 (kOhm)	2	2.7	3.6	4.7	6.8	6.2	8.2	Open
ALT/ADDR (% of VDD)	25	35	45	55	65	75	85	100

If the internal register code is read as $Code_x$ in integer decimal format, the AINx voltage transition to the internal register Reg0x03, Reg0x04 and Reg0x05 calculation as follows:

$$Code_x = \frac{V_{AINx} - 1V}{10mV} \quad \text{or} \quad V_{AINx} = (10mV \times Code_x) + 1V$$
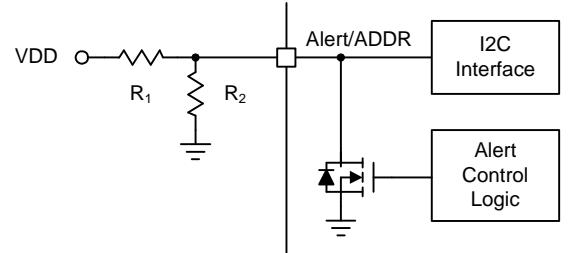
The voltage divider at VIN-R_{INx}-R_{NTCx}-GND sets the voltage AINx is calculated as:

$$V_{AINx} = VIN \times \frac{R_{NTCx}}{R_{INx} + R_{NTCx}}$$
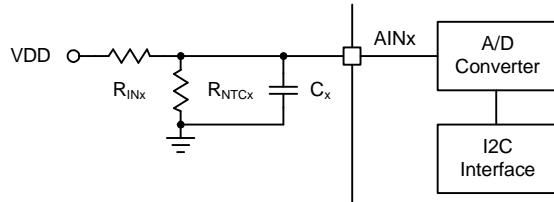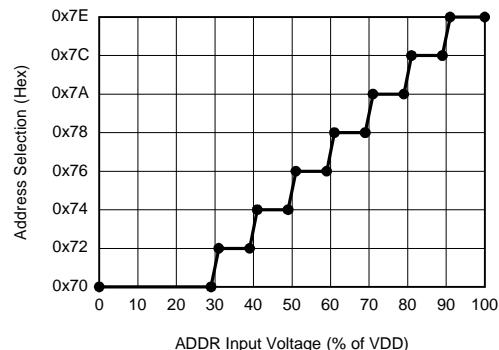
According to the above equation:

$$Code_x = \frac{\left(VIN \times \frac{R_{NTCx}}{R_{INx} + R_{NTCx}} \right) - 1V}{10mV}$$

Note: If the AINx pin is not used, that must be pulled to the high level. And the C_x is recommended to bypass the AINx pin.

Function Description (Cont.)

Alert Flag

The Alert Flag is used to indicate the system state.

When the setting condition is established at the AINx voltage, the APL6012 will make the internal MOS in the Alert pin turns on and pull low 50us every 2s cycle time.

Alert Threshold Level Setting

The Alert levels are set in the internal register by I2C interface shows as follows:

AIN1 Alert level set-up (TL1): Reg0x00[7] (MSB) ~ Reg0x00[0] (LSB)

AIN2 Alert level set-up (TL2): Reg0x01[7] (MSB) ~ Reg0x01[0] (LSB)

....

AIN14 Alert level set-up (TL14): Reg0x0D[7] (MSB) ~ Reg0x0D[0] (LSB)

AIN15 Alert level set-up (TL15): Reg0x0E[7] (MSB) ~ Reg0x0E[0] (LSB)

If one of conditions is established include TL1$\geq$TD1, TL2$\geq$TD2 ... TL14$\geq$TD14, TL15$\geq$TD15 the Alert function will be enabled, and the Alert Indication of internal resistor Reg0x1E[7:0] and Reg0x1F[6:0] will be set to 1 that shows as below:

If the Reg0x00 (TL1) $\geq$ Reg0x0F (TD1), than the bit Reg0x1E [0] = 1, else the bit Reg0x1E [0] = 0

If the Reg0x01 (TL2) $\geq$ Reg0x10 (TD2), than the bit Reg0x1E [1] = 1, else the bit Reg0x1E [1] = 0

....

If the Reg0x0D (TL14) $\geq$ Reg0x1C (TD14), than the bit Reg0x1F [5] = 1, else the bit Reg0x1F [5] = 0

If the Reg0x0E (TL15) $\geq$ Reg0x1D (TD15), than the bit Reg0x1F [6] = 1, else the bit Reg0x1F [6] = 0

Chip ID: Reg0xB2[7:0] = 0x1A

I²C Registers Summary
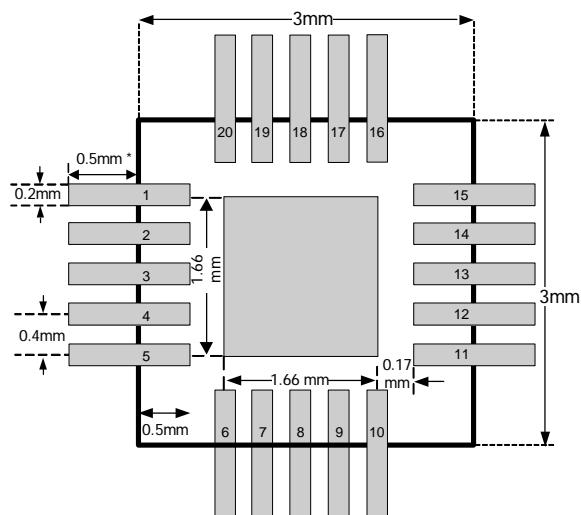
Register Address	Register Name	Bits								Read/ Write	Default Value
		D7	D6	D5	D4	D3	D2	D1	D0		
0x00	TL1	TL1[7:0]								R/W	00h
0x01	TL2	TL2[7:0]								R/W	00h
0x02	TL3	TL3[7:0]								R/W	00h
0x03	TD1	TD1[7:0]								R	00h
0x04	TD2	TD2[7:0]								R	00h
0x05	TD3	TD3[7:0]								R	00h
0x06	ALT	Reversed	AM3	AM2	AM1	Reversed				R	00h
0xB2	Chip ID	Chip ID = 0x1A								R	1Ah

Function Description (Cont.)

I²C Registers Summary

Register Address	Register Name	Bits								Read/ Write	Default Value
		D7	D6	D5	D4	D3	D2	D1	D0		
0x00	TL1	TL1[7:0]								R/W	8'h00
0x01	TL2	TL2[7:0]								R/W	8'h00
0x02	TL3	TL3[7:0]								R/W	8'h00
0x03	TL4	TL4[7:0]								R/W	8'h00
0x04	TL5	TL5[7:0]								R/W	8'h00
0x05	TL6	TL6[7:0]								R/W	8'h00
0x06	TL7	TL7[7:0]								R/W	8'h00
0x07	TL8	TL8[7:0]								R/W	8'h00
0x08	TL9	TL9[7:0]								R/W	8'h00
0x09	TL10	TL10[7:0]								R/W	8'h00
0x0A	TL11	TL11[7:0]								R/W	8'h00
0x0B	TL12	TL12[7:0]								R/W	8'h00
0x0C	TL13	TL13[7:0]								R/W	8'h00
0x0D	TL14	TL14[7:0]								R/W	8'h00
0x0E	TL15	TL15[7:0]								R/W	8'h00
0x0F	TD1	TD1[7:0]								R	8'h00
0x10	TD2	TD2[7:0]								R	8'h00
0x11	TD3	TD3[7:0]								R	8'h00
0x12	TD4	TD4[7:0]								R	8'h00
0x13	TD5	TD5[7:0]								R	8'h00
0x14	TD6	TD6[7:0]								R	8'h00
0x15	TD7	TD7[7:0]								R	8'h00
0x16	TD8	TD8[7:0]								R	8'h00
0x17	TD9	TD9[7:0]								R	8'h00
0x18	TD10	TD10[7:0]								R	8'h00
0x19	TD11	TD11[7:0]								R	8'h00
0x1A	TD12	TD12[7:0]								R	8'h00
0x1B	TD13	TD13[7:0]								R	8'h00
0x1C	TD14	TD14[7:0]								R	8'h00
0x1D	TD15	TD15[7:0]								R	8'h00
0x1E	ALT	ALT_AM8	ALT_AM7	ALT_AM6	ALT_AM5	ALT_AM4	ALT_AM3	ALT_AM2	ALT_AM1	R	8'h00
0x1F	ALT	Reserved	ALT_AM15	ALT_AM14	ALT_AM13	ALT_AM12	ALT_AM11	ALT_AM10	ALT_AM9	R	8'h00
0xB2	Chip ID	VENDOR_ID _ Chip ID = 0x1A								R	1Ah

Recommended Minimum Footprint

TQFN3x3-20

* Just Recommend

Manufature Information

APL6012 manufaturing information. Including wafer fab and assembly location.

ANPEC Device	Manufature	Assembly
APL6012	TSMC	GTK / ASE

ANPEC Electronic Corp.
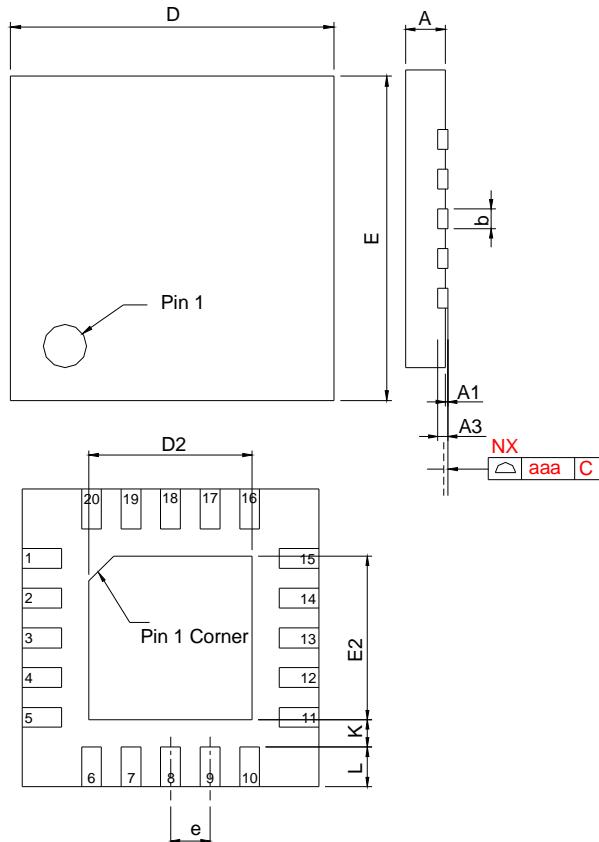
Account manager

Kevin Chang

APL6012

Package Information
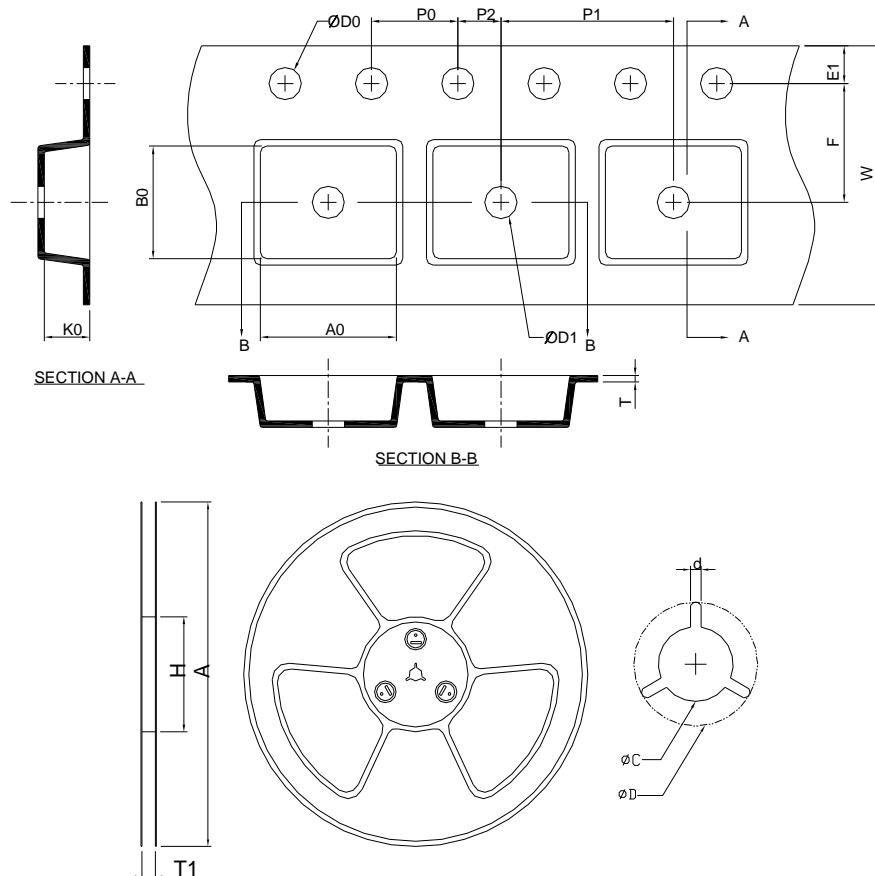
TQFN3x3-20P

SYMBOL	TQFN3x3-20			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.15	0.25	0.006	0.010
D	2.90	3.10	0.114	0.122
D2	1.50	1.80	0.059	0.071
E	2.90	3.10	0.114	0.122
E2	1.50	1.80	0.059	0.071
e	0.40 BSC		0.016 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	
aaa	0.08		0.003	

Note : 1. Followed from JEDEC MO-220 WEEE

Carrier Tape & Reel Dimensions

Application	A	H	T1	C	d	D	W	E1	F
	330±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
TQFN 3x3	**P0**	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30±0.20	3.30±0.20	1.00±0.20
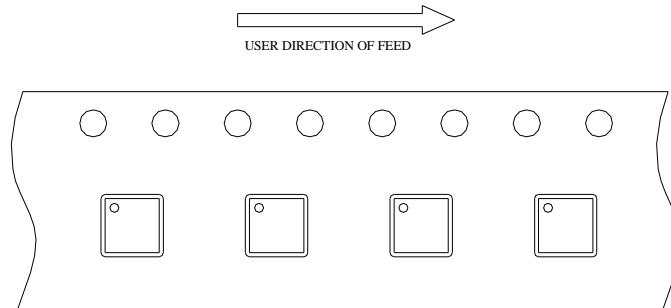
(mm)

Devices Per Unit
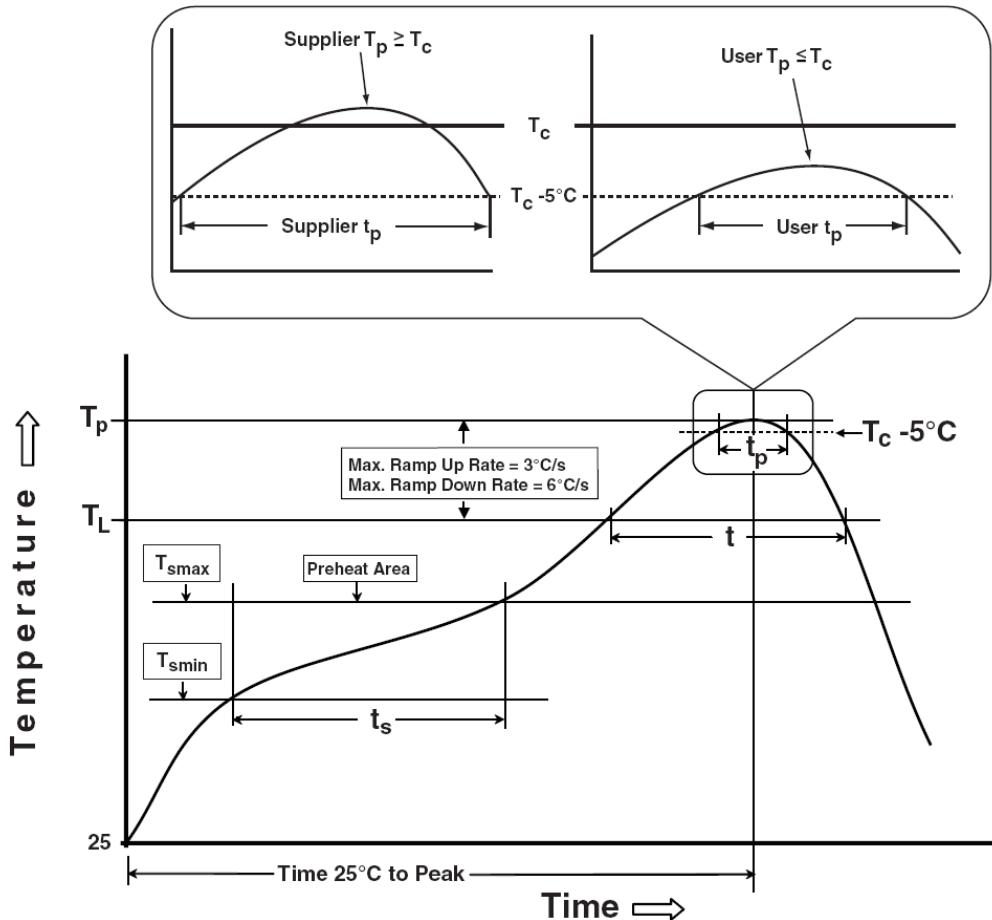
Package Type	Unit	Quantity
TQFN3x3-20	Tape & Reel	3000

Taping Direction Information

TQFN3x3-20P

USER DIRECTION OF FEED

Classification Profile

Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Classification Reflow Profiles (Cont.)

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 $\geq$350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ Tj=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM$\geq$2KV
MM	JESD-22, A115	VMM$\geq$200V
Latch-Up	JESD 78	10ms, $1_{tr}\geq$100mA

Customer Service

Anpec Electronics Corp.
Head Office :
    No.6, Dusing 1st Road, SBIP,
    Hsin-Chu, Taiwan, R.O.C.
    Tel : 886-3-5642000
    Fax : 886-3-5642050

Taipei Branch :
    2F, No. 11, Lane 218, Sec 2 Jhongsing Rd.,
    Sindian City, Taipei County 23146, Taiwan
    Tel : 886-2-2910-3838
    Fax : 886-2-2917-3838