8 + 1 Phase Output Controller with SVID Interface for Notebook and Ultrabook CPU Applications

Product Preview

NCP81229

The NCP81229 is a dual rail, eight + one phase buck solution optimized for Intel IMVP8 CPUs. The multi−phase rail control system is based on Dual−Edge pulse−width modulation (PWM) combined with DCR current sensing. This provides an ultra−fast initial response to dynamic load events and reduced system cost. The NCP81229 has an ultra−low offset current monitor amplifier with programmable offset compensation for high accuracy current monitoring.

Features

- Vin Range 4.5 V to 21 V
- Startup into Pre−Charged Loads While Avoiding False OVP
- Digital Soft Start Ramp
- Adjustable Vboot
- High Impedance Differential Output Voltage Amplifier
- Dynamic Reference Injection
- Programmable Output Voltage Slew Rates
- Dynamic VID Feed−Forward
- Differential Current Sense Amplifiers for Each Phase
- Programmable Adaptive Voltage Positioning (AVP)
- Adjustable Switching Frequency Range
- Digitally Stabilized Switching Frequency
- UltraSonic Operation
- PSYS Input Monitor (SVID address 0D)
- Meets Intel's IMVP8 Specifications
- Current Mode Dual Edge Modulation for Fast Initial Response to Transient Loading
- This is a Pb−Free Device

Typical Applications

- Notebook and Ultrabook Computers

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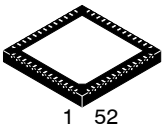


QFN52 6x6, 0.4P
CASE 485BE

MARKING DIAGRAM

A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCP81229MNTXG	QFN52 (Pb−Free)	TBD / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

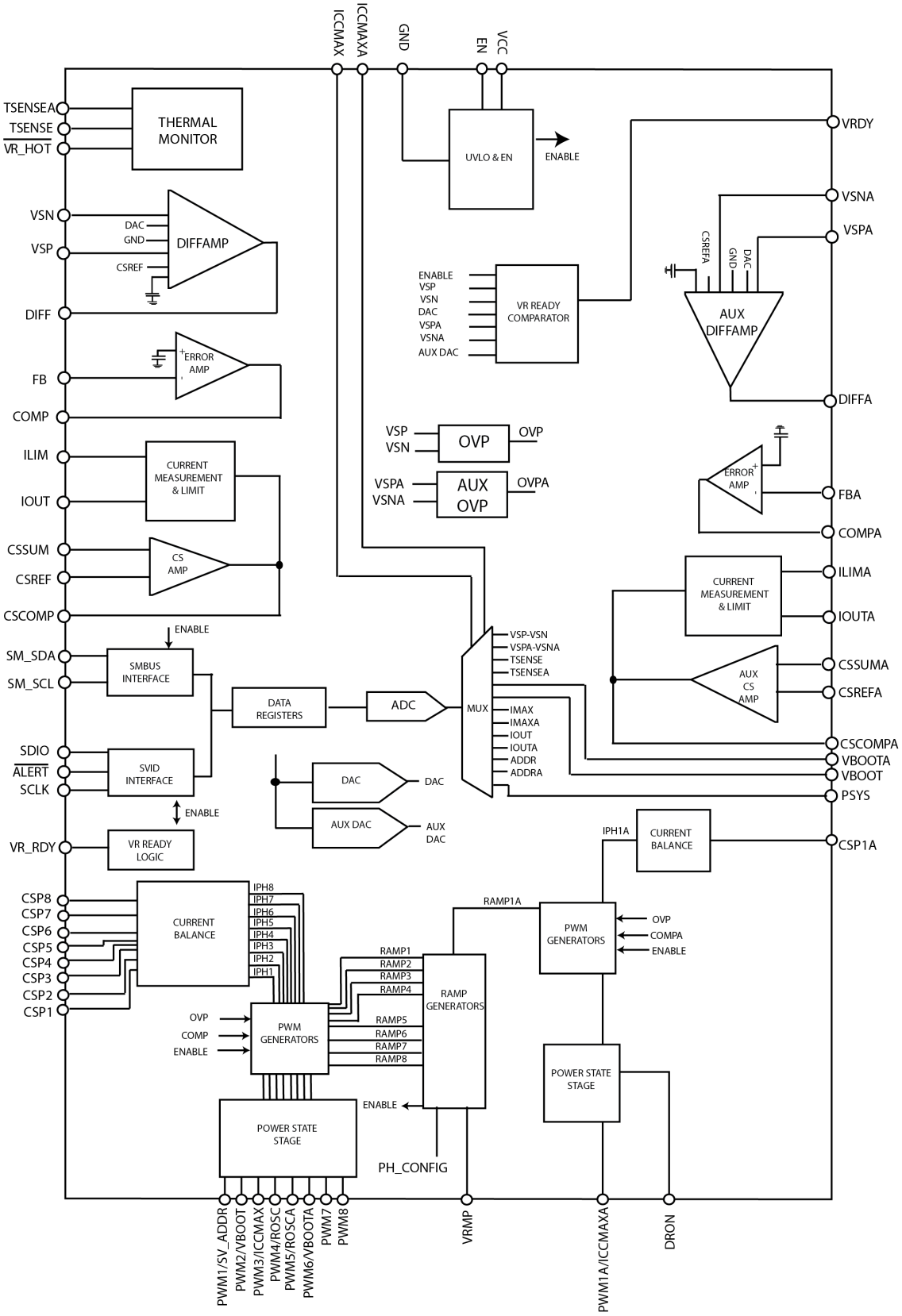


Figure 1. Internal Block Diagram

APPLICATIONS INFORMATION

Figure 2. Typical Applications Circuit (TBC)

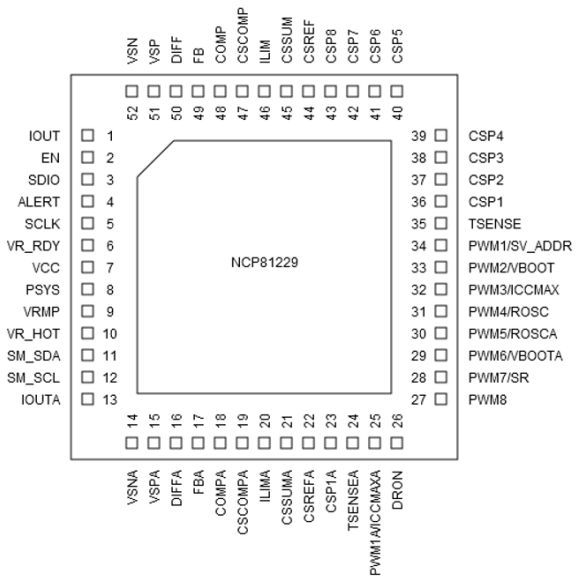


Figure 3. Pinout

Table 1. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	IOUT	Total output current monitor for eight−phase regulator
2	EN	Enable. High enables both rails
3	SDIO	Serial VID data interface
4	ALERT#	Serial VID ALERT#
5	SCLK	Serial VID clock
6	VR_RDY	VR_RDY indicates both rails are ready to accept SVID commands
7	VCC	Power for the internal control circuits. A decoupling capacitor is connected from this pin to ground
8	PSYS	System power signal input. A resistor to ground scales this signal
9	VRMP	Feed−forward input of Vin for the ramp−slope compensation. The current fed into this pin is used to control the ramp of the PWM slopes
10	VRHOT#	OD output. Indicates high VR temperature
11	SM_SDA	SMBUS serial data interface
12	SM_SCL	SMBUS clock
13	IOUTA	Total output current monitor for single−phase regulator
14	VSNA	Differential output voltage positive sense for single−phase rail
15	VSPA	Differential output voltage negative sense for single−phase rail
16	DIFFA	Output of the single−phase regulator's differential remote sense amplifier
17	FBA	Error amplifier voltage feedback for single−phase regulator
18	COMPA	Output of the error amplifier and the inverting inputs of the PWM comparators for single−phase regulator
19	CSCOMPA	Output of total−current−sense amplifier for single−phase regulator
20	ILIMA	Over−current threshold setting − programmed with a resistor to CSCOMPA for single−phase regulator
21	CSSUMA	Inverting input of total−current−sense amplifier for single−phase regulator
22	CSREFA	Total−current−sense amplifier reference voltage input for single−phase regulator
23	CSP1A	Non−inverting input to current−balance amplifier for Phase 1 of single−phase regulator.
24	TSENSEA	Temperature sense input for single−phase regulator
25	PWM1A / ICCMAXA	PWM1 output for single−phase regulator. During startup, ICCMAX for single−phase regulator is programmed with a pull−down resistor
26	DRON	External FET driver enable for discrete driver or ON Semiconductor DrMOS

Table 1. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
27	PWM8	PWM8 output for eight−phase regulator
28	PWM7 / SR	PWM7 output for eight−phase regulator / Pulldown resistor on this pin programs SR value for both main and GT rails
29	PWM6 / VBootA	PWM6 output for eight−phase regulator / Pin−program for single−phase VbootA. Can be overridden if SMBus transaction occurs between UVLO and EN.
30	PWM5 / ROSCA	PWM5 output for eight−phase regulator / Pulldown on this pin programs RoscA value for GT rail
31	PWM4 / ROSC	PWM4 output for eight−phase regulator / Pulldown on this pin programs Rosc value for main rail
32	PWM3 / ICCMAX	PWM3 output for eight−phase regulator / Pulldown on this pin programs ICCMAX for eight−phase rail during startup
33	PWM2 / VBOOT	PWM2 output for eight−phase regulator / Pin−program for eight−phase Vboot. Can be overridden if SMBus transaction occurs between UVLO and EN.
34	PWM1 / SV_ADDR	PWM1 output for eight−phase regulator / Pulldown on this pin configures SVID address
35	TSENSE	Temperature sense input for eight−phase regulator
36	CSP1	Differential current sense positive for Phase 1 of eight−phase rail
37	CSP2	Differential current sense positive for Phase 2 of eight−phase rail
38	CSP3	Differential current sense positive for Phase 3 of eight−phase rail
39	CSP4	Differential current sense positive for Phase 4 of eight−phase rail
40	CSP5	Differential current sense positive for Phase 5 of eight−phase rail
41	CSP6	Differential current sense positive for Phase 6 of eight−phase rail
42	CSP7	Differential current sense positive for Phase 7 of eight−phase rail
43	CSP8	Differential current sense positive for Phase 8 of eight−phase rail
44	CSREF	Total−current−sense amplifier reference voltage input for eight−phase rail
45	CSSUM	Inverting input of total−current−sense amplifier for eight−phase rail
46	ILIM	Over−current threshold setting − programmed with a resistor to CSCOMP for eight−phase rail
47	CSCOMP	Output of total−current−sense amplifier for eight−phase rail
48	COMP	Output of the error amplifier and the inverting inputs of the PWM comparators for eight−phase rail
49	FB	Error amplifier voltage feedback for eight−phase rail
50	DIFF	Output of the eight−phase regulator's differential remote sense amplifier
51	VSP	Differential output voltage sense positive for eight−phase rail
52	VSN	Differential output voltage sense negative for eight−phase rail
	Flag	GND

Table 2. MAXIMUM RATINGS (All signals referenced to GND unless noted otherwise.)

Pin Symbol	VMAX	VMIN	ISOURCE	ISINK
COMP_MPH	VCC + 0.3 V	−0.3 V	2 mA	2 mA
CSCOMP _MPH	VCC + 0.3 V	−0.3 V	2 mA	2 mA
PWMX	VCC + 0.3 V	−0.3 V		1 mA
VSN_MPH	GND + 0.3 V	GND − 0.3 V	1 mA	2 mA
DIFFOUT_MPH	VCC + 0.3 V	−0.3 V	2 mA	2 mA
VR_RDY	VCC + 0.3 V	−0.3 V	2 mA	
VCC	6.5 V	−0.3 V		
VRMP	25 V	−0.3 V		
All Other Pins	VCC + 0.3 V	−0.3 V		

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. THERMAL CHARACTERISTICS

Description	Symbol	Typ	Unit
Thermal Characteristic QFN Package (Note 1)	R_{JA}	68	°C/W
Operating Junction Temperature Range (Note 2)	T_J	−10 to 125	°C
Operating Ambient Temperature Range		−10 to 100	°C
Maximum Storage Temperature Range	T_{STG}	− 40 to +150	°C
Moisture Sensitivity Level QFN Package	MSL	1	

1. JESD 51−5 (1S2P Direct−Attach Method) with 0 LFM
2. JESD 51−7 (1S2P Direct−Attach Method) with 0 LFM

Table 4. ELECTRICAL CHARACTERISTICS

Unless otherwise stated:−10° < T_A < 100°C; 4.75 V < V_{CC} < 5.25 V; C_{VCC} = 0.1 μF

Parameter	Test Condition	Min	Typ	Max	Unit
BIAS SUPPLY					
VCC Voltage Range		4.75		5.25	V
Quiescent Current (PS0, 1)	PS0,1			60	mA
	PS2			60	mA
	PS3			27	mA
	PS4			300	μA
	Enable low		5		mA
UVLO Threshold	VCC rising			4.5	V
	VCC falling	4			V
VRMP					
Supply Range		4.5		20	
UVLO Threshold	VRMP Rising			4.25	V
	VRMP Falling	3			V
UVLO Hysteresis			800		mV
ENABLE INPUT					
Upper Threshold	Activation Level	0.8			V
Lower Threshold	Deactivation Level			0.3	V
PHASE DETECTION					
CSP pin pulldown current	Pulldown applied only prior to soft start		5		μA
CSP Pin Threshold Voltage		VCC − 0.4			V
Phase Detect Timer			100		μs
IMVP8 DAC (Prot 05h)					
System Voltage Accuracy	0.75 V ≤ DAC < 1.52 V	−0.5		0.5	%
	0.5V< DAC < 0.745 V	−8		8	mV
	0.25V < DAC < 0.495 V	−10		10	mV
DAC SLEW RATE					
Soft Start Slew Rate			1/2 fast		mV/μs
Slew Rate Slow			1/2 fast		mV/μs
Slew Rate Fast			>10		mV/us
VOFS Slew Rate			1/2 fast		mV/us
DRON					
Output High Voltage	Sourcing 500 μA	3			V
Output Low Voltage	Sinking 500 μA			0.1	V

Table 4. ELECTRICAL CHARACTERISTICS

Unless otherwise stated:−10° < T_A < 100°C; 4.75 V < V_{CC} < 5.25 V; C_{VCC} = 0.1 μF

Parameter	Test Condition	Min	Typ	Max	Unit
TSense					
Bias Current		115.5	120	124.5	μA
Alert# Assert Threshold			488		mV
Alert# De−Assert Threshold			510		mV
VR_Hot Assert Threshold			468		mV
VR_Hot De−Assert Threshold			488		mV
VR_RDY OUTPUT					
Output Low Saturation Voltage	I_{VR_RDY} = −4 mA		0.3		V
OVP and UVP					
Absolute Over Voltage Threshold	During Soft Start − CSREF Rising		2.5		V
Over Voltage Threshold Above DAC	VSP−VSN−VID Rising	350	400	475	mV
Over Voltage Delay	VSP−VSN Rising to PWM Low		50		ns
Under Voltage Threshold Below DAC	VSP−VSN−VID Falling	370		425	mV
Under Voltage Delay			5		μs
PWM OUTPUT					
Output High Voltage	Sourcing 500 μA	Vcc − 0.2			V
Output Mid Voltage	No Load, Power State 2	1.7	1.8	1.9	V
Output Low Voltage	Sinking 500 μA			0.7	V
DIFFERENTIAL SUMMING AMPLIFIER					
Input Bias Current		−400		400	nA
−3 dB Bandwidth	C_L = 20 pF, R_L = 10 kΩ		12		MHz
Closed Loop DC Gain	VSP − VSN = −0.3 V to 1.3 V		1		V/V
CURRENT SUMMING AMPLIFIER					
Input Bias Current	CSSUM = CSREF = 1.0 V	−14		14	μA
Offset Voltage (Vos) Note 3		−300		300	μV
Open Loop Gain			80		dB
Open Loop Unity Gain Bandwidth	C_L = 20 pF, R_L = 10 kΩ		10		MHz
CURRENT BALANCE AMPLIFIERS					
Differential Mode Input Voltage Range	CSREF = 1.2 V	−30		30	mV
−3 dB Bandwidth	Guaranteed by Simulation		8		MHz
OVER−CURRENT PROTECTION					
ILIM Threshold Current (delayed OCP shutdown, ICL)	PS0	9	10	11	μA
	PS1, PS2, PS3		10/N*		μA
ILIM Threshold Current (immediate OCP shutdown, ICLM)	PS0	11	13	15.5	μA
	PS1, PS2, PS3		13/N*		μA
Shutdown Delay	Immediate		300		ns
	Delayed		20		μs
ILIM Output Voltage Offset	ILIM to CSREF	−4		4	mV
IOUT OUTPUT					
Current Gain	IOUT/ILIM, (RLIM = 20 kΩ, RIOUT = 5 kΩ) DAC = 0.8 V, 1.25 V, 1.5 V	9.5	10	10.5	A/A
MODULATORS					
PWM Ramp Duty Cycle Matching	Comp = 2 V, PWM Ton Matching		±1		%

*N is the phase configuration number in PS0.

Table 4. ELECTRICAL CHARACTERISTICS

Unless otherwise stated:−10° < T_A < 100°C; 4.75 V < V_{CC} < 5.25 V; C_{VCC} = 0.1 μF

Parameter	Test Condition	Min	Typ	Max	Unit
PSYS					
Full Scale Input Voltage			2.5		V
Disable Threshold			VCC−0.2		V
I²C					
V_{IH} (SM_SDA, SM_SCL)	Logic High Input Voltage	2.1			V
V_{IL}	Logic Low Input Voltage			0.8	V
Hysteresis			80		mV
V_{OL} (SM_SDA)	SM_SDA Output Low Voltage, ISDA = −6 mA			0.4	V
I_{IH}; I_{IL}	Input Current	−1		1	μA
C_{SM_SDA, SM_SCL}	Input Capacitance		5		pF
f_{SM_SCL}	Clock Frequency			1	MHz
SM_SCL Falling Edge to SM_SDA Valid Time				1	μs
SCLK, SDIO					
VIL				0.45	V
VIH		0.65			V
VOL				0.3	V
Output Leakage Current when High		−0.5		0.5	μA
ALERT#					
VOL				0.3	V
Output Leakage Current when High		−0.1		0.1	μA
OSCILLATOR					
Minimum Switching Frequency			180		kHz
Maximum Switching Frequency			1170		kHz
Switching Frequency Accuracy	180 kHz < F_{SW} < 1170 kHz	−10		10	%

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Timing Diagrams

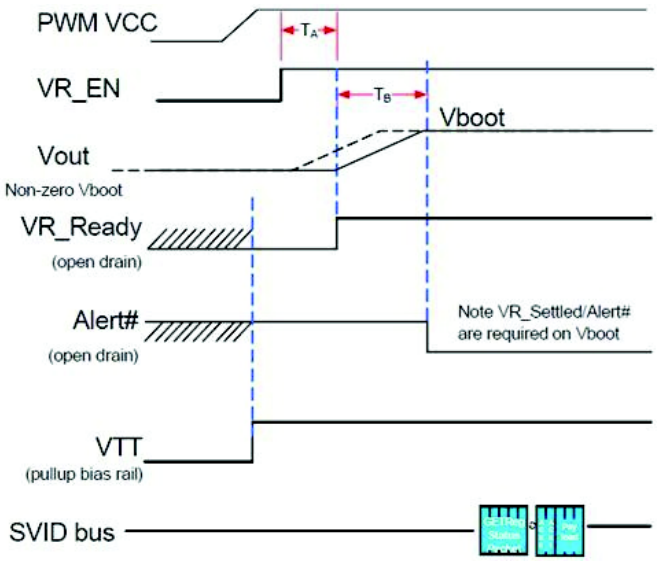


Figure 4. Start−up Timing Diagram − Non−zero VBOOT

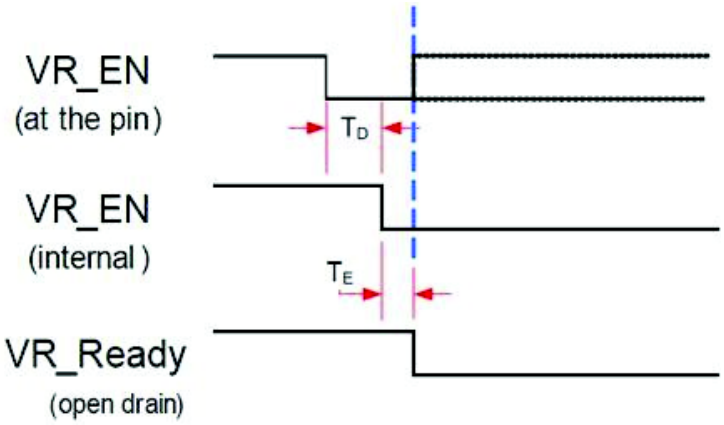


Figure 5. Shut−down Timing Diagram

Table 5.

Description		Min	Typ	Max
TA	VR_EN to VR_Ready. Controller ready accept SVID command			2.5 ms
TB	Non−zero VBOOT ramp time. May start during TA but not later than at the end of TA − to Alert# assertion.			VID/Slow
TD	External de−assertion of VR_EN to the internal recognition of VR_EN de−assertion (glitch filter)	0 μs		1 μs
TE	VR_EN internal de−assertion to VR_Ready de−assertion			500 ns

Table 6. SMBus START−UP TIMING

Parameter[1]	Tmin	Tmax	Unit	Description
f_{SCLK}		400	kHz	Clock Frequency
t_{LOW}	1.3		μs	Clock low period, between 10% points.
t_{HIGH}	0.6		μs	Clock high period, between 90% points.
t_R		300	ns	Clock/data rise time.
t_F		300	ns	Clock/data fall time.
$t_{SU;STA}$	600		ns	Start condition setup time.
$t_{HD;STA}$[2]	600	600	ns	Start condition hold time.
$t_{SU;DAT}$[3]	100	100	ns	Data setup time.
$t_{SU;STO}$[4]	600	600	ns	Stop condition setup time.
t_{BUF}	1.3		μs	Bus free time between stop and start conditions.

3. Guaranteed by design, but not production tested.
4. Time from 10% of SDATA to 90% of SCLK
5. Time for 10% or 90% of SDATA to 10% of SCLK
6. Time for 90% of SCLK to 10% of SDATA

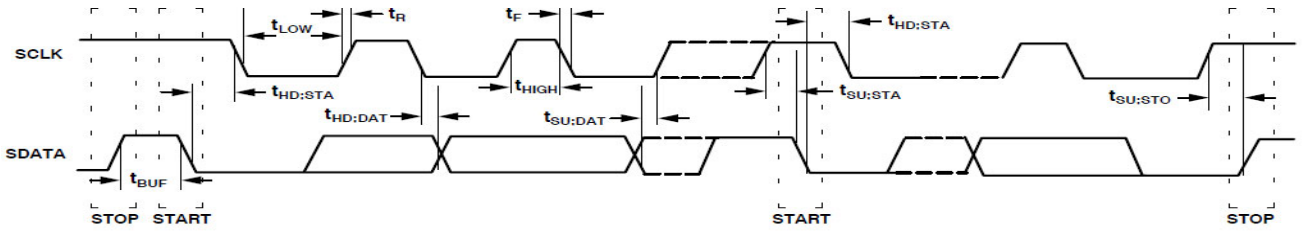


Figure 6. SMBus Timing Diagram

Start Up

Following the rise of VCC above the UVLO threshold, externally programmed configuration data is collected, and all PWM outputs are set to Mid−level to prepare the gate drivers of the power stages for activation. When the controller is enabled, DRON is asserted (high) to activate the external gate drivers. A digital counter steps the DAC up from zero to the target boot voltage based on the Soft Start Slew Rate in the spec table. As the DAC ramps, the PWM outputs of each rail will change from Mid−level to high when the first PWM pulse for that rail is produced. When the controller is disabled, the PWM signals return to Mid−level. Note the operation of the VR_RDY pin is dependent on the VBOOT status for device. If there is a non−zero VBOOT programmed using the configuration pins then the VR_RDY is asserted at the end of the VBOOT ramp, however if there is a zero VBOOT programmed the VR_RDY signal is asserted when the controller is ready to accept the first SVID command.

DEVICE CONFIGURATION

Phase and Rail Configuration

During start−up, the number of operational phases of the multiphase rail is determined by the internal circuitry monitoring the CSP inputs. If a reduced phase count is required the appropriate CSP pins externally pulled to VCC with a resistor during startup. Also, whether or not the PSYS function is active and responds to an address call on the SVID bus is determined by the internal circuitry monitoring the PSYS input. Tying the PSYS input to VCC will cause the PSYS rail to not respond to any calls to address 0Dh on the SVID bus.

NCP81229 Configurations

The NCP81229 has four Configuration features. On power up a 10 μA current is sourced from these pins (pins TBD) through a resistor connected to this pin and the resulting voltage is measured. The following features will be programmed:

- SVID address
- Slew Rate
  - Programs the slew rate of VBOOT on power up (Table 9).
- Switching Frequency
  - The Fsw values are shown in Table 7.
- Vboot
  - Vboot options are shown in Table 8.

Switching Frequency

Switching frequencies between 180 kHz and 1.17 MHz are programmed at startup with pulldown resistors on Rosc pin (please see pinout for pin number).

Table 7. SWITCHING FREQUENCY

Resistor (kΩ)	Switching Frequency (kHz)
10	180 (Default)
15	225
21	270
26.7	315
33.2	360
41.2	405
49.9	450
60.4	495
71.5	540
84.5	630
97.6	720
115	810
133	900
154	990
178	1080
210	1170

Table 8. VBOOT/VBOOTA

Resistor (kΩ)	VBOOT(V)
10	0
30	0.8
60	1.05
100	1.2
160	1.4
220	1.5

Table 9. SLEW RATE CORE/GT

Resistor (kΩ)	Slew Rate of VCore and GT (mV/us)
10	10
30	30

Table 10. SVID ADDRESS

Resistor (kΩ)	“Main” SVID Address	“A” Address
10	0 (Core)	1 (GT)
25	1 (GT)	0 (Core)
45	0 (Core)	2 (SA)
70	1 (GT)	3 (GTUS)
95	0 (Core)	1 (GT)
125	1 (GT)	0 (Core)
165	0 (Core)	2 (SA)
220	1 (GT)	3 (GTUS)

ICCMAX

The SVID interface provides the platform ICCMAX value at register 21h. A resistor to ground on the ICCMAX pin programs these registers at the time the part is enabled. 10 μA is sourced from these pins to generate a voltage on the program resistor. The value of the register is 1A per LSB and is set by the equation below. The resistor value should be no less than 10k.

$$ICC\_MAX_{21h} = \frac{R \times 10\ \mu A \times 255\ A}{2.5\ V}$$

Ultrasonic Mode

The switching frequency of a rail in DCM will decrease at very light loads. Ultrasonic Mode forces the switching frequency to stay above the audible range.

CCM/DCM Operation

In PS2 and PS3, all rails will operate in either Continuous Conduction Mode (CCM) or Discontinuous Conduction Mode (DCM) depending on load current in order to prevent loss of efficiency from negative inductor current.

Table 11. POWER STATES

SVID Power State	Typical Operating Mode
PS0	Multiphase rail dual edge
PS1	One−phase CCM RPM
PS2	One−phase DCM RPM
PS3	One−phase DCM RPM
PS4	Standby

IVID and Phase Shedding

In PS0, the each rail of the NCP81229 can change its operating mode based on output current and/or programmed VID. As the IMVP8 SVID IVID registers only define a maximum current associated with specific VIDs, each rail can make phase−shed decisions based on the IOUT level in addition to the programmed VID. If IOUT is less than IVID2−I for longer than 2 ms, the multiphase rail will shed the phase and operate in single−phase mode, even if VID is greater than IVID2−VID. The second phase can also be turned off without the 2 ms delay if programmed VID is less than IVID2−VID, and IOUT is verified to be less than IVID2−I.

Also while in PS0, the operating mode can drop to single−phase DCM operation if programmed VID is less than IVID3−VID. Each rail will not drop into DCM mode based on IOUT alone.

The controller exits Efficiency Optimized Modes and turns on all phases when any SetVID command is issued, if a transient load is detected, or if output loading crosses the IVID2−I threshold.

If a SetPS command is received, the controller will place itself in the lowest appropriate state. For example, if in PS0 the controller has automatically transitioned into DCM RPM and receives a SetPS = 1 command, the PS register will be updated, but the controller will remain in DCM RPM mode. If while in PS1 the current increases or a transient is detected, the controller will move into CCM mode.

See IMVP8 specification for more details on IVID.

PSYS

The PSYS pin is an analog input to the VR controller. It is a system input power monitor that facilitates the monitoring of the total platform system power. The system power is sensed at the platform charging device, the VR controller facilitates reporting back current and through the SVID interface at address 0Dh.

THEORY OF OPERATION

Input Voltage Feed−Forward (VRMP pin)

Ramp generator circuits are provided for the dual−edge modulator. The ramp generators implement input voltage feed−forward control by varying the ramp slopes proportional to the VRMP pin voltage. The VRMP pin also has a UVLO function, which is active only after the controller is enabled. The VRMP pin is high impedance input when the controller is disabled. For multi−phase operation, the dual−edge PWM ramp amplitude is changed according to the following:

$$VRMP\_pp = 0.1 * Vvrmp$$

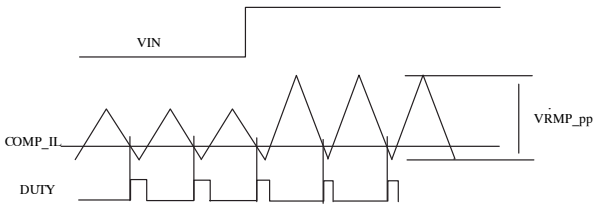


Figure 7. Ramp Feed−Forward

Differential Current Feedback Amplifiers

Each phase of the rail has a low offset, differential amplifier to sense the current of that phase in order to balance current. The CSREF and CSPx pins are high impedance inputs, but it is recommended that any external filter resistor RCSN does not exceed 10 k to avoid offset due to leakage current. It is also recommended that the voltage sense element be no less than 0.5 mΩ for best current balance.

The external filter RCSN and CCSN time constant should match the inductor L/DCR time constant, but fine tuning of this time constant is generally not required. Phase current signals are summed with the COMP or ramp signals at their respective PWM comparator inputs in order to balance phase currents via a current mode control approach.

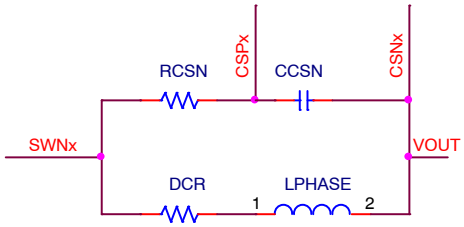


Figure 8. Per Phase Current Sense Network

$$R_{CSN} = \frac{L_{PHASE}}{C_{CSN} \times DCR}$$

Total Current Sense Amplifier

The multiphase rail uses a patented approach to sum the phase currents into a single, temperature compensated, total current signal. This signal is then used to generate the output voltage droop, total current limit, and the output current monitoring functions. The Rref(n) resistors average the voltages at the output terminals of the inductors to create a low impedance reference voltage at CSREF. The Rph resistors sum currents from the switch nodes to the virtual CSREF potential created at the CSSUM pin by the amplifier. The total current signal is the difference between the CSCOMP and CSREF voltages.

The amplifier filters, and amplifies, the voltage across the inductors in order to extract only the voltage across the inductor series resistances (DCR). An NTC thermistor (Rth) in the feedback network placed near the Phase 1 inductor senses the inductor temperature, and compensates both the DC gain and the filter time constant for the change in DCR with temperature. The thermistor location is chosen so that the temperature of the Phase 1 inductor providing the current in PS1 power mode can be determined.

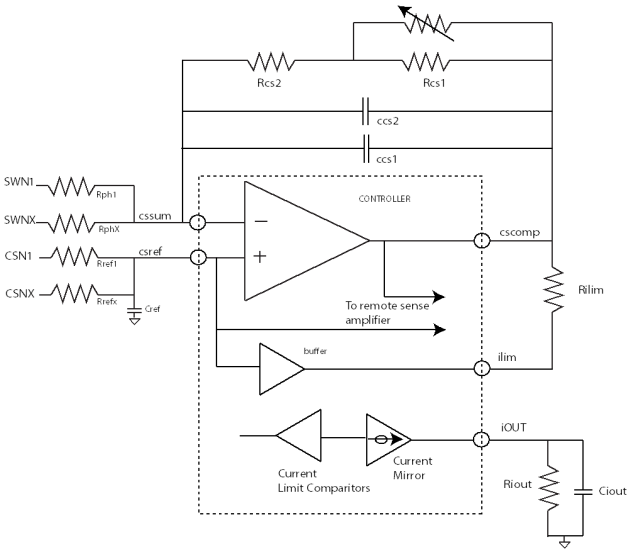


Figure 9. Total Current Sense Amplifier

The DC gain equation for the DC total current signal is:

$$V_{CSCOMP-CSREF} = -\frac{Rcs2 + \frac{Rcs1 * Rth}{Rcs1 + Rth}}{Rph} * (Iout_{Total} * DCR)$$

Set the DC gain by adjusting the value of the Rph resistors in order to make the ratio of total current signal to output current equal the desired loadline. The values of Rcs1 and Rcs2 are set based on the effect of temperature on both the thermistor and inductor, and may need to be adjusted to eliminate output voltage temperature drift with the final product enclosure and cooling.

The pole frequency of the CSCOMP filter should be set equal to the zero of the output inductor. This causes the total current signal to contain only the component of inductor voltage caused by the DCR voltage, and therefore to be proportional to inductor current. Connecting Ccs2 in parallel with Ccs1 allows fine tuning of the pole frequency using commonly available capacitor values. It is best to perform fine tuning during transient testing.

$$Fz = -\frac{(DCR\,@\,25°C)}{(2 * \pi * Lphase)}$$

$$Fp = \frac{1}{(2\pi * (Rcs2 + (\frac{Rcs1 * RTH}{Rcs1 + RTH})) * (CCs1 + CCs2))}$$

The value of the CREF capacitor (in nF) on the CSREF pin should be:

$$Ccref = \frac{(0.02 * RTH)}{Rref}$$

Rail Remote Sense Amplifier

A high performance high input impedance true differential amplifier is provided to accurately sense regulator output voltage. The VSP and VSN inputs should be connected to the regulator's output voltage sense points. The remote sense amplifier takes the difference of the output voltage with the DAC voltage and adds the droop voltage.

$$V_{DIFOUT} = (V_{VSP} - V_{VSN}) + (1.3V - V_{DAC}) + (V_{DROOP} - V_{CSREF})$$

This signal then goes through a standard error compensation network and into the inverting input of the error amplifier. Droop = DCR * (R_{CS} / Rph)

High Performance Voltage Error Amplifier

The Remote Sense Amplifier output feeds a Type III compensation network formed by the Error Amplifier and external tuning components. The non−inverting input of the error amplifier is connected to the same reference voltage used to bias the Remote Sense Amplifier output.

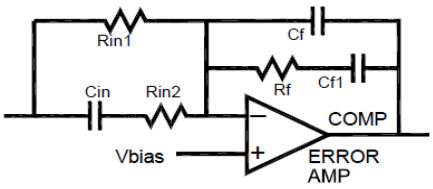


Figure 10. Error Amplifier

Loadline Programming (DROOP)

An output loadline is a power supply characteristic wherein the regulated (DC) output voltage decreases proportional to load current. This characteristic can reduce the output capacitance required to maintain output voltage within limits during load transients faster than those to which the regulation loop can respond.

A load line is produced by adding a signal proportional to output load current (VDROOP) to the output voltage feedback signal – thereby satisfying the voltage regulator at an output voltage reduced proportional to load current. The load line is programmed by setting the gain of the Total Current Sense Amplifier such that the total current signal is equal to the desired output voltage droop.

Programming the Current Limit

The current limit thresholds are programmed with a resistor between the ILIM and CSCOMP pins. The multiphase rails generates a replica of the CSREF pin voltage at the ILIM pin, and compares ILIM pin current to ICL0 and ICLM0 (ICL1 and ICLM1 in PS1, PS2 and PS3). The controller latches off if ILIM pin current exceeds ICL0 (ICL1 for PS1, PS2, and PS3) for t_OCPDLY, and latches off immediately if ILIM pin current exceeds ICLM0 (ICLM1 for PS1, PS2 and PS3). Set the value of the current

limit resistor RLIMIT according to the desired current limit Iout LIMIT.

$$R_{LIMIT} = \frac{Rcs2 + \frac{Rcs1 * Rth}{Rcs1 + Rth} * (Iout_{LIMIT} * DCR)}{Rph} \over 10\ \mu\ * K$$

where K can be set by 0x19[7:4] for main rail, and set by 0x37[7:4] for aux rail.

Programming IOUT

The IOUT pin sources a current proportional to the ILIM current. The voltage on the IOUT pin is monitored by the internal A/D converter and should be scaled with an external resistor to ground such that a load equal to ICCMAX generates a 2.5 V signal on IOUT. A pull−up resistor from 5 V VCC can be used to offset the IOUT signal positive if desired.

$$R_{IOUT} = \frac{2.5\ V \times R_{LIMIT}}{10 \times \frac{R_{CS2} + \frac{R_{CS1} \times R_{th}}{R_{CS1} + R_{th}}}{R_{ph}} \times (ICC\_MAX \times DCR)}$$

Programming DAC Feed−Forward Filter

The multiphase rail outputs a pulse of current from the VSN pin upon each increment of the internal DAC following a DVID UP command. A parallel RC network inserted into the path from VSN to the output voltage return sense point, VSS_SENSE, causes these current pulses to temporarily decrease the voltage between VSP and VSN. This causes the output voltage during DVID to be regulated slightly higher, in order to compensate for the response of the Droop function to current flowing into the charging output capacitors. In the following equations, Cout is the total output capacitance of the system.

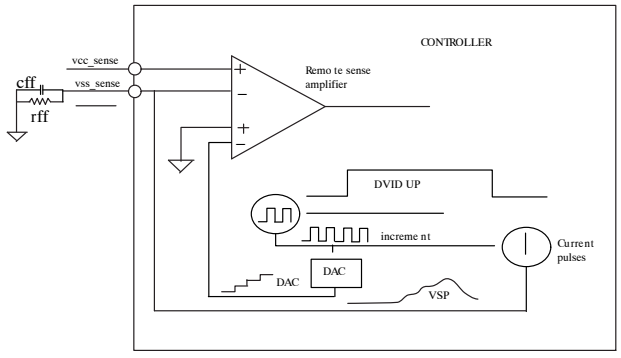


Figure 11. DAC Feed−Forward

$$Rff = Cout * LL * 453.6 \cdot 10^{6}$$

$$Cff = \frac{LL * Cout}{Rff}$$

Tsense Network

A temperature sense inputs is provided for the multiphase rail. A precision current is sourced out the output of the TSENSE pin to generate a voltage on the temperature sense networks. The voltages on the temperature sense inputs are sampled by the internal A/D converter. A 100k NTC similar to the Murata NCP15WF104E03RC should be used. Rcomp1 in the following Figure is optional, and can be used to slightly change the hysteresis. See the specification table for the thermal sensing voltage thresholds and source current.

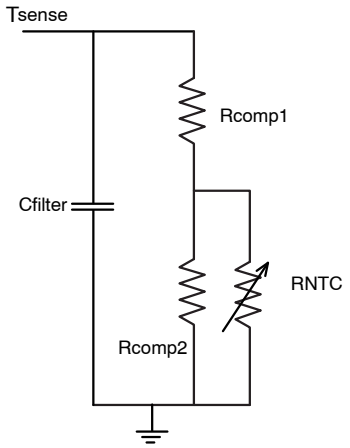


Figure 12. TSense Network

PWM Comparators

The noninverting input of each comparator (one for each phase) is connected to the summation of the error amplifier output (COMP) and each phase current (IL*DCR*Phase Balance Gain Factor). The inverting input is connected to the triangle ramp voltage of that phase. The output of the comparator generates the PWM output. During steady state PS0 operation, the main rail PWM pulses are centered on the valley of the triangle ramp waveforms and both edges of the PWM signals are modulated. During a transient event, the duty cycle can increase rapidly as the error amp signal increases with respect to the ramps, to provide a highly linear and proportional response to the step load.

Output Voltage Offset (VOFS)

According to Intel definition, output voltage offset can be implemented through SVID. SMBus also provides flexibility to change VOFS. There are four possibilities to change output voltage offset. For the default setting, VOFS is controlled by SVID. It can also be controlled by SMBus register and ignored SVID setting. When phase shedding feature enable, VOFS can also be adjusted depend on output load.

Table 12. Output Voltage Offset (VOFS) of IA rail

VOFS of IA rail		0x1D[4] OFS Control	
		0 (Follow SVID)	1 (Ignore SVID)
0x1E[5] SMBus VOFS	0 (Disable)	SVID 0x33	SMBus 0x27
	1 (Enable)	SVID 0x33 + SMBus 0x07~0x0A (Depend on phase shedding setting)	SMBus 0x27 + SMBus 0x07~0x0A (Depend on phase shedding setting)

Table 13. PHASE CONFIGURATION

Phase Configuration	Programming Pin in CSPx	Unused Pin
8+1	All CSP pins are connected normally	No unused Pin
7+1	CSP1 to CSP7 and CSP1A pins connected normally. CSP8 connected to VCC through a 2K resistor.	Float PWM8
6+1	CSP1 to CSP6 and CSP1A pins connected normally. CSP7 and CSP8 connected to VCC through a 2K resistor.	Float PWM8 Use PWM7 for programming SR only.
5+1	CSP1 to CSP5 and CSP1A pins connected normally. CSP6, CSP7, and CSP8 connected to VCC through a 2K resistor.	Float PWM8 Use PWM7 for programming SR only, and PWM6 for programming VBOOTA only.
4+1	CSP1 to CSP4 and CSP1A pins connected normally. CSP5, CSP6, CSP7, andCSP8 connected to VCC through a 2K resistor.	Float PWM8 Use PWM7 for programming SR only, PWM6 for programming VBOOTA only, PWM5 for ROSCA only.

FAULT PROTECTION

Over Current Protection (OCP)

A programmable total phase current limit is provided that is decreased when not operating in PS0 mode. This limit is programmed with a resistor between the CSCOMP and ILIM pins. The current from the ILIM pin to this resistor is compared to the ILIM Threshold Currents (ICL0, ICLM0, ICL1, and ICLM1). When the 2−phase rail is operating in PS0, if the ILIM pin current exceeds ICL0, an internal latch−off timer starts.

If the fault is not removed, the controller shuts down when the timer expires. If the current into the pin exceeds ICLM0, the controller shuts down immediately. When operating in PS1, PS2, or PS3, the ILIM pin current limits are ICL1 and ICLM1. To recover from an OCP fault, the EN pin or VCC voltage must be cycled low.

Input Under−voltage Lockouts (UVLO)

The VR monitors the 5 V VCC supply as well as the VRMP pin voltage. Hysteresis is incorporated within these monitors.

Output Under Voltage Monitor

The multiphase phase rail output voltage is monitored for under voltage at the output of the differential amplifier. If the multiphase−phase rail output falls more than VUVM2 below the DAC−DROOP voltage, the UVM comparator will trip – sending the VR_RDY signal low.

Output Over Voltage Protection

The multiphase phase output voltage is monitored for OVP at the output of the differential amplifier and also at the CSREF pin. During normal operation, if an output voltage exceeds the DAC voltage by VOVP, the VR_RDY flag goes low, and the DAC voltage of the overvoltage rail will be slowly ramped down to 0 V to avoid producing a negative output voltage. At the same time, the PWM outputs of the overvoltage rail are sent low. The PWM output will pulse to mid−level during the DAC ramp down period if the output decreases below the DAC + OVP Threshold as DAC decreases. When the DAC gets to zero, the PWMs will be held low, and the VR will stay in this mode until the VCC voltage or EN is toggled.

Absolute OVP

During start up, the OVP threshold is set to the Absolute Over Voltage Threshold. This allows the controller to start up without false triggering OVP.

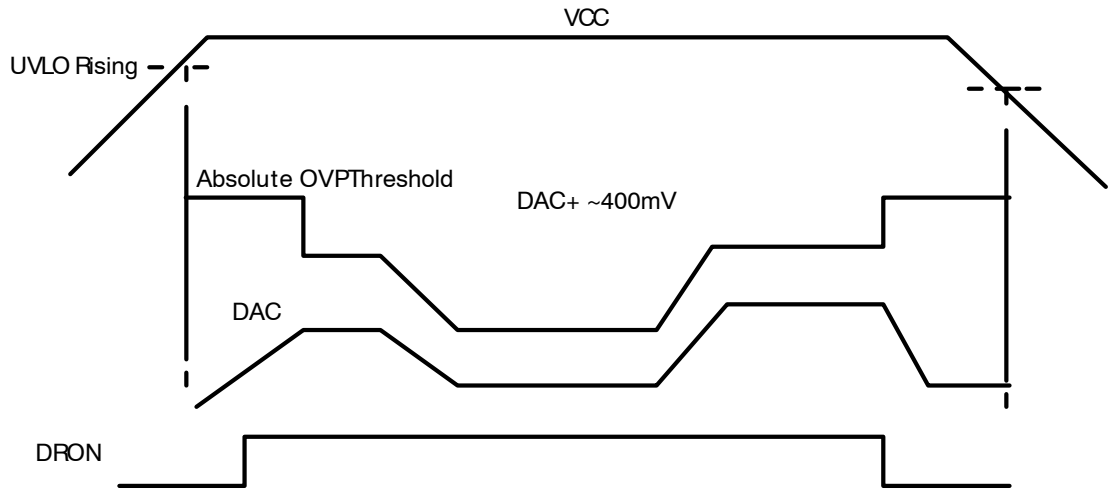


Figure 13. OVP Threshold Behavior

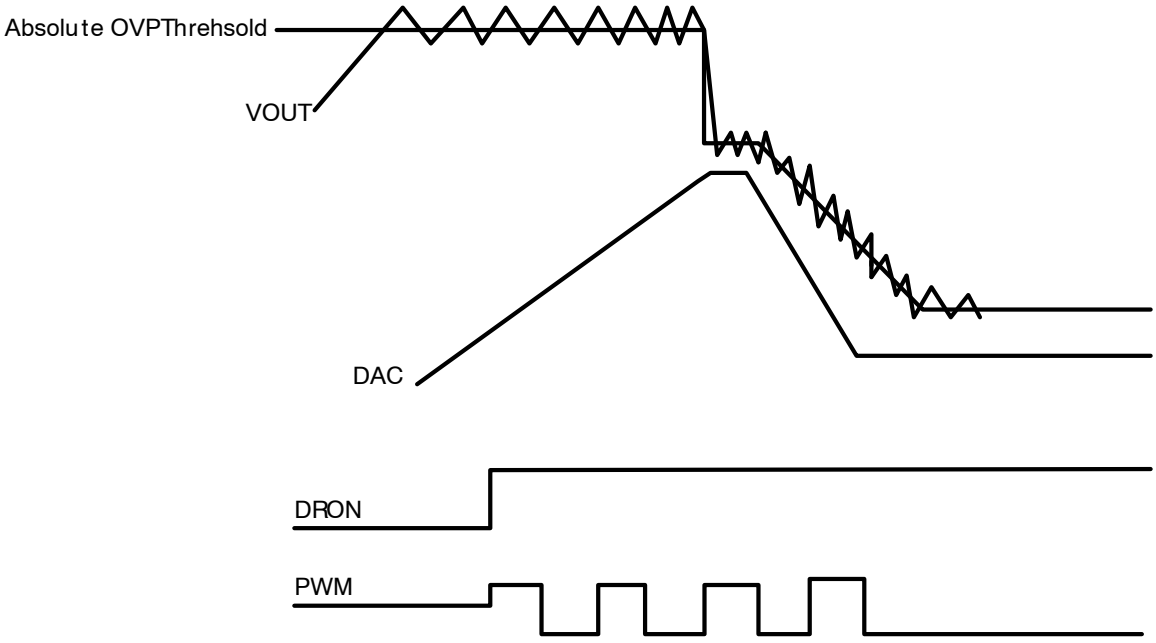


Figure 14. OVP Behavior at Start−up

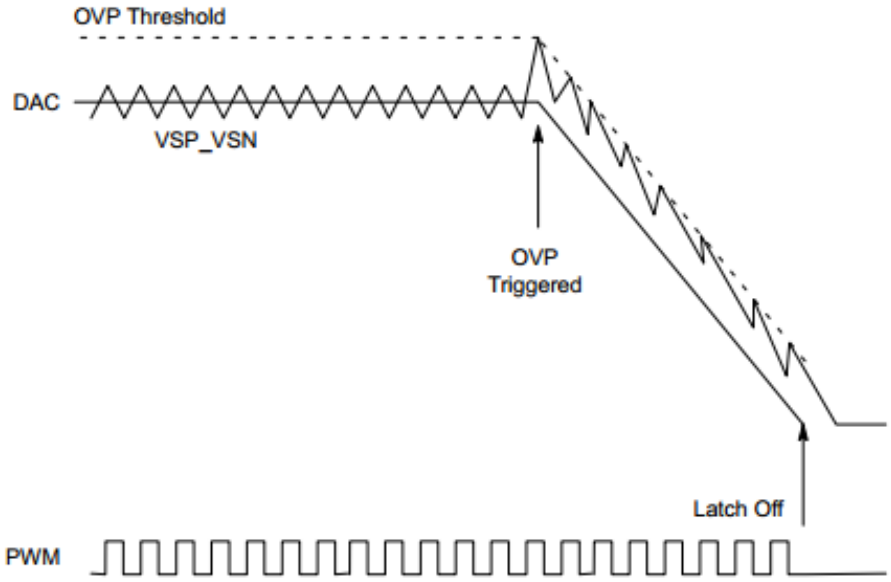


Figure 15. OVP during Normal Operation Mode

Serial VID Interface (SVID)

The Serial VID Interface (SVID Interface) is a 3 wire digital interface used to transfer power management information between the CPU (Master) and the VR controller (Slave). The 3 wires are clock (SCLK), data (SDIO) and ALERT#. The SCLK is unidirectional and generated by the master. The SDIO is bi−directional, used for transferring data from the microprocessor to the VR controller and from the VR controller to the CPU. The ALERT# is an open drain output from the VR controller to signal to the master that the Status Register should be read.

Refer to the relevant Intel document for SVID routing and pull−up topologies.

The SVID bus will operate at a max frequency of 43 MHz.

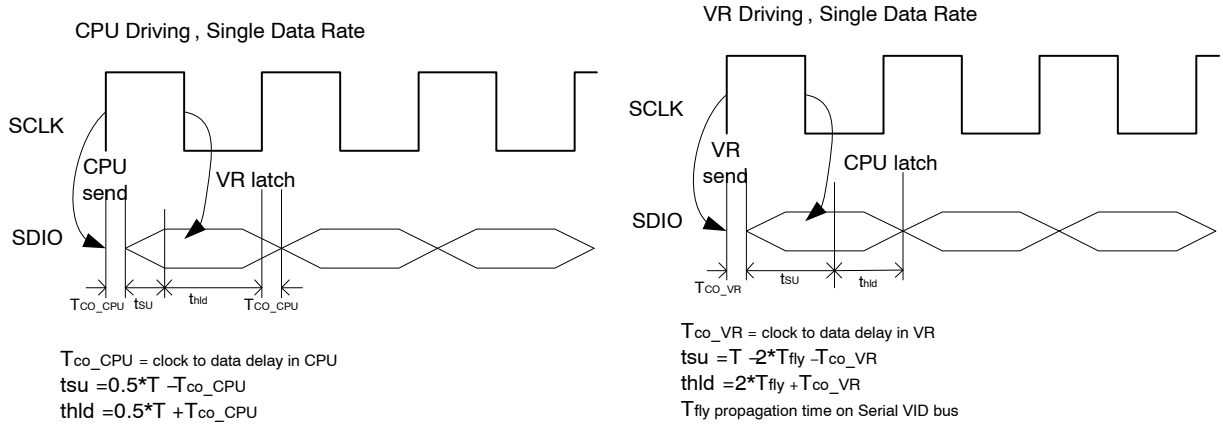


Figure 16. SVID Timing Diagram

Table 14. SLEW RATE

Option	SVID Command Code	Feature Description	Register Address (Indicating the slew rate of VID code change)
SetVID_Fast	01h	10 mV/μs or 30 mV/μs VID code change slew rate	24h
SetVID_Slow	02h	=1/2 of SetVID_Fast VID code change slew rate	25h
SetVID_Decay	03h	No control, VID code down	N/A

SMBus (I^2C) Address

In addition to the SVID interface between the CPU and VR, the NCP81229 also supports communication via I^2C over the SMBus. The I^2C interface consists of SM_SDA and SM_SCL. Communication over SMBus can occur once Vcc is ready (even prior to enabling the NCP81229), however, you should wait a min of 5 ms after Vcc is ready before communicating. The slave address for the SMBus in is fixed at 0x20.

Table 15. SVID REGISTER MAP

Index	Name	Description	Access	Default 00h	PSYS 0Dh
00h	Vendor ID	Uniquely identifies the VR vendor. The vendor ID assigned by Intel to ON Semiconductor is 0x1Ah	R	1Ah	1Ah
01h	Product ID	Uniquely identifies the VR product. The VR vendor assigns this number.	R	29h	29h
02h	Product Revision	Uniquely identifies the revision or stepping of the VR control IC. The VR vendor assigns this data.	R	00h	0x00
05h	Protocol ID	Identifies the SVID Protocol the controller supports	R	05h	05h
06h	Capability	Informs the Master of the controller's Capabilities, 1 = supported, 0 = not supported	R	D7h	N/A
		Bit 7 = Iout_format. Bit 7 = 0 when 1A = 1LSB of Reg 15h. Bit 7 = 1 when Reg 15 FFh = Icc_Max. Default = 1			
		Bit 6 = ADC Measurement of Temp Supported = 1			
		Bit 5 = ADC Measurement of Pin Supported = 0			
		Bit 4 = ADC Measurement of Vin Supported = 1			
		Bit 3 = ADC Measurement of Iin Supported = 0			
		Bit 2 = ADC Measurement of Pout Supported = 1			
		Bit 1 = ADC Measurement of Vout Supported = 1			
		Bit 0 = ADC Measurement of Iout Supported = 1			
10h	Status_1	Data register read after the ALERT# signal is asserted. Conveying the status of the VR.	R	00h	00h
11h	Status_2	Data register showing optional status_2 data.	R	00h	00h
12h	Temp zone	Data register showing temperature zones the system is operating in	R	00h	N/A
15h	I_out	8 bit binary word ADC of current. This register reads 0xFF when the output current is at Icc_Max	R	01h	N/A
16h	V_out	8 bit binary word ADC of output voltage, measured between VSP and VSN. LSB size is 8 mV	R	01h	N/A
17h	VR_Temp	8 bit binary word ADC of voltage. Binary format in deg C, IE 100C=64h. A value of 00h indicates this function is not supported. To get accurate temperature, specific Tsense network is required. Place one NTC and one normal resister in parallel. NTC uses 100 kΩ under 25°C and B25/50 approximates 4250. Use 20 kΩ for parallel resister.	R	00h	N/A
18h	P_out	8 bit binary word representative of output power. The output voltage is multiplied by the output current value and the result is stored in this register. A value of 00h indicates this function is not supported	R	01h	N/A
1Ah	V_in	8 bit binary word ADC of voltage. Input voltage is (1Ah−2)/7, unit is Volt. Full scale voltage is approximate 36V.	R	00h	N/A
1Bh	Input Power	Required for Input Power Domain Address 0Dh	R	N/A	00h
1Ch	Status2_last read	When the status 2 register is read its contents are copied into this register. The format is the same as the Status 2 Register.	R	00h	
21h	Icc_Max	Data register containing the Icc_Max the platform supports. The value is measured on the ICCMAX pin on power up and placed in this register. From that point on the register is read only.	R	00h	N/A
22h	Temp_Max	Data register containing the max temperature the platform supports and the level VR_HOT# asserts. This value defaults to 100°C and programmable over the SVID Interface	R/W	6Ah	N/A

Table 15. SVID REGISTER MAP (continued)

Index	Name	Description	Access	Default 00h	PSYS 0Dh
24h	SR_fast	Slew Rate for SetVID_fast commands. Binary format in mV/us.	R	10mV/us or 30mV/us	N/A
25h	SR_slow	Slew Rate for SetVID_slow commands. It is 16, 8, 4 or 2 times slower than the SR_fast rate. Binary format in mV/us. FAST/2 is default for IMVP8	R	1/2 fast	N/A
26h	VBOOT	The VBOOT is resistor programmed at startup. The controller will ramp to VBOOT and hold at VBOOT until it receives a new SVID SetVID command to move to a different voltage.	R	xxh	N/A
2Ah	SR_Slow selector	Fast_SR/2	R/W	01h	N/A
		Fast_SR/4			
		Fast_SR/8			
		Fast_SR/16			
2Bh	PS4 exit latency	Reflects the latency of exiting PS4 state. The exit latency is defined as the time duration, in μs, from the ACK of the SETVID Slow/Fast command to the output voltage beginning to ramp	R	8Ch	N/A
2Ch	PS3 exit latency	Reflects the latency of exiting PS3 state. The exit latency is defined as the time duration, in μs, from the ACK of the SETVID/SetPS command until the controller is capable of supplying max current of the command PS state.	R	55h	N/A
2Dh	EN to Ready for SVID command (TA)	Reflects the latency from enable assertion to the VR controller being ready to accept SVID commands.	R	CAh	N/A
2Eh	PIN Max	Input Power max for input power sensor			
2Fh	Pin _Alert _Th	Input Power Alert Threshold			
30h	Vout_Max	Programmed by master and sets the maximum VID the VR will support. If a higher VID code is received, the VR should respond with “not supported” acknowledge. IMVP8 VID format.	RW	FBh	N/A
31h	VID setting	Data register containing currently programmed VID voltage. VID data format.	RW	xxh	N/A
32h	Pwr State	Register containing the current programmed power state.	RW	00h	N/A
33h	Offset	Sets offset in VID steps added to the VID setting for voltage margining. Bit 7 is sign bit, 0=positive margin, 1= negative margin. Remaining 7 BITS are # VID steps for margin 2s complement.	RW	00h	N/A
		00h= no margin			
		01h= +1 VID step			
		02h= +2 VID steps			
		FFh= −1 VID step			
		FEh= −2 VID steps.			
34h	Multi VR config	Bit mapped data register that configures multiple VRs behavior on the same bus and can be programmed to reset behavior of VR_Ready under 0.0 V VID command.	RW	00h	
35h	Set Reg Addrs	Write address pointer for main addr space	RW	35h	N/A
42h	IVID1_VID	VID for max current from IVID1_I	RW	00h	N/A
43h	IVID1_I	Max current for IVID1_VID ≥ VID setting ≥ IVID2_VID	RW	00h	N/A
44h	IVID2_VID	VID for max current from IVID2_I	RW	00h	N/A
45h	IVID2_I	Max current for IVID2_VID ≥ VID setting ≥ IVID3_VID	RW	00h	N/A
46h	IVID3_VID	VID for max current from IVID3_I	RW	00h	N/A
47h	IVID3_I	Max current for IVID3_VID ≥ VID setting	RW	00h	N/A

Table 16. IMVP8 VID TABLE

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
0	0	0	0	0	0	0	0	0	00
0	0	0	0	0	0	0	1	0.25	01
0	0	0	0	0	0	1	0	0.255	02
0	0	0	0	0	0	1	1	0.26	03
0	0	0	0	0	1	0	0	0.265	04
0	0	0	0	0	1	0	1	0.27	05
0	0	0	0	0	1	1	0	0.275	06
0	0	0	0	0	1	1	1	0.28	07
0	0	0	0	1	0	0	0	0.285	08
0	0	0	0	1	0	0	1	0.29	09
0	0	0	0	1	0	1	0	0.295	0A
0	0	0	0	1	0	1	1	0.3	0B
0	0	0	0	1	1	0	0	0.305	0C
0	0	0	0	1	1	0	1	0.31	0D
0	0	0	0	1	1	1	0	0.315	0E
0	0	0	0	1	1	1	1	0.32	0F
0	0	0	1	0	0	0	0	0.325	10
0	0	0	1	0	0	0	1	0.33	11
0	0	0	1	0	0	1	0	0.335	12
0	0	0	1	0	0	1	1	0.34	13
0	0	0	1	0	1	0	0	0.345	14
0	0	0	1	0	1	0	1	0.35	15
0	0	0	1	0	1	1	0	0.355	16
0	0	0	1	0	1	1	1	0.36	17
0	0	0	1	1	0	0	0	0.365	18
0	0	0	1	1	0	0	1	0.37	19
0	0	0	1	1	0	1	0	0.375	1A
0	0	0	1	1	0	1	1	0.38	1B
0	0	0	1	1	1	0	0	0.385	1C
0	0	0	1	1	1	0	1	0.39	1D
0	0	0	1	1	1	1	0	0.395	1E
0	0	0	1	1	1	1	1	0.4	1F
0	0	1	0	0	0	0	0	0.405	20
0	0	1	0	0	0	0	1	0.41	21
0	0	1	0	0	0	1	0	0.415	22
0	0	1	0	0	0	1	1	0.42	23
0	0	1	0	0	1	0	0	0.425	24
0	0	1	0	0	1	0	1	0.43	25
0	0	1	0	0	1	1	0	0.435	26
0	0	1	0	0	1	1	0	0.435	26
0	0	1	0	0	1	1	1	0.44	27
0	0	1	0	1	0	0	0	0.445	28
0	0	1	0	1	0	0	1	0.45	29
0	0	1	0	1	0	1	0	0.455	2A
0	0	1	0	1	0	1	1	0.46	2B

Table 16. IMVP8 VID TABLE (continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
0	0	1	0	1	1	0	0	0.465	2C
0	0	1	0	1	1	0	1	0.47	2D
0	0	1	0	1	1	1	0	0.475	2E
0	0	1	0	1	1	1	1	0.48	2F
0	0	1	1	0	0	0	0	0.485	30
0	0	1	1	0	0	0	1	0.49	31
0	0	1	1	0	0	1	0	0.495	32
0	0	1	1	0	0	1	1	0.5	33
0	0	1	1	0	1	0	0	0.505	34
0	0	1	1	0	1	0	1	0.51	35
0	0	1	1	0	1	1	0	0.515	36
0	0	1	1	0	1	1	1	0.52	37
0	0	1	1	1	0	0	0	0.525	38
0	0	1	1	1	0	0	1	0.53	39
0	0	1	1	1	0	1	0	0.535	3A
0	0	1	1	1	0	1	1	0.54	3B
0	0	1	1	1	1	0	0	0.545	3C
0	0	1	1	1	1	0	1	0.55	3D
0	0	1	1	1	1	1	0	0.555	3E
0	0	1	1	1	1	1	1	0.56	3F
0	1	0	0	0	0	0	0	0.565	40
0	1	0	0	0	0	0	1	0.57	41
0	1	0	0	0	0	1	0	0.575	42
0	1	0	0	0	0	1	1	0.58	43
0	1	0	0	0	1	0	0	0.585	44
0	1	0	0	0	1	0	1	0.59	45
0	1	0	0	0	1	1	0	0.595	46
0	1	0	0	0	1	1	1	0.6	47
0	1	0	0	1	0	0	0	0.605	48
0	1	0	0	1	0	0	1	0.61	49
0	1	0	0	1	0	1	0	0.615	4A
0	1	0	0	1	0	1	1	0.62	4B
0	1	0	0	1	1	0	0	0.625	4C
0	1	0	0	1	1	0	1	0.63	4D
0	1	0	0	1	1	1	0	0.635	4E
0	1	0	0	1	1	1	1	0.64	4F
0	1	0	1	0	0	0	0	0.645	50
0	1	0	1	0	0	0	1	0.65	51
0	1	0	1	0	0	1	0	0.655	52
0	1	0	1	0	0	1	1	0.66	53
0	1	0	1	0	1	0	0	0.665	54
0	1	0	1	0	1	0	1	0.67	55
0	1	0	1	0	1	1	0	0.675	56
0	1	0	1	0	1	1	1	0.68	57
0	1	0	1	1	0	0	0	0.685	58

Table 16. IMVP8 VID TABLE (continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
0	1	0	1	1	0	0	1	0.69	59
0	1	0	1	1	0	1	0	0.695	5A
0	1	0	1	1	0	1	1	0.7	5B
0	1	0	1	1	1	0	0	0.705	5C
0	1	0	1	1	1	0	1	0.71	5D
0	1	0	1	1	1	1	0	0.715	5E
0	1	0	1	1	1	1	1	0.72	5F
0	1	1	0	0	0	0	0	0.725	60
0	1	1	0	0	0	0	1	0.73	61
0	1	1	0	0	0	1	0	0.735	62
0	1	1	0	0	0	1	1	0.74	63
0	1	1	0	0	1	0	0	0.745	64
0	1	1	0	0	1	0	1	0.75	65
0	1	1	0	0	1	1	0	0.755	66
0	1	1	0	0	1	1	1	0.76	67
0	1	1	0	1	0	0	0	0.765	68
0	1	1	0	1	0	0	1	0.77	69
0	1	1	0	1	0	1	0	0.775	6A
0	1	1	0	1	0	1	1	0.78	6B
0	1	1	0	1	1	0	0	0.785	6C
0	1	1	0	1	1	0	1	0.79	6D
0	1	1	0	1	1	1	0	0.795	6E
0	1	1	0	1	1	1	1	0.8	6F
0	1	1	1	0	0	0	0	0.805	70
0	1	1	1	0	0	0	1	0.81	71
0	1	1	1	0	0	1	0	0.815	72
0	1	1	1	0	0	1	1	0.82	73
0	1	1	1	0	1	0	0	0.825	74
0	1	1	1	0	1	0	1	0.83	75
0	1	1	1	0	1	1	0	0.835	76
0	1	1	1	0	1	1	1	0.84	77
0	1	1	1	1	0	0	0	0.845	78
0	1	1	1	1	0	0	1	0.85	79
0	1	1	1	1	0	1	0	0.855	7A
0	1	1	1	1	0	1	1	0.86	7B
0	1	1	1	1	1	0	0	0.865	7C
0	1	1	1	1	1	0	1	0.87	7D
0	1	1	1	1	1	1	0	0.875	7E
0	1	1	1	1	1	1	1	0.88	7F
1	0	0	0	0	0	0	0	0.885	80
1	0	0	0	0	0	0	1	0.89	81
1	0	0	0	0	0	1	0	0.895	82
1	0	0	0	0	0	1	1	0.9	83
1	0	0	0	0	1	0	0	0.905	84
1	0	0	0	0	1	0	1	0.91	85

Table 16. IMVP8 VID TABLE (continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
1	0	0	0	0	1	1	0	0.915	86
1	0	0	0	0	1	1	1	0.92	87
1	0	0	0	1	0	0	0	0.925	88
1	0	0	0	1	0	0	1	0.93	89
1	0	0	0	1	0	1	0	0.935	8A
1	0	0	0	1	0	1	1	0.94	8B
1	0	0	0	1	1	0	0	0.945	8C
1	0	0	0	1	1	0	1	0.95	8D
1	0	0	0	1	1	1	0	0.955	8E
1	0	0	0	1	1	1	1	0.96	8F
1	0	0	1	0	0	0	0	0.965	90
1	0	0	1	0	0	0	1	0.97	91
1	0	0	1	0	0	1	0	0.975	92
1	0	0	1	0	0	1	1	0.98	93
1	0	0	1	0	1	0	0	0.985	94
1	0	0	1	0	1	0	1	0.99	95
1	0	0	1	0	1	1	0	0.995	96
1	0	0	1	0	1	1	1	1	97
1	0	0	1	1	0	0	0	1.005	98
1	0	0	1	1	0	0	1	1.01	99
1	0	0	1	1	0	1	0	1.015	9A
1	0	0	1	1	0	1	1	1.02	9B
1	0	0	1	1	1	0	0	1.025	9C
1	0	0	1	1	1	0	1	1.03	9D
1	0	0	1	1	1	1	0	1.035	9E
1	0	0	1	1	1	1	1	1.04	9F
1	0	1	0	0	0	0	0	1.045	A0
1	0	1	0	0	0	0	1	1.05	A1
1	0	1	0	0	0	1	0	1.055	A2
1	0	1	0	0	0	1	1	1.06	A3
1	0	1	0	0	1	0	0	1.065	A4
1	0	1	0	0	1	0	1	1.07	A5
1	0	1	0	0	1	1	0	1.075	A6
1	0	1	0	0	1	1	1	1.08	A7
1	0	1	0	1	0	0	0	1.085	A8
1	0	1	0	1	0	0	1	1.09	A9
1	0	1	0	1	0	1	0	1.095	AA
1	0	1	0	1	0	1	1	1.1	AB
1	0	1	0	1	1	0	0	1.105	AC
1	0	1	0	1	1	0	1	1.11	AD
1	0	1	0	1	1	1	0	1.115	AE
1	0	1	0	1	1	1	1	1.12	AF
1	0	1	1	0	0	0	0	1.125	B0
1	0	1	1	0	0	0	1	1.13	B1
1	0	1	1	0	0	1	0	1.135	B2

Table 16. IMVP8 VID TABLE (continued)

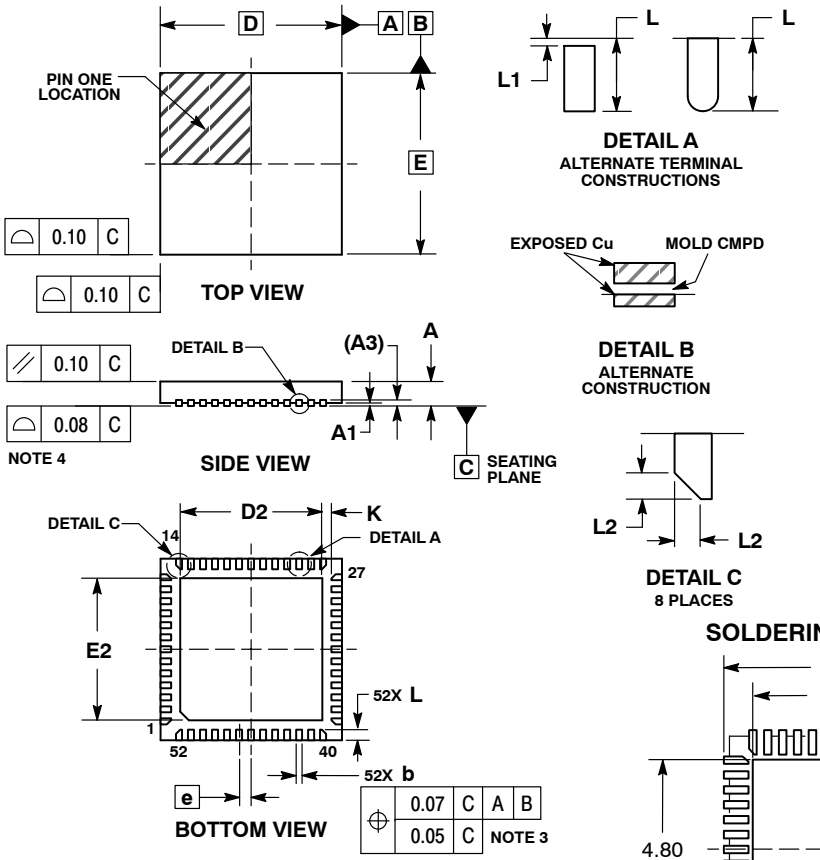
VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
1	0	1	1	0	0	1	1	1.14	B3
1	0	1	1	0	1	0	0	1.145	B4
1	0	1	1	0	1	0	1	1.15	B5
1	0	1	1	0	1	1	0	1.155	B6
1	0	1	1	0	1	1	1	1.16	B7
1	0	1	1	1	0	0	0	1.165	B8
1	0	1	1	1	0	0	1	1.17	B9
1	0	1	1	1	0	1	0	1.175	BA
1	0	1	1	1	0	1	1	1.18	BB
1	0	1	1	1	1	0	0	1.185	BC
1	0	1	1	1	1	0	1	1.19	BD
1	0	1	1	1	1	1	0	1.195	BE
1	0	1	1	1	1	1	1	1.2	BF
1	1	0	0	0	0	0	0	1.205	C0
1	1	0	0	0	0	0	1	1.21	C1
1	1	0	0	0	0	1	0	1.215	C2
1	1	0	0	0	0	1	1	1.22	C3
1	1	0	0	0	1	0	0	1.225	C4
1	1	0	0	0	1	0	1	1.23	C5
1	1	0	0	0	1	1	0	1.235	C6
1	1	0	0	0	1	1	1	1.24	C7
1	1	0	0	1	0	0	0	1.245	C8
1	1	0	0	1	0	0	1	1.25	C9
1	1	0	0	1	0	1	0	1.255	CA
1	1	0	0	1	0	1	1	1.26	CB
1	1	0	0	1	1	0	0	1.265	CC
1	1	0	0	1	1	0	1	1.27	CD
1	1	0	0	1	1	1	0	1.275	CE
1	1	0	0	1	1	1	1	1.28	CF
1	1	0	1	0	0	0	0	1.285	D0
1	1	0	1	0	0	0	1	1.29	D1
1	1	0	1	0	0	1	0	1.295	D2
1	1	0	1	0	0	1	1	1.3	D3
1	1	0	1	0	1	0	0	1.305	D4
1	1	0	1	0	1	0	1	1.31	D5
1	1	0	1	0	1	1	0	1.315	D6
1	1	0	1	0	1	1	1	1.32	D7
1	1	0	1	1	0	0	0	1.325	D8
1	1	0	1	1	0	0	1	1.33	D9
1	1	0	1	1	0	1	0	1.335	DA
1	1	0	1	1	0	1	1	1.34	DB
1	1	0	1	1	1	0	0	1.345	DC
1	1	0	1	1	1	0	1	1.35	DD
1	1	0	1	1	1	1	0	1.355	DE
1	1	0	1	1	1	1	1	1.36	DF

Table 16. IMVP8 VID TABLE (continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Voltage (V)	HEX
1	1	1	0	0	0	0	0	1.365	E0
1	1	1	0	0	0	0	1	1.37	E1
1	1	1	0	0	0	1	0	1.375	E2
1	1	1	0	0	0	1	1	1.38	E3
1	1	1	0	0	1	0	0	1.385	E4
1	1	1	0	0	1	0	1	1.39	E5
1	1	1	0	0	1	1	0	1.395	E6
1	1	1	0	0	1	1	1	1.4	E7
1	1	1	0	1	0	0	0	1.405	E8
1	1	1	0	1	0	0	1	1.41	E9
1	1	1	0	1	0	1	0	1.415	EA
1	1	1	0	1	0	1	1	1.42	EB
1	1	1	0	1	1	0	0	1.425	EC
1	1	1	0	1	1	0	1	1.43	ED
1	1	1	0	1	1	1	0	1.435	EE
1	1	1	0	1	1	1	1	1.44	EF
1	1	1	1	0	0	0	0	1.445	F0
1	1	1	1	0	0	0	1	1.45	F1
1	1	1	1	0	0	1	0	1.455	F2
1	1	1	1	0	0	1	1	1.46	F3
1	1	1	1	0	1	0	0	1.465	F4
1	1	1	1	0	1	0	1	1.47	F5
1	1	1	1	0	1	1	0	1.475	F6
1	1	1	1	0	1	1	1	1.48	F7
1	1	1	1	1	0	0	0	1.485	F8
1	1	1	1	1	0	0	1	1.49	F9
1	1	1	1	1	0	1	0	1.495	FA
1	1	1	1	1	0	1	1	1.5	FB
1	1	1	1	1	1	0	0	1.505	FC
1	1	1	1	1	1	0	1	1.51	FD
1	1	1	1	1	1	1	0	1.515	FE
1	1	1	1	1	1	1	1	1.52	FF

PACKAGE DIMENSIONS

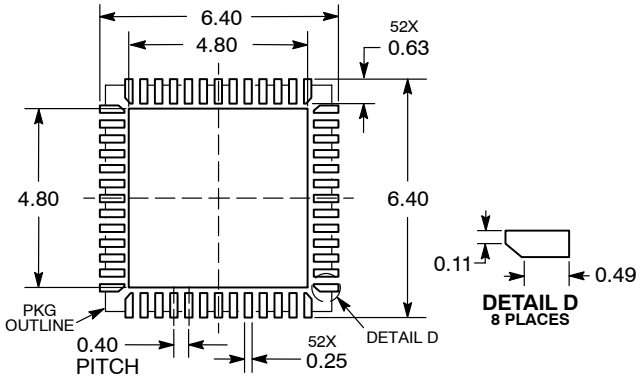
QFN52 6x6, 0.4P
CASE 485BE
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.15	0.25
D	6.00 BSC	
D2	4.60	4.80
E	6.00 BSC	
E2	4.60	4.80
e	0.40 BSC	
K	0.30 REF	
L	0.25	0.45
L1	0.00	0.15
L2	0.15 REF	

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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