NOT FOR PUBLIC RELEASE

# RTL8309G-GR

# SINGLE-CHIP 9-PORT 10/100MBPS SWITCH CONTROLLER

## DATASHEET

**(CONFIDENTIAL: Development Partners Only)**

**Rev. 1.2**
**18 Dec 2009**
**Track ID: JATR-1076-21**

**Realtek Semiconductor Corp.**
**No. 2, Innovation Road II, Hsinchu Science Park, Hsinchu 300, Taiwan**
**Tel.: +886-3-578-0211. Fax: +886-3-577-6047**
**www.realtek.com**

## COPYRIGHT



## DISCLAIMER

Realtek provides this document "as is", without warranty of any kind, neither expressed nor implied, including, but not limited to, the particular purpose. Realtek may make improvements and/or changes in this document or in the product described in this document at any time. This document could include technical inaccuracies or typographical errors.

## TRADEMARKS

Realtek is a trademark of Realtek Semiconductor Corporation. Other names mentioned in this document are trademarks/registered trademarks of their respective owners.

## USING THIS DOCUMENT

This document is intended for use by the software engineer when programming for Realtek RTL8309G switch controller chips.

Though every effort has been made to assure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

## REVISION HISTORY

| Revision | Release Date | Summary |
|---|---|---|
| 1.0 | 2008/08/12 | First release. |
| 1.1 | 2008/08/22 | Correct operating temperature. |
| 1.2 | 2009/12/18 | Update thermal characteristics. |

# Table of Contents

# List of Tables

# List of Figures

# 1. General Description

The RTL8309G is a 128-pin, ultra-low-power, high-performance 8-port Fast Ethernet single-chip switch with one extra MII port for specific applications. It integrates all the functions of a high-speed switch system—including SRAM for packet buffering, non-blocking switch fabric, address management, one general use MII interface, eight 10/100Base-TX transceivers, and nine Media Access Controllers—into a single 0.16µm CMOS device. It provides compatibility with all industry standard Ethernet and Fast Ethernet devices. Only a 25MHz crystal is required; the EEPROM is optional to save BOM costs.

The embedded packet storage SRAM in the RTL8309G features superior memory management technology to efficiently utilize the memory space. An integrated 1024-entry look-up table stores MAC address and associated information in a 10-bit direct mapping scheme. The table provides read/write access from the SMI interface, and each of the entries can be configured as a static entry. A static entry indicates that this entry is controlled by the external management processor and automatic aging and learning of the entry will not take place. To prevent MAC address mapping collisions, the embedded 16-entry Content-Addressable Memory (CAM) offers another memory space for recording the MAC address when the mapped entry in the lookup table is occupied. For each incoming packet, the RTL8309G searches the entries in the lookup table and the 16-entry CAM simultaneously. Then it obtains the correct destination port information to determine which output port the packet should be forwarded to. The aging time of the RTL8309G is around 300 seconds (this may be sped up to 800µs via EEPROM configuration).

The ninth port of the RTL8309G implements a MAC module without a PHY transceiver to provide an MII interface for connection with an external PHY or MAC in specific applications. This MII interface may be set to MII PHY mode, SNI PHY mode, or MII MAC mode to work with an external MAC module in a routing engine application, PHY module in a HomePNA application, or other physical layer transceivers. In order to operate correctly, both sides of the connection must be configured to the same speed, duplex, and flow control settings. Four pins are used for the ninth port to force the link status. This interface should be 2.5V or 3.3V compatible depending on the voltage supplied to the power pin VDDIO of this interface.

The RTL8309G is capable of preventing broadcast storms by setting strapping pins upon system reset. When this function is enabled, it will drop broadcast packets after receiving 64 continuous broadcast packets. This counter will be reset to 0 every 800ms or when the RTL8309G receives a non-broadcast packet.

The RTL8309G displays the port status via four LED indicators (with optional blinking time setting). These LEDs blink for diagnostic purposes at system reset time. The RTL8309G provides various type of LED combinations to fit different applications. Eight combinations of link, activity, speed, duplex, and collision, are available. Bi-color LED mode is also supported on the Link/Act LED.

The RTL8309G supports standard 802.3x flow control frames for full duplex, and optional backpressure for half duplex. It determines when to invoke the flow control mechanism by checking the availability of system resources, including the packet buffers and transmitting queues. If one of the forwarding ports is blocked, or system resources are unavailable, broadcast frames will be dropped according to the system configuration. The RTL8309G support two types of dropping methods. The input dropping method will not forward broadcast packets to any output ports and will drop these packets directly. The output dropping method will forward broadcast packets to non-blocked ports only.

To improve real-time and multimedia networking applications, the RTL8309G supports four types of QoS (Quality of Service). These are based on (1) Port-based priority, (2) 802.1p/Q VLAN priority tag, (3) TOS field in IPv4 header, (4) Specific IP address. Each output port supports a weighted ratio of high-priority and low-priority queues to fit bandwidth requirements in different applications.

The RTL8309G provides 802.1Q port-based VLAN operation to separate logical connectivity from physical connectivity. Each port may be set to any topology via EEPROM upon reset or SMI after reset. The RTL8309G also provides options to meet special application requirements. The first option is the ARP VLAN function, which is used to select to broadcast ARP frames to all VLANs or only forward ARP frames to the originating VLAN. The second option is the Leaky VLAN function, which is used to select to send unicast frames to other VLANs or only forward unicast frames to the originating VLAN. The VLAN tags can be inserted or removed on a per-port basis.

In router applications, the router may want to know which input port this packet came from. The RTL8309G supports Port VID (PVID) for each port to insert a PVID in the VLAN tag on egress. In this function, the VID information carried in the VLAN tag will be changed to PVID. The RTL8309G also provides an option to admit VLAN tagged packet with a specific PVID only. If this function is enabled, it will drop non-tagged packets and packets with an incorrect PVID.

Each physical layer channel consists of a 4B5B encoder/decoder, Manchester encoder/decoder, transmit output driver, scrambler/descrambler, output wave shaping, filters, digital adaptive equalizer, PLL circuit, and DC restoration circuit for clock/data recovery. This integrated chip benefits from low power consumption and offers advanced functions with flexible configuration for a small workgroup switch, multimedia, or real-time traffic mixed with other data type traffic, and other applications.

Green Ethernet features include:

**Link-On and Cable Length Power Saving**

The RTL8309G provides link-on and dynamic detection of cable length and dynamic adjustment of power required for the detected cable length. This feature provides high performance with minimum power consumption.

**Link-Down Power Saving**

The RTL8309G implements link-down power saving on a per-port basis, greatly cutting power consumption when the network cable is disconnected.

# 2. Features

- Integrates eight 10/100 transceivers and nine MAC units for 10Base-T and 100Base-TX
- Embedded SRAM for packet storage
- On-chip 1024-entry look-up table in direct mapping mode
- Embedded 16-entry CAM for hash collision mapping
- Provides read/write access to look-up table entries via SMI interface
- Provides non-blocking wire speed reception and transmission
- Flow control fully supported:
  - Half-duplex: backpressure flow control
  - Full-duplex: IEEE 802.3x flow control
- Support for 4 LEDs per-port in various combinations for comprehensive applications
- Optional loop detection function with an LED to indicate the existence of a loop
- LEDs blink upon reset for LED diagnostics
- Flexible system configuration by strapping pins, EEPROM, or SMI interface
- Optional crossover detection and auto correction for plug-and-play
- Fully compliant with IEEE 802.3/802.3u.
- Optional Forwarding/Filtering reserved control frames (DID=0180C2000003~0180C200000F)
- Optional Broadcast Input/Output Drop flow control
- Optional maximum packet length 1536/1552 Bytes
- Green Ethernet Features
  - Link-On and Cable Length Power Saving
  - Link-Down Power Saving
- Supports two Power Reduction methods:
  - Power saving mode (automatic cable detection)
  - Power down mode (via PHY register 0.11)
- Supports QoS function:
  - QoS based on: (1) Port-based priority (2) 802.1p VLAN tag (3) DiffServ/TOS field in TCP/IP header (4) IP address
  - Supports two-level priority queues with various weighting ratios
  - Queue service rate based on weighted round robin algorithm

- Optional auto turn off Flow Control for 1~2 sec to avoid head-of-line blocking

- Supports MII interface connection to external MAC or PHY via 3 modes:
  - PHY mode MII for router applications
  - PHY mode SNI for router applications
  - MAC mode MII for HomePNA or other PHY applications

- Flexible 802.1Q port/tag-based VLAN.
  - Optional 802.1Q tag-VID aware function
  - Optional VLAN Ingress Tag Admit Control
  - Optional VLAN Ingress Member set filtering
  - Optional ARP VLAN for broadcast packet
  - Optional Leaky VLAN for unicast packet

- Optional 802.1P/Q tag insertion or removal on per-port basis (egress)

- 25MHz crystal input

- 0.16µm, CMOS technology

- 128-pin PQFP package

- 1.8V core voltage

- Independent power options for 2.5V or 3.3V MII interface

# 3. System Applications

- Broadband gateway/firewall/VPN

- Wireless LAN access point + gateway

- Home networking expansion

- Standalone 10/100 switch

- Small workgroup switch

- VoIP infrastructure switch

# 4. Block Diagram

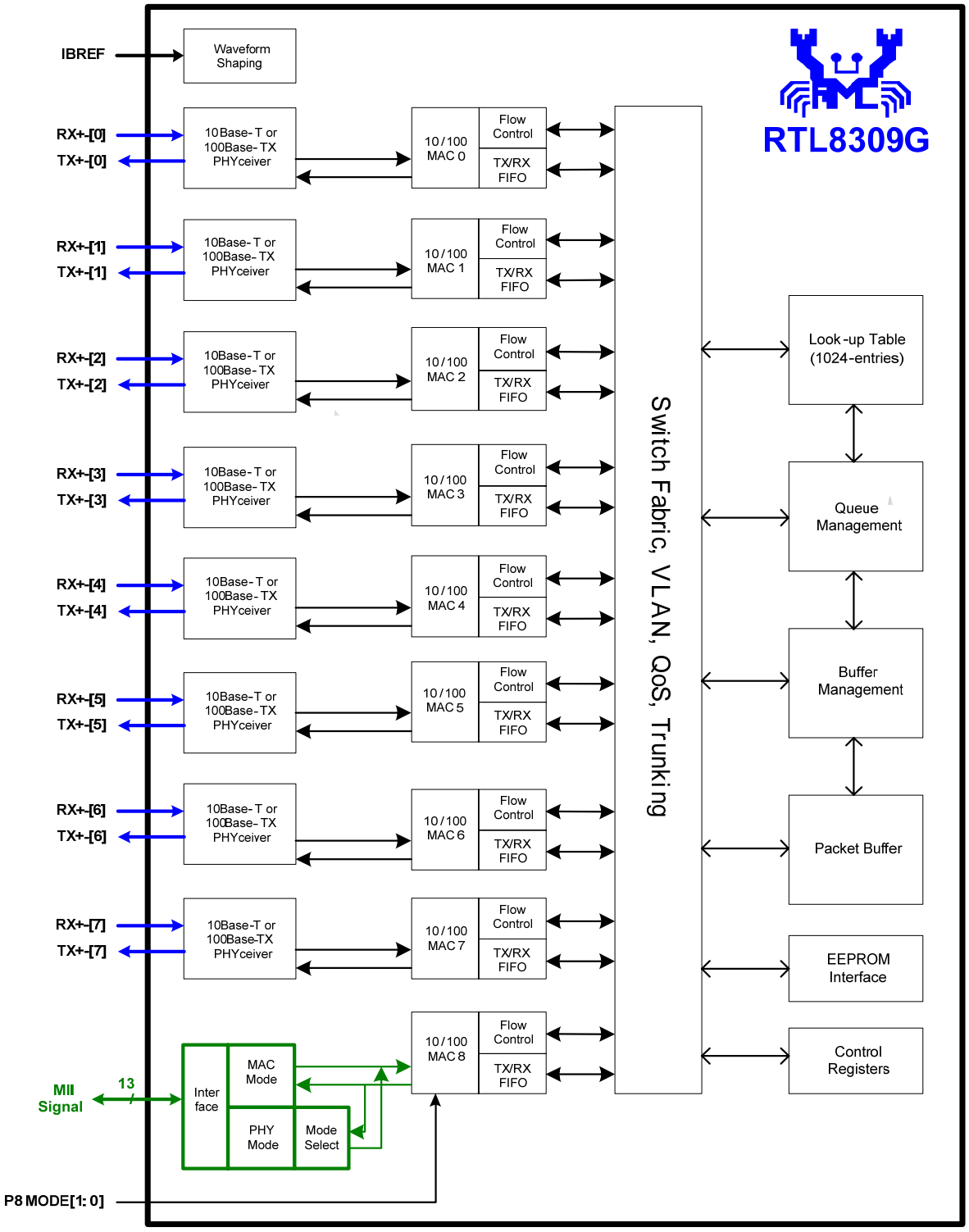



**Figure 1. Block Diagram**

# 5. Pin Assignments

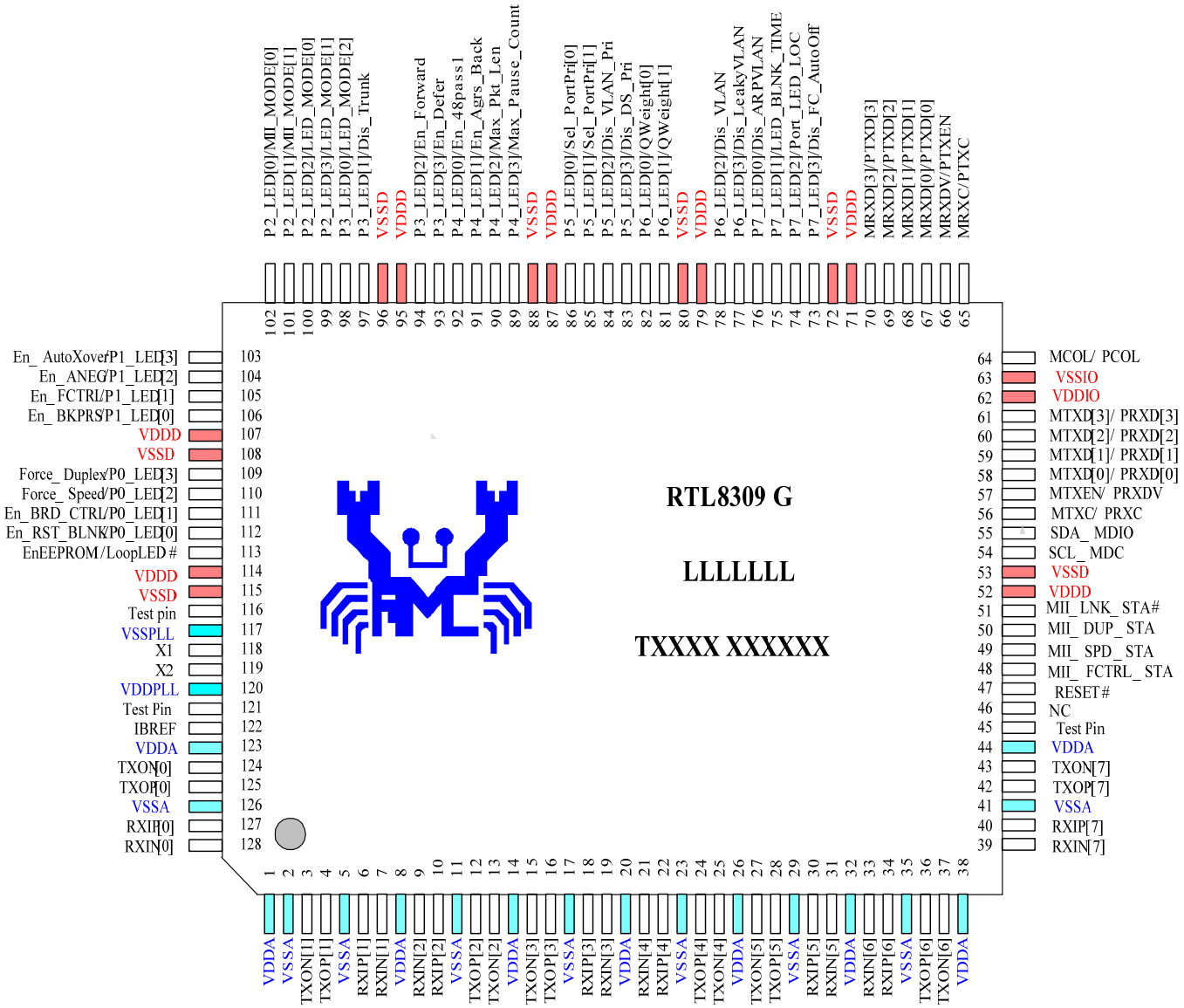



**Figure 2. Pin Assignments**

## *5.1. Package Identification*

Green package is indicated by a ‘G’ in the location marked ‘T’ in Figure 2.

## 5.2. Pin Assignments Table

Type codes used in the following tables: ‘A’ stands for analog; ‘D’ stands for digital, ‘I’ stands for input; ‘O’ stands for output.

**Table 1. Pin Assignments**

| Name | Pin No. | Type |
|---|---|---|
| VDDA | 1 | AVDD |
| VSSA | 2 | AGND |
| TXON[1] | 3 | AO |
| TXOP[1] | 4 | AO |
| VSSA | 5 | AGND |
| RXIP[1] | 6 | AI |
| RXIN[1] | 7 | AI |
| VDDA | 8 | AVDD |
| RXIN[2] | 9 | AI |
| RXIP[2] | 10 | AI |
| VSSA | 11 | AGND |
| TXOP[2] | 12 | AO |
| TXON[2] | 13 | AO |
| VDDA | 14 | AVDD |
| TXON[3] | 15 | AO |
| TXOP[3] | 16 | AO |
| VSSA | 17 | AGND |
| RXIP[3] | 18 | AI |
| RXIN[3] | 19 | AI |
| VDDA | 20 | AVDD |
| RXIN[4] | 21 | AI |
| RXIP[4] | 22 | AI |
| VSSA | 23 | AGND |
| TXOP[4] | 24 | AO |
| TXON[4] | 25 | AO |
| VDDA | 26 | AVDD |
| TXON[5] | 27 | AO |
| TXOP[5] | 28 | AO |
| VSSA | 29 | AGND |
| RXIP[5] | 30 | AI |
| RXIN[5] | 31 | AI |
| VDDA | 32 | AVDD |
| RXIN[6] | 33 | AI |
| RXIP[6] | 34 | AI |
| VSSA | 35 | AGND |
| TXOP[6] | 36 | AO |
| TXON[6] | 37 | AO |

| Name | Pin No. | Type |
|---|---|---|
| VDDA | 38 | AVDD |
| RXIN[7] | 39 | AI |
| RXIP[7] | 40 | AI |
| VSSA | 41 | AGND |
| TXOP[7] | 42 | AO |
| TXON[7] | 43 | AO |
| VDDA | 44 | AVDD |
| NC | 45 | - |
| NC | 46 | - |
| RESET# | 47 | I* |
| MII_FCTRL_STA | 48 | I* |
| MII_SPD_STA | 49 | I* |
| MII_DUP_STA | 50 | I* |
| MII_LNK_STA# | 51 | I* |
| VDDD | 52 | DVDD |
| VSSD | 53 | DGND |
| SCL_MDC | 54 | I/O |
| SDA_MDIO | 55 | I/O |
| MTXC/PRXC | 56 | I/O |
| MTXEN/PRXDV | 57 | O |
| MTXD[0]/PRXD[0] | 58 | I/O |
| MTXD[1]/PRXD[1] | 59 | I/O |
| MTXD[2]/PRXD[2] | 60 | I/O |
| MTXD[3]/PRXD[3] | 61 | I/O |
| VDDIO | 62 | DVDD |
| VSSIO | 63 | DGND |
| MCOL/PCOL | 64 | I/O |
| MRXC/PTXC | 65 | I/O |
| MRXDV/PTXDV | 66 | I |
| MRXD[0]/PTXD[0] | 67 | I |
| MRXD[1]/PTXD[1] | 68 | I |
| MRXD[2]/PTXD[2] | 69 | I |
| MRXD[3]/PTXD[3] | 70 | I |
| VDDD | 71 | DVDD |
| VSSD | 72 | DGND |
| P7_LED[3]/Dis_FC_AutoOff | 73 | I/O* |
| P7_LED[2]/Port_LED_LOC | 74 | I/O* |

| Name | Pin No. | Type |
|---|---|---|
| P7_LED[1]/LED_BLNK_TIME | 75 | I/O* |
| P7_LED[0]/Dis_ARPVLAN | 76 | I/O* |
| P6_LED[3]/Dis_LeakyVLAN | 77 | I/O* |
| P6_LED[2]/Dis_VLAN | 78 | I/O* |
| VDDD | 79 | DVDD |
| VSSD | 80 | DGND |
| P6_LED[1]/QWeight[1] | 81 | I/O* |
| P6_LED[0]/QWeight[0] | 82 | I/O* |
| P5_LED[3]/Dis_DS_Pri | 83 | I/O* |
| P5_LED[2]/Dis_VLAN_Pri | 84 | I/O* |
| P5_LED[1]/Sel_PortPri[1] | 85 | I/O* |
| P5_LED[0]/Sel_PortPri[0] | 86 | I/O* |
| VDDD | 87 | DVDD |
| VSSD | 88 | DGND |
| P4_LED[3]/Max_Pause_Count | 89 | I/O* |
| P4_LED[2]/Max_Pkt_Len | 90 | I/O* |
| P4_LED[1]/En_Agrs_Back | 91 | I/O* |
| P4_LED[0]/En_48pass1 | 92 | I/O* |
| P3_LED[3]/En_Defer | 93 | I/O* |
| P3_LED[2]/En_Forward | 94 | I/O* |
| VDDD | 95 | DVDD |
| VSSD | 96 | DGND |
| P3_LED[1]/Dis_Trunk | 97 | I/O* |
| P3_LED[0]/LED_MODE[2] | 98 | I/O* |
| P2_LED[3]/LED_MODE[1] | 99 | I/O* |
| P2_LED[2]/LED_MODE[0] | 100 | I/O* |
| P2_LED[1]/MII_MODE[1] | 101 | I/O* |

| Name | Pin No. | Type |
|---|---|---|
| P2_LED[0]/MII_MODE[0] | 102 | I/O* |
| P1_LED[3]/En_AutoXover | 103 | I/O* |
| P1_LED[2]/En_ANEG | 104 | I/O* |
| P1_LED[1]/En_FCTRL | 105 | I/O* |
| P1_LED[0]/En_BKPRS | 106 | I/O* |
| VDDD | 107 | DVDD |
| VSSD | 108 | DGND |
| P0_LED[3]/Force_Duplex | 109 | I/O* |
| P0_LED[2]/Force_Speed | 110 | I/O* |
| P0_LED[1]/En_BRD_CTRL | 111 | I/O* |
| P0_LED[0]/En_RST_BLNK | 112 | I/O* |
| LoopLED#,/EnEEPROM | 113 | I/O* |
| VDDD | 114 | DVDD |
| VSSD | 115 | DGND |
| NC | 116 | - |
| VSSPLL | 117 | AGND |
| X1 | 118 | I* |
| X2 | 119 | O* |
| VDDPLL | 120 | AVDD |
| NC | 121 | - |
| IBREF | 122 | AO |
| VDDA | 123 | AVDD |
| TXON[0] | 124 | AO |
| TXOP[0] | 125 | AO |
| VSSA | 126 | AGND |
| RXIP[0] | 127 | AI |
| RXIN[0] | 128 | AI |

*Note: '*' indicates voltage level is 1.8V.*

# 6. Pin Descriptions

'Type' codes used in the following tables.

A: Analog

D: Digital

I: Input

O: Output

I/O: Input/Output

IPU: Internal Pull-Up

IPD: Internal Pull-Down

All internal pull-up and pull-down resistors are 31K ohm resistors.

Upon Reset: Defined as a short time after the end of a hardware reset.

After Reset: Defined as the time after the specified 'Upon Reset' time.

## *6.1. Media Connection Pins*

**Table 2. Media Connection Pins**

| Pin Name | Pin No. | Type | Description |
|---|---|---|---|
| RXIP[7:0]<br>RXIN[7:0] | 40, 34, 30, 22, 18, 10, 6, 127, 39, 33, 31, 21, 19, 9, 7, 128 | AI | Differential Receive Data Input shared by 100Base-TX, 10Base-T for connection to a transformer. |
| TXOP[7:0]<br>TXON[7:0] | 42, 36, 28, 24, 16, 12, 4, 125, 43, 37, 27, 25, 15, 13, 3, 124 | AO | Differential Transmit Data Output shared by 100Base-TX, 10Base-T for connection to a transformer. |

## 6.2. MII Port MAC Interface Pins

The external device can be either 2.5V or 3.3V compatible depending on the power supplied to VDDIO. The input and input/output pins listed below do not implement an internal pull-high resistor. An external pull-high resistor is required for these floating input pins to reduce power consumption.

**Table 3. MII Port MAC Interface Pins**

| Pin Name | Pin No. | Type | Description | Default |
|---|---|---|---|---|
| MRXD[3:0] /PTXD[3:0] | 70, 69, 68, 67 | I | For MII MAC mode, these pins are MRXD[3:0], MII receive data nibble.<br>For MII PHY mode, these pins are PTXD[3:0], MII transmit data nibble.<br>For SNI PHY mode, PTXD[0] is serial transmit data. | - |
| MRXDV/PTXEN | 66 | I | For MII MAC mode, this pin represents MRXDV, MII receive data valid.<br>For MII PHY mode, this pin represents PTXEN, MII transmit enable.<br>For SNI PHY mode, this pin represents PTXEN, transmit enable. | - |
| MRXC/PTXC | 65 | I/O | For MII MAC mode, this pin represents MRXC/MII receive clock (acts as input).<br>For MII/SNI PHY mode, this pin represent PTXC/MII transmit clock (acts as output). | - |
| MCOL/PCOL | 64 | I/O | For MII MAC mode, this pin represents MCOL, MII collision detect (acts as input).<br>For MII/SNI PHY mode, this pin represents PCOL, MII collision detect (acts as output). | - |
| MTXD[3:0] /PRXD[3:0] | 61, 60, 59, 58 | O | Output After Reset.<br>For MII MAC mode, these pins are MTXD[3:0], MII transmit data of MAC.<br>For MII PHY mode, these pins are PRXD[3:0], MII receive data of MAC.<br>For SNI PHY mode, PRXD[0] is SNI serial receive data. PRXD[3:1] are unused. | - |
| MTXEN/PRXDV | 57 | O | For MII MAC mode, this pin represents MTXEN, MII transmit enable.<br>For MII PHY mode, this pin represents PRXDV, MII receive data valid.<br>For SNI PHY mode, this pin represents PRXDV, SNI receive data valid. | - |
| MTXC/PRXC | 56 | I/O | For MII MAC mode, this pin represents MTXC, MII transmit clock (acts as input).<br>For MII/SNI PHY mode, this pin represents MRXC, MII/SNI receive clock (acts as output). | - |
| MII_MODE[1:0] /P2_LED[1:0] | 101, 102 | Ipu* | Input Upon Reset.<br>Select MII port (9th port) operating mode.<br>11: Tri-state MII output<br>10: MII MAC mode<br>01: MII PHY mode<br>00: SNI PHY mode | 11 |

| Pin Name | Pin No. | Type | Description | Default |
|---|---|---|---|---|
| MII_LNK_STA# | 51 | Ipu* | Provides MII port (9th port) Link Status for MAC module at MII MAC/MII PHY/SNI PHY operation mode in real time.<br>This pin sets the link status of the MII port MAC module in real-time. | 1 |
| MII_DUP_STA | 50 | Ipu* | Provides MII port (9th port) duplex status for MAC module at MII MAC/MII PHY/SNI PHY operation mode in real time.<br>1: MII port operates in full duplex mode<br>0: MII port operates in half duplex mode | 1 |
| MII_SPD_STA | 49 | Ipu* | Provides MII port (9th port) speed status for MAC module at MII MAC/MII PHY/SNI PHY operation mode in real time.<br>1: MII port operates at 100Mbps speed<br>0: MII port operates at 10Mbps speed<br>In the applications outlined below, this pin should be left floating:<br>For HomePNA (MII MAC mode), speed is determined by RXC and TXC from PHY of HomePNA running at 1Mbps.<br>For SNI PHY mode, speed is fixed at 10MHz clock rate. | 1 |
| MII_FCTRL_STA | 48 | Ipu* | Provides MII port (9th port) flow control status for MAC module at MII MAC/MII PHY/SNI PHY operation mode in real time.<br>1: MII port has flow control ability<br>0: MII port does not have flow control ability | 1 |

*Note: '*' indicates voltage level is 1.8V.*

## 6.3. Miscellaneous Pins

**Table 4. Miscellaneous Pins**

| Pin Name | Pin No. | Type | Description | Default |
|---|---|---|---|---|
| X1 | 118 | I* | 25MHz Crystal Input.<br>The clock tolerance is ±50ppm.<br>When crystal is not used, the pin accepts 25MHz clock with 1.8V amplitude. | - |
| X2 | 119 | O* | 25MHz Crystal Output. | - |
| RESET# | 47 | I* | Active Low Reset Signal.<br>To complete the reset function, this pin must be asserted for at least 10ms. After reset, about 30ms is needed for the RTL8309G to complete the internal test function and initialization.<br>*Note: This pin is a Schmitt input pin.* | - |
| IBREF | 122 | A | Control Transmit Output Waveform Vpp.<br>This pin should be grounded through a 2.0K ohm resistor. | - |
| NC | 45, 46, 116, 121 | - | Not Connected. Floating in normal operation. | - |

*Note: '*' indicates voltage level is 1.8V.*

## 6.4. Port LED Pins

Each port supports four LED pins for status indication. The indicated status of these four LED pins may be changed by setting different values for strapping pin LED_MODE[2:0].

*Note 1: All LED statuses are represented as active-low or high depending on input strapping, except Bi-color Link/Act in Bi-color LED mode, whose polarity depends on Bi-color Speed status.*

*Note 2: Those pins are dual function pins: output for LED and input for strapping.*

**Table 5. Port LED Pins**

| Pin Name | Pin No. | Type | Description | Default |
|---|---|---|---|---|
| P0_LED[0] | 112 | Ipu/O* | Output After Reset = Used for the 1st LED. | |
| P1_LED[0] | 106 | | Mode 7: Speed (On =100 Mbps, Off =10Mbps) | 1 |
| P2_LED[0] | 102 | | Mode 6: Activity (Flash=Tx or Rx activity) | 1 |
| P3_LED[0] | 98 | | Mode 5: Speed (On =100 Mbps, Off =10Mbps) | 1 |
| P4_LED[0] | 92 | | Mode 4: Collision (Flash=Collision) | 1 |
| P5_LED[0] | 86 | | Mode 3: Reserved for internal use | 1 |
| P6_LED[0] | 82 | | Mode 2: RxAct+10/100 (Flash every 120ms=10Mbps Rx activity, Flash every 43ms = 100Mbps Rx activity). | 1 |
| P7_LED[0] | 76 | | Mode 1: Duplex+Collision (On=Full, Off=Half with no collision, Flash = Collision) | 1 |
| | | | Mode 0: Bi-color Speed. Polarity depends on Bi-color Link+Activity LED status. Refer to section 9.3.17 LEDs, page 101, for detailed information. | 1 |
| P0_LED[1] | 111 | Ipu/O* | Output After Reset = Used for the 2nd LED. | |
| P1_LED[1] | 105 | | Mode 7: Duplex+Collision (On=Full, Off=Half with no collision, Flash = Collision) | 1 |
| P2_LED[1] | 101 | | | |
| P3_LED[1] | 97 | | Mode 6: Speed (On =100 Mbps, Off =10Mbps) | 1 |
| P4_LED[1] | 91 | | Mode 5: Duplex (On=Full, Off=Half) | 1 |
| P5_LED[1] | 85 | | Mode 4: Duplex (On=Full, Off=Half) | 1 |
| P6_LED[1] | 81 | | Mode 3: Duplex+Collision (On=Full, Off=Half with no collision, Flash = Collision) | 1 |
| P7_LED[1] | 75 | | Mode 2: TxAct+10/100 (Flash every 120ms = 10Mbps Tx activity, Flash every 43ms = 100Mbps Tx activity) | 1 |
| | | | Mode 1: 10Link+Act (On=Link on 10Mbps, Off=No link on 10Mbps, Flash=10Mbps Tx or Rx activity) | 1 |
| | | | Mode 0: Duplex+Collision (On=Full, Off=Half with no collision, Flash = Collision) | 1 |

| Pin Name | Pin No. | Type | Description | Default |
|---|---|---|---|---|
| P0_LED[2]<br>P1_LED[2]<br>P2_LED[2]<br>P3_LED[2]<br>P4_LED[2]<br>P5_LED[2]<br>P6_LED[2]<br>P7_LED[2] | 110<br>104<br>100<br>94<br>90<br>84<br>78<br>74 | Ipu/O* | Output After Reset = Used for the 3rd LED.<br>Mode 7: Link+Act (On=Link, Off=No link, Flash=Tx or Rx activity)<br>Mode 6: Link (On=Link, Off=No link)<br>Mode 5: Link+Act (On=Link, Off=No link, Flash=Tx or Rx activity)<br>Mode 4: Link+Act+Speed (On=Link, Off=No link, Flash every 120ms=10Mbps activity, flash every 43ms=100Mbps)<br>Mode 3: Link+Act+Speed (On=Link, Off=No link, Flash every 120ms=10Mbps activity, flash every 43ms=100Mbps)<br>Mode 2: Link (On=Link, Off=No link)<br>Mode 1: 100Link+Act (On=Link on 100Mbps, Off=No link on 100Mbps, Flash=100Mbps Tx or Rx activity)<br>Mode 0: Bi-color Speed. Polarity depends on Bi-color Link+Activity LED status. Refer to section 9.3.17 LEDs, page 101, for detailed information. | <br>1<br>1<br>1<br>1<br><br>1<br><br>1<br><br>1 |
| P0_LED[3]<br>P1_LED[3]<br>P2_LED[3]<br>P3_LED[3]<br>P4_LED[3]<br>P5_LED[3]<br>P6_LED[3]<br>P7_LED[3] | 109<br>103<br>99<br>93<br>89<br>83<br>77<br>73 | Ipu/O* | Output After Reset = Used for the 4th LED.<br>Mode 7: Reserved for internal use<br>Mode 6: Reserved for internal use<br>Mode 5: Bi-color Link+Act<br>Mode 4: Reserved for internal use<br>Mode 3: 10/100 (On =100 Mbps, Off =10Mbps)<br>Mode 2: Reserved for internal use<br>Mode 1: Reserved for internal use<br>Mode 0: Reserved for internal use | <br>1<br>1<br>1<br>1<br>1<br>1<br>1<br>1 |
| LED_MODE[2]<br>/P3_LED[0]<br>LED_MODE[1]<br>/P2_LED[3]<br>LED_MODE[0]<br>/P2_LED[2] | 98<br><br>99<br><br>100 | I/O* | Input Upon Reset = Select LED display mode upon reset.<br>LED_MODE[2:0]=111 -> Mode 7: Speed, Duplex+Collision, Link+Act, Reserved<br>LED_MODE[2:0]=110 -> Mode 6: Activity, Speed, Link, Reserved<br>LED_MODE[2:0]=101 -> Mode 5: Speed, Duplex, Link+Act, Bi-color Link+Act<br>LED_MODE[2:0]=100 -> Mode 4: Collision, Duplex, Link+Act+Speed, Reserved<br>LED_MODE[2:0]=011 -> Mode 3: Reserved, Duplex+Collision, Link+Act+Speed, 10/100<br>LED_MODE[2:0]=010 -> Mode 2: RxAct+10/100, TxAct+10/100, Link, Reserved<br>LED_MODE[2:0]=001 -> Mode 1: Duplex+Collision, 10Link+Act, 100Link+Act, Reserved.<br>LEDM_ODE[2:0]=000 -> Mode 0: Bi-color Speed, Duplex+Collision, Bi-color Link+Act, Reserved | 111 |

| Pin Name | Pin No. | Type | Description | Default |
|---|---|---|---|---|
| Port_LED_LOC /P7_LED[2] | 74 | Ipu/O* | Input Upon Reset = Per port LED pin location reversed.<br>1: For designs where LEDs are placed at the opposite side to the phone jack<br>Port 0 LEDs are assigned at pins 109~112<br>Port 1 LEDs are assigned at pins 103~106<br>Port 2 LEDs are assigned at pins 99~102<br>Port 3 LEDs are assigned at pins 93, 94, 97, 98<br>Port 4 LEDs are assigned at pins 89~92<br>Port 5 LEDs are assigned at pins 83~86<br>Port 6 LEDs are assigned at pins 77, 78, 80, 81<br>Port 7 LEDs are assigned at pins 73~76<br><br>0: Suitable for designs where LEDs are placed on the same side as the phone jack<br>Port 0 LEDs are assigned at pins 73~76<br>Port 1 LEDs are assigned at pins 77, 78, 80, 81<br>Port 2 LEDs are assigned at pins 83~86<br>Port 3 LEDs are assigned at pins 89~92<br>Port 4 LEDs are assigned at pins 93, 94, 97, 98<br>Port 5 LEDs are assigned at pins 99~102<br>Port 6 LEDs are assigned at pins 103~106<br>Port 7 LEDs are assigned at pins 109~112 | 1 |
| LoopLED# /EnEEPROM | 113 | Ipu/O* | Output After Reset = LoopLED# used for LED.<br>If Loop detection is enabled, this pin indicates whether a Network loop is detected or not. Otherwise, this pin has no function.<br>*Note: The LED statuses are represented as active-low or high depending on input strapping.*<br>=> If Input=1: Output 0=Network loop is detected. 1=No loop.<br>=> If Input=0: Output 1=Network loop is detected. 0= No loop. | 1 |

*Note: '*' indicates voltage level is 1.8V.*

## 6.5. Serial EEPROM and SMI Pins

**Table 6. Serial EEPROM and SMI Pins**

| Pin Name | Pin No. | Type | Description | Default |
|---|---|---|---|---|
| EnEEPROM /LoopLED# | 113 | Ipu/O* | Input Upon Reset = Enable loading of serial EEPROM upon reset.<br>1: Enable Serial EEPROM load upon reset<br>0: Disable Serial EEPROM load upon reset | 1 |
| SCL_MDC | 54 | I/O | EEPROM Serial Clock or MDC.<br>This pin is three state when pin RESET#=0.<br>When the RTL8309G detects an EEPROM connected to it, this pin becomes SCL (output) to load the serial EEPROM upon reset. Then the pin changes to MDC (input) after reset. In this case, this pin should be pulled high (VDDIO 2.5V/3.3V) by external register.<br>When the RTL8309G does not detect an EEPROM connected to it, this pin is MDC (input). In this case, it needs an external pull-high resistor, unless it is floated. | - |
| SDA_MDIO | 55 | I/O | EEPROM Serial Data Input/Output or MDIO.<br>This pin is three state when pin RESET#=0.<br>When the RTL8309G detects an EEPROM connected to it, this pin becomes SDA (input/output) to load the serial EEPROM upon reset. The pin changes to MDIO (input/output) after reset.<br>When the RTL8309G does not detect an EEPROM connected to it, this pin is MDIO (input/output). It should be pulled high by an external resistor. | - |

*Note: '*' indicates voltage level is 1.8V.*

## 6.6. Strapping Pins

*Note: All strapping pins are dual function pins: output for LED and input for strapping. The table below covers strapping only. See Port LED Pins, on page 13, for LED pin settings.*

**Table 7. Strapping Pins**

| Pin Name | Pin No. | Type | Description | Default |
|---|---|---|---|---|
| En_ANEG /P1_LED[2] | 104 | Ipu* | Input Upon Reset = Enable Auto-negotiation function.<br>1: Enable the auto-negotiation function (NWay mode) and set PHY register 0.12<br>0: Disable the auto-negotiation function (force mode) and deselect PHY register 0.12<br>Output after reset = used for LED. | 1 |
| En_FCTRL /P1_LED[1] | 105 | Ipu* | Input Upon Reset = Enable flow control ability in full duplex mode.<br>1: In NWay mode, this pin sets PHY register 4.10, but the flow control function is finally enabled based on the auto negotiation result. In force mode, this pin will always enable the flow control function<br>0: Disable the flow control function<br>Output after reset = used for LED. | 1 |

| Pin Name | Pin No. | Type | Description | Default |
|---|---|---|---|---|
| En_BKPRS /P1_LED[0] | 106 | Ipu* | Input Upon Reset = Enable backpressure ability in half duplex mode.<br>1: Enable backpressure<br>0: Disable backpressure<br>Output after reset = used for LED. | 1 |
| Force_Duplex /P0_LED[3] | 109 | Ipu* | Force Duplex Mode.<br>This pin sets PHY Reg.0.8 and influences the contents of PHY Reg.4.<br>1: Force full duplex if auto-negotiation is disabled<br>0: Force half duplex if auto-negotiation is disabled<br>Output after reset = used for LED. | 1 |
| Force_Speed /P0_LED[2] | 110 | Ipu* | Force Operating Speed.<br>This pin sets PHY Reg.0.13 and influences the contents of PHY Reg.4.<br>1: Force 100Mbps speed if auto-negotiation is disabled<br>0: Force 10Mbps speed if auto-negotiation is disabled<br>Output after reset = used for LED. | 1 |
| En_BRD_CTRL /P0_LED[1] | 111 | Ipu* | Input Upon Reset = Disable Broadcast Storm Control.<br>1: Disable Broadcast Storm Control<br>0: Enable Broadcast Storm Control<br>Output after reset = used for LED. | 1 |
| En_RST_BLNK /P0_LED[0] | 112 | Ipu* | Input Upon Reset = Enable blinking of LEDs upon reset.<br>1: Enable power-on LED blinking for diagnosis<br>0: Disable power-on LED blinking<br>Output after reset = used for LED. | 1 |
| En_AutoXover /P1_LED[3] | 103 | Ipu* | Input Upon Reset = Enable Auto crossover detection.<br>1: Enable auto crossover detection<br>0: Disable auto crossover detection. MDI only<br>Output after reset = used for LED. | 1 |
| Dis_FC_AtuoOff /P7_LED[3] | 73 | Ipu* | Disable Auto Turn Off of Flow Control Ability.<br>1: Disable<br>0: Enable auto turn off flow control ability on the low priority queue for 1~2 seconds whenever the port receives a high priority frame. The flow control ability will be re-enabled if this port does not receive another high priority frame during this 1~2 second duration.<br>Output after reset = used for LED. | 1 |
| En_Forward /P3_LED[2] | 94 | Ipu* | Input Upon Reset = Enable forwarding of 802.1D specified reserved group MAC address frames.<br>1: Forward reserved control packets with DID=01-80-C2-00-00-03 to 01-80-C2-00-00-0F<br>0: Filter reserved control packets with DID=01-80-C2-00-00-03 to 01-80-C2-00-00-0F<br>Output after reset = used for LED. | 1 |
| En_Defer /P3_LED[3] | 93 | Ipu* | Input Upon Reset = Enable carrier sense defering function.<br>1: Enable carrier sense deferring function for half duplex backpressure<br>0: Disable carrier sense deferring function for half duplex backpressure<br>Output after reset = used for LED. | 1 |

| Pin Name | Pin No. | Type | Description | Default |
|---|---|---|---|---|
| En_48pass1<br>/P4_LED[0] | 92 | Ipu* | Enable 48 Pass 1 Mechanism.<br>1: 48 pass 1. Continuously collides 48 input packets then passes 1 packet to retain system resources and avoid repeater partition when buffer is full<br>0: Continuously collides input packets to avoid packet loss when buffer is full<br>Output after reset = used for LED. | 1 |
| En_Agrs_Back<br>/P4_LED[1] | 91 | Ipu* | Input Upon Reset = Enable aggressive back-off mechanism.<br>1: Enable more aggressive back-off mechanism in half duplex mode for performance enhancement. The back-off limitation will become 3 in this mode (default is 10)<br>0: Disable aggressive back-off mechanism in half duplex mode<br>Output after reset = used for LED. | 1 |
| Max_Pkt_Len<br>/P4_LED[2] | 90 | Ipu* | Input Upon Reset = Select maximum frame length.<br>1: 1536 bytes<br>0: 1552 bytes<br>Output after reset = used for LED. | 1 |
| Max_Pause_Count<br>/P4_LED[3] | 89 | Ipu* | Input Upon Reset = Select the max Pause frame count during a congested event.<br>1: Generates maximum of 32 pause frames, even if congestion still exists<br>0: Continuously generates pause frames until congestion is resolved<br>Output after reset = used for LED. | 1 |
| Dis_Trunk<br>/P3_LED[1] | 97 | Ipu* | Disable Two-Port Trunking Function.<br>1: Disable two-port trunking function<br>0: Port 0 and port 1 are combined as one trunk<br>Output after reset = used for LED. | 1 |
| Sel_PortPri[1:0]<br>/P5_LED[1:0] | 85, 86 | Ipu* | Input Upon Reset = Select high priority port for port-based priority QoS.<br>11: Disable port-based priority function<br>10: Select port 0 as high-priority port<br>01: Select port 2 as high-priority port<br>00: Select port 3 as high-priority port<br>Output after reset = used for LED. | 1 |
| Dis_VLAN_Pri<br>/P5_LED[2] | 84 | Ipu* | Input Upon Reset = Disable 802.1p VLAN tag priority based QoS.<br>1: Disable 802.1p priority classification for ingress packets on each port<br>0: Enable 802.1p priority classification for ingress packets on each port. A User priority field in the VLAN tag greater or equal to 4 will be considered a high priority packet<br>Output after reset = used for LED. | 1 |
| Dis_DS_Pri<br>/P5_LED[3] | 83 | Ipu* | Input Upon Reset = Disable Diffserv priority based QoS.<br>1: Disable diffserv priority classification for ingress packets on each port<br>0: Enable diffserv priority classification for ingress packets on each port<br>Output after reset = used for LED. | 1 |

| Pin Name | Pin No. | Type | Description | Default |
|---|---|---|---|---|
| QWeight[1:0]<br>/P6_LED[1:0] | 81, 82 | Ipu* | Input Upon Reset = Weighted round robin ratio priority queue.<br>The frame service ratio between the high priority queue and low priority queue is:<br>11: 16:1 10: Always high priority queue first<br>01: 8:1 00: 4:1<br>Output after reset = used for LED. | 1 |
| Dis_VLAN<br>/P6_LED[2] | 78 | Ipu* | Input Upon Reset = Disable VLAN.<br>1: Disable VLAN<br>0: Enable VLAN. The default VLAN membership configuration is MII port overlapped with all the other ports to form 8 individual VLANs. The default membership configuration may be modified by setting internal registers via the SMI interface or EEPROM<br>Output after reset = used for LED. | 1 |
| Dis_LeakyVLAN<br>/P6_LED[3] | 77 | Ipu* | Input Upon Reset = Disable Leaky VLAN.<br>1: Disable forwarding of unicast frames to other VLANs<br>0: Enable forwarding of unicast frames to other VLANs<br>*Note: Broadcast and multicast frames adhere to the VLAN configuration.*<br>Output after reset = used for LED. | 1 |
| Dis_ARPVLAN<br>/P7_LED[0] | 76 | Ipu* | Input Upon Reset = Disable ARP broadcast to all VLANs.<br>1: Disable broadcast of ARP broadcast packets to all VLANs<br>0: Enable broadcast of ARP broadcast packets to all VLANs<br>Output after reset = used for LED. | 1 |
| LED_BLNK_TIME<br>/P7_LED[1] | 75 | Ipu* | Input Upon Reset = Select blinking speed of activity and collision LED.<br>1: On 43ms then Off 43ms<br>0: On 120ms then Off 120ms<br>*Note: This pin only affects LEDs that are configured in LED mode 1, 5, and 7.*<br>Output after reset = used for LED. | 1 |

*Note: '*' indicates voltage level is 1.8V.*

## 6.7. Power Pins

**Table 8. Power Pins**

| Pin Name | Pin No. | Type | Description |
|---|---|---|---|
| VDDD | 52, 71, 79, 87, 95, 107, 114 | P | 1.8V Digital Power. Maximum current consumption is 0.2A. |
| VSSD | 53, 72, 80, 88, 96, 108, 115 | G | Digital Ground. |
| VDDIO | 62 | P | 2.5/3.3V Digital VDD for MII Interface.<br>Maximum current consumption is 0.003A. |
| VSSIO | 63 | G | Digital Ground for MII Interface. |
| VDDPLL | 120 | P | 1.8V Analog Power for PLL. |
| VSSPLL | 117 | G | 1.8V Analog Ground for PLL. |
| VDDA | 1, 8, 14, 20, 26, 32, 38, 44, 123 | P | 1.8V Analog Power (Used for Transmitters and Equalizers).<br>Maximum current consumption (VDDA+VDDPLL) is 0.7A. |
| VSSA | 2, 5, 11, 17, 23, 29, 35, 41, 126 | G | Analog Ground. |

# 7. EEPROM Register Description

## *7.1. Global Control Registers*

### 7.1.1. Global Control Register0

**Table 9. Global Control Register0**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| EEPROM Existence | 0.7 | 1: EEPROM does not exist<br>0: EEPROM exists | 0 |
| Accept Error Disable | 0.6 | 1: Filter bad packets in normal operation<br>0: Switch all packets including bad ones | 1 |
| IEEE 802.3x Transmit Flow Control Enable | 0.5 | 1: Invoke transmit flow control based on auto-negotiation result<br>0: Switch will not enable transmit flow control | 1 |
| IEEE 802.3x Receive Flow Control Enable | 0.4 | 1: When the switch receives a pause control frame, it has the ability to stop the next transmission of a normal frame until the timer has expired based on the auto negotiation result<br>0: Receive flow control not enabled | 1 |
| Broadcast Input or Output Drop | 0.3 | 1: Broadcast input drop is selected<br>0: Broadcast output drop is selected | 1 |
| Aging Enable | 0.2 | 1: Enable aging function in the switch<br>0: Disable aging function in the switch | 1 |
| Fast Aging Enable | 0.1 | 1: An entry learned in the lookup table will be aged out if it is not updated within an 800µs period<br>0: Disable fast aging function. The normal aging time of the RTL8309G is around 200~300 seconds | 0 |
| Enable ISP MAC Address Translation | 0.0 | 1: Enable ISP MAC Address Translation<br>0: Disable ISP MAC Address Translation | 0 |

## 7.1.2. Global Control Register1

**Table 10. Global Control Register1**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| LED Mode | 1.7~1.5 | 111: Mode 7: Speed, Duplex+Collision, Link+Act, SQI<br>110: Mode 6: Activity, Speed, Link, SQI<br>101: Mode 5: Speed, Duplex, Link+Act, Bi-color Link+Act<br>100: Mode 4: Collision, Duplex, Link+Act+Speed, SQI<br>011: Mode 3: SQI, Duplex+Collision, Link+Act+Speed,10/100<br>010: Mode 2: RxAct+10/100, TxAct+10/100, Link, SQI<br>001: Mode 1: Duplex+Collision, 10Link+Act, 100Link+Act, SQI<br>000: Mode 0: Duplex+Collision, Bi-color Speed, Bi-color Link+Act, SQI | 111 |
| Reserved | 1.4 | Reserved | 1 |
| Disable VLAN | 1.3 | 1: Disable VLAN<br>0: Enable VLAN | 1 |
| Disable 802.1Q Tag Aware VLAN | 1.2 | 1: Disable the 802.1Q tagged-VID Aware function<br>0: Use tagged-VID VLAN mapping for tagged frames but still use Port-Based VLAN mapping for priority-tagged and untagged frame | 0 |
| Disable VLAN Member Set Ingress Filtering | 1.1 | 1: The switch will not drop the received frame if the ingress port of this packet is not included in the matched VLAN member set<br>0: The switch will drop the received frame if the ingress port of this packet is not included in the matched VLAN member set | 1 |
| Disable VLAN Tag Admit Control | 1.0 | 1: The switch accepts all frames received<br>0: The switch will only accept tagged frames and will drop untagged frames | 1 |

## 7.1.3. Global Control Register2

**Table 11. Global Control Register2**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Enable Default High Priority DiffServ Code Point | 2.7 | 1: The default DiffServ code point listed below will be considered a high priority code point if DiffServ priority function is enabled<br>EF – 101110<br>AF – 001010, 010010, 011010, 100010<br>Network Control – 111000, 110000<br>0: The default DiffServ code point will be considered low priority | 1 |
| Reserved | 2.6~2.0 | Reserved | 1111<br>111 |

## 7.1.4. Global Control Register3

**Table 12. Global Control Register3**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| 802.1p Base Priority | 3.7~3.5 | Used to classify priority for incoming 802.1Q packets when 802.1p priority classification is enabled. 'User priority' compares against this value.<br>≥: Classify as high priority<br><: Classify as low priority | 100 |
| Trunking Port Assignment | 3.4 | 1: Combine port 0 and 1 as one trunking port, if trunking is enabled by strapping pin 'Dis_Trunk'<br>0: Combine port 6 and 7 as one trunking port, if trunking is enabled by strapping pin 'Dis_Trunk' | 1 |
| Queue Weight | 3.3~3.2 | The frame service ratio between the high priority queue and low priority queue is:<br>11: 16:1<br>10: Always high priority queue first<br>01: 8:1<br>00: 4:1 | 11 |
| Disable IP Priority for IP Address [A] | 3.1 | 1: The switch will compare both the source and destination IP addresses of an incoming packet against the value, IP address [A] AND IP mask [A], to classify priority for the packet<br>0: The switch will not compare the source or destination IP addresses of an incoming packet against the value, IP address [A] AND IP mask [A] | 0 |
| Disable IP Priority for IP Address [B] | 3.0 | 1: The switch will compare both the source and destination IP addresses of an incoming packet against the value, IP address [B] AND IP mask [B], to classify priority for the packet<br>0: The switch will not compare the source and destination IP addresses of an incoming packet against the value, IP address [B] AND IP mask [B] | 0 |

## 7.1.5. Global Control Register4

**Table 13. Global Control Register4**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Enable Differential Service Code Point [B] | 4.7 | 1: If Differential Service Priority is enabled, this bit specifies differential service code point [B] is high priority<br>0: If Differential Service Priority is enabled, this bit specifies differential service code point [B] is low priority | 0 |
| Reserved | 4.6 | Reserved | 1 |
| Differential Service Code Point [B] | 4.5~4.0 | Used to specify a high priority differential service code point B. For example, if these bits are set to '000000', all incoming packets with a TOS field equal to '000000' will be considered high priority packets. | 111111 |

### 7.1.6. Global Control Register5

**Table 14. Global Control Register5**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Enable Differential Service Code Point [A] | 5.7 | 1: If Differential Service Priority is enabled, this bit specifies differential service code point [A] is high priority<br>0: If Differential Service Priority is enabled, this bit specifies differential service code point [A] is low priority | 0 |
| Reserved | 5.6 | Reserved | 1 |
| Differential Service Code Point [A] | 5.5~5.0 | Used to specify a high priority differential service code point A. For example, if these bits are set to '111111', all incoming packets with a TOS field equal to '000000' will be considered high priority packets. | 111111 |

### 7.1.7. Global Control Register6

**Table 15. Global Control Register6**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Reserved | 6.7~6.0 | Reserved | 0000<br>0001 |

### 7.1.8. Global Control Register7

**Table 16. Global Control Register7**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Enable Drop for 48 Pass 1 | 7.7 | 1: Enable drop packet when SRAM full for 48 pass 1<br>0: Disable drop packet when SRAM full for 48 pass 1. This will result in SRAM run out | 1 |
| Reserved | 7.6 | Reserved | 1 |
| TX IPG Compensation | 7.5 | 1: 90ppm TX IPG compensation<br>0: 65ppm TX IPG compensation | 1 |
| Disable Loop Detection | 7.4 | 1: Disable loop detection function<br>0: Enable loop detection function | 1 |
| Reserved | 7.3 | Reserved | 1 |
| Lookup Table Accessible Enable | 7.2 | 1: Lookup table is accessible via indirect access registers<br>0: Lookup table is not accessible | 0 |
| Reserved | 7.1~7.0 | Reserved | 11 |

# 7.2. Port 0~7 Control Pins

## 7.2.1. Port 0 Control 0

**Table 17. Port 0 Control 0**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Reserved | 8.7~8.6 | Reserved | 11 |
| Speed and Duplex Ability | 8.5~8.4 | In Auto Negotiation Mode:<br>11: MII Reg0.13=1, 0.8=1, 4.8=1, 4.7=1, 4.6=1, 4.5=1<br>10: MII Reg0.13=1, 0.8=0, 4.8=0, 4.7=1, 4.6=1, 4.5=1<br>01: MII Reg0.13=0, 0.8=1, 4.8=0, 4.7=0, 4.6=1, 4.5=1<br>00: MII Reg0.13=0, 0.8=0, 4.8=0, 4.7=0, 4.6=0, 4.5=1<br>In Force Mode:<br>11: MII Reg0.13=1, 0.8=1, 4.8=1, 4.7=0, 4.6=0, 4.5=0<br>10: MII Reg0.13=1, 0.8=0, 4.8=0, 4.7=1, 4.6=0, 4.5=0<br>01: MII Reg0.13=0, 0.8=1, 4.8=0, 4.7=0, 4.6=1, 4.5=0<br>00: MII Reg0.13=0, 0.8=0, 4.8=0, 4.7=0, 4.6=0, 4.5=1 | 11 |
| Reserved | 8.3 | Reserved | 1 |
| Backpressure Enable | 8.2 | 1: Enable port 0 half duplex backpressure<br>0: Disable port 0 half duplex backpressure | 1 |
| VLAN Tag Insertion and Removal | 8.1~8.0 | 11: Do not insert or remove VLAN tags to/from packet<br>10: Insert PVID to non-tagged packets<br>01: Remove tag from tagged packets<br>00: Replace the VID with a PVID for tagged packets and insert a PVID to non-tagged packets | 11 |

## 7.2.2. Port 0 Control 1

**Table 18. Port 0 Control 1**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Reserved | 9.7~9.6 | Reserved | 11 |
| Local Loopback | 9.5 | 1: Perform ‘local loopback’, i.e., loop back MAC’s RX back to TX<br>0: Normal operation | 0 |
| Null VID Replacement | 9.4 | 1: The switch will replace a NULL VID with a port VID (12 bits)<br>0: No replacement for a NULL VID | 0 |
| Discard Non PVID Packets | 9.3 | 1: If the received packets are tagged, the switch will discard packets whose VID does not match the ingress port’s PVID<br>0: No packets will be dropped | 0 |
| Disable 802.1p Priority | 9.2 | 1: Disable 802.1p priority classification for ingress packets on port 0<br>0: Enable 802.1p priority classification on port 0 | 1 |
| Disable Diffserv Priority | 9.1 | 1: Disable Diffserv priority classification for ingress packets on port 0<br>0: Enable Diffserv priority classification on Port 0 | 1 |
| Disable Port-Based Priority | 9.0 | 1: Disable port priority function<br>0: Enable port priority function. Ingress packets from port 0 will be classified as high priority | 1 |

### 7.2.3. Port 0 Control 2

**Table 19. Port 0 Control 2**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Reserved | 10.7~10.0 | Reserved | 1111<br>1000 |

### 7.2.4. Port 0 Control 3

**Table 20. Port 0 Control 3**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Reserved | 11.7~11.4 | Reserved | 1111 |
| Transmission Enable | 11.3 | 1: Enable packet transmission on port 0<br>0: Disable packet transmission on port 0 | 1 |
| Reception Enable | 11.2 | 1: Enable packet reception on port 0<br>0: Disable packet reception on port 0 | 1 |
| Learning Enable | 11.1 | 1: Enable switch address learning capability<br>0: Disable switch address learning capability | 1 |
| Reserved | 11.0 | Reserved | 1 |
| **VLAN Entry [A]** | | | |
| VLAN ID [A] Membership Bit [7:0] | 12.7~12.0 | This register along with byte 13.0 forms a 9-bit field that specifies which ports are members of the VLAN. If a destination address look up fails, packets associated with this VLAN will be forwarded to ports specified in this field. E.g., 1 0000 0001 means port 8 and 0 are in this VLAN. | 0000<br>0001 |

## 7.2.5. Port 0 Control 4

**Table 21. Port 0 Control 4**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Port 0 VLAN Index [3:0] | 13.7~13.4 | In a port-based VLAN configuration, this register indexes port 0's 'Port VLAN Membership', which may be defined in one of the registers 'VLAN ID [A] Membership' to "VLAN ID [I] Membership". Port 0 can only communicate within the membership. This register also indexes to a default Port VID (PVID) for each port. The PVID is used in tag insertion and filtering if the tagged VID is not the same as the PVID. | 0000 |
| Reserved | 13.3~13.1 | Reserved | 111 |
| VLAN ID [A] Membership Bit [8] | 13.0 | This register along with byte 12.7~12.0 forms a 9-bit field that specifies which ports are members of the VLAN. If a destination address look up fails, packets associated with this VLAN will be forwarded to ports specified in this field. E.g., 1 0000 0001 means port 8 and 0 are in this VLAN. | 1 |
| **VLAN Entry [A]** | | | |
| VLAN ID [A] [7:0] | 14.7~14.0 | This register along with byte 15.3~15.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN A. | 0000 0000 |
| Reserved | 15.7~15.4 | Reserved | 1111 |
| VLAN ID [A] [11:8] | 15.3~15.0 | This register along with byte 14.7~14.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN A. | 0000 |

## 7.2.6. IP Address

**Table 22. IP Address**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| **IP Address [A]** | | | |
| IP Address [A] [16:23] | 16.7~16.0 | If IP priority for IP address [A] is enabled, the switch will compare the source IP address of an incoming packet against the value, IP address [A] AND IP mask [A], to classify priority for the packet. | 0xff |
| IP Address [A] [31:24] | 17.7~17.0 | If IP priority for IP address [A] is enabled, the switch will compare the source IP address of an incoming packet against the value, IP address [A] AND IP mask [A], to classify priority for the packet. | 0xff |
| IP Address [A] [7:0] | 18.7~18.0 | If IP priority for IP address [A] is enabled, the switch will compare the source IP address of an incoming packet against the value, IP address [A] AND IP mask [A], to classify priority for the packet. | 0xff |
| IP Address [A] [15:8] | 19.7~19.0 | If IP priority for IP address [A] is enabled, the switch will compare the source IP address of an incoming packet against the value, IP address [A] AND IP mask [A], to classify priority for the packet. | 0xff |
| **IP Address [B]** | | | |
| IP Address [B] [16:23] | 20.7~20.0 | If IP priority for IP address [B] is enabled, the switch will compare the source IP address of an incoming packet against the value, IP address [B] AND IP mask [B], to classify priority for the packet. | 0xff |

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| IP Address [B] [31:24] | 21.7~21.0 | If IP priority for IP address [B] is enabled, the switch will compare the source IP address of an incoming packet against the value, IP address [B] AND IP mask [B], to classify priority for the packet. | 0xff |
| IP Address [B] [7:0] | 22.7~22.0 | If IP priority for IP address [B] is enabled, the switch will compare the source IP address of an incoming packet against the value, IP address [B] AND IP mask [B], to classify priority for the packet. | 0xff |
| IP Address [B] [15:8] | 23.7~23.0 | If IP priority for IP address [B] is enabled, the switch will compare the source IP address of an incoming packet against the value, IP address [B] AND IP mask [B], to classify priority for the packet. | 0xff |

## 7.2.7. Port 1 Control 0

**Table 23. Port 1 Control 0**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Reserved | 24.7~24.6 | Reserved | 11 |
| Speed and Duplex Ability | 24.5~24.4 | In Auto Negotiation Mode:<br>11: MII Reg0.13=1, 0.8=1, 4.8=1, 4.7=1, 4.6=1, 4.5=1<br>10: MII Reg0.13=1, 0.8=0, 4.8=0, 4.7=1, 4.6=1, 4.5=1<br>01: MII Reg0.13=0, 0.8=1, 4.8=0, 4.7=0, 4.6=1, 4.5=1<br>00: MII Reg0.13=0, 0.8=0, 4.8=0, 4.7=0, 4.6=0, 4.5=1<br>In Force Mode:<br>11: MII Reg0.13=1, 0.8=1, 4.8=1, 4.7=0, 4.6=0, 4.5=0<br>10: MII Reg0.13=1, 0.8=0, 4.8=0, 4.7=1, 4.6=0, 4.5=0<br>01: MII Reg0.13=0, 0.8=1, 4.8=0, 4.7=0, 4.6=1, 4.5=0<br>00: MII Reg0.13=0, 0.8=0, 4.8=0, 4.7=0, 4.6=0, 4.5=1 | 11 |
| Reserved | 24.3 | Reserved | 1 |
| Backpressure Enable | 24.2 | 1: Enable port 1 half duplex backpressure<br>0: Disable port 1 half duplex backpressure | 1 |
| VLAN Tag Insertion and Removal | 24.1~24.0 | 11: Do not insert or remove VLAN tags to/from packets.<br>10: Insert PVID to non-tagged packets.<br>01: Remove tag from tagged packets.<br>00: Replace the VID with a PVID for tagged packets and insert a PVID to non-tagged packets. | 11 |

## 7.2.8. Port 1 Control 1

**Table 24. Port 1 Control 1**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Reserved | 25.7~25.6 | Reserved | 11 |
| Local Loopback | 25.5 | 1: Perform 'local loopback', i.e. loop back MAC's RX back to TX<br>0: Normal operation | 0 |
| Null VID Replacement | 25.4 | 1: The switch will replace a NULL VID with a port VID (12 bits)<br>0: No replacement for a NULL VID | 0 |
| Discard Non PVID Packets | 25.3 | 1: If the received packets are tagged, the switch will discard packets whose VID does not match the ingress port's PVID<br>0: No packets will be dropped | 0 |
| Disable 802.1p Priority | 25.2 | 1: Disable 802.1p priority classification for ingress packets on port 1<br>0: Enable 802.1p priority classification | 1 |
| Disable Diffserv Priority | 25.1 | 1: Disable Diffserv priority classification for ingress packets on port 1<br>0: Enable Diffserv priority classification | 1 |
| Disable Port-Based Priority | 25.0 | 1: Disable port priority function<br>0: Enable port priority function. Ingress packets from port 1 will be classified as high priority | 1 |

## 7.2.9. Port 1 Control 2

**Table 25. Port 1 Control 2**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Reserved | 26.7~26.0 | Reserved | 1111 1000 |

## 7.2.10. Port 1 Control 3

**Table 26. Port 1 Control 3**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Reserved | 27.7~27.4 | Reserved | 1111 |
| Transmission Enable | 27.3 | 1: Enable packet transmission on port 1<br>0: Disable packet transmission on port 1 | 1 |
| Reception Enable | 27.2 | 1: Enable packet reception on port 1<br>0: Disable packet reception on port 1 | 1 |
| Learning Enable | 27.1 | 1: Enable switch address learning capability<br>0: Disable switch address learning capability | 1 |
| Reserved | 27.0 | Reserved | 1 |
| **VLAN Entry [B]** | | | |
| VLAN ID [B] Membership Bit [7:0] | 28.7~28.0 | This register along with byte 29.0 forms a 9-bit field that specifies which ports are members of the VLAN. If a destination address look up fails, packets associated with this VLAN will be forwarded to ports specified in this field. E.g., 1 0000 0001 means port 8 and 0 are in this VLAN. | 0000 0010 |

## 7.2.11. Port 1 Control 4

**Table 27. Port 1 Control 4**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Port 1 VLAN Index [3:0] | 29.7~29.4 | In a port-based VLAN configuration, this register indexes port 1's 'Port VLAN Membership', which may be defined in one of the registers 'VLAN ID [A] Membership' to "VLAN ID [I] Membership". Port 1 can only communicate within the membership. This register also indexes to a default Port VID (PVID) for each port. The PVID is used in tag insertion and filtering if the tagged VID is not the same as the PVID. | 0001 |
| Reserved | 29.3~29.1 | Reserved | 111 |
| VLAN ID [B] Membership Bit [8] | 29.0 | This register along with byte 28.7~28.0 forms a 9-bit field that specifies which ports are members of the VLAN. If a destination address look up fails, packets associated with this VLAN will be forwarded to ports specified in this field. E.g., 1 0000 0001 means port 8 and 0 are in this VLAN. | 1 |
| **VLAN Entry [B]** | | | |
| VLAN ID [B] [7:0] | 30.7~30.0 | This register along with byte 31.3~31.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN B. | 0000 0001 |
| Reserved | 31.7~31.4 | Reserved | 1111 |
| VLAN ID [B] [11:8] | 31.3~31.0 | This register along with byte 30.7~30.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN B. | 0000 |

## 7.2.12. IP Mask

**Table 28. IP Mask**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| **IP Mask [A]** | | | |
| IP Mask [A] [16:23] | 32.7~32.0 | If IP priority for IP address [A] is enabled, the switch will compare the source IP address of an incoming packet against the value, IP address [A] AND IP mask [A], to classify priority for the packet. | 0xff |
| IP Mask [A] [31:24] | 33.7~33.0 | If IP priority for IP address [A] is enabled, the switch will compare the source IP address of an incoming packet against the value, IP address [A] AND IP mask [A], to classify priority for the packet. | 0xff |
| IP Mask [A] [7:0] | 34.7~34.0 | If IP priority for IP address [A] is enabled, the switch will compare the source IP address of an incoming packet against the value, IP address [A] AND IP mask [A], to classify priority for the packet. | 0xff |
| IP Mask [A] [15:8] | 35.7~35.0 | If IP priority for IP address [A] is enabled, the switch will compare the source IP address of an incoming packet against the value, IP address [A] AND IP mask [A], to classify priority for the packet. | 0xff |
| **IP Mask [B]** | | | |
| IP Mask [B] [16:23] | 36.7~36.0 | If IP priority for IP address [B] is enabled, the switch will compare the source IP address of an incoming packet against the value, IP address [B] AND IP mask [B], to classify priority for the packet. | 0xff |
| IP Mask [B] [31:24] | 37.7~37.0 | If IP priority for IP address [B] is enabled, the switch will compare the source IP address of an incoming packet against the value, IP address [B] AND IP mask [B], to classify priority for the packet. | 0xff |
| IP Mask [B] [7:0] | 38.7~38.0 | If IP priority for IP address [B] is enabled, the switch will compare the source IP address of an incoming packet against the value, IP address [B] AND IP mask [B], to classify priority for the packet. | 0xff |
| IP Mask [B] [15:8] | 39.7~39.0 | If IP priority for IP address [B] is enabled, the switch will compare the source IP address of an incoming packet against the value, IP address [B] AND IP mask [B], to classify priority for the packet. | 0xff |

## 7.2.13. Port 2 Control 0

**Table 29. Port 2 Control 0**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Reserved | 40.7~40.6 | Reserved | 11 |
| Speed and Duplex Ability | 40.5~40.4 | In Auto Negotiation Mode:<br>11: MII Reg0.13=1, 0.8=1, 4.8=1, 4.7=1, 4.6=1, 4.5=1<br>10: MII Reg0.13=1, 0.8=0, 4.8=0, 4.7=1, 4.6=1, 4.5=1<br>01: MII Reg0.13=0, 0.8=1, 4.8=0, 4.7=0, 4.6=1, 4.5=1<br>00: MII Reg0.13=0, 0.8=0, 4.8=0, 4.7=0, 4.6=0, 4.5=1<br>In Force Mode:<br>11: MII Reg0.13=1, 0.8=1, 4.8=1, 4.7=0, 4.6=0, 4.5=0<br>10: MII Reg0.13=1, 0.8=0, 4.8=0, 4.7=1, 4.6=0, 4.5=0<br>01: MII Reg0.13=0, 0.8=1, 4.8=0, 4.7=0, 4.6=1, 4.5=0<br>00: MII Reg0.13=0, 0.8=0, 4.8=0, 4.7=0, 4.6=0, 4.5=1 | 11 |

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Reserved | 40.3 | Reserved | 1 |
| Backpressure Enable | 40.2 | 1: Enable port 2 half duplex backpressure<br>0: Disable port 2 half duplex backpressure | 1 |
| VLAN Tag Insertion and Removal | 40.1~40.0 | 11: Do not insert or remove VLAN tags to/from packets.<br>10: Insert PVID to non-tagged packets.<br>01: Remove tag from tagged packets.<br>00: Replace VID with PVID for tagged packets and insert PVID to non-tagged packets. | 11 |

## 7.2.14. Port 2 Control 1

**Table 30. Port 2 Control 1**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Reserved | 41.7~41.6 | Reserved | 11 |
| Local Loopback | 41.5 | 1: Perform 'local loopback', i.e., loop back MAC's RX back to TX<br>0: Normal operation | 0 |
| Null VID Replacement | 41.4 | 1: The switch will replace a NULL VID with a port VID (12 bits)<br>0: No replacement for a NULL VID | 0 |
| Discard Non PVID Packets | 41.3 | 1: If the received packets are tagged, the switch will discard packets whose VID does not match the ingress port's PVID<br>0: No packets will be dropped | 0 |
| Disable 802.1p Priority | 41.2 | 1: Disable 802.1p priority classification for ingress packets on port 2<br>0: Enable 802.1p priority classification | 1 |
| Disable Diffserv Priority | 41.1 | 1: Disable Diffserv priority classification for ingress packets on port 2<br>0: Enable Diffserv priority classification | 1 |
| Disable Port-Based Priority | 41.0 | 1: Disable port priority function<br>0: Enable port priority function. Ingress packets from port 2 will be classified as high priority | 1 |

## 7.2.15. Port 2 Control 2

**Table 31. Port 2 Control 2**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Reserved | 42.7~42.0 | Reserved | 1111 1000 |

## 7.2.16. Port 2 Control 3

**Table 32. Port 2 Control 3**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Reserved | 43.7~43.4 | Reserved | 1111 |
| Transmission Enable | 43.3 | 1: Enable packet transmission on port 2<br>0: Disable packet transmission on port 2 | 1 |
| Reception Enable | 43.2 | 1: Enable packet reception on port 2<br>0: Disable packet reception on port 2 | 1 |
| Learning Enable | 43.1 | 1: Enable switch address learning capability<br>0: Disable switch address learning capability | 1 |
| Reserved | 43.0 | Reserved | 1 |
| **VLAN Entry [C]** | | | |
| VLAN ID [C] Membership Bit [7:0] | 44.7~44.0 | This register along with byte 45.0 forms a 9-bit field that specifies which ports are members of the VLAN. If a destination address look up fails, packets associated with this VLAN will be forwarded to ports specified in this field. E.g., 1 0000 0001 means port 8 and 0 are in this VLAN. | 0000<br>0100 |

## 7.2.17. Port 2 Control 4

**Table 33. Port 2 Control 4**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Port 2 VLAN Index [3:0] | 45.7~45.4 | In a port-based VLAN configuration, this register indexes port 2's 'Port VLAN Membership', which may be defined in one of the registers 'VLAN ID [A] Membership' to 'VLAN ID [I] Membership'. Port 2 can only communicate within the membership. This register also indexes to a default Port VID (PVID) for each port. The PVID is used in tag insertion and filtering if the tagged VID is not the same as the PVID. | 0010 |
| Reserved | 45.3~45.1 | Reserved | 111 |
| VLAN ID [C] Membership Bit [8] | 45.0 | This register along with byte 44.7~44.0 forms a 9-bit field that specifies which ports are members of the VLAN. If a destination address look up fails, packets associated with this VLAN will be forwarded to ports specified in this field. E.g., 1 0000 0001 means port 8 and 0 are in this VLAN. | 1 |
| **VLAN Entry [C]** | | | |
| VLAN ID [C] [7:0] | 46.7~46.0 | This register along with byte 47.3~47.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN C. | 0000<br>0010 |
| Reserved | 47.7~47.4 | Reserved | 1111 |
| VLAN ID [C] [11:8] | 47.3~47.0 | This register along with byte 46.7~46.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN C. | 0000 |

## 7.2.18. Switch MAC Address

The Switch MAC address is used as the source address in MAC pause control frames.

**Table 34. Switch MAC Address**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Switch MAC Address [47:40] | 48.7~48.0 | Switch MAC Address Byte 5. | 0x52 |
| Switch MAC Address [39:32] | 49.7~49.0 | Switch MAC Address Byte 4. | 0x54 |
| Switch MAC Address [31:24] | 50.7~50.0 | Switch MAC Address Byte 3. | 0x4C |
| Switch MAC Address [23:16] | 51.7~51.0 | Switch MAC Address Byte 2. | 0x83 |
| Switch MAC Address [15:8] | 52.7~52.0 | Switch MAC Address Byte 1. | 0x09 |
| Switch MAC Address [7:0] | 53.7~53.0 | Switch MAC Address Byte 0. | 0xB0 |

## 7.2.19. Port 3 Control 0

**Table 35. Port 3 Control 0**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Reserved | 54.7~54.6 | Reserved | 11 |
| Speed and Duplex Ability | 54.5~54.4 | In Auto Negotiation Mode:<br>11: MII Reg0.13=1, 0.8=1, 4.8=1, 4.7=1, 4.6=1, 4.5=1<br>10: MII Reg0.13=1, 0.8=0, 4.8=0, 4.7=1, 4.6=1, 4.5=1<br>01: MII Reg0.13=0, 0.8=1, 4.8=0, 4.7=0, 4.6=1, 4.5=1<br>00: MII Reg0.13=0, 0.8=0, 4.8=0, 4.7=0, 4.6=0, 4.5=1<br>In Force Mode:<br>11: MII Reg0.13=1, 0.8=1, 4.8=1, 4.7=0, 4.6=0, 4.5=0<br>10: MII Reg0.13=1, 0.8=0, 4.8=0, 4.7=1, 4.6=0, 4.5=0<br>01: MII Reg0.13=0, 0.8=1, 4.8=0, 4.7=0, 4.6=1, 4.5=0<br>00: MII Reg0.13=0, 0.8=0, 4.8=0, 4.7=0, 4.6=0, 4.5=1 | 11 |
| Reserved | 54.3 | Reserved | 1 |
| Backpressure Enable | 54.2 | 1: Enable port 3 half duplex backpressure.<br>0: Disable port 3 half duplex backpressure. | 1 |
| VLAN Tag Insertion and Removal | 54.1~54.0 | 11: Do not insert or remove VLAN tags to/from packets.<br>10: Insert PVID to non-tagged packets.<br>01: Remove tag from tagged packets.<br>00: Replace the VID with a PVID for tagged packets and insert a PVID to non-tagged packets. | 11 |

## 7.2.20. Port 3 Control 1

**Table 36. Port 3 Control 1**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Reserved | 55.7~55.6 | Reserved | 11 |
| Local Loopback | 55.5 | 1: Perform 'local loopback', i.e., loop back MAC's RX back to TX<br>0: Normal operation | 0 |
| Null VID Replacement | 55.4 | 1: The switch will replace a NULL VID with a port VID (12 bits)<br>0: No replacement for a NULL VID | 0 |
| Discard Non PVID Packets | 55.3 | 1: If the received packets are tagged, the switch will discard packets whose VID does not match the ingress port's PVID<br>0: No packets will be dropped | 0 |
| Disable 802.1p Priority | 55.2 | 1: Disable 802.1p priority classification for ingress packets on port 3<br>0: Enable 802.1p priority classification | 1 |
| Disable Diffserv Priority | 55.1 | 1: Disable Diffserv priority classification for ingress packets on port 3<br>0: Enable Diffserv priority classification | 1 |
| Disable Port-Based Priority | 55.0 | 1: Disable port priority function<br>0: Enable port priority function. Ingress packets from port 3 will be classified as high priority | 1 |

## 7.2.21. Port 3 Control 2

**Table 37. Port 3 Control 2**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Reserved | 56.7~56.0 | Reserved | 1111 1000 |

## 7.2.22. Port 3 Control 3

**Table 38. Port 3 Control 3**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Reserved | 57.7~57.4 | Reserved | 1111 |
| Transmission Enable | 57.3 | 1: Enable packet transmission on port 3<br>0: Disable packet transmission on port 3 | 1 |
| Reception Enable | 57.2 | 1: Enable packet reception on port 3<br>0: Disable packet reception on port 3 | 1 |
| Learning Enable | 57.1 | 1: Enable switch address learning capability<br>0: Disable switch address learning capability | 1 |
| Reserved | 57.0 | Reserved | 1 |
| **VLAN Entry [D]** | | | |
| VLAN ID [D] Membership Bit [7:0] | 58.7~58.0 | This register along with byte 59.0 forms a 9-bit field that specifies which ports are members of the VLAN. If a destination address look up fails, packets associated with this VLAN will be forwarded to ports specified in this field. E.g., 1 0000 0001 means port 8 and 0 are in this VLAN. | 0000<br>1000 |

## 7.2.23. Port 3 Control 4

**Table 39. Port 3 Control 4**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Port 3 VLAN Index [3:0] | 59.7~59.4 | In a port-based VLAN configuration, this register indexes port 3's 'Port VLAN Membership', which may be defined in one of the registers 'VLAN ID [A] Membership' to "VLAN ID [I] Membership". Port 3 can only communicate within the membership. This register also indexes to a default Port VID (PVID) for each port. The PVID is used in tag insertion and filtering if the tagged VID is not the same as the PVID. | 0011 |
| Reserved | 59.3~59.1 | Reserved | 111 |
| VLAN ID [D] Membership Bit [8] | 59.0 | This register along with byte 58.7~58.0 forms a 9-bit field that specifies which ports are members of the VLAN. If a destination address look up fails, packets associated with this VLAN will be forwarded to ports specified in this field. E.g., 1 0000 0001 means port 8 and 0 are in this VLAN. | 1 |
| **VLAN Entry [D]** | | | |
| VLAN ID [D] [7:0] | 60.7~60.0 | This register along with byte 61.3~61.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN D. | 0000<br>0011 |
| Reserved | 61.7~61.4 | Reserved | 1111 |
| VLAN ID [D] [11:8] | 61.3~61.0 | This register along with byte 60.7~60.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN D. | 0000 |

## 7.2.24. ISP MAC Address

The ISP MAC address is used as the source address in MAC address translation.

**Table 40. ISP MAC Address**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| ISP MAC Address [47:40] | 62.7~62.0 | ISP MAC Address Byte 5. | 0x05 |
| ISP MAC Address [39:32] | 63.7~63.0 | ISP MAC Address Byte 4. | 0x42 |
| ISP MAC Address [31:24] | 64.7~64.0 | ISP MAC Address Byte 3. | 0x2F |
| ISP MAC Address [23:16] | 65.7~65.0 | ISP MAC Address Byte 2. | 0x21 |
| ISP MAC Address [15:8] | 66.7~66.0 | ISP MAC Address Byte 1. | 0x91 |
| ISP MAC Address [7:0] | 67.7~67.0 | ISP MAC Address Byte 0. | 0x5C |

## 7.2.25. Port 4 Control 0

**Table 41. Port 4 Control 0**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Reserved | 68.7~68.6 | Reserved | 11 |
| Speed and Duplex Ability | 68.5~68.4 | In Auto Negotiation Mode:<br>11: MII Reg0.13=1, 0.8=1, 4.8=1, 4.7=1, 4.6=1, 4.5=1<br>10: MII Reg0.13=1, 0.8=0, 4.8=0, 4.7=1, 4.6=1, 4.5=1<br>01: MII Reg0.13=0, 0.8=1, 4.8=0, 4.7=0, 4.6=1, 4.5=1<br>00: MII Reg0.13=0, 0.8=0, 4.8=0, 4.7=0, 4.6=0, 4.5=1<br>In Force Mode:<br>11: MII Reg0.13=1, 0.8=1, 4.8=1, 4.7=0, 4.6=0, 4.5=0<br>10: MII Reg0.13=1, 0.8=0, 4.8=0, 4.7=1, 4.6=0, 4.5=0<br>01: MII Reg0.13=0, 0.8=1, 4.8=0, 4.7=0, 4.6=1, 4.5=0<br>00: MII Reg0.13=0, 0.8=0, 4.8=0, 4.7=0, 4.6=0, 4.5=1 | 11 |
| Reserved | 68.3 | Reserved | 1 |
| Backpressure Enable | 68.2 | 1: Enable port 4 half duplex backpressure<br>0: Disable port 4 half duplex backpressure | 1 |
| VLAN Tag Insertion and Removal | 68.1~68.0 | 11: Do not insert or remove VLAN tags to/from packet.<br>10: Insert PVID to non-tagged packets.<br>01: Remove tag from tagged packets.<br>00: Replace the VID with a PVID for tagged packets and insert a PVID to non-tagged packets. | 11 |

## 7.2.26. Port 4 Control 1

**Table 42. Port 4 Control 1**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Reserved | 69.7~68.6 | Reserved | 11 |
| Local Loopback | 69.5 | 1: Perform 'local loopback', i.e., loop back MAC's RX back to TX<br>0: Normal operation | 0 |
| Null VID Replacement | 69.4 | 1: The switch will replace a NULL VID with a port VID (12 bits)<br>0: No replacement for a NULL VID | 0 |
| Discard Non PVID Packets | 69.3 | 1: If the received packets are tagged, the switch will discard packets whose VID does not match the ingress port's PVID<br>0: No packets will be dropped | 0 |
| Disable 802.1p Priority | 69.2 | 1: Disable 802.1p priority classification for ingress packets on port 4<br>0: Enable 802.1p priority classification | 1 |
| Disable Diffserv Priority | 69.1 | 1: Disable Diffserv priority classification for ingress packets on port 4<br>0: Enable Diffserv priority classification | 1 |
| Disable Port-Based Priority | 69.0 | 1: Disable port priority function<br>0: Enable port priority function. Ingress packets on port 4 will be classified as high priority | 1 |

## 7.2.27. Port 4 Control 2

**Table 43. Port 4 Control 2**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Reserved | 70.7~70.0 | Reserved | 1111 1000 |

## 7.2.28. Port 4 Control 3

**Table 44. Port 4 Control 3**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Reserved | 71.7~71.4 | Reserved | 1111 |
| Transmission Enable | 71.3 | 1: Enable packet transmission on port 4<br>0: Disable packet transmission on port 4 | 1 |
| Reception Enable | 71.2 | 1: Enable packet reception on port 4<br>0: Disable packet reception on port 4 | 1 |
| Learning Enable | 71.1 | 1: Enable switch address learning capability<br>0: Disable switch address learning capability | 1 |
| Reserved | 71.0 | Reserved | 1 |
| **VLAN Entry [E]** | | | |
| VLAN ID [E] Membership Bit[7:0] | 72.7~72.0 | This register along with byte 73.0 forms a 9-bit field that specifies which ports are members of the VLAN. If a destination address look up fails, packets associated with this VLAN will be forwarded to ports specified in this field. E.g., 1 0000 0001 means port 8 and 0 are in this VLAN. | 0001 0000 |

## 7.2.29. Port 4 Control 4

**Table 45. Port 4 Control 4**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Port 4 VLAN Index [3:0] | 73.7~73.4 | In a port-based VLAN configuration, this register indexes port 4's 'Port VLAN Membership', which could be defined in one of the registers 'VLAN ID [A] Membership' to 'VLAN ID [I] Membership'. Port 4 can only communicate within the membership. This register also indexes to a default Port VID (PVID) for each port. The PVID is used in tag insertion and filtering if the tagged VID is not the same as the PVID. | 0100 |
| Reserved | 73.3~73.1 | Reserved | 111 |
| VLAN ID [E] Membership Bit[8] | 73.0 | This register along with byte 72.7~72.0 forms a 9-bit field that specifies which ports are members of the VLAN. If a destination address look up fails, packets associated with this VLAN will be forwarded to ports specified in this field. E.g., 1 0000 0001 means port 8 and 0 are in this VLAN. | 1 |
| **VLAN Entry [E]** | | | |
| VLAN ID [E] [7:0] | 74.7~74.0 | This register along with byte 75.3~75.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN E. | 0000 0100 |
| Reserved | 75.7~75.4 | Reserved | 1111 |
| VLAN ID [E] [11:8] | 75.3~75.0 | This register along with byte 74.7~74.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN E. | 0000 |

# 7.3. MII Port Control Pins

## 7.3.1. MII Port Control 0

**Table 46. MII Port Control 0**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Reserved | 76.7~76.2 | Reserved | 1111 11 |
| VLAN Tag Insertion and Removal | 76.1~76.0 | 11: Do not insert or remove VLAN tags to/from packets.<br>10: Insert PVID to non-tagged packets.<br>01: Remove tag from tagged packets.<br>00: Replace the VID with a PVID for tagged packets and insert a PVID to non-tagged packets. | 11 |

## 7.3.2. MII Port Control 1

**Table 47. MII Port Control 1**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Transmission Enable | 77.7 | 1: Enable packet transmission on MII interface<br>0: Disable packet transmission on MII interface | 1 |
| Reception Enable | 77.6 | 1: Enable packet reception on MII interface<br>0: Disable packet reception on MII interface | 1 |
| Learning Enable | 77.5 | 1: Enable switch address learning capability<br>0: Disable switch address learning capability | 1 |
| Reserved | 77.4 | Reserved | 0 |
| Disable 802.1p Priority | 77.3 | 1: Disable 802.1p priority classification for ingress packets on MII port<br>0: Enable 802.1p priority classification | 1 |
| Disable Diffserv Priority | 77.2 | 1: Disable Diffserv priority classification for ingress packets on MII port<br>0: Enable Diffserv priority classification | 1 |
| Disable Port-Based Priority | 77.1 | 1: Disable port priority function<br>0: Enable port priority function. Ingress packets from the MII port will be classified as high priority | 1 |
| Reserved | 77.0 | Reserved | 0 |
| **VLAN Entry [I]** | | | |
| VLAN ID [I] Membership Bit [7:0] | 78.7~78.0 | This register along with byte 79.0 forms a 9-bit field that specifies which ports are members of the VLAN. If a destination address look up fails, packets associated with this VLAN will be forwarded to ports specified in this field. E.g., 1 0000 0001 means port 8 and 0 are in this VLAN. | 1111 1111 |

## 7.3.3. MII Port Control 2

**Table 48. MII Port Control 2**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Null VID Replacement | 79.7 | 1: The switch will replace a NULL VID with a port VID (12 bits)<br>0: No replacement for a NULL VID | 0 |
| Discard Non PVID Packets | 79.6 | 1: If the received packets are tagged, the switch will discard packets with a VID that does not match the ingress port default VID, which is indexed by port 8's 'Port-based VLAN index'<br>0: No packets will be dropped | 0 |
| Reserved | 79.5 | Reserved | 1 |
| Port 8 VLAN Index [3:0] | 79.4~79.1 | In a port-based VLAN configuration, this register indexes port 8's 'Port VLAN Membership', which may be defined in one of the registers 'VLAN ID [A] Membership' to 'VLAN ID [I] Membership'. Port 8 can only communicate within the membership. This register also indexes to a default Port VID (PVID) for each port. The PVID is used in tag insertion and filtering if the tagged VID is not the same as the PVID. | 1000 |
| VLAN ID [I] Membership Bit [8] | 79.0 | This register along with byte 78.7~78.0 forms a 9-bit field that specifies which ports are members of the VLAN. If a destination address look up fails, packets associated with this VLAN will be forwarded to ports specified in this field. E.g., 1 0000 0001 means port 8 and 0 are in this VLAN. | 1 |
| **VLAN Entry [I]** | | | |
| VLAN ID [I] [7:0] | 80.7~80.0 | This register along with byte 81.3~81.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN I. | 0000 1000 |
| Reserved | 81.7~81.4 | Reserved | 1111 |
| VLAN ID [I] [11:8] | 81.3~81.0 | This register along with byte 80.7~80.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN I. | 0000 |

## 7.3.4. CPU Port and WAN Port

**Table 49. CPU Port and WAN Port**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| WAN Port | 82.7~82.4 | Specifies the WAN port on the RTL8309G.<br>1000: MII Port is WAN Port<br>0111: Port 7 is WAN Port 0110: Port 6 is WAN Port<br>0101: Port 5 is WAN Port 0100: Port 4 is WAN Port<br>0011: Port 3 is WAN Port 0010: Port 2 is WAN Port<br>0001: Port 1 is WAN Port 0000: Port 0 is WAN Port | 0111 |
| CPU Port | 82.3~82.0 | Specifies the CPU port on the RTL8309G.<br>1000: MII Port is CPU Port<br>0111: Port 7 is CPU Port 0110: Port 6 is CPU Port<br>0101: Port 5 is CPU Port 0100: Port 4 is CPU Port<br>0011: Port 3 is CPU Port 0010: Port 2 is CPU Port<br>0001: Port 1 is CPU Port 0000: Port 0 is CPU Port | 0000 |

# 7.4. Port 5~7 Control Pins

## 7.4.1. Port 5 Control 0

**Table 50. Port 5 Control 0**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Reserved | 83.7~83.6 | Reserved | 11 |
| Speed and Duplex Ability | 83.5~83.4 | In Auto Negotiation Mode:<br>11: MII Reg0.13=1, 0.8=1, 4.8=1, 4.7=1, 4.6=1, 4.5=1<br>10: MII Reg0.13=1, 0.8=0, 4.8=0, 4.7=1, 4.6=1, 4.5=1<br>01: MII Reg0.13=0, 0.8=1, 4.8=0, 4.7=0, 4.6=1, 4.5=1<br>00: MII Reg0.13=0, 0.8=0, 4.8=0, 4.7=0, 4.6=0, 4.5=1<br>In Force Mode:<br>11: MII Reg0.13=1, 0.8=1, 4.8=1, 4.7=0, 4.6=0, 4.5=0<br>10: MII Reg0.13=1, 0.8=0, 4.8=0, 4.7=1, 4.6=0, 4.5=0<br>01: MII Reg0.13=0, 0.8=1, 4.8=0, 4.7=0, 4.6=1, 4.5=0<br>00: MII Reg0.13=0, 0.8=0, 4.8=0, 4.7=0, 4.6=0, 4.5=1 | 11 |
| Reserved | 83.3 | Reserved | 1 |
| Backpressure Enable | 83.2 | 1: Enable port 5 half duplex backpressure<br>0: Disable port 5 half duplex backpressure | 1 |
| VLAN Tag Insertion and Removal | 83.1~83.0 | 11: Do not insert or remove VLAN tags to/from packet.<br>10: Insert PVID to non-tagged packets.<br>01: Remove tag from tagged packets.<br>00: Replace the VID with a PVID for tagged packets and insert a PVID to non-tagged packets. | 11 |

## 7.4.2. Port 5 Control 1

**Table 51. Port 5 Control 1**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Reserved | 84.7~84.6 | Reserved | 11 |
| Local Loopback | 84.5 | 1: Perform ‘local loopback’, i.e., loop back MAC’s RX back to TX<br>0: Normal operation | 0 |
| Null VID Replacement | 84.4 | 1: The switch will replace a NULL VID with a port VID (12 bits)<br>0: No replacement for a NULL VID | 0 |
| Discard Non PVID Packets | 84.3 | 1: If the received packets are tagged, the switch will discard packets whose VID does not match the ingress port’s PVID<br>0: No packets will be dropped | 0 |
| Disable 802.1p Priority | 84.2 | 1: Disable 802.1p priority classification for ingress packets on port 5<br>0: Enable 802.1p priority classification | 1 |
| Disable Diffserv Priority | 84.1 | 1: Disable Diffserv priority classification for ingress packets on port 5<br>0: Enable Diffserv priority classification | 1 |
| Disable Port-Based Priority | 84.0 | 1: Disable port priority function<br>0: Enable port priority function. Ingress packets from port 5 will be classified as high priority | 1 |

## 7.4.3. Port 5 Control 2

**Table 52. Port 5 Control 2**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Reserved | 85.7~85.0 | Reserved | 1111<br>1000 |

## 7.4.4. Port 5 Control 3

**Table 53. Port 5 Control 3**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Reserved | 86.7~86.4 | Reserved | 1111 |
| Transmission Enable | 86.3 | 1: Enable packet transmission on port 5<br>0: Disable packet transmission on port 5 | 1 |
| Reception Enable | 86.2 | 1: Enable packet reception on port 5<br>0: Disable packet reception on port 5 | 1 |
| Learning Enable | 86.1 | 1: Enable switch address learning capability<br>0: Disable switch address learning capability | 1 |
| Reserved | 86.0 | Reserved | 1 |
| **VLAN Entry [F]** | | | |
| VLAN ID [F] Membership Bit [7:0] | 87.7~87.0 | This register, along with byte 88.0, forms a 9-bit field that specifies which ports are members of the VLAN. If a destination address look up fails, packets associated with this VLAN will be forwarded to ports specified in this field. E.g., 1 0000 0001 means port 8 and 0 are in this VLAN. | 0010<br>0000 |

## 7.4.5. Port 5 Control 4

**Table 54. Port 5 Control 4**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Port 5 VLAN Index [3:0] | 88.7~88.4 | In a port-based VLAN configuration, this register indexes port 5's 'Port VLAN Membership', which may be defined in one of the registers 'VLAN ID [A] Membership' to 'VLAN ID [I] Membership'. Port 5 can only communicate within the membership. This register also indexes to a default Port VID (PVID) for each port. The PVID is used in tag insertion and filtering if the tagged VID is not the same as the PVID. | 0101 |
| Reserved | 88.3~88.1 | Reserved | 111 |
| VLAN ID [F] Membership Bit [8] | 88.0 | This register along with byte 87.7~87.0 forms a 9-bit field that specifies which ports are members of the VLAN. If a destination address look up fails, packets associated with this VLAN will be forwarded to ports specified in this field. E.g., 1 0000 0001 means port 8 and 0 are in this VLAN. | 1 |
| **VLAN Entry [F]** | | | |
| VLAN ID [F] [7:0] | 89.7~89.0 | This register along with byte 90.3~90.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN F. | 0000 0101 |
| Reserved | 90.7~90.4 | Reserved | 1111 |
| VLAN ID [F] [11:8] | 90.3~90.0 | This register along with byte 89.7~89.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN F. | 0000 |

## 7.4.6. Port 6 Control 0

**Table 55. Port 6 Control 0**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Reserved | 91.7~91.6 | Reserved | 11 |
| Speed and Duplex Ability | 91.5~91.4 | In Auto Negotiation Mode:<br>11: MII Reg0.13=1, 0.8=1, 4.8=1, 4.7=1, 4.6=1, 4.5=1<br>10: MII Reg0.13=1, 0.8=0, 4.8=0, 4.7=1, 4.6=1, 4.5=1<br>01: MII Reg0.13=0, 0.8=1, 4.8=0, 4.7=0, 4.6=1, 4.5=1<br>00: MII Reg0.13=0, 0.8=0, 4.8=0, 4.7=0, 4.6=0, 4.5=1<br>In Force Mode:<br>11: MII Reg0.13=1, 0.8=1, 4.8=1, 4.7=0, 4.6=0, 4.5=0<br>10: MII Reg0.13=1, 0.8=0, 4.8=0, 4.7=1, 4.6=0, 4.5=0<br>01: MII Reg0.13=0, 0.8=1, 4.8=0, 4.7=0, 4.6=1, 4.5=0<br>00: MII Reg0.13=0, 0.8=0, 4.8=0, 4.7=0, 4.6=0, 4.5=1 | 11 |
| Reserved | 91.3 | Reserved | 1 |
| Backpressure Enable | 91.2 | 1: Enable port 6 half duplex backpressure<br>0: Disable port 6 half duplex backpressure | 1 |
| VLAN Tag Insertion and Removal | 91.1~91.0 | 11: Do not insert or remove VLAN tags to/from packet.<br>10: Insert PVID to non-tagged packets.<br>01: Remove tag from tagged packets.<br>00: Replace the VID with a PVID for tagged packets and insert a PVID to non-tagged packets. | 11 |

## 7.4.7. Port 6 Control 1

**Table 56. Port 6 Control 1**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Reserved | 92.7~92.6 | Reserved | 11 |
| Local Loopback | 92.5 | 1: Perform 'local loopback', i.e., loop back MAC's RX back to TX<br>0: Normal operation | 0 |
| Null VID Replacement | 92.4 | 1: The switch will replace a NULL VID with a port VID (12 bits)<br>0: No replacement for a NULL VID | 0 |
| Discard Non PVID Packets | 92.3 | 1: If the received packets are tagged, the switch will discard packets whose VID does not match the ingress port's PVID<br>0: No packets will be dropped | 0 |
| Disable 802.1p Priority | 92.2 | 1: Disable 802.1p priority classification for ingress packets on port 6<br>0: Enable 802.1p priority classification | 1 |
| Disable Diffserv Priority | 92.1 | 1: Disable Diffserv priority classification for ingress packets on port 6<br>0: Enable Diffserv priority classification | 1 |
| Disable Port-Based Priority | 92.0 | 1: Disable port priority function<br>0: Enable port priority function. Ingress packets from port 6 will be classified as high priority | 1 |

## 7.4.8. Port 6 Control 2

**Table 57. Port 6 Control 2**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Reserved | 93.7~93.0 | Reserved | 1111 1000 |

## 7.4.9. Port 6 Control 3

**Table 58. Port 6 Control 3**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Reserved | 94.7~94.4 | Reserved | 1111 |
| Transmission Enable | 94.3 | 1: Enable packet transmission on port 6<br>0: Disable packet transmission on port 6 | 1 |
| Reception Enable | 94.2 | 1: Enable packet reception on port 6<br>0: Disable packet reception on port 6 | 1 |
| Learning Enable | 94.1 | 1: Enable switch address learning capability<br>0: Disable switch address learning capability | 1 |
| Reserved | 94.0 | Reserved | 0 |
| **VLAN Entry [G]** | | | |
| VLAN ID [G] Membership Bit [7:0] | 95.7~95.0 | This register along with byte 96.0 forms a 9-bit field that specifies which ports are members of the VLAN. If a destination address look up fails, packets associated with this VLAN will be forwarded to ports specified in this field. E.g., 1 0000 0001 means port 8 and 0 are in this VLAN. | 0100 0000 |

## 7.4.10. Port 6 Control 4

**Table 59. Port 6 Control 4**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Port 6 VLAN Index [3:0] | 96.7~96.4 | In a port-based VLAN configuration, this register indexes port 6's 'Port VLAN Membership', which may be defined in one of the registers 'VLAN ID [A] Membership' to "VLAN ID [I] Membership". Port 6 can only communicate within the membership. This register also indexes to a default Port VID (PVID) for each port. The PVID is used in tag insertion and filtering if the tagged VID is not the same as the PVID. | 0110 |
| Reserved | 96.3~96.1 | Reserved | 111 |
| VLAN ID [G] Membership Bit [8] | 96.0 | This register along with byte 95.7~95.0 forms a 9-bit field that specifies which ports are members of the VLAN. If a destination address look up fails, packets associated with this VLAN will be forwarded to ports specified in this field. E.g., 1 0000 0001 means port 8 and 0 are in this VLAN. | 1 |
| **VLAN Entry [G]** | | | |
| VLAN ID [G] [7:0] | 97.7~97.0 | This register along with byte 98.3~98.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN G. | 0000 0110 |
| Reserved | 98.7~98.4 | Reserved | 1111 |
| VLAN ID [G] [11:8] | 98.3~98.0 | This register along with byte 97.7~97.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN C. | 0000 |

## 7.4.11. Port 7 Control 0

**Table 60. Port 7 Control 0**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Reserved | 99.7~99.6 | Reserved | 11 |
| Speed and Duplex Ability | 99.5~99.4 | In Auto Negotiation Mode:<br>11: MII Reg0.13=1, 0.8=1, 4.8=1, 4.7=1, 4.6=1, 4.5=1<br>10: MII Reg0.13=1, 0.8=0, 4.8=0, 4.7=1, 4.6=1, 4.5=1<br>01: MII Reg0.13=0, 0.8=1, 4.8=0, 4.7=0, 4.6=1, 4.5=1<br>00: MII Reg0.13=0, 0.8=0, 4.8=0, 4.7=0, 4.6=0, 4.5=1<br>In Force Mode:<br>11: MII Reg0.13=1, 0.8=1, 4.8=1, 4.7=0, 4.6=0, 4.5=0<br>10: MII Reg0.13=1, 0.8=0, 4.8=0, 4.7=1, 4.6=0, 4.5=0<br>01: MII Reg0.13=0, 0.8=1, 4.8=0, 4.7=0, 4.6=1, 4.5=0<br>00: MII Reg0.13=0, 0.8=0, 4.8=0, 4.7=0, 4.6=0, 4.5=1 | 11 |
| Reserved | 99.3 | Reserved | 1 |
| Backpressure Enable | 99.2 | 1: Enable port 7 half duplex backpressure<br>0: Disable port 7 half duplex backpressure | 1 |
| VLAN Tag Insertion and Removal | 99.1~99.0 | 11: Do not insert or remove VLAN tags to/from packet.<br>10: Insert PVID to non-tagged packets.<br>01: Remove tag from tagged packets.<br>00: Replace the VID with a PVID for tagged packets and insert a PVID to non-tagged packets. | 11 |

## 7.4.12. Port 7 Control 1

**Table 61. Port 7 Control 1**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Reserved | 100.7~100.6 | Reserved | 11 |
| Local Loopback | 100.5 | 1: Perform ‘local loopback’, i.e. loop back MAC’s RX back to TX<br>0: Normal operation | 0 |
| Null VID Replacement | 100.4 | 1: The switch will replace a NULL VID with a port VID (12 bits)<br>0: No replacement for a NULL VID | 0 |
| Discard Non PVID Packets | 100.3 | 1: If the received packets are tagged, the switch will discard packets whose VID does not match ingress port’s PVID<br>0: No packets will be dropped | 0 |
| Disable 802.1p Priority | 100.2 | 1: Disable 802.1p priority classification for ingress packets on port 7<br>0: Enable 802.1p priority classification | 1 |
| Disable Diffserv Priority | 100.1 | 1: Disable Diffserv priority classification for ingress packets on port 7<br>0: Enable Diffserv priority classification | 1 |
| Disable Port-Based Priority | 100.0 | 1: Disable port priority function<br>0: Enable port priority function. Ingress packets from port 7 will be classified as high priority | 1 |

## 7.4.13. Port 7 Control 2

**Table 62. Port 7 Control 2**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Reserved | 101.7~101.0 | Reserved | 1111 1000 |

## 7.4.14. Port 7 Control 3

**Table 63. Port 7 Control 3**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Reserved | 102.7~102.4 | Reserved | 1111 |
| Transmission Enable | 102.3 | 1: Enable packet transmission on port 7<br>0: Disable packet transmission on port 7 | 1 |
| Reception Enable | 102.2 | 1: Enable packet reception on port 7<br>0: Disable packet reception on port 7 | 1 |
| Learning Enable | 102.1 | 1: Enable switch address learning capability<br>0: Disable switch address learning capability | 1 |
| Reserved | 102.0 | Reserved | 1 |
| **VLAN Entry [H]** | | | |
| VLAN ID [H] Membership Bit [7:0] | 103.7~103.0 | This register along with byte 104.0 forms a 9-bit field that specifies which ports are members of the VLAN. If a destination address look up fails, packets associated with this VLAN will be forwarded to ports specified in this field. E.g., 1 0000 0001 means port 8 and 0 are in this VLAN. | 1000 0000 |

## 7.4.15. Port 7 Control 4

**Table 64. Port 7 Control 4**

| Name | Byte.bit | Description | Default |
|---|---|---|---|
| Port 7 VLAN Index [3:0] | 104.7~104.4 | In a port-based VLAN configuration, this register indexes port 7's 'Port VLAN Membership', which may be defined in one of the registers 'VLAN ID [A] Membership' to 'VLAN ID [I] Membership'. Port 7 can only communicate within the membership. This register also indexes to a default Port VID (PVID) for each port. The PVID is used in tag insertion and filtering if the tagged VID is not the same as the PVID. | 0111 |
| Reserved | 104.3~104.1 | Reserved | 111 |
| VLAN ID [H] Membership Bit [8] | 104.0 | This register along with byte 103.7~103.0 forms a 9-bit field that specifies which ports are members of the VLAN. If a destination address look up fails, packets associated with this VLAN will be forwarded to ports specified in this field. E.g., 1 0000 0001 means port 8 and 0 are in this VLAN. | 1 |
| **VLAN Entry [H]** | | | |
| VLAN ID [H] [7:0] | 105.7~105.0 | This register along with byte 106.3~106.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN H. | 0000 0111 |
| Reserved | 106.7~106.4 | Reserved | 1111 |
| VLAN ID [H] [11:8] | 106.3~106.0 | This register along with byte 105.7~105.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN H. | 0000 |

# 8. PHY Registers Description

Mode codes used in the following tables:

RO: Read Only

RW: Read/Write

SC: Self Clearing

LH: Latch High Until Clear

LL: Latch Low Until Clear

## *8.1. PHY 0 Registers*

### 8.1.1. PHY 0 Register 0: Control

PHY address (Port 0 ~ port 7) = 0x0 ~ 0x7. PHY address (MII port) = 0x8

**Table 65. PHY 0 Register 0: Control**

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 0.15 | Reset | RW/SC | 1: PHY reset. This bit is self-clearing. | 0 |
| 0.14 | Loopback (digital loopback) | RW | 1: Enable loopback. This will loopback TXD to RXD and ignore all activity on the cable media<br>0: Normal operation | 0 |
| 0.13 | Speed Select | RW | 1: 100Mbps<br>0: 10Mbps<br>When NWay is enabled, this bit reflects the result of auto-negotiation (Read only).<br>When NWay is disabled, this bit is strap option 'Force_Speed' and can be configured through SMI (Read/Write). | 1 |
| 0.12 | Auto Negotiation Enable | RW | 1: Enable auto-negotiation process<br>0: Disable auto-negotiation process<br>This bit can be set through SMI (Read/Write). | Pin En_ANEG strap option |
| 0.11 | Power Down | RW | 1: Power down. All functions will be disabled except SMI function<br>0: Normal operation | 0 |
| 0.10 | Isolate | RW | 1: Electrically isolates the PHY from RMII/SMII. PHY is still able to respond to MDC/MDIO<br>0: Normal operation | 0 |
| 0.9 | Restart Auto Negotiation | RW/SC | 1: Restart Auto-Negotiation process<br>0: Normal operation | 0 |
| 0.8 | Duplex Mode | RW | 1: Full duplex operation<br>0: Half duplex operation<br>When NWay is enabled, this bit reflects the result of auto-negotiation (Read only).<br>When NWay is disabled, this bit is strap option 'Force_Duplex' and can be configured through SMI (Read/Write). | 1 |
| 0.[7:0] | Reserved | - | Reserved | 0 |

## 8.1.2. PHY 0 Register 1: Status

**Table 66. PHY 0 Register 1: Status**

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 1.15 | 100Base_T4 | RO | 0: No 100Base-T4 capability | 0 |
| 1.14 | 100Base_TX_FD | RO | 1: 100Base-TX full duplex capable<br>0: Not 100Base-TX full duplex capable | 1 |
| 1.13 | 100Base_TX_HD | RO | 1: 100Base-TX half duplex capable<br>0: Not 100Base-TX half duplex capable | 1 |
| 1.12 | 10Base_T_FD | RO | 1: 10Base-TX full duplex capable<br>0: Not 10Base-TX full duplex capable | 1 |
| 1.11 | 10Base_T_HD | RO | 1: 10Base-TX half duplex capable<br>0: Not 10Base-TX half duplex capable | 1 |
| 1.[10:7] | Reserved | RO | Reserved | 0 |
| 1.6 | MF Preamble Suppression | RO | The RTL8309G will accept management frames with preamble suppressed.<br>The RTL8309G accepts management frames without preamble. 32 minimum preamble bits are required for the first SMI read/write transaction after reset. One idle bit is required between any two management transactions as defined in the IEEE 802.3u specifications. | 1 |
| 1.5 | Auto-Negotiate Complete | RO | 1: Auto-negotiation process completed. MII Reg.4, 5 are valid if this bit is set<br>0: Auto-negotiation process not completed | 0 |
| 1.4 | Remote Fault | RO/LH | 1: Remote fault condition detected<br>0: No remote fault | 0 |
| 1.3 | Auto-Negotiation Ability | RO | 1: NWay auto-negotiation capable (permanently=1) | 1 |
| 1.2 | Link Status | RO/LL | 1: Link is established. If the link fails, this bit will be 0 until after reading this bit again<br>0: Link has failed | 0 |
| 1.1 | Jabber Detect | RO/LH | 1: Jabber detect enabled<br>0: Jabber detect disabled<br>The jabber function is disabled in 100Base-TX operation. Jabber occurs when a predefined excessively long packet is detected for 10Base-T. When the duration of TXEN exceeds the jabber timer (21ms), the transmission and loopback function are disabled and the COL LED starts blinking. After TXEN goes low for more than 500 ms, the transmitter will be re-enabled and the COL LED will stop blinking. Jabber detect is supported only in 10Base-T operation. | 0 |
| 1.0 | Extended Capability | RO | 1: Extended register capable (permanently=1) | 1 |

### 8.1.3. PHY 0 Register 4: Auto-Negotiation Advertisement

*Note: Whenever the link ability of the RTL8309G is reconfigured, the auto-negotiation process should be executed again to allow the configuration to take effect.*

**Table 67. PHY 0 Register 4: Auto-Negotiation Advertisement**

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 4.15 | Next Page | RO | 0: Next Page disabled (Permanently=0) | 0 |
| 4.14 | Acknowledge | RO | Permanently=0. | 0 |
| 4.13 | Remote Fault | RW | 1: Advertises that the RTL8309G has detected a remote fault<br>0: No remote fault detected | 0 |
| 4.[12:11] | Reserved | RO | Reserved | 0 |
| 4.10 | Pause | RW | 1: Advertises that the RTL8309G possesses 802.3x flow control capability<br>0: No flow control capability | Pin En_FCTRL strap option |
| 4.9 | 100Base-T4 | RO | Technology not supported (Permanently=0). | 0 |
| 4.8 | 100Base-TX-FD | RW | 1: 100Base-TX full duplex capable<br>0: Not 100Base-TX full duplex capable | 1 |
| 4.7 | 100Base-TX | RW | 1: 100Base-TX half duplex capable<br>0: Not 100Base-TX half duplex capable | 1 |
| 4.6 | 10Base-T-FD | RW | 1: 10Base-TX full duplex capable<br>0: Not 10Base-TX full duplex capable | 1 |
| 4.5 | 10Base-T | RW | 1: 10Base-TX half duplex capable<br>0: Not 10Base-TX half duplex capable | 1 |
| 4.[4:0] | Selector Field | RO | [00001]=IEEE 802.3. | 00001 |

## 8.1.4. PHY 0 Register 5: Auto-Negotiation Link Partner Ability

**Table 68. PHY 0 Register 5: Auto-Negotiation Link Partner Ability**

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 5.15 | Next Page | RO | 1: Link partner desires Next Page transfer<br>0: Link partner does not desire Next Page transfer | 0 |
| 5.14 | Acknowledge | RO | 1: Link Partner acknowledges reception of Fast Link Pulse (FLP) words<br>0: Not acknowledged by Link Partner | 0 |
| 5.13 | Remote Fault | RO | 1: Remote Fault indicated by Link Partner<br>0: No remote fault indicated by Link Partner | 0 |
| 5.[12:11] | Reserved | RO | Reserved | 0 |
| 5.10 | Pause | RO | 1: Flow control supported by Link Partner<br>0: Flow control not supported by Link Partner | 0 |
| 5.9 | 100Base-T4 | RO | 1: 100Base-T4 supported by Link Partner<br>0: 100Base-T4 not supported by Link Partner | 0 |
| 5.8 | 100Base-TX-FD | RO | 1: 100Base-TX full duplex supported by Link Partner<br>0: 100Base-TX full duplex not supported by Link Partner<br>Note: If auto negotiation is disabled and this bit is set, Reg0.13 and Reg0.8 will be set to 1 after link is established. | 0 |
| 5.7 | 100Base-TX | RO | 1: 100Base-TX half duplex supported by Link Partner<br>0: 100Base-TX half duplex not supported by Link Partner<br>Note: If auto negotiation is disabled and this bit is set, Reg0.13 will be set to 1 and Reg0.8 will be set to 0 after link is established. | 0 |
| 5.6 | 10Base-T-FD | RO | 1: 10Base-TX full duplex supported by Link Partner<br>0: 10Base-TX full duplex not supported by Link Partner<br>Note: If auto negotiation is disabled and this bit is set, Reg0.13 will be set to 0 and Reg0.8 will be set to 1 after link is established. | 0 |
| 5.5 | 10Base-T | RO | 1: 10Base-TX half duplex supported by Link Partner<br>0: 10Base-TX half duplex not supported by Link Partner<br>Note: If auto negotiation is disabled and this bit is set, Reg0.13 and Reg0.8 will be set to 0 after a link is established. | 0 |
| 5.[4:0] | Selector Field | RO | [00001]=IEEE802.3. | 00001 |

## 8.1.5. PHY 0 Register 16: Global Control 0

**Table 69. PHY 0 Register 16: Global Control 0**

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 16.[15:13] | LED Mode | RW | 111: Mode 7: Speed, Duplex+Collision, Link+Act, SQI<br>110: Mode 6: Activity, Speed, Link, SQI<br>101: Mode 5: Speed, Duplex, Link+Act, Bi-color Link+ActSpeed, Duplex, Link+Act, SQI<br>100: Mode 4: Collision, Duplex, Link+Act+Speed, SQI<br>011: Mode 3: SQI, Duplex+Collision, Link+Act+Speed,10/100.<br>010: Mode 2: RxAct+10/100, TxAct+10/100, Link, SQI<br>001: Mode 1: Duplex+Collision, 10Link+Act, 100Link+Act, SQI<br>000: Mode 0: Duplex+Collision, Bi-color Speed, Bi-color Link+Act, SQI. | 111 |
| 16.12 | Software Reset | RW/ SC | 1: Soft reset. This bit is self-clearing<br>If this bit is set to 1, the RTL8309G will reset all registers in it except PHY registers and will not load configurations from EEPROM or strapping pins. Software reset is designed to provide a convenient way for users to change the configuration via SMI. After changing register values in the RTL8309G (except PHY registers) via SMI, the external device must execute a soft reset in order to update the configuration by setting this bit to 1. | 0 |
| 16.11 | Disable VLAN | RW | 1: Disable VLAN<br>0: Enable VLAN. The default VLAN membership configuration by internal register is MII port overlapped with all the other ports to form 8 individual VLANs. This default membership configuration may be modified by setting internal registers via the SMI interface or EEPROM. | 1 |
| 16.10 | Disable 802.1Q Tag Aware VLAN | RW | 1: Disable 802.1Q tagged-VID Aware function. The RTL8309G will not check the tagged VID on received frames to perform tagged-VID VLAN mapping. Under this configuration, the RTL8309G only uses the per port VLAN index register to perform Port-Based VLAN mapping<br>0: Enable the Member Set Filtering function of VLAN Ingress Rule. The RTL8309G checks the tagged VID on received frames with the VIDA[11:0]~VIDH[11:0] to index to a member set, then performs VLAN mapping. The RTL8309G uses tagged-VID VLAN mapping for tagged frames but still uses port-based VLAN mapping for priority-tagged and untagged frames | 0 |
| 16.9 | Disable VLAN Member Set Ingress Filtering | RW | 1: The switch will not drop a received frame if the ingress port of this packet is not included in the matched VLAN member set. It will still forward the packet to the VLAN members specified in the matched member set. This setting works on both port-based and tag-based VLAN configurations<br>0: The switch will drop the received frame if the ingress port of this packet is not included in the matched VLAN member set | 1 |
| 16.8 | Disable VLAN Tag Admit Control | RW | 1: The switch accepts all frames it receives whether tagged or untagged<br>0: The switch will only accept tagged frames and will drop untagged frames | 1 |

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 16.7 | EEPROM Existence | RO | 1: EEPROM does not exist (pin EnEEPROM=0 or pin EnEEPROM=1 but EEPROM does not exist)<br>0: EEPROM exists (pin EnEEPROM=1 and EEPROM exists) | 0 |
| 16.6 | Accept Error Disable | RW | 1: Filter bad packets in normal operation<br>0: Switch all packets including bad ones. This bit is intended for debugging purposes only | 1 |
| 16.5 | IEEE 802.3x Transmit Flow Control Enable | RW | 1: Determines when to invoke flow control based on auto negotiation results<br>0: Will not enable transmit flow control no matter what the auto negotiation result is | 1 |
| 16.4 | IEEE 802.3x Receive Flow Control Enable | RW | 1: When the RTL8309G receives a pause control frame, it has the ability to stop the next transmission of a normal frame until the timer is expired based on the auto negotiation result<br>0: Will not receive flow control no matter what the auto negotiation result is | 1 |
| 16.3 | Broadcast Input or Output Drop | RW | 1: Broadcast input drop is selected<br>0: Broadcast output drop is selected | 1 |
| 16.2 | Aging Enable | RW | 1: Enable aging function<br>0: Disable aging function. The addresses learned in the lookup table will not be aged out. If the table is full, the last entry in the table will be deleted to make room for the new entry | 1 |
| 16.1 | Fast Aging Enable | RW | 1: Enable fast aging function. The entry learned in the lookup table will be aged out if it is not updated within an 800µs period<br>0: Disable fast aging function | 0 |
| 16.0 | Enable ISP MAC Address Translation | RW | 1: Enable ISP MAC Address Translation function<br>0: Disable ISP MAC Address Translation function | 0 |

## 8.1.6. PHY 0 Register 17: Global Control 1

**Table 70. PHY 0 Register 17: Global Control 1**

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 17.[15:13] | 802.1p Base Priority | RW | Classifies priority for incoming 802.1Q packets, if 802.1p priority classification is enabled. 'User priority' is compared against this value.<br>≥: Classify as high priority<br><: Classify as low priority | 100 |
| 17.12 | Trunking Port Assignment | RW | 1: Combine port 0 and 1 as one trunking port, if trunking is enabled via strapping pin 'Dis_Trunk'<br>0: Combine port 6 and 7 as one trunking port, if trunking is enabled via strapping pin 'Dis_Trunk' | 1 |
| 17.[11:10] | Queue Weight | RW | The frame service ratio between the high priority queue and low priority queue is:<br>11: 16:1 10: Always high priority queue first<br>01: 8:1 00: 4:1 | 11 |

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 17.9 | Disable IP Priority for IP Address [A] | RW | 1: Compare both the source and destination IP address of incoming packets against the value, IP address [A] AND IP mask [A], to classify packet priority<br>0: Do not compare the source or destination IP address of incoming packets against the value 'IP address [A] AND IP mask [A]' | 0 |
| 17.8 | Disable IP Priority for IP Address [B] | RW | 1: Compare both the source and destination IP address of incoming packets against the value, IP address [B] AND IP mask [B], to classify packet priority<br>0: Do not compare the source or destination IP address of incoming packets against the value 'IP address [B] AND IP mask [B]' | 0 |
| 17.[7:0] | Reserved | - | Reserved | 00000000 |

## 8.1.7. PHY 0 Register 18: Global Control 2

**Table 71. PHY 0 Register 18: Global Control 2**

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 18.15 | Enable Differential Service Code Point [A] | RW | 1: If differential service priority is enabled, this bit specifies differential service code point [A] is high priority<br>0: If differential service priority is enabled, this bit specifies differential services code point [A] is low priority | 0 |
| 18.14 | Reserved | - | Reserved | 1 |
| 18.[13:8] | Differential Service Code Point [A] | RW | Used to specify the high priority differential service code point A. For example, if these bits are set to 111111, incoming packets with a TOS field equal to 111111 will be considered high priority packets. | 111111 |
| 18.7 | Enable Differential Service Code Point [B] | RW | 1: If differential service priority is enabled, this bit specifies differential services code point [B] is high priority<br>0: If differential service priority is enabled, this bit specifies differential services code point [B] is low priority | 0 |
| 18.6 | Reserved | - | Reserved | 1 |
| 18.[5:0] | Differential Service Code Point [B] | RW | Used to specify a high priority differential service code point B. For example, if these bits are set to 000000, incoming packets with a TOS field equal to 000000 will be considered high priority packets. | 111111 |

## 8.1.8. PHY 0 Register 19: Global Control 3

**Table 72. PHY 0 Register 19: Global Control 3**

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 19.15 | Enable Drop for 48 Pass 1 | RW | 1: Enable drop packet after SRAM full for 48 pass 1<br>0: Disable drop packet after SRAM full for 48 pass 1. This will result in SRAM run out | 1 |
| 19.14 | Reserved | - | Reserved | 1 |
| 19.13 | TX IPG Compensation | RW | 1: 90ppm TX IPG (InterPacket Gap) compensation<br>0: 65ppm TX IPG (InterPacket Gap) compensation | 1 |
| 19.12 | Disable Loop Detection | RW | 1: Disable loop detection function<br>0: Enable loop detection function | 1 |
| 19.11 | Lookup Table Accessible Enable | RW | 1: Lookup table is accessible via indirect access registers<br>0: Lookup table is not accessible | 0 |
| 19.10 | Reserved | - | Reserved | 1 |
| 19.[9:0] | Reserved | - | Reserved | 11 1100 0001 |

## 8.1.9. PHY 0 Register 22: Port 0 Control 0

**Table 73. PHY 0 Register 22: Port 0 Control 0**

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 22.[15:14] | Reserved | RW | Reserved. | 11 |
| 22.13 | Local Loopback | RW | 1: Perform ‘local loopback’, i.e., loop MAC’s RX back to TX<br>0: Normal operation | 0 |
| 22.12 | Null VID Replacement | RW | 1: The switch will replace a NULL VID with a port VID (12 bits)<br>0: No replacement for a NULL VID | 0 |
| 22.11 | Discard Non PVID Packets | RW | 1: If the received packets are tagged, the switch will discard packets with a VID that does not match the ingress port default VID, which is indexed by port 0’s ‘Port-based VLAN index’<br>0: No packets will be dropped | 0 |
| 22.10 | Disable 802.1p Priority | RW | 1: Disable 802.1p priority classification for ingress packets on port 0<br>0: Enable 802.1p priority classification | Pin Dis_VLAN_Pri strap option<br>Default = 1 |
| 22.9 | Disable Diffserv Priority | RW | 1: Disable Diffserv priority classification for ingress packets on port 0<br>0: Enable Diffserv priority classification | Pin Dis_DS_Pri strap option<br>Default = 1 |
| 22.8 | Disable Port-Based Priority | RW | 1: Disable port priority function<br>0: Enable port priority function. Ingress packets from port 0 will be classified as high priority | Pin Sel_Port_Pri strap option<br>Default = 1 |
| 22.[7:2] | Reserved | RW | Reserved | 1111111 |

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 22.[1:0] | VLAN Tag Insertion and Removal | RW | 11: Do not insert or remove VLAN tags to/from packets sent out from this port.<br>10: The switch will add VLAN tags to packets if they are not tagged. The switch will not add tags to packets already tagged. The inserted tag is the ingress port's 'Default tag', which is indexed by port 0's 'Port-based VLAN index'.<br>01: The switch will remove VLAN tags from packets, if they are tagged when these packets are send out from port 0. The switch will not modify packets received without tags.<br>00: The switch will remove VLAN tags from packets then add new tags to them. The inserted tag is the ingress port's 'Default tag', which is indexed by port 0's 'Port-based VLAN index'. This is a replacement processing for tagged packets and an insertion for untagged packets. | 11 |

## 8.1.10. PHY 0 Register 23: Port 0 Control 1

**Table 74. PHY 0 Register 23: Port 0 Control 1**

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 23.[15:12] | Reserved | - | Reserved | 1111 |
| 23.11 | Transmission Enable | RW | 1: Enable packet transmission on port 0<br>0: Disable packet transmission on port 0 | 1 |
| 23.10 | Reception Enable | RW | 1: Enable packet reception on port 0<br>0: Disable packet reception on port 0 | 1 |
| 23.9 | Learning Enable | RW | 1: Enable switch address learning capability<br>0: Disable switch address learning capability | 1 |
| 23.8 | Loop Status | RO | 1: A loop has been detected on port 0<br>0: No loop exists on port 0 | 0 |
| 23.[7:4] | Link Quality | RO | 4-bit field indicating the link quality of the receive twisted-pair or fiber link.<br>0000: Highest link quality<br>1111: Lowest link quality | - |
| 23.[3:0] | Reserved | - | Reserved | 1000 |

## 8.1.11. PHY 0 Register 24: Port 0 Control 2 & VLAN Entry [A]

**Table 75. PHY 0 Register 24: Port 0 Control 2 & VLAN Entry [A]**

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 24.[15:12] | Port 0 VLAN Index [3:0] | - | In a port-based VLAN configuration, this register indexes port 0's 'Port VLAN Membership', which can be defined in one of the registers 'VLAN ID [A] Membership' to 'VLAN ID [I] Membership'. Port 0 can only communicate within the membership. This register also indexes to a default Port VID (PVID) for each port. The PVID is used in tag insertion and filtering if the tagged VID is not the same as the PVID. | 0000 |
| 24.[11~9] | Reserved | - | Reserved | 111 |
| 24.[8:0] | VLAN ID [A] Membership Bit [8:0] | RW | This 9-bit field specifies which ports are members of VLAN A. If a destination address look up fails, the packet associated with this VLAN will be broadcast to ports specified in this field. Bit 0 stands for port 0, bit 1 stands for port 8.<br>E.g., 1 0000 0001 means port 8 and 0 are in this VLAN. | 1<br>0000<br>0001 |

## 8.1.12. PHY 0 Register 25: VLAN Entry [A]

**Table 76. PHY 0 Register 25: VLAN Entry [A]**

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 25.[15:12] | Reserved | - | Reserved | 1111 |
| 25.[11:0] | VLAN ID [A] | RW | Defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN A. | 0000<br>0000<br>0000 |

# 8.2. PHY 1 Registers

## 8.2.1. PHY 1 Register 0: Control

This register has the same definition as PHY 0 Register 0: Control, page 49.

## 8.2.2. PHY 1 Register 1: Status

This register has the same definition as PHY 0 Register 1: Status, page 50.

## 8.2.3. PHY 1 Register 4: Auto-Negotiation Advertisement

This register has the same definition as PHY 0 Register 4: Auto-Negotiation Advertisement, page 51.

## 8.2.4. PHY 1 Register 5: Auto-Negotiation Link Partner Ability

This register has the same definition as PHY 0 Register 5: Auto-Negotiation Link Partner Ability, page 52.

## 8.2.5. PHY 1 Register 16~17: IP Priority Address [A]

**Table 77. PHY 1 Register 16~17: IP Priority Address [A]**

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 16 | IP Address [A] [31:16] | RW | The switch will compare both the source and destination IP addresses of an incoming packet against the value, IP address [A] AND IP mask [A], to classify priority for the packet. | 0xFFFF |
| 17 | IP Address [A] [15:0] | RW | The switch will both compare the source and destination IP addresses of an incoming packet against the value, IP address [A] AND IP mask [A], to classify priority for the packet. | 0xFFFF |

## 8.2.6. PHY 1 Register 18~19: IP Priority Address [B]

**Table 78. PHY 1 Register 18~19: IP Priority Address [B]**

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 18 | IP Address [B] [31:16] | RW | The switch will compare both the source and destination IP addresses of an incoming packet against the value, IP address [B] AND IP mask [B], to classify priority for the packet, if IP priority for IP address [B] is enabled. | 0xFFFF |

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 19 | IP Address [B] [15:0] | RW | The switch will compare both the source and destination IP addresses of an incoming packet against the value, IP address [B] AND IP mask [B], to classify priority for the packet, if IP priority for IP address [B] is enabled. | 0xFFFF |

## 8.2.7. PHY 1 Register 22: Port 1 Control 0

This register has the same definition as PHY 0 Register 22: Port 0 Control 0, page 56.

*Note: Reg 22.8 is not pin Sel_PortPri strap option for port 1. Default value for 22.8 is 1.*

## 8.2.8. PHY 1 Register 23: Port 1 Control 1

This register has the same definition as PHY 0 Register 23: Port 0 Control 1, page 57.

## 8.2.9. PHY 1 Register 24: Port 1 Control 2 & VLAN Entry [B]

**Table 79. PHY 1 Register 24: Port 1 Control 2 & VLAN Entry [B]**

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 24.[15~12] | Port 1 VLAN Index [3:0] | RW | In a port-based VLAN configuration, this register indexes port 1's 'Port VLAN Membership', which could be defined in one of the registers 'VLAN ID [A] Membership' to 'VLAN ID [I] Membership'. Port 1 can only communicate within the membership. This register also indexes to a default Port VID (PVID) for each port. The PVID is used in tag insertion and filtering if the tagged VID is not the same as the PVID. | 0001 |
| 24.[11:9] | Reserved | - | Reserved | 111 |
| 24.[8:0] | VLAN ID [B] Membership Bit [8:0] | RW | This 9-bit field specifies which ports are members of VLAN B. If a destination address look up fails, packets associated with this VLAN will be forwarded to ports specified in this field. E.g., 1 0000 0001 means port 8 and 0 are in this VLAN. | 1<br>0000<br>0010 |

## 8.2.10. PHY 1 Register 25: VLAN Entry [B]

**Table 80. PHY 1 Register 25: VLAN Entry [B]**

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 25.[15:12] | Reserved | - | Reserved | 1111 |
| 25.[11:0] | VLAN ID [B] | RW | Defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN B. | 0000<br>0000<br>0001 |

## 8.3. PHY 2 Registers

### 8.3.1. PHY 2 Register 0: Control

This register has the same definition as PHY 0 Register 0: Control, page 49.

### 8.3.2. PHY 2 Register 1: Status

This register has the same definition as PHY 0 Register 1: Status, page 50.

### 8.3.3. PHY 2 Register 4: Auto-Negotiation Advertisement

This register has the same definition as PHY 0 Register 4: Auto-Negotiation Advertisement, page 51.

### 8.3.4. PHY 2 Register 5: Auto-Negotiation Link Partner Ability

This register has the same definition as PHY 0 Register 5: Auto-Negotiation Link Partner Ability, page 52.

### 8.3.5. PHY 2 Register 16~17: IP Priority Mask [A]

**Table 81. PHY 2 Register 16~17: IP Priority Mask [A]**

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 16 | IP Mask [A] [31:16] | RW | The switch will compare both the source and destination IP addresses of an incoming packet against the value, IP address [A] AND IP mask [A], to classify priority for the packet. | 0xFFFF |
| 17 | IP Mask [A] [15:0] | RW | The switch will compare both the source and destination IP addresses of an incoming packet against the value, IP address [A] AND IP mask [A], to classify priority for the packet. | 0xFFFF |

### 8.3.6. PHY 2 Register 18~19: IP Priority Mask [B]

**Table 82. PHY 2 Register 18~19: IP Priority Mask [B]**

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 18 | IP Mask [B] [31:16] | RW | The switch will compare both the source and destination IP addresses of an incoming packet against the value, IP address [B] AND IP mask [B], to classify priority for the packet, if IP priority for IP address [B] is enabled. | 0xFFFF |

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 19 | IP Mask [B] [15:0] | RW | The switch will compare both the source and destination IP addresses of an incoming packet against the value, IP address [B] AND IP mask [B], to classify priority for the packet, if IP priority for IP address [B] is enabled. | 0xFFFF |

## 8.3.7. PHY 2 Register 22: Port 2 Control 0

This register has the same definition as PHY 0 Register 22: Port 0 Control 0, page 56.

*Note: Reg 22.8 is pin Sel_PortPri strap option for port 2. Default value for 22.8 is 1.*

## 8.3.8. PHY 2 Register 23: Port 2 Control 1

This register has the same definition as PHY 0 Register 23: Port 0 Control 1, page 57.

## 8.3.9. PHY 2 Register 24: Port 2 Control 2 & VLAN Entry [C]

**Table 83. PHY 2 Register 24: Port 2 Control 2 & VLAN Entry [C]**

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 24.[15:12] | Port 2 VLAN Index [3:0] | RW | In a port-based VLAN configuration, this register indexes port 2's 'Port VLAN Membership', which can be defined in one of the registers 'VLAN ID [A] Membership' to 'VLAN ID [I] Membership'. Port 2 can only communicate within the membership. This register also indexes to a default Port VID (PVID) for each port. The PVID is used in tag insertion and filtering if the tagged VID is not the same as the PVID. | 0010 |
| 24.[11~9] | Reserved | - | Reserved | 111 |
| 24.[8:0] | VLAN ID [C] Membership Bit [8:0] | RW | This 9-bit field specifies which ports are members of VLAN C. If a destination address look up fails, packets associated with this VLAN will be forwarded to ports specified in this field. E.g., 1 0000 0001 means port 8 and 0 are in this VLAN. | 1<br>0000<br>0100 |

## 8.3.10. PHY 2 Register 25: VLAN Entry [C]

**Table 84. PHY 2 Register 25: VLAN Entry [C]**

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 25.[15:12] | Reserved | - | Reserved | 1111 |
| 25.[11:0] | VLAN ID [C] | RW | Defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN C. | 0000<br>0000<br>0010 |

## 8.4. PHY 3 Registers

### 8.4.1. PHY 3 Register 0: Control

This register has the same definition as PHY 0 Register 0: Control, page 49.

### 8.4.2. PHY 3 Register 1: Status

This register has the same definition as PHY 0 Register 1: Status, page 50.

### 8.4.3. PHY 3 Register 4: Auto-Negotiation Advertisement

This register has the same definition as PHY 0 Register 4: Auto-Negotiation Advertisement, page 51.

### 8.4.4. PHY 3 Register 5: Auto-Negotiation Link Partner Ability

This register has the same definition as PHY 0 Register 5: Auto-Negotiation Link Partner Ability, page 52.

### 8.4.5. PHY 3 Register 16~18: Switch MAC Address

The Switch MAC address is used as the source address in MAC pause control frames.

**Table 85. PHY 3 Register 16~18: Switch MAC Address**

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 16 | Switch MAC Address [47:32] | RW | 16.[15:8] = Switch MAC Address Byte 4.<br>16.[7:0] = Switch MAC Address Byte 5. | 0x5452 |
| 17 | Switch MAC Address [31:16] | RW | 17.[15:8] = Switch MAC Address Byte 2.<br>17.[7:0] = Switch MAC Address Byte 3. | 0x834C |
| 18 | Switch MAC Address [15:0] | RW | 18.[15:8] = Switch MAC Address Byte 0.<br>18.[7:0] = Switch MAC Address Byte 1. | 0xB009 |

### 8.4.6. PHY 3 Register 22: Port 3 Control 0

This register has the same definition as PHY 0 Register 22: Port 0 Control 0, page 56.

*Note: Reg 22.8 is pin Sel_PortPri strap option for port 3. Default value for 22.8 is 1.*

## 8.4.7. PHY 3 Register 23: Port 3 Control 1

This register has the same definition as PHY 0 Register 23: Port 0 Control 1, page 57.

## 8.4.8. PHY 3 Register 24: Port 3 Control 2 & VLAN Entry [D]

**Table 86. PHY 3 Register 24: Port 3 Control 2 & VLAN Entry [D]**

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 24.[15:12] | Port 3 VLAN Index [3:0] | RW | In a port-based VLAN configuration, this register indexes port 3's 'Port VLAN Membership', which may be defined in one of the registers 'VLAN ID [A] Membership' to 'VLAN ID [I] Membership'. Port 3 can only communicate within the membership. This register also indexes to a default Port VID (PVID) for each port. The PVID is used in tag insertion and filtering if the tagged VID is not the same as the PVID. | 0011 |
| 24.[11~9] | Reserved | - | Reserved | 111 |
| 24.[8:0] | VLAN ID [D] Membership Bit [8:0] | RW | This 9-bit field specifies which ports are members of VLAN D. If a destination address look up fails, packets associated with this VLAN will be forwarded to ports specified in this field. E.g., 1 0000 0001 means port 8 and 0 are in this VLAN. | 1 0000 1000 |

## 8.4.9. PHY 3 Register 25: VLAN Entry [D]

**Table 87. PHY 3 Register 25: VLAN Entry [D]**

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 25.[15:12] | Reserved | - | Reserved | 1111 |
| 25.[11:0] | VLAN ID [D] | RW | Defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN D. | 0000 0000 0011 |

## 8.5. PHY 4 Registers

### 8.5.1. PHY 4 Register 0: Control

This register has the same definition as PHY 0 Register 0: Control, page 49.

### 8.5.2. PHY 4 Register 1: Status

This register has the same definition as PHY 0 Register 1: Status, page 50.

### 8.5.3. PHY 4 Register 4: Auto-Negotiation Advertisement

This register has the same definition as PHY 0 Register 4: Auto-Negotiation Advertisement, page 51.

### 8.5.4. PHY 4 Register 5: Auto-Negotiation Link Partner Ability

This register has the same definition as PHY 0 Register 5: Auto-Negotiation Link Partner Ability, page 52.

### 8.5.5. PHY 4 Register 16~18: ISP MAC Address

The ISP's MAC address is used as the source address in MAC address translation functions.

**Table 88. PHY 4 Register 16~18: ISP MAC Address**

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 16 | ISP MAC Address [15:0] | RW | 16.[15:8] = ISP MAC Address Byte 1.<br>16.[7:0] = ISP MAC Address Byte 0. | 0x4205 |
| 17 | ISP MAC Address [31:16] | RW | 17.[15:8] = ISP MAC Address Byte 3.<br>17.[7:0] = ISP MAC Address Byte 2. | 0x212F |
| 18 | ISP MAC Address [47:32] | RW | 18.[15:8] = ISP MAC Address Byte 5.<br>18.[7:0] = ISP MAC Address Byte 4. | 0x5C91 |

### 8.5.6. PHY 4 Register 22: Port 4 Control 0

This register has the same definition as PHY 0 Register 22: Port 0 Control 0, page 56.

*Note: Reg 22.8 is not pin Sel_PortPri strap option for port 4. Default value for 22.8 is 1.*

## 8.5.7. PHY 4 Register 23: Port 4 Control 1

This register has the same definition as PHY 0 Register 23: Port 0 Control 1, page 57.

## 8.5.8. PHY 4 Register 24: Port 4 Control 2 & VLAN Entry [E]

**Table 89. PHY 4 Register 24: Port 4 Control 2 & VLAN Entry [E]**

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 24.[15:12] | Port 4 VLAN Index | RW | In a port-based VLAN configuration, this register indexes port 4's 'Port VLAN Membership', which may be defined in one of the registers 'VLAN ID [A] Membership' to 'VLAN ID [I] Membership'. Port 4 can only communicate within the membership. This register also indexes to a default Port VID (PVID) for each port. The PVID is used in tag insertion and filtering if the tagged VID is not the same as the PVID. | 0100 |
| 24.[11~9] | Reserved | - | Reserved | 111 |
| 24.[8:0] | VLAN ID [E] Membership Bit [8:0] | RW | This 9-bit field specifies which ports are members of VLAN E. If a destination address look up fails, packets associated with this VLAN will be forwarded to ports specified in this field. E.g., 1 0000 0001 means port 8 and 0 are in this VLAN. | 1 0001 0000 |

## 8.5.9. PHY 4 Register 25: VLAN Entry [E]

**Table 90. PHY 4 Register 25: VLAN Entry [E]**

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 25.[15:12] | Reserved | - | Reserved | 1111 |
| 25.[11:0] | VLAN ID [E] | RW | Defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN E. | 0000 0000 0100 |

# 8.6. PHY 5 Registers

## 8.6.1. PHY 5 Register 0: Control

This register has the same definition as PHY 0 Register 0: Control, page 49.

## 8.6.2. PHY 5 Register 1: Status

This register has the same definition as PHY 0 Register 1: Status, page 50.

## 8.6.3. PHY 5 Register 4: Auto-Negotiation Advertisement

This register has the same definition as PHY 0 Register 4: Auto-Negotiation Advertisement, page 51.

## 8.6.4. PHY 5 Register 5: Auto-Negotiation Link Partner Ability

This register has the same definition as PHY 0 Register 5: Auto-Negotiation Link Partner Ability, page 52.

## 8.6.5. PHY 5 Register 16: MII Port Control 0

**Table 91. PHY 5 Register 16: MII Port Control 0**

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 16.15 | Transmission Enable | RW | 1: Enable packet transmission on MII interface<br>0: Disable packet transmission on MII interface | 1 |
| 16.14 | Reception Enable | RW | 1: Enable packet reception on MII interface<br>0: Disable packet reception on MII interface | 1 |
| 16.13 | Learning Enable | RW | 1: Enable switch address learning capability<br>0: Disable switch address learning capability | 1 |
| 16.12 | Reserved | - | Reserved | 0 |
| 16.11 | Disable 802.1p Priority | RW | 1: Disable 802.1p priority classification for ingress packets on port 8<br>0: Enable 802.1p priority classification | Pin Dis_VLAN_Pri strap option<br>Default = 1 |
| 16.10 | Disable Diffserv Priority | RW | 1: Disable Diffserv priority classification for ingress packets on port 8<br>0: Enable Diffserv priority classification | Pin Dis_DS_Pri strap option<br>Default = 1 |
| 16.9 | Disable Port-Based Priority | RW | 1: Disable port priority function<br>0: Enable port priority function. Ingress packets from port 8 will be classified as high priority | Pin Sel_Port_Pri strap option<br>Default = 1 |
| 16.8 | Reserved | - | Reserved | 1 |

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 16.[7:2] | Reserved | - | Reserved | 111111 |
| 16.[1:0] | VLAN Tag Insertion and Removal | RW | 11: Do not insert or remove VLAN tags to/from packets sent out from this port.<br>10: The switch will add VLAN tags to packets if they are not tagged. The switch will not add tags to packets already tagged. The inserted tag is the ingress port's 'Default tag', which is indexed by the MII port's 'Port-based VLAN index'.<br>01: The switch will remove VLAN tags from packets, if they are tagged when these packets are send out from MII port. The switch will not modify packets received without tags.<br>00: The switch will remove VLAN tags from packets then add new tags to them. The inserted tag is the ingress port's 'Default tag', which is indexed by MII port's 'Port-based VLAN index'. This is a replacement processing for tagged packets and an insertion for untagged packets. | 11 |

## 8.6.6. PHY 5 Register 17: MII Port Control 1 & VLAN Entry [I]

**Table 92. PHY 5 Register 17: MII Port Control 1 & VLAN Entry [I]**

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 17.15 | Null VID Replacement | RW | 1: The switch will replace a NULL VID with a port VID (12 bits)<br>0: No replacement for a NULL VID | 0 |
| 17.14 | Discard Non-PVID Packets | RW | 1: If the received packets are tagged, the switch will discard packets with a VID that does not match the ingress port default VID, which is indexed by the MII port's 'Port-based VLAN index'<br>0: No packets will be dropped | 0 |
| 17.13 | Reserved | - | Reserved | 1 |
| 17.[12~9] | Port 8 VLAN Index [3:0] | | In port-based VLAN configuration, this register indexs to port 8's 'Port VLAN Membership', which can be defined in register 'VLAN ID [A] Membership' to 'VLAN ID [I] Membership'. Port 8 can only communicate within the membership. This register also indexes to a default Port VID (PVID) for each port. The PVID is used in tag insertion and filtering if the tagged VID is not the same as the PVID. | 1000 |
| 17.[8:0] | VLAN ID [I] Membership Bit [8:0] | RW | This 9-bit field specifies which ports are members of VLAN I. If a destination address look up fails, packets associated with this VLAN will be forwarded to ports specified in this field. E.g., 1 0000 0001 means port 8 and 0 are in this VLAN. | 1 1111 1111 |

## 8.6.7. PHY 5 Register 18: VLAN Entry [I]

**Table 93. PHY 5 Register 18: VLAN Entry [I]**

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 18.[15:12] | Reserved | - | Reserved | 1111 |
| 18.[11:0] | VLAN ID [I] | RW | Defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN I. | 0000<br>0001<br>0000 |

## 8.6.8. PHY 5 Register 19: CPU Port & WAN Port

**Table 94. PHY 5 Register 19: CPU Port & WAN Port**

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 19.[15:8] | Reserved | - | Reserved | 0xFF |
| 19.[7:4] | WAN Port | RW | Specify the WAN Port on the RTL8309G.<br>1000: MII Port is WAN Port<br>0111: Port 7 is WAN Port 0110: Port 6 is WAN Port<br>0101: Port 5 is WAN Port 0100: Port 4 is WAN Port<br>0011: Port 3 is WAN Port 0010: Port 2 is WAN Port<br>0001: Port 1 is WAN Port 0000: Port 0 is WAN Port | 0111 |
| 19.[3:0] | CPU Port | RW | Specify the CPU Port on the RTL8309G.<br>1000: MII Port is CPU Port<br>0111: Port 7 is CPU Port 0110: Port 6 is CPU Port<br>0101: Port 5 is CPU Port 0100: Port 4 is CPU Port<br>0011: Port 3 is CPU Port 0010: Port 2 is CPU Port<br>0001: Port 1 is CPU Port 0000: Port 0 is CPU Port | 0000 |

## 8.6.9. PHY 5 Register 22: Port 5 Control 0

This register has the same definition as PHY 0 Register 22: Port 0 Control 0, page 56.

*Note: Reg 22.8 is not pin Sel_PortPri strap option for port 5. Default value for 22.8 is 1.*

## 8.6.10. PHY 5 Register 23: Port 5 Control 1

This register has the same definition as PHY 0 Register 23: Port 0 Control 1, page 57.

## 8.6.11. PHY 5 Register 24: Port 5 Control 2 & VLAN Entry [F]

**Table 95. PHY 5 Register 24: Port 5 Control 2 & VLAN Entry [F]**

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 24.[15:12] | Port 5 VLAN Index [3:0] | RW | In a port-based VLAN configuration, this register indexes port 5's 'Port VLAN Membership', which may be defined in one of the registers 'VLAN ID [A] Membership' to 'VLAN ID [I] Membership'. Port 5 can only communicate within the membership. This register also indexes to a default Port VID (PVID) for each port. The PVID is used in tag insertion and filtering if the tagged VID is not the same as the PVID. | 0101 |
| 24.[11~9] | Reserved | - | Reserved | 111 |
| 24.[8:0] | VLAN ID [F] Membership Bit [8:0] | RW | This 9-bit field specifies which ports are members of VLAN F. If a destination address look up fails, packets associated with this VLAN will be forwarded to ports specified in this field. E.g., 1 0000 0001 means port 8 and 0 are in this VLAN. | 1 0010 0000 |

## 8.6.12. PHY 5 Register 25: VLAN Entry [F]

**Table 96. PHY 5 Register 25: VLAN Entry [F]**

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 25.[15:12] | Reserved | - | Reserved | 1111 |
| 25.[11:0] | VLAN ID [F] | RW | Defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN F. | 0000 0000 0101 |

## *8.7. PHY 6 Registers*

### 8.7.1. PHY 6 Register 0: Control

This register has the same definition as PHY 0 Register 0: Control, page 49.

### 8.7.2. PHY 6 Register 1: Status

This register has the same definition as PHY 0 Register 1: Status, page 50.

### 8.7.3. PHY 6 Register 4: Auto-Negotiation Advertisement

This register has the same definition as PHY 0 Register 4: Auto-Negotiation Advertisement, page 51.

### 8.7.4. PHY 6 Register 5: Auto-Negotiation Link Partner Ability

This register has the same definition as PHY 0 Register 5: Auto-Negotiation Link Partner Ability, page 52.

### 8.7.5. PHY 6 Register 22: Port 6 Control 0

This register has the same definition as PHY 0 Register 22: Port 0 Control 0, page 56.

*Note: Reg 22.8 is not pin Sel_PortPri strap option for port 6. Default value for 22.8 is 1.*

### 8.7.6. PHY 6 Register 23: Port 6 Control 1

This register has the same definition as PHY 0 Register 23: Port 0 Control 1, page 57.

## 8.7.7. PHY 6 Register 24: Port 6 Control 2 & VLAN Entry [G]

**Table 97. PHY 6 Register 24: Port 6 Control 2 & VLAN Entry [G]**

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 24.[15:12] | Port 6 VLAN Index [3:0] | RW | In a port-based VLAN configuration, this register indexes port 6's 'Port VLAN Membership', which may be defined in one of the registers 'VLAN ID [A] Membership' to 'VLAN ID [I] Membership'. Port 6 can only communicate within the membership. This register also indexes to a default Port VID (PVID) for each port. The PVID is used in tag insertion and filtering if the tagged VID is not the same as the PVID. | 0110 |
| 24.[11~9] | Reserved | - | Reserved | 111 |
| 24.[8:0] | VLAN ID [G] Membership Bit [8:0] | RW | This 9-bit field specifies which ports are members of VLAN G. If a destination address look up fails, packets associated with this VLAN will be forwarded to ports specified in this field. E.g., 1 0000 0001 means port 8 and 0 are in this VLAN. | 1 0100 0000 |

## 8.7.8. PHY 6 Register 25: VLAN Entry [G]

**Table 98. PHY 6 Register 25: VLAN Entry [G]**

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 25.[15:12] | Reserved | - | Reserved | 1111 |
| 25.[11:0] | VLAN ID [G] | RW | Defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN G. | 0000 0000 0110 |

# 8.8. PHY 7 Registers

## 8.8.1. PHY 7 Register 0: Control

This register has the same definition as PHY 0 Register 0: Control, page 49.

## 8.8.2. PHY 7 Register 1: Status

This register has the same definition as PHY 0 Register 1: Status, page 50.

## 8.8.3. PHY 7 Register 4: Auto-Negotiation Advertisement

This register has the same definition as PHY 0 Register 4: Auto-Negotiation Advertisement, page 51.

## 8.8.4. PHY 7 Register 5: Auto-Negotiation Link Partner Ability

This register has the same definition as PHY 0 Register 5: Auto-Negotiation Link Partner Ability, page 52.

## 8.8.5. PHY 7 Register 16: Indirect Access Control

PHY 7 register 16 is used for reading or writing data to the MAC address table.

**Table 99. PHY 7 Register 16: Indirect Access Control**

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 16.[15:2] | Reserved | - | Reserved | 1111 1111 1111 11 |
| 16.1 | Command Execution | RW | 1: Trigger a command to read or write the lookup table<br>0: Indicates this command has completed | 0 |
| 16.0 | Read or Write Operation | RW | 1: Read cycle<br>0: Write cycle | 0 |

## 8.8.6. PHY 7 Register 17~20: Indirect Access Data

**Table 100. PHY 7 Register 17~20: Indirect Access Data**

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 17 | Indirect Data [63:48] | RW | Bit 63~48 of Indirect Data.<br>Indirect Data [54] = If this bit is 1, indicates this entry is static and will never be aged out. If this bit is 0, indicates this entry is dynamically learned, aged, updated, and deleted.<br>Indirect Data [53:52] = 2-bit counter for internal aging.<br>Indirect Data [51:48] = The source port of this Source MAC Address is learned. | 0x00 |
| 18 | Indirect Data [47:32] | RW | Bit 47~32 of Indirect Data.<br>Indirect Data [47:40] = Source MAC Address [7:0].<br>Indirect Data [39:32] = Source MAC Address [15:8]. | 0x00 |
| 19 | Indirect Data [31:16] | RW | Bit 31~16 of Indirect Data.<br>Indirect Data [31:24] = Source MAC Address [23:16].<br>Indirect Data [23:16] = Source MAC Address [31:24]. | 0x00 |
| 20 | Indirect Data [15:0] | RW | Bit 15~0 of Indirect Data.<br>Indirect Data [15:8] = Source MAC Address [39:32].<br>Indirect Data [7:0] = Source MAC Address [47:40].<br>Bits 1~0 and Bits 15~8 of this register also determine the address of data in the lookup table.<br>In a write cycle: Bits 1~0 and Bits 15~8 indirectly map to an entry in the lookup table. The written data should be filled in Indirect Data [63:0]<br>In a read cycle: Bits 1~0 and Bits 15~8 indirectly map to an entry in the lookup table. The read back data will be shown in Indirect Data [63:0]. | 0x00 |

## 8.8.7. PHY 7 Register 22: Port 7 Control 0

This register has the same definition as PHY 0 Register 22: Port 0 Control 0, page 56.

*Note: Reg 22.8 is not pin Sel_PortPri strap option for port 7. Default value for 22.8 is 1.*

## 8.8.8. PHY 7 Register 23: Port 7 Control 1

This register has the same definition as PHY 0 Register 23: Port 0 Control 1, page 57.

## 8.8.9. PHY 7 Register 24: Port 7 Control 2 & VLAN Entry [H]

**Table 101. PHY 7 Register 24: Port 7 Control 2 & VLAN Entry [H]**

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 24.[15:12] | Port 7 VLAN Index [3:0] | RW | In a port-based VLAN configuration, this register indexes port 7's 'Port VLAN Membership', which can be defined in one of the registers 'VLAN ID [A] Membership' to 'VLAN ID [I] Membership'. Port 7 can only communicate within the membership. This register also indexes to a default Port VID (PVID) for each port. The PVID is used in tag insertion and filtering if the tagged VID is not the same as the PVID. | 0111 |
| 24.[11~9] | Reserved | - | Reserved | 111 |
| 24.[8:0] | VLAN ID [H] Membership Bit [8:0] | RW | This 9-bit field specifies which ports are members of VLAN H. If a destination address look up fails, packets associated with this VLAN will be forwarded to ports specified in this field. E.g., 1 0000 0001 means port 8 and 0 are in this VLAN. | 1 1000 0000 |

## 8.8.10. PHY 7 Register 25: VLAN Entry [H]

**Table 102. PHY 7 Register 25: VLAN Entry [H]**

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 25.[15:12] | Reserved | - | Reserved | 1111 |
| 25.[11:0] | VLAN ID [H] | RW | Defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN H. | 0000 0000 0111 |

# 8.9. PHY 8 Registers

## 8.9.1. PHY 8 Register 0: Control

*Note: This register only works in MII PHY and SNI PHY mode. In MII MAC mode, these registers have no meaning.*

**Table 103. PHY 8 Register 0: Control**

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 0.15 | Reset | RO | 0: No reset allowed (permanently=0) | 0 |
| 0.14 | Loopback<br>(digital loopback) | RO | 0: Normal operation (permanently=0) | 0 |
| 0.13 | Speed Select | RW | 1: 100Mbps<br>0: 10Mbps<br>When NWay is enabled, this bit reflects the result of auto-negotiation (Read only).<br>When NWay is disabled, this bit can be set through SMI (Read/Write). | Pin MII_SPD_STA strap option |
| 0.12 | Auto Negotiation Enable | RW | 1: Enable auto-negotiation process<br>0: disable auto-negotiation process<br>This bit can be set through SMI (Read/Write). | 1 |
| 0.11 | Power Down | RO | 0: Normal operation (permanently=0) | 0 |
| 0.10 | Isolate | RO | 0: Normal operation (permanently=0) | 0 |
| 0.9 | Restart Auto Negotiation | RO | 0: Normal operation (permanently=0) | 0 |
| 0.8 | Duplex Mode | RW | 1: Full duplex operation<br>0: Half duplex operation<br>When NWay is enabled, this bit reflects the result of auto-negotiation (Read only).<br>When NWay is disabled, this bit may be set through SMI (Read/Write). | Pin MII_DUP_STA strap option |
| 0.[7:0] | Reserved | - | Reserved | 0 |

## 8.9.2. PHY 8 Register 1: Status

*Note: This register only works in MII PHY and SNI PHY mode. In MII MAC mode, these registers have no meaning.*

**Table 104. PHY 8 Register 1: Status**

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 1.15 | 100Base_T4 | RO | 0: No 100Base-T4 capability | 0 |
| 1.14 | 100Base_TX_FD | RO | 1: 100Base-TX full duplex capable (permanently=1) | 1 |
| 1.13 | 100Base_TX_HD | RO | 1: 100Base-TX half duplex capable (permanently=1) | 1 |

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 1.12 | 10Base_T_FD | RO | 1: 10Base-TX full duplex capable (permanently=1) | 1 |
| 1.11 | 10Base_T_HD | RO | 1: 10Base-TX half duplex capable (permanently=1) | 1 |
| 1.[10:7] | Reserved | RO | Reserved | 0 |
| 1.6 | MF Preamble Suppression | RO | The RTL8309G will accept management frames with preamble suppressed (permanently=1) | 1 |
| 1.5 | Auto-Negotiate Complete | RO | 1: Auto-negotiation process completed. MII Reg.4, 5 are valid if this bit is set (permanently=1) | 1 |
| 1.4 | Remote Fault | RO | 0: No remote fault (permanently=0) | 0 |
| 1.3 | Auto-Negotiation Ability | RO | 1: NWay auto-negotiation capable (permanently=1) | 1 |
| 1.2 | Link Status | RO | 1: Link is established. If the link should fail, this bit will be 0 until after reading this bit again<br>0: Link failed | Pin MII_LNK_STA# strap option |
| 1.1 | Jabber Detect | RO | 0: No Jabber detected (permanently=0) | 0 |
| 1.0 | Extended Capability | RO | 1: Extended register capable (permanently=1) | 1 |

## 8.9.3. PHY 8 Register 4: Auto-Negotiation Advertisement

*Note: This register only works in MII PHY and SNI PHY mode. In MII MAC mode, these registers have no meaning.*

**Table 105. PHY 8 Register 4: Auto-Negotiation Advertisement**

| Reg.bit | Name | Mode | Description | Default |
|---|---|---|---|---|
| 4.15 | Next Page | RO | 1: Next Page enabled<br>0: Next Page disabled (Permanently=0) | 0 |
| 4.14 | Acknowledge | RO | Permanently=0 | 0 |
| 4.13 | Remote Fault | RO | 1: Advertises that the RTL8309G has detected a remote fault<br>0: No remote fault detected | 0 |
| 4.[12:11] | Reserved | RO | Reserved | 0 |
| 4.10 | Pause | RW | 1: Advertises that the RTL8309G possesses 802.3x flow control capability<br>0: No flow control capability | Pin MII_FCTRL_STA strap option |
| 4.9 | 100Base-T4 | RO | Technology not supported (Permanently=0). | 0 |
| 4.8 | 100Base-TX-FD | RW | 1: 100Base-TX full duplex capable<br>0: Not 100Base-TX full duplex capable | 1 |
| 4.7 | 100Base-TX | RW | 1: 100Base-TX half duplex capable<br>0: Not 100Base-TX half duplex capable | 1 |
| 4.6 | 10Base-T-FD | RW | 1: 10Base-TX full duplex capable<br>0: Not 10Base-TX full duplex capable | 1 |
| 4.5 | 10Base-T | RW | 1: 10Base-TX half duplex capable<br>0: Not 10Base-TX half duplex capable | 1 |
| 4.[4:0] | Selector Field | RO | [00001]=IEEE 802.3. | 00001 |

## 8.9.4. MII Port NWay Mode

**Table 106. MII Port NWay Mode**

| Condition | Description |
|---|---|
| Upon Reset | Strapping MII_SPD_STA=1 and MII_DUP_STA=1 → Reg0.13=1, Reg0.8=1<br>Strapping MII_SPD_STA=1 and MII_DUP_STA=0 → Reg0.13=1, Reg0.8=0<br>Strapping MII_SPD_STA=0 and MII_DUP_STA=1 → Reg0.13=0, Reg0.8=1<br>Strapping MII_SPD_STA=0 and MII_DUP_STA=0 → Reg0.13=0, Reg0.8=0<br>Defau1t value of Reg4.10 is strapped from pin MII_FCTRL_STA<br>Default value of Reg1.2 is strapped from pin MII_LNK_STA#.<br>MII_LNK_STA# pulled down → Reg1.2=1.<br>MII_LNK_STA# pulled up → Reg1.2=0. |
| After Reset | If PHY 8 register 4 is configured as Reg4.8=1, Reg4.7=1, Reg4.6=1, Reg4.5=1, the RTL8309G will reflect this configuration in PHY 8 register 0 as Reg0.13=1 and Reg0.8=1.<br>If PHY 8 register 4 is configured as Reg4.8=0, Reg4.7=1, Reg4.6=1, Reg4.5=1, the RTL8309G will reflect this configuration in PHY 8 register 0 as Reg0.13=1 and Reg0.8=0.<br>If PHY 8 register 4 is configured as Reg4.8=0, Reg4.7=0, Reg4.6=1, Reg4.5=1, the RTL8309G will reflect this configuration in PHY 8 register 0 as Reg0.13=0 and Reg0.8=1.<br>If PHY 8 register 4 is configured as Reg4.8=0, Reg4.7=0, Reg4.6=0, Reg4.5=1, the RTL8309G will reflect this configuration in PHY 8 register 0 as Reg0.13=0 and Reg0.8=0.<br>If the CPU polls register 5, the RTL8309G replies with the contents in register 4.<br>If the CPU polls register 4, the RTL8309G replies with the contents in register 4. |

## 8.9.5. MII Port Force Mode

**Table 107. MII Port Force Mode**

| Condition | Description |
|---|---|
| Upon Reset | Strapping MII_SPD_STA=1 and MII_DUP_STA=1 → Reg0.13=1, Reg0.8=1<br>Strapping MII_SPD_STA=1 and MII_DUP_STA=0 → Reg0.13=1, Reg0.8=0<br>Strapping MII_SPD_STA=0 and MII_DUP_STA=1 → Reg0.13=0, Reg0.8=1<br>Strapping MII_SPD_STA=0 and MII_DUP_STA=0 → Reg0.13=0, Reg0.8=0<br>Defau1t value of Reg4.10 is strapped from pin MII_FCTRL_STA.<br>Default value of Reg1.2 is strapped from pin MII_LNK_STA#.<br>MII_LNK_STA# pulled down → Reg1.2=1.<br>MII_LNK_STA# pulled up → Reg1.2=0. |
| After Reset | The CPU only writes register 0.13 and 0.8 to configure a link status, then reads register 1.2 to determine whether the link partner can link with this status. |

# 9. Functional Description

## *9.1. Physical Layer Transceiver Functional Overview*

### 9.1.1. Auto Negotiation for UTP

The RTL8309G obtains the states of duplex, speed, and flow control ability for each port in UTP mode through the auto-negotiation mechanism defined in the IEEE 802.3u specifications. During auto-negotiation, each port advertises its ability to its link partner and compares its ability with advertisements received from its link partner. By default, the RTL8309G advertises full capabilities (100Full, 100Half, 10Full, 10Half) together with flow control ability.

If the link partner to the RTL8309G is forced to bypass auto negotiation, or auto negotiation is not supported, the link status of the RTL8309G is determined by observing the signal at the receiver.

### 9.1.2. 100Base-Tx Transmit Function

The 100Base-TX transmit function performs parallel to serial conversion, 4B/5B coding, scrambling, NRZ/NRZI conversion, and MLT-3 encoding. The 5-bit serial data stream after 4B/5B coding is then scrambled as defined by the TP-PMD Stream Cipher function to flatten the power spectrum energy such that EMI effects can be reduced significantly.

The scrambled seed is based on PHY addresses and is unique for each port. After scrambling, the bit stream is driven onto the network media in the form of MLT-3 signaling. The MLT-3 multi-level signaling technology moves the power spectrum energy from high frequency to low frequency, which also benefits EMI emission.

### 9.1.3. 100Base-Tx Receive Function

The 100Base-TX receive mechanism includes an adaptive equalizer, DC restoration, MLT3 to NRZI conversion, data and clock recovery, NRZI to NRZ conversion, de-scrambling, 4B/5B decoding, and serial to parallel conversion. The process starts with the adaptive equalizer and DC restoration circuits to compensate for the distortion in the MLT-3 signal. This variable equalizer makes an estimate by comparing the received signal strength against some known cable characteristic, then tunes itself for optimization. This on-going process allows the RTL8309G to adjust itself to environmental changes such as temperature variations. The equalized data then goes through a DC restoration circuit to compensate for the effects of base line wander in order to improve the dynamic range.

After restoration, the MLT-3 to NRZI, NRZI to NRZ converters then convert the analog signal to a digital bit-stream. The clock recovery circuit extracts the 125MHz clock from the edges of the NRI signal. A De-scrambler, 5B/4B decoder and serial-to-parallel conversion circuits follow. Finally, the converted parallel data is fed into the MAC.

### 9.1.4. 10Base-T Transmit Function

The output 10Base-T waveform is Manchester-encoded before it is driven into the network media with a typical 2.3V amplitude. The internal filter shapes the driven signals to reduce EMI emission, eliminating the need for an external filter. The harmonic contents are at least 27dB below the fundamental when the RTL8309G drives an all-ones Manchester-encoded signal.

### 9.1.5. 10Base-T Receive Function

The Manchester decoder converts the incoming serial stream to NRZ data when the squelch circuit detects the signal level is above squelch level.

### 9.1.6. Link Monitor

The 10Base-T link pulse detection circuit continually monitors the RXIP/RXIN pins for the presence of valid link pulses. Auto-polarity is implemented to correct the detected reverse polarity of RXIP/RXIN signal pairs.

### 9.1.7. Power-Down Mode

The RTL8309G implements power-down mode on a per-port basis. Setting MII Reg.0.11 forces the corresponding port of the RTL8309G to enter power-down mode. This disables all transmit/receive functions, except SMI (Serial Management Interface: MDC/MDIO, also known as MII Management Interface).

### 9.1.8. Auto Crossover Detection

During the link setup phase, the RTL8309G checks whether it receives active signals on every port in order to determine if a connection can be established. In cases where the receiver data pin pair is connected to the transmitter data pin pair of the peer device and vice versa, the RTL8309G will automatically change its configuration to swap receiver data pins with transmitter data pins. In other words, the RTL8309G adapts automatically to a peer device's configuration. If a port is connected with a crossover cable to a NIC with an MDI-X interface, the RTL8309G will reconfigure the port to ensure proper connection. This effectively replaces the DIP switch commonly used for reconfiguring a port on a hub or switch.

By pulling-up EN_AUTOXOVER, the RTL8309G identifies the type of connected cable and sets the port to MDI or MDIX. When switching to MDI mode, the RTL8309G uses TXOP/N as transmit pairs; when switching to MDIX mode, the RTL8309G uses RXIP/N as transmit pairs. This function is port-based. Pulling-down EN_AUTOXOVER disables this function and the RTL8309G operates in MDI mode, in which TXOP/N represents transmit pairs and RXIP/N represents receive pairs.

IEEE 802.3 compliant forced mode 100M ports with auto crossover have link issues with NWay (Auto-Negotiation) ports. It is recommended to not use auto crossover for forced 100M.

## *9.2. Switch Core Functional Overview*

### 9.2.1. Address Search, Learning, and Aging

When a packet is received, the RTL8309G uses the least 10 bits of the destination MAC address to index the 1024-entry look-up table, and at the same time compares the destination MAC address with the contents of the 16-entry CAM. If the indexed entry is valid or the CAM comparison is matched, the received packet will be forwarded to the corresponding destination port. Otherwise, the RTL8309G will broadcast the packet. This is the 'Address Search'.

The RTL8309G then extracts the least 10 bits of the source MAC address to index the 1024-entry look-up table. If the entry is not already in the table it will record the source MAC address and add switching information. If this is an occupied entry, it will update the entry with new information. This is called 'Learning'. If the indexed location has been occupied by a different MAC address (hash collision), the new source MAC address will be recorded into the 16-entry CAM. The 16-entry CAM reduces address hash collisions and improves switching performance.

Address aging is used to keep the contents of the address table correct in a dynamic network topology. The look-up engine will update the time stamp information of an entry whenever the corresponding source MAC address appears. An entry will be invalid (aged out) if its time stamp information is not refreshed by the address learning process during the aging time period. The aging time of the RTL8309G is around 300 seconds.

### 9.2.2. Flow Control

The RTL8309G supports standard IEEE 802.3x full duplex flow control ability on both transmit and receive sides. If the RTL8309G recognizes that the resources of the destination port of this packet are being used up, it will issue a 'pause on' frame to the source port of this packet with a maximum time as defined in IEEE 802.3x. Once the resource is available, the RTL8309G sends a 'pause off' frame with zero pause time to turn on transmissions.

On the receive side, when the RTL8309G receives a pause control packet on a port, it stops transmitting any packets to this port, except flow control packets, for a period of time specified in the received pause control frame. If it receives another pause control packet in this period of time on the same port, the timer will be updated with the new value specified in the latest pause control packet. The RTL8309G will re-start transmitting packets on this port after the timer has expired.

### 9.2.3. Half Duplex Operation

In half duplex mode, the CSMA/CD media access method is the means by which two or more stations share a common transmission medium. To transmit, a station waits (defers) for a quiet period on the medium (that is, no other station is transmitting) and then sends the intended message in bit-serial form. If the message collides with that of another station, then each transmitting station intentionally transmits for an additional predefined period to ensure propagation of the collision throughout the system. The station remains silent for a random amount of time (backoff) before attempting to transmit again.

When a transmission attempt has terminated due to a collision, it is retried until it is successful. A controlled randomization process called 'truncated binary exponential backoff' determines the scheduling of the retransmissions. At the end of enforcing a collision (jamming), the switch delays before attempting to retransmit the frame. The delay is an integer multiple of slotTime (512 bit times). The number of slot times to delay before the $n^{th}$ retransmission attempt is chosen as a uniformly distributed random integer 'r' in the range:

$0 \leq r < 2^k$

where:

k =min (n, backoffLimit). IEEE 802.3 defines the backoffLimit as 10.

### 9.2.4. Backpressure

The RTL8309G provides two methods of preventing packet congestion when resources are about to be used up. The first is by colliding incoming packets when the packets are going to a congested port. The second is by sending preambles to defer other station's transmissions.

Backpressure: When the switch is overloaded it will assert a jam pattern to collide incoming packets until the congestion condition of the destination port is resolved. The 48 pass 1 mechanism prevents the port being partitioned by excessive collisions. The RTL8309G will forward one packet successfully after 48 forced collisions. This method carries some risk since the resource may not be available after 48 forced collisions. If the 48 pass 1 function is turned off, the RTL8309G will always collide incoming packets with a jam pattern.

By deferring, the RTL8309G sends preambles to defer other stations' transmissions. To avoid jabber and excessive deference as defined in IEEE 803.3, the RTL8309G will pull down the carrier sense signal for a short time and then raise it up it quickly. This short silence time is to prevent other stations seizing the medium and sending packets out. If there are packets to send out during the carrier sense rising up period,

carrier sense flow control will be replaced by those packets. After the packets are sent, carrier sense rises up again, repeating the pattern until the system is available.

## 9.2.5. UTP Port Status Configuration

The RTL8309G supports flexible status configuration via strapping pins for each PHY, En_ANEG, En_FCTRL, Force_Duplex, and Force_Speed, on a group basis. These pins are used to assign the initial values to PHY register 0 and 4 upon reset. The configuration parameters set by these four strapping pins globally control the abilities of each port. For advanced applications requiring configuration on a per-port basis, a serial EEPROM should be attached.

If auto negotiation is enabled by strapping pin 'En_ANEG', the link status is determined by the result of the auto negotiation process. The default configuration of the RTL8309G is all abilities enabled (the content of the PHY registers will be Reg0.12=1, Reg4.5=1, Reg4.6=1, Reg4.7=1, Reg4.8=1, and Reg4.10=1). If auto negotiation is disabled by EN_ANEG, the link speed and duplex mode is forced by strapping pins, Force_Duplex and Force_Speed. These two pins have no effect if auto negotiation is enabled.

## 9.2.6. MII Port (The 9th Port)

The RTL8309G is an 8-port Fast Ethernet switch with one extra MII port for specific applications. It integrates embedded SRAM for packet storage, nine MAC, and eight physical layer transceivers for 10Base-T and 100Base-TX, into a single chip.

### *9.2.6.1 MII Port Operating Mode*

The MII port only provides a MAC part to support the MII interface for connection with an external MAC or PHY. Two strapping pins, MII_MODE[1:0], are used to configure this interface to act as MII PHY mode, SNI PHY mode, or MII MAC mode to work with the external MAC of a routing engine, PHY of a HomePNA, or other physical layer transceivers.

If the MII port connects with an external MAC, such as the processor of a router application, it will act as a PHY. This is PHY mode MII, or PHY mode SNI. In PHY mode MII or PHY mode SNI, the MII port uses the MAC part only, and provides an external MAC interface to connect MACs of external devices. In order to connect both MACs, the MII of the switch MAC should be reversed into PHY mode.

If the MII port connects with an external PHY, such as the PHY of a HomePNA application, it will act as a MAC. This is MAC mode MII. In MAC mode MII, the MII port uses its MAC to connect to an external PHY and ignores the internal PHY part.

The following figures illustrate various utilizations of the ninth port by setting strapping pins. They consist of the following general system applications:

General standalone 8-port switch applications.

Router applications.

HomePNA applications.

Other PHY applications.

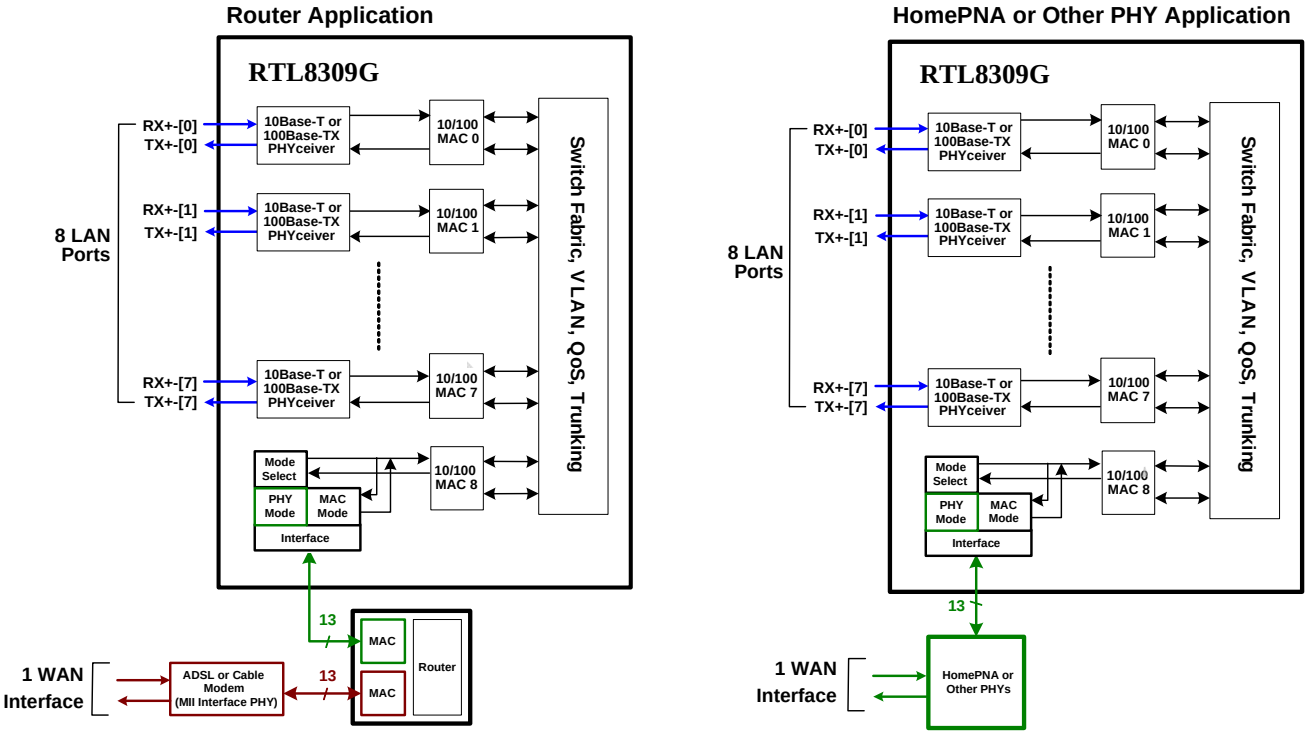



**Figure 3. MII Port Application**

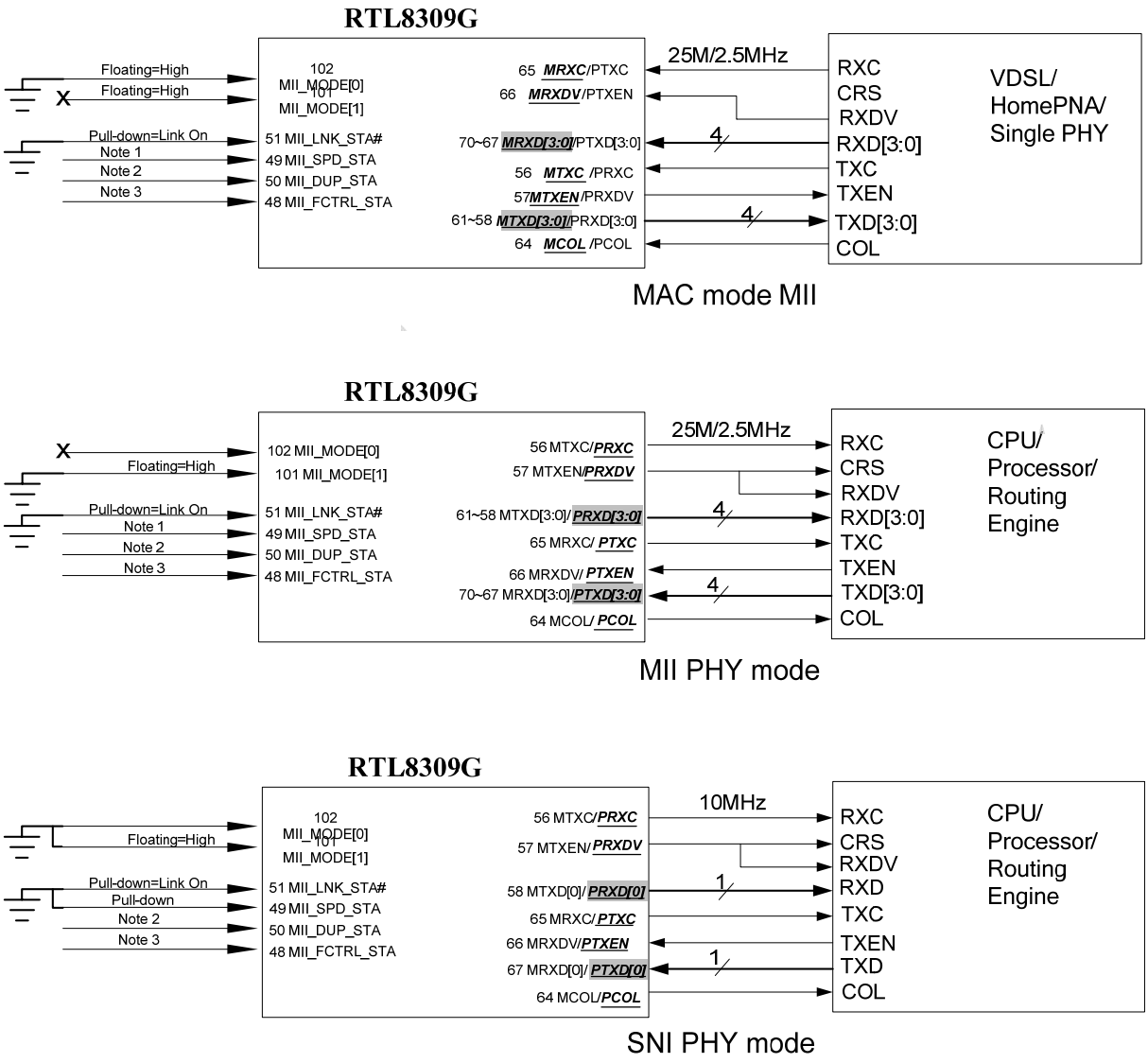
### *9.2.6.2 MII Interface*

In order to act as a PHY when the MII port is in PHY mode, some pins of the external MAC interface must be changed. For example, TXC are input pins for MAC but output pins for PHY; so the pin MTXC/PRXC is input for MAC mode and output for PHY mode. Refer to Figure 4, on page 86 to check the relationship between the RTL8309G and the external device.

*Note: Connect the input of the RTL8309G to the output of the external device. The RTL8309G has no RXER, TXER, and CRS pins for MII signaling. As the RTL8309G does not support pin CRS, it is necessary to connect the MTXEN/PRXDV (output) of PHY mode to both CRS and RXDV (input) of the external device.*

### 9.2.6.3 *MII Port Status Pins*

Four signaling pins (MII_LNK_STA#, MII_SPD_STA, MII_DUP_STA, MII_FCTRL_STA) are used to provide operating status to the MII port MAC in real time after reset. This means the external MAC or PHY must be forced to the same port status as the MII port. The MII port automatically detects the link status both from the TXC of the external PHY and MII_LNK_STA#.




*Note 1: Pulled high or floating sets the speed to 100Mbps. Pulled down sets the speed to 10Mbps.*

*Note 2: Pulled high or floating enables full duplex. Pulled down sets half duplex.*

*Note 3: Pulled high or floating enables flow control or backpressure. Pulled down disables flow control or backpressure.*

**Figure 4. MII Port Operating Mode Overview**

#### 9.2.6.4 MII PHY Mode/SNI PHY Mode

In routing applications, the RTL8309G cooperates with a routing engine to communicate with the WAN (Wide Area Network) through MII/SNI.

In MII PHY mode, pulling MII_SPD_STA up results in the MII port operating at 100Mbps with MTXC, and MRXC running at 25MHz. Pulling MII_SPD_STA down results in the MII port operating at 10Mbps with MTXC, and MRXC running at 2.5MHz.

In SNI PHY mode, MII_SPD_STA has no effect and should be pulled down. SNI mode operates at 10Mbps only, with MTXC and MRXC running at 10MHz. In SNI mode, the RTL8309G does not loop back a RXDV signal as a response to TXEN and does not support the heartbeat function (asserting COL signal for each complete TXEN signal). This interface is a bit-wide data interface used with some controllers to function as a network layer protocol in half duplex operation.

#### 9.2.6.5 MII MAC Mode

In HomePNA or other PHY applications, the RTL8309G provides an MII interface to the underlying HomePNA or other physical devices so as to communicate with other types of LAN media. In such applications, MII_MODE[1:0] should be pulled high or be floated upon reset.

In HomePNA applications, MII_DUP_STA must be pulled down since HomePNA is half-duplex only. The link speed of the RTL8309G is determined by RXC and TXC from the PHY of the HomePNA (running at 1Mbps). Thus, the MII_SPD_STA has no effect and should be pulled down for compatibility with HomePNA's PHY. The link state of HomePNA is unstable (a characteristic of the HomePNA 1.0 standard) such that MII_LNK_STA# must be pulled down instead of being wired to the LINK LED pin of the HomePNA.

Because the HomePNA PHY physical layer is half duplex and can only detect a collision event during the AID header interval (the time when transmitting the Ethernet preamble), the backpressure flow control algorithm is not suitable for a HomePNA network and MII_FCTRL_STA should be pulled down.

For other PHY applications, the strap status set by MII_SPD_STA, MII_DUP_STA, and MII_FCTRL_STA depends on the particular application.

#### *9.2.6.6 MII Port PHY Register*

The external MAC automatically polls and accesses the internal PHY registers in the RTL8309G when the MII port is operated in MII PHY mode with auto negotiation enabled. For the auto negotiation process in the CPU to function properly, the RTL8309G provides PHY register 0, 1, and 4, to virtually provide the MII port's PHY status to the external MAC. Because the MII port of the RTL8309G does not have a true PHY in it, it does not process the auto negotiation. The contents of PHY registers 4 and 5 should be the same for both terminals of the MII bus when operating on the same link status. Thus, the RTL8309G does not provide PHY register 5; it only emulates it. If the CPU polls PHY register 5, the RTL8309G returns the contents of PHY register 4 since it cannot execute the auto negotiation process. If the CPU polls PHY register 4, the RTL8309G returns the contents of PHY register 4.

## *9.3. Advanced Functionality Overview*

### 9.3.1. Port-Based VLAN

If the VLAN function is enabled by pulling down the Dis_VLAN strapping pin, the default VLAN membership configuration by internal register is the MII port overlapped with all the other ports to form nine individual VLANs. Via an attached serial EEPROM or via SMI, the default configuration may be modified to allow the input ports to join any of the nine VLAN groups: VLAN A, B, C, D, E, F, G, H, and I. Each input port can be a member of more than one VLAN group.

Port-based VLAN mapping is the simplest implicit mapping rule. Each incoming frame is assigned to a VLAN based on the input port into which it arrived at the switch. It is not necessary to parse and inspect frames in real-time to determine their VLAN mapping. All frames received on a given input port will be forwarded to members of that port's VLAN group. The RTL8309G supports nine VLAN indexes to individually index received packets to one of the nine VLAN membership registers. These nine groups of VLAN membership registers, VLAN ID [A] membership bit [8:0] ~ VLAN ID [I] membership bit [8:0], determine which ports are members of this VLAN. The RTL8309G forwards frames to members of this VLAN only (excluding the input port of this frame). VLAN membership registers descript which port are members in a VLAN member set. A port that is not specified in this port's member set should generally not be receiving and/or transmitting frames for that VLAN.

Figure 5 illustrates a typical application. VLAN indexes and VLAN member definitions are set to form three different VLAN groups.

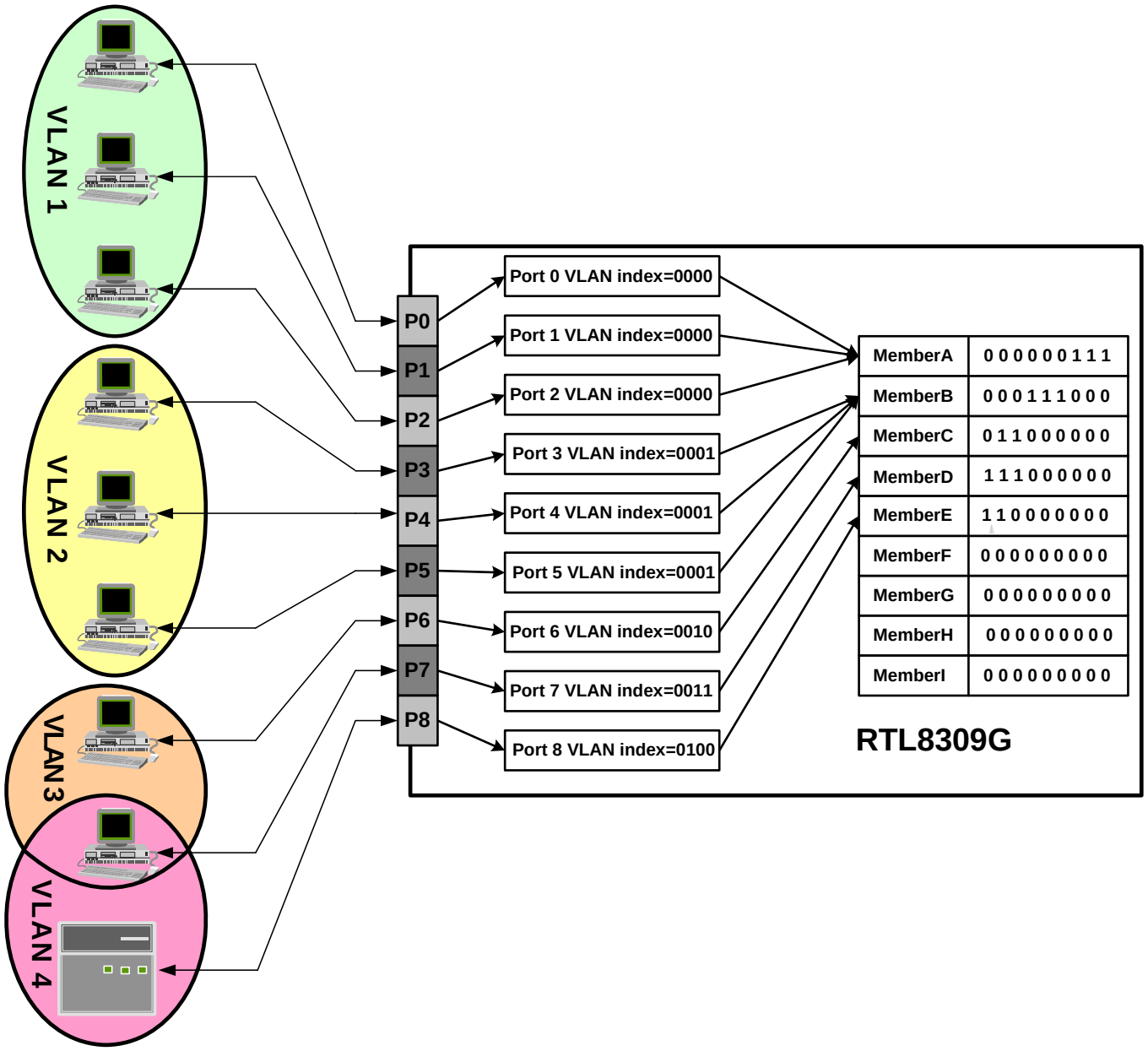



**Figure 5. VLAN Grouping Example**

In cases where VLAN and trunking are both enabled at the same time, a situation may occur where a packet is forwarded to a trunk but one of the members of this trunk is not in the same VLAN group associated with the source port. In this situation, the VLAN function has higher priority than the trunking operation. The packet will not be forwarded to the port of this trunk.

For non-VLAN tagged frames, the RTL8309G performs port-based VLAN. It will use Port n VLAN index [3:0] to index to a VLAN membership. The VLAN ID associated with this indexed VLAN membership is the Port VID (PVID) of this port.

### 9.3.2. IEEE 802.1Q Tagged VID-based VLAN

IEEE 802.1Q tagged-VID based VLAN mapping uses a 12-bit explicit identifier in the VLAN tag to associate received packets with a VLAN. Nine groups of VLAN membership registers, VLAN ID [A] membership [8:0] ~ VLAN ID [I] membership [8:0], consist of ports that are in the same VLAN corresponding to the registers defined in VLAN ID [A] [11:0] ~ VLAN ID [I] [11:0]. If the VID of a VLAN-tagged frame does not hit the VLAN ID [A] [11:0] ~ VLAN ID [I] [11:0], then the RTL8309G will drop the VLAN-tagged frame. Otherwise, the RTL8309G compares the explicit identifier in the VLAN tag with the nine VLAN registers to determine the VLAN association of this frame, then forwards it to the member set of this VLAN. Two VIDs are reserved for special purposes. One of them is all ones and is currently unused. The other is all zeros and indicates a priority tag, which is treated as an untagged frame.

When 802.1Q tag aware VLAN is enabled, the RTL8309G performs 802.1Q tag-based VLAN mapping for tagged frames, but performs port-based VLAN mapping for untagged frames. If 802.1Q tag-aware VLAN is disabled, the RTL8309G performs only port-based VLAN mapping both for non-tagged and tagged frames. Figure 6 illustrates the processing flow when 802.1Q tag aware VLAN is disabled.

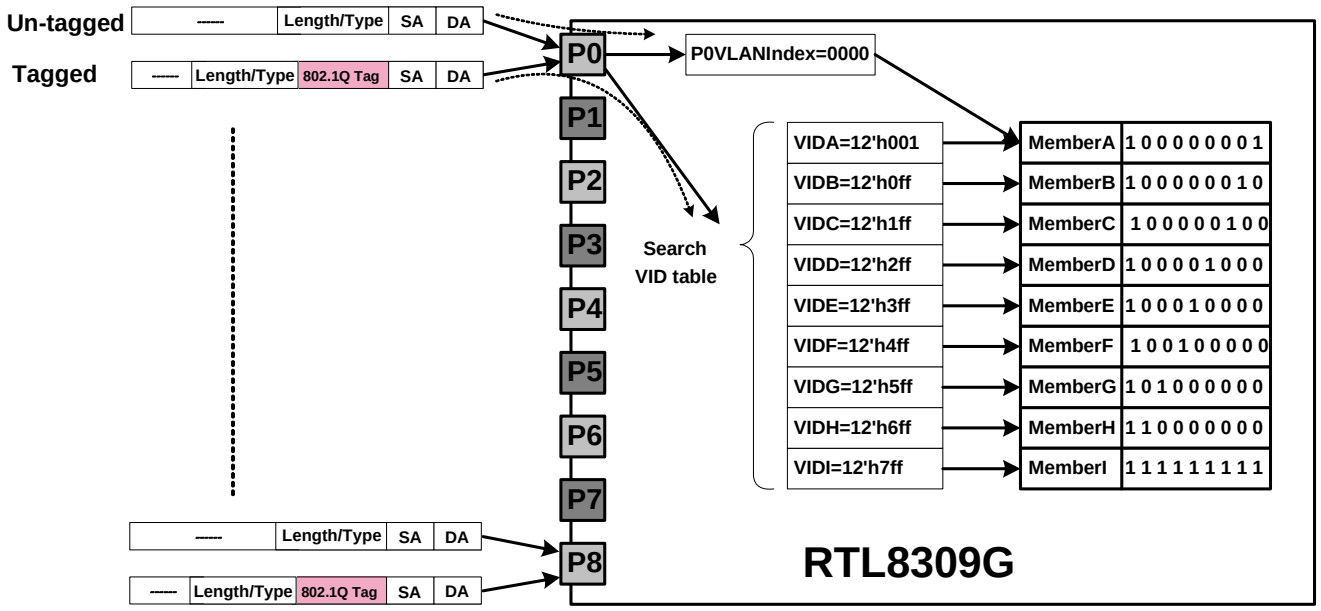



**Figure 6. Tagged and Untagged Packet Forwarding When 802.1Q Tag Aware VLAN is Disabled**

Two VLAN ingress filtering functions are supported by the RTL8309G in registers. One is the 'admit VLAN tagged frame' function, which provides the ability to receive VLAN-tagged frames only. Untagged or priority tagged (VID=0) frames will be dropped. The other is the 'ingress member set filtering', which will drop frames if the receive port is not in the member set.

There are also two optional egress filtering functions supported by the RTL8309G through strapping. One is 'Leaky VLAN', which enables inter-VLAN unicast packet forwarding. That is, if the layer 2 look-up table search has a hit, then the unicast packet will be forwarded to the egress port, ignoring the egress rule. The other is 'ARP VLAN', which broadcasts ARP packets to all other ports, ignoring the egress rule.

## 9.3.3. QoS Operation

The RTL8309G can recognize the QoS priority information of incoming packets to give a different egress service priority. The RTL8309G identifies the packets as high priority based on several types of QoS priority information:

Port-based priority

802.1p/Q VLAN priority tag

TCP/IP's TOS/DiffServ (DS) priority field

IP Address

There are two priority queues; a high-priority queue and a low-priority queue. The queue service rate is based on the Weighted Round Robin algorithm. The packet-based service weight ratio of the high-priority queue and low-priority queue can be set to 4:1, 8:1, 16:1 or 'Always high priority first' by hardware pins upon reset, or internal register via SMI after reset.

### *9.3.3.1 Port-Based Priority*

When port-based priority is applied, packets received from the high-priority port are sent to the high-priority queue of the destination port. High priority ports can be partially set by hardware pins, and wholly configured in internal registers.

#### 9.3.3.2 802.1p-Based Priority

When 802.1p VLAN tag priority applies, the RTL8309G recognizes the 802.1Q VLAN tag frames and extracts the 3-bit User Priority information from the VLAN tag. The RTL8309G sets the threshold of User Priority as 3. Therefore, VLAN tagged frames with User Priority value = 4~7 will be treated as high priority frames, other User Priority values (0~3) as low priority frames (follows 802.1p standard). The threshold value can be modified in internal registers via an SMI interface or configured in EEPROM.

#### 9.3.3.3 DiffServ-Based Priority

When TCP/IP's TOS/DiffServ(DS) based priority is applied, the RTL8309G recognizes TCP/IP Differential Services Code Point (DSCP) priority information from the DS-field defined in RFC2474. The DS field byte for the IPv4 is a Type-of-Service (TOS) octet. The recommended DiffServ Code Point is defined in RFC2597 to classify the traffic into different service classes. The RTL8309G extracts the codepoint value of DS-fields from IPv4 packets and identifies the priority of the incoming IP packet following the definition below:

High priority: where the DS-field = (EF, Expected Forwarding:) 101110

(AF, Assured Forwarding:) 001010; 010010; 011010; 100010

(Network Control:) 110000 and 111000

Differential service code point [A] specified in internal register;

Differential service code point [B] specified in internal register;

Low priority: where the DS-field = other values.

The VLAN tagged frame and 6-bit DS-field in the IPv4 frame format are shown below:

**Table 108. 802.1Q VLAN Tag Frame Format**

| 6 bytes | 6 bytes | 2 bytes | 3 bits | |
|---|---|---|---|---|
| DA | SA | 81-00 | User-Priority (0~3:Low-pri; 4~7: High-pri) | --- |

**Table 109. IPv4 Frame Format**

| 6 bytes | 6 bytes | 4 bytes | 2 bytes | 4 bits | 4 bits | 6 bits | |
|---|---|---|---|---|---|---|---|
| DA | SA | 802.1Q Tag (optional) | 08-00 | Version IPv4= 0100 | IHL | TOS[0:5] = DS-field | --- |

#### *9.3.3.4 IP-Based Priority*

When IP-based based priority is applied, any incoming packets with IP priority equal to IP address [A] AND IP mask [A] or IP address [B] AND IP mask [B] will be treated as high priority packets. IP priority [A] and IP priority [B] may be enabled or disabled independently.

#### *9.3.3.5 Flow Control Auto Turn Off*

The RTL8309G can be configured to turn off 802.3x flow control and backpressure flow control for 1~2 seconds whenever the port receives VLAN-tagged or TOS/DS high priority frames. Flow control is re-enabled when no priority frame is received for a 1~2 second duration. The purpose of this function is to avoid head-of-line blocking on priority classification.

### 9.3.4. Insert/Remove VLAN Priority Tag

The RTL8309G supports four types of insertion/removal of VLAN tags in packet, controlled by internal registers on a per-port basis. They are classified as follows:

**Type 11**

Do not change packets (Default).

**Type 10**

Insert input port's PVID for non-tagged packets. Do not change packets if they are already tagged.

**Type 01**

Remove VLAN tags from tagged packets. Do not change packets if they are not tagged.

**Type 00**

Remove VLAN tags from tagged packets then insert the input port's PVID. For non-tagged packets, insert the input port's PVID.

In Type 10, if Null VID replacement is enabled, this function has higher priority than type 10. If both type 10 is selected and Null VID replacement is enabled, the RTL8309G inserts a PVID to non-tagged packets and replaces a null VID with a PVID for tagged packets, and does nothing in tagged packets with a non-null VID.

If the tag removed frame is less than 64 bytes, it will be padded with an 0x20 pattern before the packet's CRC field to fit the 64-byte minimum packet length of the IEEE 802.3 spec. The RTL8309G will recalculate the FCS (Frame Check Sequence) if the frame has been changed.

### 9.3.5. Port VID (PVID)

In a router application, the router may want to know which input port this packet came from. The RTL8309G supports Port VID (PVID) for each port to insert a PVID in the VLAN tag on an egress packet. The VID information carried in the VLAN tag will be changed to a PVID. The RTL8309G also provides an option to admit VLAN-tagged packets with a specific PVID only. When this function is enabled, packets with an incorrect PVID and non-tagged packets will be dropped.

The RTL8309G uses an internal register, 'Port n VLAN index [3:0]' to index to a VLAN membership. The VLAN ID associated with this indexed VLAN membership is the PVID for this port. Users may select VLAN insert/remove type 10 or 00 to insert a PVID on egress packets.

On 802.1Q tag-based VLANs, do not use a port-based VLAN in PVID applications, as the VID information carried in the VLAN tag will be replaced with a PVID.

### 9.3.6. Port Trunking

The RTL8309G can combine two UTP ports into one trunking port (with a balancing mechanism). The default configuration is to combine port 0 and 1 as one trunk, even if they are operating with different duplex or speed settings. If port 0 and/or port 1 are assigned as a high priority port, this trunk will also be considered as a high priority trunk when the trunking function is enabled. The RTL8309G also provides the option to set port 6 and port 7 as a trunk by configuring the 'trunking port assignment' bit in the internal register.

### 9.3.7. ISP MAC Address Translation

Some Internet Service Providers only provide service to a single pre-registered MAC address. To share the Internet Service with more than one station, the RTL8309G translates the MAC address of multiple NICs to the ISP registered MAC address.

Figure 7, page 95, illustrates an outbound process. When station G tries to send a packet to the WAN, it broadcasts or unicasts this packet to the CPU port with a NIC MAC address. After the CPU receives this packet, it translates this MAC address to the ISP registered MAC address and stores this information in its mapping table. It then forwards this packet to the WAN port through the CPU port. The RTL8309G will not learn this packet into it's forwarding table. This is a special learning mechanism, which states that any frame coming from the CPU port with a source MAC address equal to internal register 'ISP MAC [47:0]'

will not be learned. This function must be correctly configured in the VLAN configuration, otherwise the RTL8309G will drop such packets.

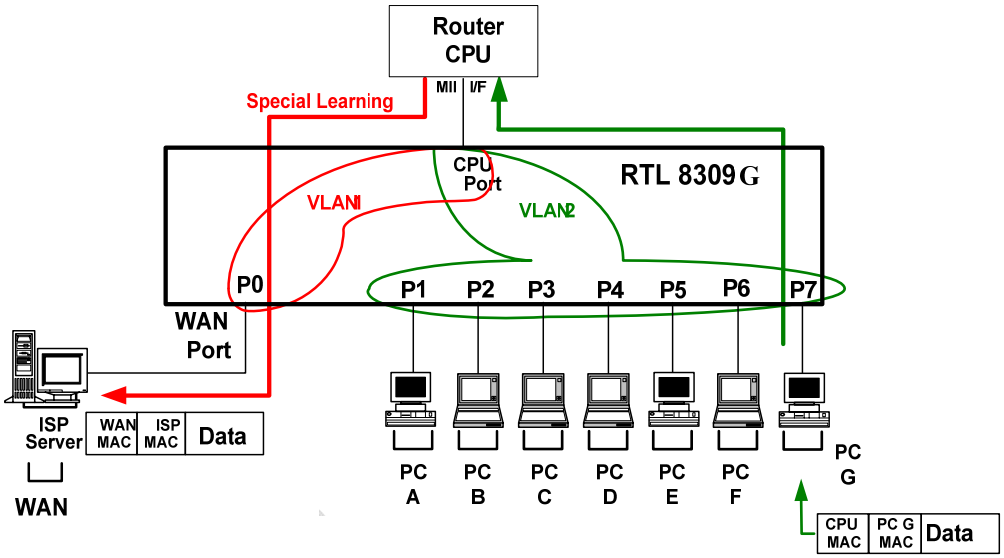



**Figure 7. ISP MAC Outbound Process**

In the inbound process, when the RTL8309G receives a packet from the WAN port, it will be directly forwarded to the CPU port according to the VLAN 1 configuration. The CPU looks up the mapping table to reverse translate the destination MAC address from the ISP MAC to the MAC address of the station G NIC. Figure 8 illustrates this inbound process.

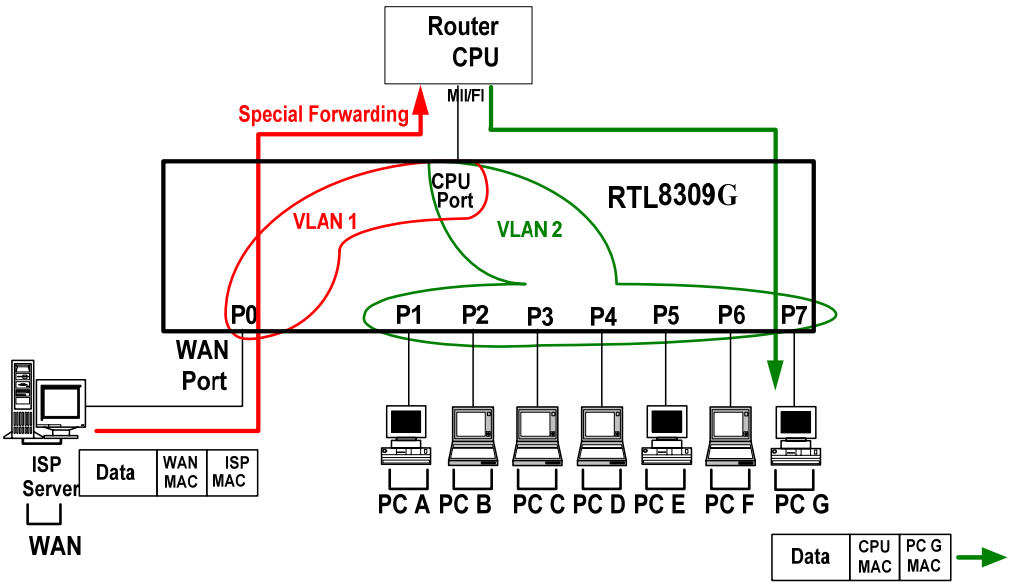



**Figure 8. ISP MAC Inbound Process**

## 9.3.8. Lookup Table Access

The RTL8309G supports registers for the CPU to read/write to an internal 1024-entry lookup table via the SMI interface. Before reading/writing from/to the internal forwarding table, the contents of internal register 'Indirect Access Control [15:0]' should be filled correctly.

In a write cycle, the user must assign the write data in register 'Indirect Access Data [63:0]' first. Bits 1~0 along with bits 15~8 form a 10-bit field that indirectly maps to an entry in the lookup table. To execute a write access, bit 0 in the 'Indirect Access Control' register should be set to 0, and bit 1 should be set to 1. The CPU will poll bit 1 in 'Indirect Access Control' to determine whether the write access is complete or not.

The 10-bit field composed of bits 1~0 and bits 15~8 in PHY7 Reg.20 indirectly maps to an entry in the lookup table for reading. The read back data is shown in PHY7 Reg.17~20. To execute read access, bit 0 in the 'Indirect Access Control' register should be set to 1, and bit 1 should be set to 1 to trigger this command. The CPU will poll bit 1 in 'Indirect Access Control' to determine whether read access is complete or not.

## 9.3.9. Serial Management Interface (SMI)

SMI is also known as the MII Management Interface. It consists of two signals (MDIO and MDC) that allow an external device in SMI master mode (MDC is output) to control the state of PHY, and in SMI slave mode (MDC is input) to control the internal register. MDC is an input clock for the RTL8309G to latch MDIO on its rising edge. The clock can run from 0MHz to 25MHz. MDIO is a bi-directional signal that is used to write data to, or read data from, the RTL8309G. Table 110 shows the read and write cycle format of the RTL8309G.

**Table 110. SMI Read/Write Cycles**

| | Preamble (32 bits) | Start (2 bits) | OP Code (2 bits) | PHYAD (5 bits) | REGAD (5 bits) | Turn Around (2 bits) | Data (16 bits) | Idle |
|---|---|---|---|---|---|---|---|---|
| **Read** | 1……..1 | 01 | 10 | $A_4A_3A_2A_1A_0$ | $R_4R_3R_2R_1R_0$ | Z0 | $D_{15}$…….$D_0$ | Z* |
| **Write** | 1……..1 | 01 | 01 | $A_4A_3A_2A_1A_0$ | $R_4R_3R_2R_1R_0$ | 10 | $D_{15}$…….$D_0$ | Z* |

*Note: high-impedance. During idle time, an external 1.5KΩ pull-up resistor determines MDIO state.*

The RTL8309G supports Preamble Suppression, which allows the MAC to issue Read/Write Cycles without preamble bits. The RTL8309G can accept MDIO commands after a 1 bit preamble. However, for the first cycle of MII management after power-on reset, a 32-bit preamble is needed.

To guarantee the first successful SMI transaction after power-on reset, an external device should delay at least 1 second before issuing the first SMI Read/Write Cycle relative to the rising edge of reset. The output voltage level of the RTL8309G is configurable by supplying different voltages to pin VDDIO. VDDIO can be supplied with either 2.5V or 3.3V power.

## 9.3.10. Broadcast Storm Control

After 64 consecutive broadcast packets (DID=FFFF-FFFF-FFFF) have been received by a particular port, any following incoming broadcast packets will be discarded by this port for approximately 800ms. Any non-broadcast packet can reset the time window and broadcast counter such that the scheme restarts.

*Note: Trigger condition is consecutive 64 DID = FFFF-FFFF-FFFF packets. Release condition: receive non-broadcast packet on or after 800ms.*

## 9.3.11. Broadcast In/Out Drop

If some destination ports are blocking and the buffer is full, broadcast frames are dropped according to the internal configuration. There are two options:

**Broadcast Input Drop**

Forwards any broadcast packet to any output port and will drop packets at the source port directly. Although this function effectively reduces the loading on the RTL8309G, packets broadcast to non-congested ports will also be dropped.

**Broadcast Output Drop**

Only forwards broadcast packets to non-congested ports. But if a dropped packet is re-transmitted by a higher protocol in the congested port, the non-congested port will receive duplicate packets. Figure 9, page 98 illustrates this concept.

1. Input Drop: Drop the frame directly. Do not forward to any port

2. Output Drop: Forward only to non-blocking ports (broadcast becomes multicast)

**1. Broadcast packet from Port 0**
**2. Buffer of Port 7 is full, others are not full**

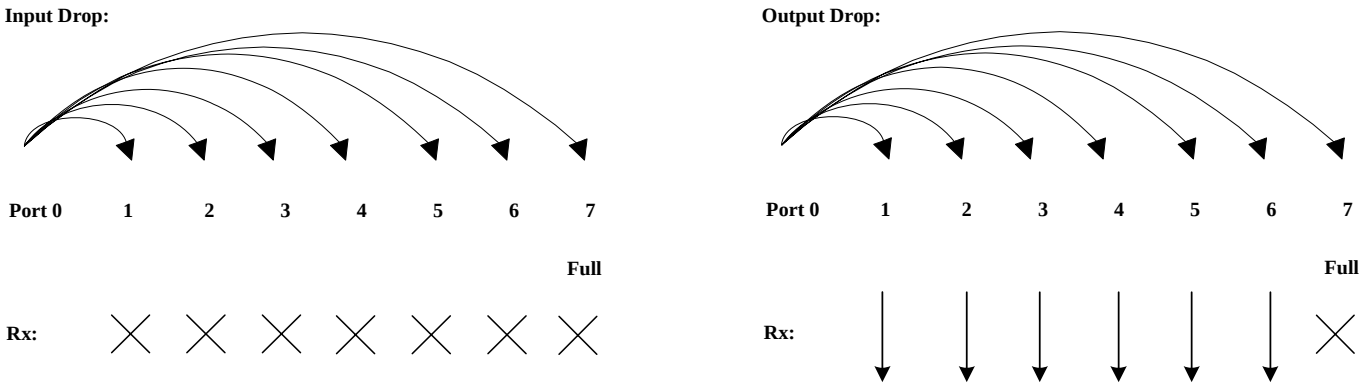



**Figure 9. Input Drop vs. Output Drop**

## 9.3.12. EEPROM Configuration Interface

The EEPROM interface is a 2-wire serial EEPROM interface providing 2Kbits of storage space. The external device connected to the RTL8309G should be 2.5V or 3.3V depending on the VDDIO setting.

## 9.3.13. 24LC02 Device Operation

Clock and Data transitions: The SDA pin is normally pulled high with an external resistor. Data on the SDA pin may change only during SCL low periods. Data changes during SCL high periods will indicate a start or stop condition as defined below.

### Start Condition

A high-to-low transition of SDA with SCL high is the start condition and must precede any other command.

### Stop Condition

A low-to-high transition of SDA with SCL high is a stop condition.

### Acknowledge

All addresses and data are transmitted serially to and from the EEPROM in 8-bit words. The 24LC02 sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.

### Random Read

A random read requires a ‘dummy’ byte write sequence to load in the data word address.

### Sequential Read

For the RTL8309G, the sequential reads are initiated by a random address read. After the 24LC02 receives a data word, it responds with an acknowledgement. As long as the 24LC02 receives an acknowledgement, it will continue to increment the data word address and clock out sequential data words in series.

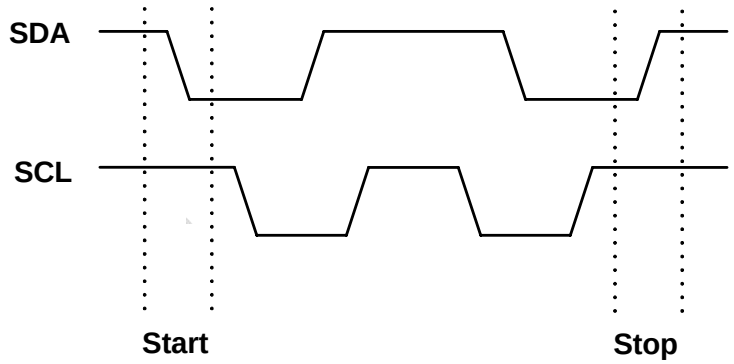



**Figure 10. Start and Stop Definition**

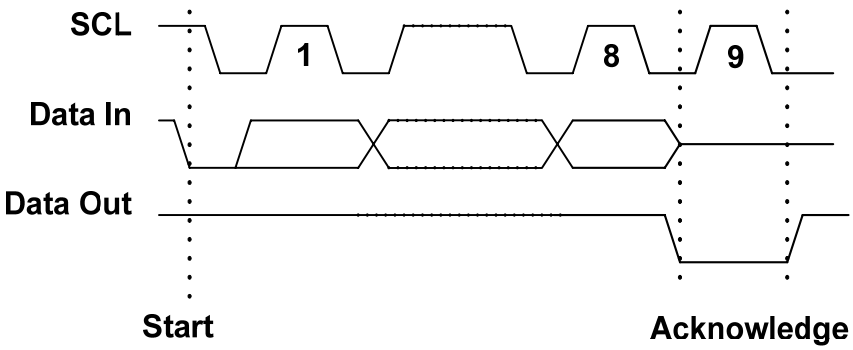



**Figure 11. Output Acknowledge**

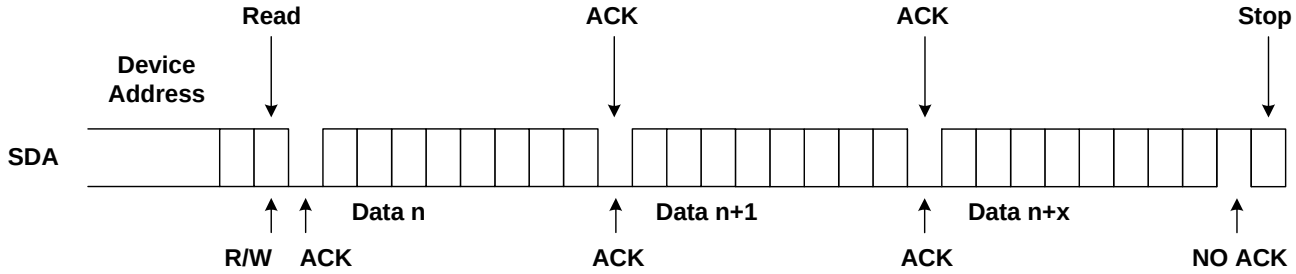



Figure 12. Sequential Read

## 9.3.14. Head-of-Line Blocking

The RTL8309G incorporates an advanced mechanism to prevent Head-Of-Line blocking problems when flow control is disabled. When the flow control function is disabled, the RTL8309G first checks the destination address of the incoming packet. If the destination port is congested, the RTL8309G will discard this packet to avoid blocking the next packet, which is going to a non-congested port.

## 9.3.15. MII Port Diagnostic Loopback

The RTL8309G provides a MAC loopback function on the MII port to detect cable problems or far end existence. When this function is enabled, the RTL8309G will forward local and broadcast packets from the input of the MII port to the output of the MII port, and drop unicast packets from the input of the MII port. The other port can still forward broadcast or unicast packets to the MII port. This is especially useful for router application mass production tests.

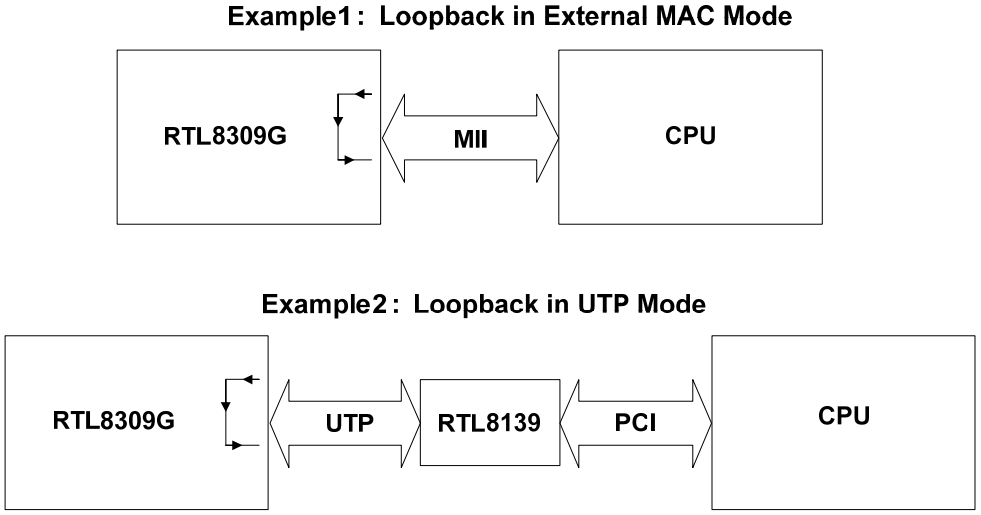



Figure 13. MII Port Loopback

## 9.3.16. Loop Detection

Loops should be avoided between switch applications. The simplest loop as shown below results in: 1) Unicast frame duplication; 2) Broadcast frame multiplication; 3) Address table non-convergence. Frames may be transmitted from Switch1 to Switch2 via Link1, then returned to Switch1 via Link2.

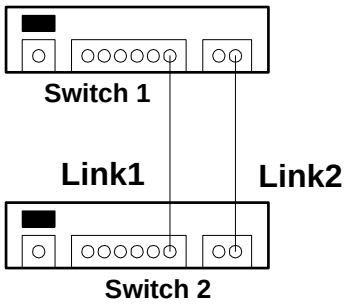



**Figure 14. Loop Example**

When the loop detection function is enabled, the RTL8309G periodically sends out a broadcast packet every 3~5 minutes and automatically detects whether there is a network loop (or bridge loop). If a loop is detected the LoopLED# will be ON (active low or high). The LED goes out when the network loop no longer exists. The Loop frame length is 64 bytes and its format is shown below.

**Table 111. Loop Frame Format**

| | | | | |
|---|---|---|---|---|
| FFFF FFFF FFFF | SID | 8899 | 0300 000…0000 | CRC |

In order to achieve loop detection, each switch device needs a unique SID (the source MAC address). If the EEPROM is not used, a unique SID should be assigned via SMI after reset, and the default SID (0x52 54 4c83 09 b0) should not be used.

## 9.3.17. LEDs (Light Emitting Diodes)

The RTL8309G supports four parallel LEDs for each port, and one special LED (LOOPLED#). Each port has four LED indicator pins. Each pin may have different indicator meanings set by pins LED_MODE[2:0]. Refer to the pin descriptions for details (see

Port LED Pins, on page 13). Upon reset, the RTL8309G supports chip diagnostics and LED functions by blinking all LEDs once for 320ms. This function can be disabled by asserting EN_RST_BLNK to 0.

LED_BLNK_TIME determines the LED blinking period for activity and collision (1 = 43ms and 0 = 120ms).

All LED pins are dual function pins: input operation for configuration upon reset, and output operation for LED after reset. If the pin input is floating upon reset, the pin output is active low after reset. Otherwise, if the pin input is pulled down upon reset, the pin output is active high after reset. Below is an example circuit for LEDs. The typical value for pull-down resistors is 10KΩ.

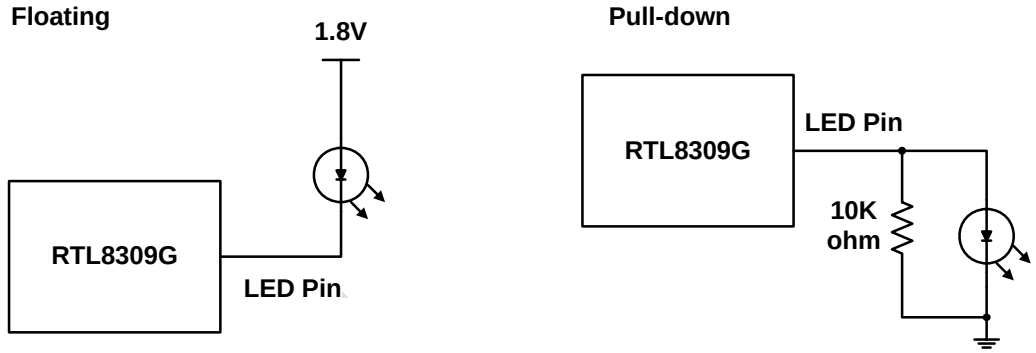



**Figure 15. Floating and Pull-Down of LED Pins**

For two-pin Bi-color LED mode, Bi-color Link/Act and Speed can be used for one Bi-color LED package, which is a single LED package with two LEDs connected in parallel with opposite polarity. As all LED pins are dual function pins, strapping LED pins to high or low will affect their active status. In Bi-color LED mode, the Link/Act and Speed LED pins may both be strapped to high or low but their active status will be opposed.

*Note: For Bi-color LEDs, the 1.8V supply voltage may not be sufficient to turn the LED on. The application schematic in Figure 18, on page 104, illustrates how to directly utilize 7.5 ~ 12V from the DC adapter as the power source for Bi-color LEDs.*

**Table 112. Speed and Bi-Color Link/Act Truth Table**

| | | **Speed:Input=Floating, Active Low. Bi-Color Link/Act: the active status of LED_ADD is the opposite of LED_SPD and does not interact with input upon reset.** | | **Speed:Input=Pull-down, Active High. Bi-Color Link/Act: the active status of LED_ADD is the opposite of LED_SPD and does not interact with input upon reset.** | |
|---|---|---|---|---|---|
| **Indication** | **Bi-Color State** | **Speed** | **Link/Act** | **Speed** | **Link/Act** |
| No Link | Both Off | 1 | 1 | 0 | 0 |
| 100M Link | Green On | 0 | 1 | 1 | 0 |
| 10M Link | Yellow On | 1 | 0 | 0 | 1 |
| 100M Act | Green Flash | 0 | Flash | 1 | Flash |
| 10M Act | Yellow Flash | 1 | Flash | 0 | Flash |

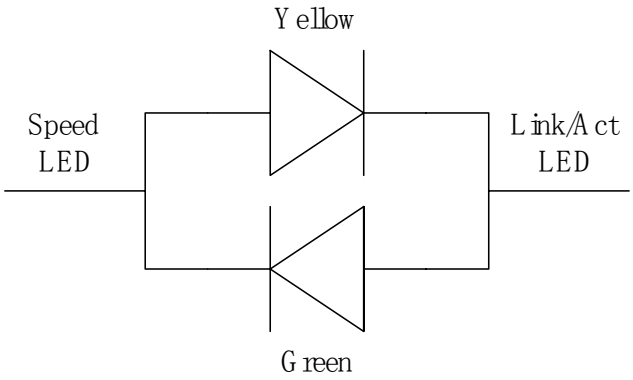



**Figure 16. Two-Pin Bi-Color LED for SPD Floating or Pull-high**

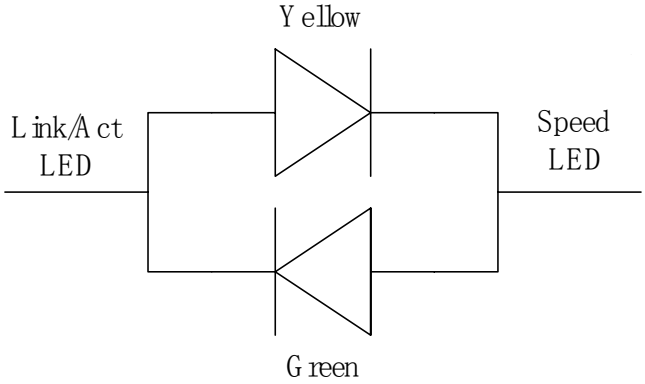



**Figure 17. Two-Pin Bi-Color LED for SPD Pull-down**

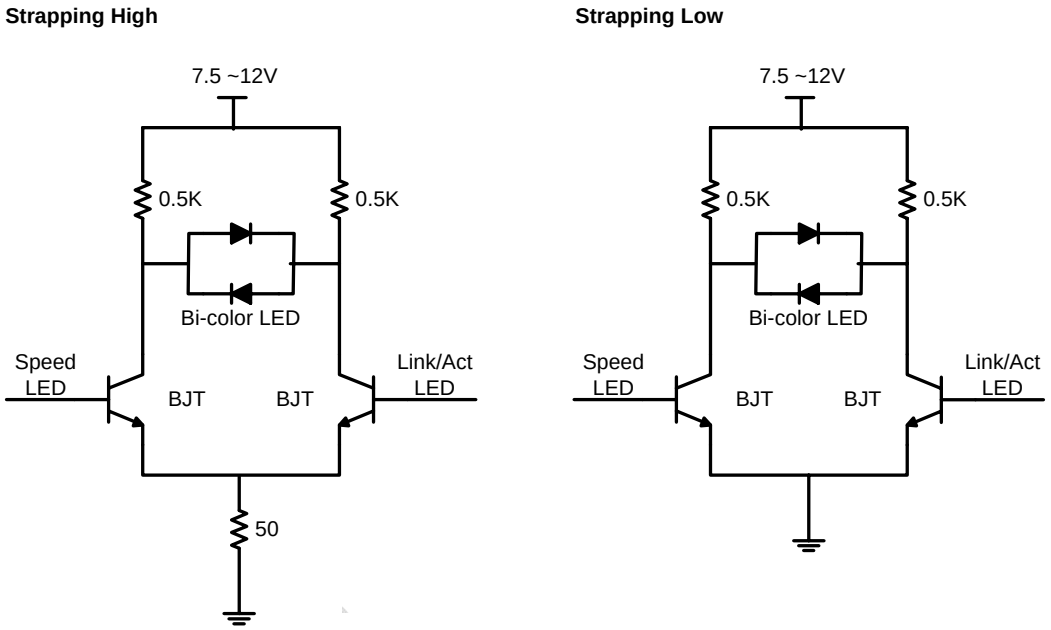



**Figure 18. Bi-Color LED Reference Schematic**

# *9.4. Green Ethernet*

## 9.4.1. Link-On and Cable Length Power Saving

The RTL8309G provides link-on and dynamic detection of cable length and dynamic adjustment of power required for the detected cable length. This feature provides high performance with minimum power consumption.

## 9.4.2. Link-Down Power Saving

The RTL8309G implements link-down power saving on a per-port basis, greatly cutting power consumption when the network cable is disconnected.

# 10. Characteristics

## 10.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability may be affected. All voltages are specified reference to GND unless otherwise specified.

**Table 113. Absolute Maximum Ratings**

| Parameter | Min | Max | Units |
|---|---|---|---|
| Storage Temperature | -55 | 150 | °C |
| Supply Voltage Referenced to GND: VDDD, VDDA, and 1.8V VDDIO | GND-0.5 | +2.16 | V |
| Supply Voltage Referenced to GND: 2.5V VDDIO | GND-0.5 | +3.00 | V |
| Supply Voltage Referenced to GND: 3.3V VDDIO | GND-0.5 | +3.96 | V |
| Digital Input Voltage | GND-0.5 | VDDD | V |
| DC Output Voltage | GND-0.5 | VDDD | V |

## 10.2. Operating Range

**Table 114. Operating Range**

| Parameter | Min | Max | Units |
|---|---|---|---|
| Ambient Operating Temperature (Ta) | 0 | 70 | °C |
| 1.8V VDDD, VDDA, and VDDIO Supply Voltage Range | 1.71 | 1.95 | V |
| 2.5V VDDIO Supply Voltage Range | 2.375 | 2.625 | V |
| 3.3V VDDIO Supply Voltage Range | 3.15 | 3.45 | V |

## 10.3. DC Characteristics

**Table 115. DC Characteristics**

| Parameter | SYM | Condition | Min | Typical | Max | Units |
|---|---|---|---|---|---|---|
| TTL Input High Voltage | $V_{ih}$ | VDDIO = 1.8V<br>VDDIO = 3.3V | 1.5<br>2.0 | -<br>- | -<br>- | V<br>V |
| TTL Input Low Voltage | $V_{il}$ | VDDIO = 1.8V<br>VDDIO = 3.3V | -<br>- | -<br>- | 0.8<br>0.8 | V<br>V |
| TTL Input Current | $I_{in}$ | - | -10 | - | 10 | µA |
| TTL Input Capacitance | $C_{in}$ | - | - | 3 | - | pF |
| Output High Voltage | $V_{oh}$ | VDDIO = 1.8V<br>VDDIO = 3.3V | 1.7<br>2.6 | -<br>- | -<br>3.6 | V<br>V |
| Output Low Voltage | $V_{ol}$ | VDDIO = 1.8V<br>VDDIO = 3.3V | 0.0<br>0.0 | -<br>- | 0.4<br>0.4 | V<br>V |
| Output Three State Leakage Current | $\|I_{OZ}\|$ | - | - | - | 10 | µA |
| **Transmitter, 100Base-TX (1:1 Transformer Ratio)** | | | | | | |
| TX+/- Output Current High | $I_{OH}$ | - | - | - | 40 | mA |
| TX+/- Output Current Low | $I_{OL}$ | - | 0 | - | - | µA |
| **Transmitter, 10Base-T (1:1 Transformer Ratio)** | | | | | | |
| TX+/- Output Current High | $I_{OH}$ | - | - | - | 100 | mA |
| TX+/- Output Current Low | $I_{OL}$ | - | 0 | - | - | µA |
| **Receiver, 100Base-TX** | | | | | | |
| RX+/- Common-Mode Input Voltage | - | - | - | 1.8 | - | V |
| RX+/- Differential Input Resistance | - | - | - | 2.4 | - | kΩ |
| **Receiver, 10Base-T** | | | | | | |
| Differential Input Resistance | - | - | - | 2.4 | - | kΩ |

## 10.4. AC Characteristics

**Table 116. AC Characteristics**

| Parameter | SYM | Condition | Min | Typical | Max | Units |
|---|---|---|---|---|---|---|
| **Transmitter, 100Base-TX** | | | | | | |
| Differential Output Voltage, Peak-to-Peak | $V_{OD}$ | 50Ω from each output to Vcc, Best-fit over 14 bit times | 0.997 | 1.002 | 1.008 | V |
| Differential Output Voltage Symmetry | $V_{OS}$ | 50Ω from each output to Vcc, \|Vp+\|/ \|Vp-\| | 100.8 | 101.3 | 101.9 | % |
| Differential Output Overshoot | $V_{OO}$ | Percent of Vp+ or Vp- | 3.20 | 3.68 | 4.31 | % |
| Rise/Fall Time | $t_r$ ,$t_f$ | 10-90% of Vp+ or Vp- | 3.61 | 3.73 | 3.82 | ns |
| Rise/Fall Time Imbalance | $\|t_r - t_f\|$ | - | 10 | 30 | 80 | ps |
| Duty Cycle Distortion | - | Deviation from best-fit time-grid, 010101 … Sequence | 20 | 40 | 90 | ps |
| Timing Jitter | - | Idle pattern | 675 | 825 | 900 | ns |
| **Transmitter, 10Base-T** | | | | | | |
| Differential Output Voltage, Peak-to-Peak | $V_{OD}$ | 50Ω from each output to Vcc, all pattern | 2.30 | 2.31 | 2.32 | V |
| TP_IDL Silence Duration | - | Period of time from start of TP_IDL to link pulses or period of time between link pulses | 15.72 | 15.73 | 15.76 | ms |
| TD Short Circuit Fault Tolerance | - | Peak output current on TD short circuit for 10 seconds. | 245 | 254 | 273 | mA |
| TD Differential Output Impedance (Return Loss) | - | Return loss from 5MHz to 10MHz for reference resistance of 100Ω. | 24.0 | 24.5 | 25.0 | dB |
| TD Common-Mode Output Voltage | Ecm | Terminate each end with 50Ω resistive load. | 40.2 | 44.3 | 45.1 | mV |
| Transmitter Output Jitter | - | - | 6.4 | 8.5 | 11.5 | ns |
| RD Differential Output Impedance (Return Loss) | - | Return loss from 5MHz to 10MHz for reference resistance of 100Ω. | 24.0 | 24.5 | 25.0 | dB |
| Harmonic Content | - | dB below fundamental, 20 cycles of all ones data | 28.0 | 28.3 | 28.5 | dB |

## 10.5. Digital Timing Characteristics

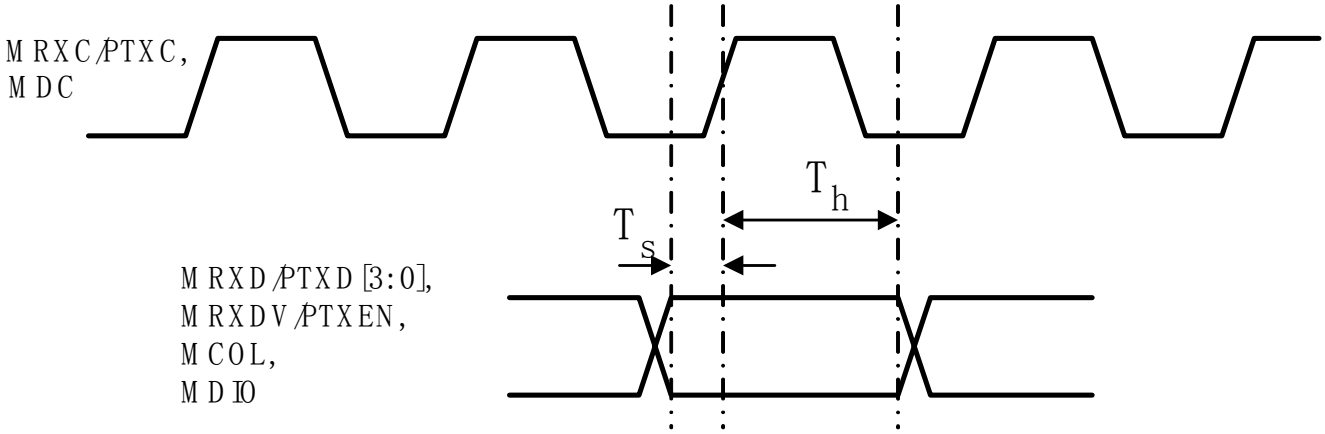



**Figure 19. Reception Data Timing of MII/SNI/SMI Interface**

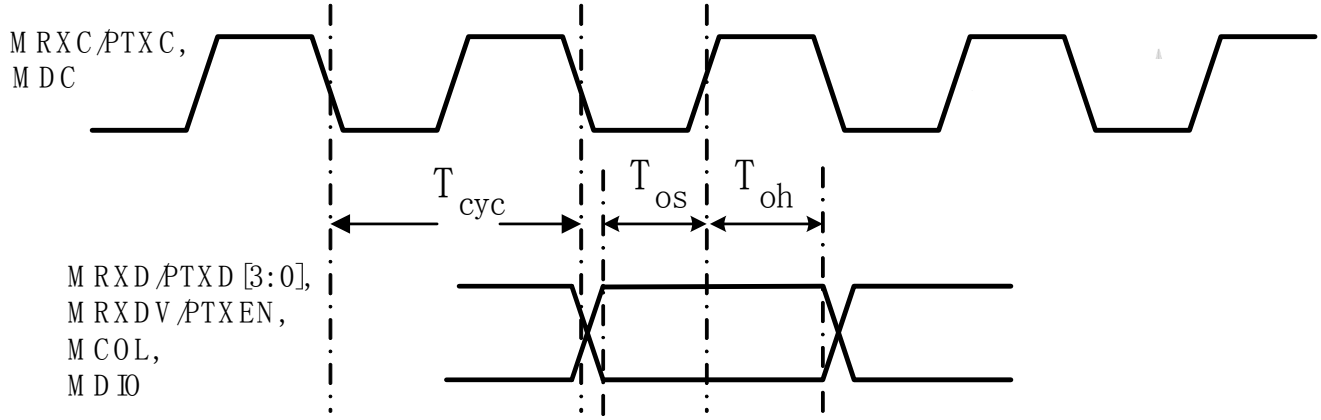



**Figure 20. Transmission Data Timing of MII/SNI/SMI Interface**

**Table 117. Digital Timing Characteristics**

| Parameter | SYM | Condition | I/O | Min | Type | Max | Units |
|---|---|---|---|---|---|---|---|
| **MAC Mode MII Timing** | | | | | | | |
| 100BaseT MTXC/MRXC, MRXC/PTXC | $T_{cyc}$ | MTXC/MRXC, MRXC/PTXC clock cycle time | I | - | 40±50 ppm | - | ns |
| 10BaseT MTXC/MRXC, MRXC/PTXC | $T_{cyc}$ | MTXC/MRXC, MRXC/PTXC clock cycle time | I | - | 400±50 ppm | - | ns |
| MTXD[3:0]/PRXD[3:0], MTXEN/PRXDV Output Setup Time | $T_{os}$ | Output Setup time from REFCLK rising edge to MTXD[3:0]/PRXD[3:0], MTXEN/PRXDV | O | 22 | 24 | 26 | ns |

| Parameter | SYM | Condition | I/O | Min | Type | Max | Units |
|---|---|---|---|---|---|---|---|
| MTXD[3:0]/PRXD[3:0], MTXEN/PRXDV Output Hold Time | $T_{oh}$ | Output Hold time from REFCLK rising edge to MTXD[3:0]/PRXD[3:0], MTXEN/PRXDV | O | 14 | 16 | 18 | ns |
| MRXD[3:0]/PTXD[3:0], MRXDV/PTXEN, MCOL/PCOL Setup Time | $T_s$ | MTXD[3:0]/PRXD[3:0], MRXDV/PTXEN to REFCLK rising edge setup time | I | 4 | - | - | ns |
| MRXD/PTXD, MRXDV/PTXEN, MCOL/PCOL Hold Time | $T_h$ | MTXD[3:0]/PRXD[3:0], MRXDV/PTXEN to REFCLK rising edge hold time | I | 2 | - | - | ns |
| **PHY Mode MII Timing** | | | | | | | |
| 100BaseT MTXC/MRXC, MRXC/PTXC, | $T_{cyc}$ | MTXC/MRXC, MRXC/PTXC, PHY2PTXC, PHY2PRXC clock cycle time | O | - | 40±50 ppm | - | ns |
| 10BaseT MTXC/PRXC, MRXC/PTXC, | $T_{cyc}$ | MTXC/MRXC, MRXC/PTXC, PHY2PTXC, PHY2PRXC clock cycle time | O | - | 400±50 ppm | - | ns |
| MTXD/PRXD[3:0], MTXEN/PRXDV, MCOL/PCOL, Output Setup Time | $T_{os}$ | Output Setup time from REFCLK rising edge to MTXD[3:0]/PRXD[3:0], PHY2PRXD[3:0], MTXEN/PRXDV, PHY2PRXDV MCOL/PCOL, PHY2PCOL | O | 14 | 16 | 18 | ns |
| MTXD/PRXD[3:0], MTXEN/PRXDV, MCOL/PCOL, Output Hold Time | $T_{oh}$ | Output Hold time from REFCLK rising edge to MTXD[3:0]/PRXD[3:0], MTXEN/PRXDV, MCOL/PCOL | O | 22 | 24 | 26 | ns |
| MRXD/PTXD[3:0], MRXDV/PTXEN, Setup Time | $T_s$ | MTXD[3:0]/PRXD[3:0], MRXDV/PTXEN to REFCLK rising edge setup time | I | 4 | - | - | ns |
| MRXD/PTXD[3:0], MRXDV/PTXEN, Hold Time | $T_h$ | MTXD[3:0]/PRXD[3:0], MRXDV/PTXEN to REFCLK rising edge hold time | I | 2 | - | - | ns |
| **PHY Mode SNI Timing** | | | | | | | |
| MTXC/MRXC, MRXC/PTXC | $T_{cyc}$ | MTXC/PRXC, MRXC/PTXC clock cycle time | O | - | 100±50 ppm | - | ns |
| MTXD/PRXD[0], MTXEN/PRXDV, MCOL/PCOL Output Setup Time | $T_{os}$ | Output Setup time from REFCLK rising edge to MTXD[0]/PRXD[0], MTXEN/PRXDV, MCOL/PCOL | O | 28 | 30 | 32 | ns |
| MTXD/PRXD[0], MTXEN/PRXDV, MCOL/PCOL Output Hold Time | $T_{oh}$ | Output Hold time from REFCLK rising edge to MTXD[0]/PRXD[0], MTXEN/PRXDV, MCOL/PCOL | O | 68 | 70 | 72 | ns |
| MRXD/PTXD[0], MRXDV/PTXEN Setup Time | $T_s$ | MTXD[0]/PRXD[0], MRXDV/PTXEN to REFCLK rising edge setup time | I | 4 | - | - | ns |
| MTXD/PRXD[0], MTXEN/PRXDV, MCOL/PCOL Hold Time | $T_h$ | MTXD[0]/PRXD[0], MRXDV/PTXEN to REFCLK rising edge hold time | I | 2 | - | - | ns |
| **LED Timing** | | | | | | | |
| LED On Time | tLEDon | While LED blinking | O | 43 | - | 120 | ms |
| LED Off Time | tLEDoff | While LED blinking | O | 43 | - | 120 | ms |

## 10.6. Thermal Characteristics

Heat generated by the chip causes a temperature rise of the package. If the temperature of the chip (Tj, junction temperature) is beyond the design limits, there will be negative effects on operation and the life of the IC package. Heat dissipation, either through a heat sink or electrical fan, is necessary to provide a reasonable environment (Ta, ambient temperature) in a closed case. As power density increases, thermal management becomes more critical. A method to estimate the possible Ta is outlined below.

Thermal parameters are defined as below according to JEDEC standard JESD 51-2, 51-6:

θja (Thermal resistance from junction to ambient), represents resistance to heat flow from the chip to ambient air. This is an index of heat dissipation capability. A lower θja means better thermal performance.

$\theta ja = (Tj - Ta) / Ph$

Where Tj is the junction temperature

Ta is the ambient temperature

Ph is the power dissipation

ψJT (Thermal resistance from junction to case), represents resistance to heat flow from the chip to the package top case.

$\psi JT = (Tj - Tc) / Ph$, where Tj is the junction temperature.

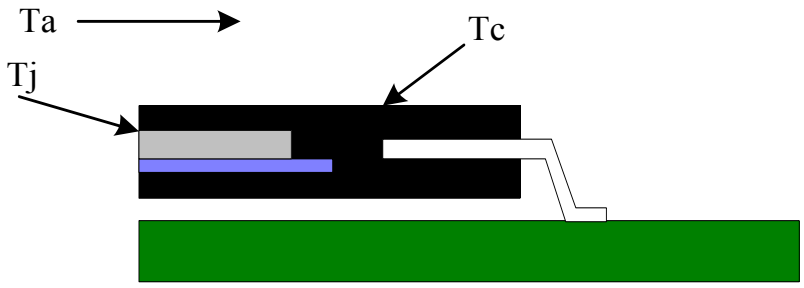



**Figure 21. Cross-section of 128-Pin PQFP**

**Table 118. Thermal Operating Range**

| Parameter | SYM | Condition | Min | Typical | Max | Units |
|---|---|---|---|---|---|---|
| Junction Operating Temperature | Tj | - | 0 | 25 | 125 | °C |
| Ambient Operating Temperature | Ta | - | 0 | 25 | 55 | °C |

**Table 119. Thermal Resistance**

| Parameter | SYM | Condition | Min | Typical | Max | Units |
|---|---|---|---|---|---|---|
| Thermal Resistance: Junction to Ambient | θja | 2 layer PCB, 0 ft/s airflow, ambient temperature 25°C | - | 36.7 | - | °C/W |
| Thermal Resistance: Junction to Case | ψJT | 2 layer PCB, 0 ft/s airflow, ambient temperature 25°C | - | 6.1 | - | °C/W |

*Note: PCB conditions. Dimensions: 85 x 110mm. Thickness: 1.6mm.*

# 11. Design and Layout

In order to achieve maximum performance using the RTL8309G, good design attention is required throughout the design and layout process. The following are some recommendations on how to implement a high-performance system.

### General Guidelines

Provide a good power source, minimizing noise from switching power supply circuits (<50mV).

Keep power and ground noise levels below 50mV.

Verify the ability of critical components, e.g., clock source and transformer, to meet application requirements.

Use bulk capacitors (4.7µF-10µF) between the power and ground planes.

Use 0.1µF de-coupling capacitors to reduce high-frequency noise on the power and ground planes.

Keep de-coupling capacitors as close as possible to the RTL8309G.

### Differential Signal Layout Guidelines

Keep differential pairs as close as possible and route both traces as identically as possible.

Avoid vias and layer changes if possible.

Keep transmit and receive pairs away from each other. Run orthogonal or separate by a ground plane.

Keep each different pair on the same plane.

### Clock Circuit

The clock should be 25M 100ppm with jitter less than 0.5ns.

If possible, surround the clock by ground trace to minimize high-frequency emissions.

### Power Planes

Divide the power plane into 1.8V digital, 1.8V analog.

Use 0.1µF decoupling capacitors and bulk capacitors between each power plane and ground plane.

Place two 47µF bulk capacitors on the device-side (primary) center tap of the transformer.

### Ground Plane

Keep the system ground region as one continuous, unbroken plane that extends from the primary side of the transformer to the rest of the board.

Place a moat (gap) between the system ground and chassis ground.

Ensure the chassis ground area is voided at some point such that no ground loop exists on the chassis ground area.

### Transformer Options

The RTL8309G can use a transformer that supports auto crossover detection and auto correction with a 1:1 turn ratio on both transmit and receive paths. There are many venders improving their transformer design to meet the RTL8309G's requirement.

| Vendor | Quad |
|---|---|
| Pulse | H1164 |
| Magnetic 1 | ML164 |
| BothHand | 40ST1041AX |
| Macronics | HS2275 |

The center taps on the primary side of the transmit and receive paths in the transformer should be connected together inside the transformer and provide one common external pin (Figure 22). This common pin should connect to 1.8V directly and connect to ground via a 0.1µF capacitor as shown in Figure 22. This schematic will force the signal on the primary side to bias at 1.8V.

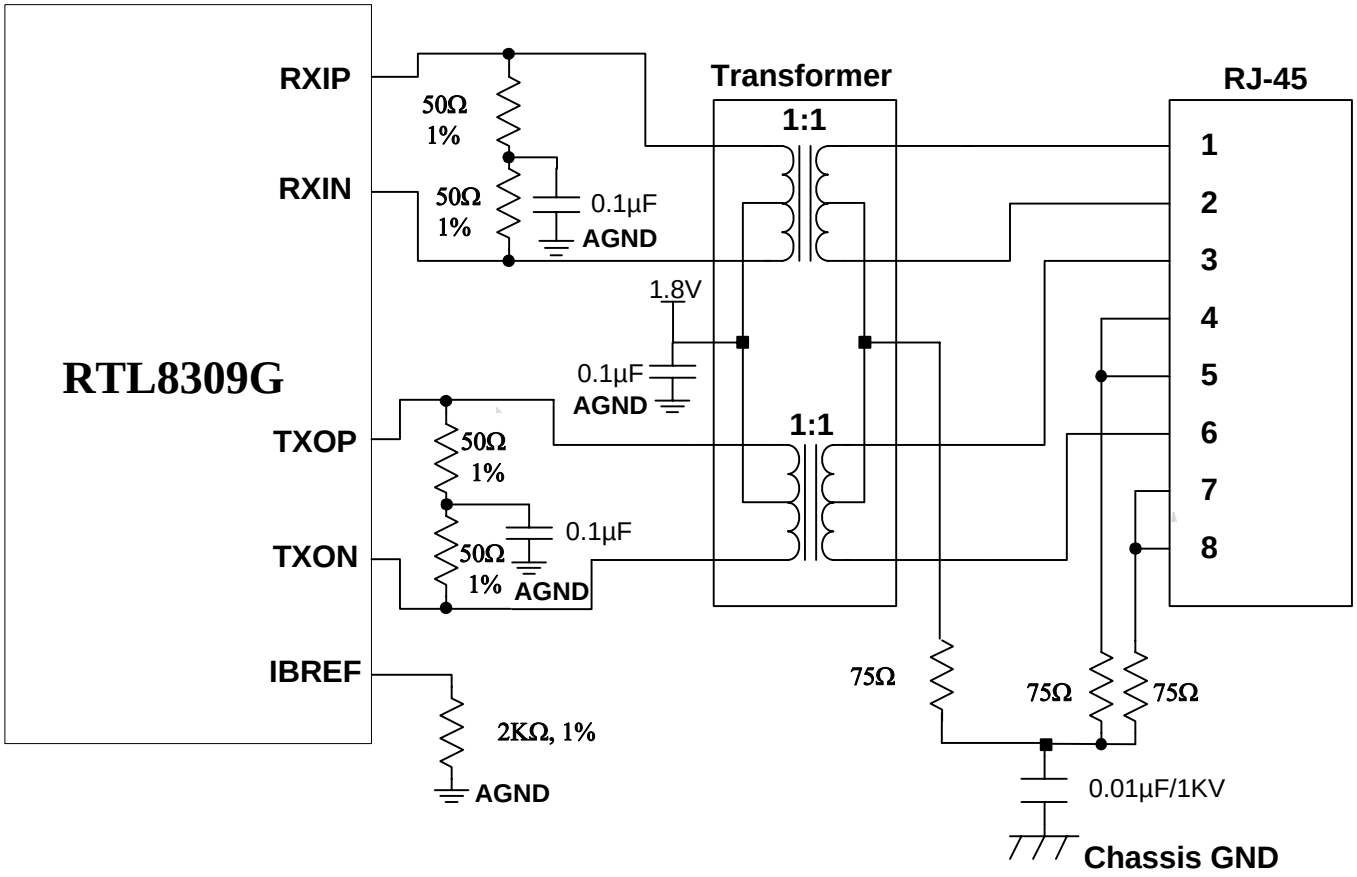



**Figure 22. Application for Transformer with Connected Central Tap**

### Bob Smith Termination

'Bob Smith' termination is often provided for the unused signal pairs of RJ-45 pins 4 & 5, and 7 & 8 to minimize the common mode noise induced from RJ-45 pins 1 & 2, and 3 & 6.

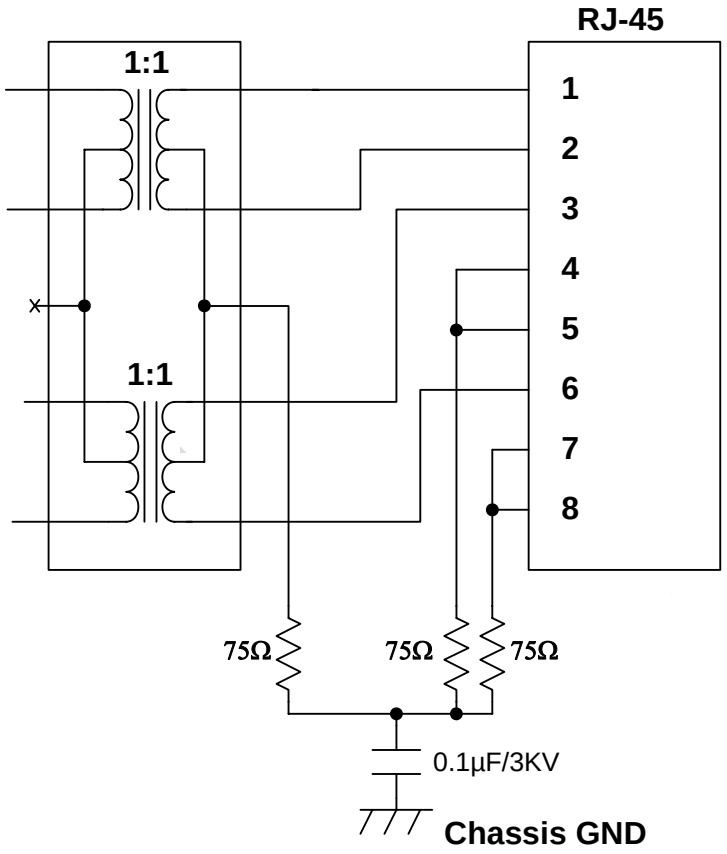
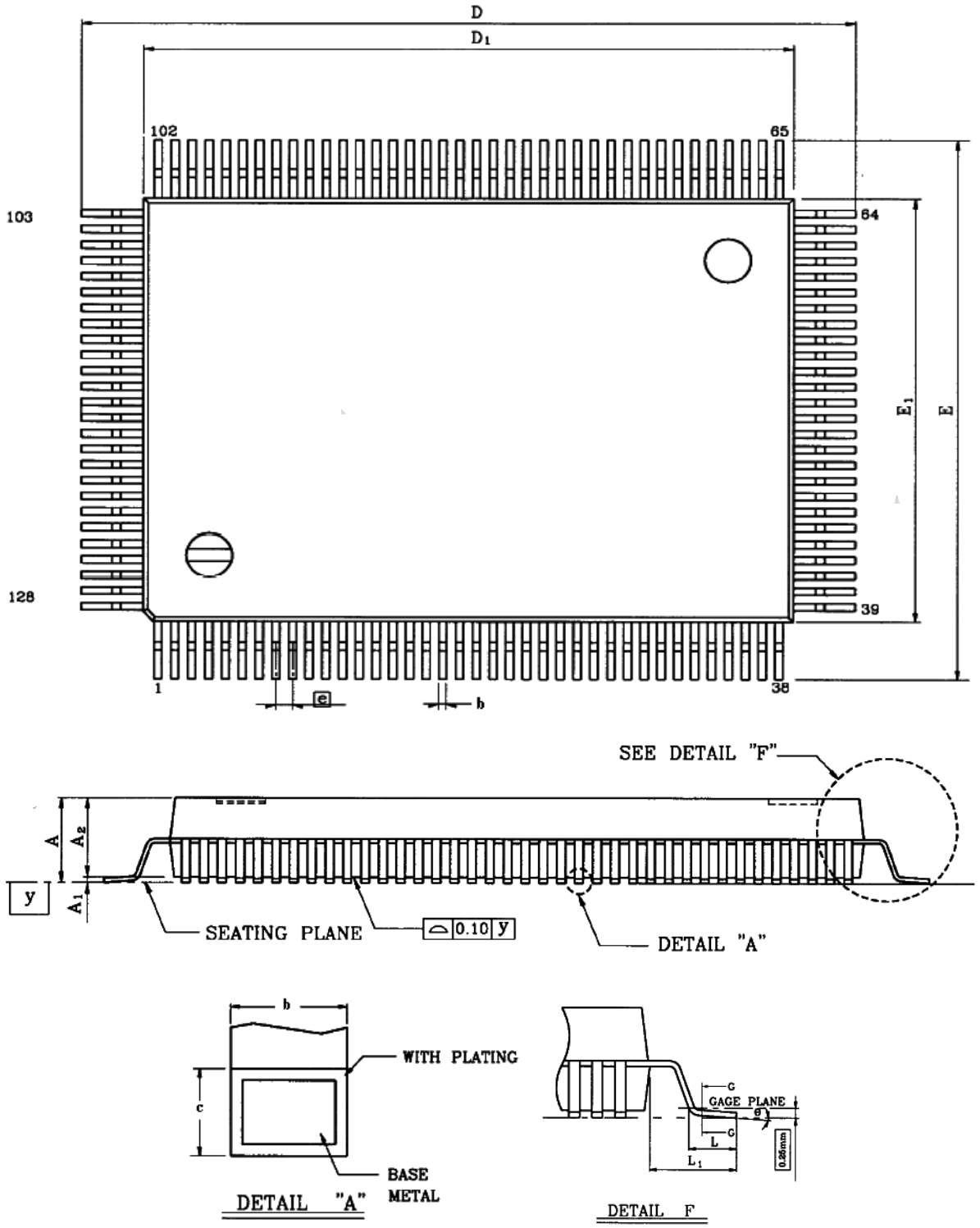



**Figure 23. Bob Smith Termination**

# 12. Mechanical Dimensions




See the Mechanical Dimensions notes on the next page.

## 12.1. Notes for Mechanical Dimensions

| Symbol | Dimensions in mm | | | Dimensions in inch | | |
|---|---|---|---|---|---|---|
| | Min | Typical | Max | Min | Typical | Max |
| A | - | - | 3.40 | - | - | 0.134 |
| A1 | 0.25 | - | - | 0.01 | - | - |
| A2 | 2.50 | 2.72 | 2.97 | 0.101 | 0.107 | 0.117 |
| b | 0.10 | 0.20 | 0.30 | 0.004 | 0.008 | 0.012 |
| c | 0.09 | - | 0.23 | 0.004 | - | 0.008 |
| D | 23.2 BSC | | | 0.913 BSC | | |
| $D_1$ | 20.00 BSC | | | 0.787 BSC | | |
| E | 17.20 BSC | | | 0.677 BSC | | |
| $E_1$ | 14.00 BSC | | | 0.551 BSC | | |
| e | 0.5 BSC | | | 0.20 BSC | | |
| L | 0.65 | 0.88 | 1.03 | 0.026 | 0.035 | 0.041 |
| $L_1$ | 1.60 BSC | | | 0.063 BSC | | |
| y | - | - | 0.10 | - | - | 0.004 |
| θ | 0° | - | 12° | 0° | - | 12° |

1. Dimensions D & E do not include interlead flash.
2. Dimension b does not include dambar rotrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. Should be based on final visual inspection.

| TITLE: -CU L/F, FOOTPRINT 3.2 mm | | | |
|---|---|---|---|
| LEADFRAME MATERIAL: | | | |
| APPROVE | | DOC. NO. | |
| | | VERSION | |
| | | PAGE | |
| | | | |
| | | DATE | |
| REALTEK SEMICONDUCTOR CORP. | | | |

# 13. Ordering Information

**Table 120. Ordering Information**

| Part Number | Package | Status |
|---|---|---|
| RTL8309G-GR | 128-Pin PQFP with 'Green' Package | Production |

*Note: See page 7 for package identification information.*

**Realtek Semiconductor Corp.**

**Headquarters**

No. 2, Innovation Road II

Hsinchu Science Park, Hsinchu 300, Taiwan

Tel.: +886-3-578-0211. Fax: +886-3-577-6047

www.realtek.com