

ISL8009A

1.5A Low Quiescent Current 1.6MHz High Efficiency Synchronous Buck Regulator

FN6656  
Rev 3.00  
February 28, 2013

The ISL8009A is a high efficiency, monolithic, synchronous step-down DC/DC regulator that can deliver up to 1.5A continuous output current. It is optimized for generating low output voltages down to 0.8V. The supply voltage range of 2.7V to 5.5V allows for the use of single Li+cell, three NiMH cells or a regulated 5V input. The ISL8009A uses current mode control architecture to deliver very low duty cycle operation at high frequency with fast transient response and excellent loop stability. It has flexible operation mode selection of forced PWM mode and automatic PFM/PWM with as low as 17µA quiescent current, achieving high power conversion efficiency under light load condition, hence maximizing battery life. High 1.6MHz pulse-width modulation (PWM) switching frequency allows the use of small external components.

The ISL8009A integrates a pair of low ON-resistance P-Channel and N-Channel internal MOSFETs to maximize efficiency and minimize external component count. The 100% duty-cycle operation allows less than 400mV dropout voltage at 1.5A output current.

The ISL8009A offers a 2ms Power-On-Reset (POR) timer at power-up. The timer output can be reset by RSI. When shutdown, ISL8009A discharges the output capacitor through a 100Ω resistor. Other features include internal digital soft-start, enable for power sequence, overcurrent protection, and thermal shutdown.

The ISL8009A is offered in a 2mmx3mm 8 Ld DFN package with 1mm maximum height. The complete converter occupies less than 1cm<sup>2</sup> area.

**Features**

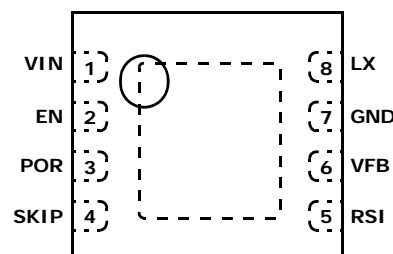
- High Efficiency Synchronous Buck Regulator with up to 95% Efficiency
- 2ms Reset Timer
- 2.7V to 5.5V Supply Voltage
- 3% Output Accuracy Over-Temperature/Load/Line
- 1.5A Guaranteed Output Current
- 17µA Quiescent Supply Current in PFM Mode
- Selectable Forced PWM Mode and PFM Mode
- Less Than 1µA Logic Controlled Shutdown Current
- 90% Maximum Duty Cycle for Lowest Dropout at 1.5A
- Internal Current Mode Compensation
- Internal Digital Soft-Start
- Peak Current Limiting, Short Circuit Protection
- Over-Temperature Protection
- Enable
- Soft Discharge Disable
- Small 8 Ld 2mmx3mm DFN
- Pb-Free (RoHS Compliant)

**Applications**

- DC/DC POL Modules
- µC/µP, FPGA and DSP Power
- Plug-in DC/DC Modules for Routers and Switchers
- Portable Instruments
- Test and Measurement Systems

**Pin Configuration**

ISL8009A  
(8 LD DFN)  
TOP VIEW



\*EXPOSED PAD MUST BE CONNECTED TO THE GND PIN\*

## Ordering Information

| PART NUMBER<br>(Notes 1, 2, 3) | PART<br>MARKING | TEMP. RANGE<br>(°C) | PACKAGE<br>(Pb-free) | PKG.<br>DWG. # |
|--------------------------------|-----------------|---------------------|----------------------|----------------|
| ISL8009AIRZ-T                  | 09A             | -40 to +85          | 8 Ld 2x3 DFN         | L8.2x3         |
| ISL8009AIRZ-TK                 | 09A             | -40 to +85          | 8 Ld 2x3 DFN         | L8.2x3         |
| ISL8009AIRZ-T7A                | 09A             | -40 to +85          | 8 Ld 2x3 DFN         | L8.2x3         |

### NOTES:

1. Please refer to [TB347](#) for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for [ISL8009A](#). For more information on MSL please see techbrief [TB363](#).

**Absolute Maximum Ratings** (Reference to GND)

|                             |                          |
|-----------------------------|--------------------------|
| Supply Voltage ( $V_{IN}$ ) | -0.3V to 6.5V            |
| EN, RSI, SKIP, VFB, POR     | -0.3V to $V_{IN} + 0.3V$ |
| LX                          | -1.5V to 6.5V            |
| VFB                         | -0.3V to 2.7V            |

**Thermal Information**

|                              |   |                                 |
|------------------------------|---|---------------------------------|
| Thermal Resistance (Typical) | $\theta_{JA}$ ( $^{\circ}C/W$ )   | $\theta_{JC}$ ( $^{\circ}C/W$ ) |
| 8 Ld 2x3 DFN (Notes 4, 5)    | 55  | 5.5                             |
| Junction Temperature Range   | -55 $^{\circ}C$ to +125 $^{\circ}C$   |                                 |
| Storage Temperature Range    | -65 $^{\circ}C$ to +150 $^{\circ}C$   |                                 |
| Pb-Free Reflow Profile       | see link below<br><a href="http://www.intersil.com/pbfree/Pb-FreeReflow.asp">http://www.intersil.com/pbfree/Pb-FreeReflow.asp</a> |                                 |

**Recommended Operating Conditions**

|                           |                                    |
|---------------------------|------------------------------------|
| VIN Supply Voltage Range  | 2.7V to 5.5V                       |
| Load Current Range        | 0A to 1.5A                         |
| Ambient Temperature Range | -40 $^{\circ}C$ to +85 $^{\circ}C$ |

**CAUTION:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

**NOTES:**

- $\theta_{JA}$  is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief [TB379](#).
- For  $\theta_{JC}$ , the "case temp" location is the center of the exposed metal pad on the package underside.

**Electrical Specifications** Typical specifications are measured at the following conditions:  $T_A = +25^{\circ}C$ , EN = VIN, RSI = SKIP = 0V,  $V_{IN} = 5V$ , L = 2.2 $\mu H$ ,  $C_1 = C_2 = 20\mu F$ ,  $I_{OUT} = 0A$  to 1.5A. See "Typical Applications" on page 9.

| PARAMETER                           | SYMBOL     | TEST CONDITIONS   | MIN<br>(Note 7) | TYP  | MAX<br>(Note 7) | UNITS     |
|-------------------------------------|------------|---|-----------------|------|-----------------|-----------|
| <b>INPUT SUPPLY</b>                 |            |   |                 |      |                 |           |
| VIN Undervoltage Lockout Threshold  | $V_{UVLO}$ | Rising  | -               | 2.5  | 2.7             | V         |
|                                     |            | Falling   | 2.2             | 2.4  | -               | V         |
| Quiescent Supply Current            | $I_{VIN}$  | SKIP = $V_{IN}$ , no load at the output   | -               | 17   | 30              | $\mu A$   |
|                                     |            | SKIP = $V_{IN}$ , no load at the output and no switches switching, design info only | -               | 15   | -               | $\mu A$   |
|                                     |            | SKIP = GND, no load at the output   | -               | 3.7  | 6               | mA        |
| Shutdown Supply Current             | $I_{SD}$   | $V_{IN} = 5.5V$ , EN = low  | -               | 0.1  | 2               | $\mu A$   |
| <b>OUTPUT REGULATION</b>            |            |   |                 |      |                 |           |
| VFB Regulation Voltage              | $V_{VFB}$  |   | 0.784           | 0.8  | 0.816           | V         |
| VFB Bias Current                    | $I_{VFB}$  | VFB = 0.75V   | -               | 0.1  | -               | $\mu A$   |
| Output Voltage Accuracy             |            | $V_{IN} = V_O + 0.5V$ to 5.5V, $I_O = 0A$ to 1A (Note 6)                            | -3              | -    | 3               | %         |
| Line Regulation                     |            | $V_{IN} = V_O + 0.5V$ to 5.5V (minimal 2.7V)  | -               | 0.2  | -               | %/V       |
| <b>COMPENSATION</b>                 |            |   |                 |      |                 |           |
| Error Amplifier Trans-Conductance   |            | Adjustable version, design info only  | -               | 20   | -               | $\mu A/V$ |
| <b>LX</b>                           |            |   |                 |      |                 |           |
| P-Channel MOSFET ON-Resistance      |            | $V_{IN} = 5.5V$ , $I_O = 200mA$   | -               | 0.12 | 0.22            | $\Omega$  |
|                                     |            | $V_{IN} = 2.7V$ , $I_O = 200mA$   | -               | 0.16 | 0.27            | $\Omega$  |
| N-Channel MOSFET ON-Resistance      |            | $V_{IN} = 5.5V$ , $I_O = 200mA$   | -               | 0.11 | 0.22            | $\Omega$  |
|                                     |            | $V_{IN} = 2.7V$ , $I_O = 200mA$   | -               | 0.15 | 0.27            | $\Omega$  |
| P-Channel MOSFET Peak Current Limit | $I_{PK}$   |   | 1.8             | 2.1  | 2.6             | A         |
| LX Maximum Duty Cycle               |            | $I_O = 1.5A$  | 90              | -    | -               | %         |
| PWM Switching Frequency             | $f_S$      |   | 1.35            | 1.6  | 1.75            | MHz       |
| LX Minimum On-Time                  |            | SKIP = low (forced PWM mode)  | -               | 70   | 100             | ns        |
| Soft-Start-Up Time                  |            |   | -               | 1.1  | -               | ms        |
| Soft-Discharge Resistor             |            | Enable = 0  | 80              | 100  | 120             | $\Omega$  |

**Electrical Specifications** Typical specifications are measured at the following conditions:  $T_A = +25^\circ\text{C}$ ,  $EN = VIN$ ,  $RSI = SKIP = 0V$ ,  $V_{IN} = 5V$ ,  $L = 2.2\mu\text{H}$ ,  $C_1 = C_2 = 20\mu\text{F}$ ,  $I_{OUT} = 0A$  to  $1.5A$ . See "Typical Applications" on page 9.

| PARAMETER                                   | SYMBOL | TEST CONDITIONS                          | MIN<br>(Note 7) | TYP  | MAX<br>(Note 7) | UNITS            |
|---|--------|--|-----------------|------|-----------------|------------------|
| <b>POR</b>                                  |        |  |                 |      |                 |                  |
| Output Low Voltage                          |        | Sinking 1mA, VFB = 0.7V                  | -               | -    | 0.3             | V                |
| Delay Time                                  |        |  | -               | 2    | -               | ms               |
| POR Pin Leakage Current                     |        | POR = VIN = 3.6V                         | -               | 0.01 | 0.1             | $\mu\text{A}$    |
| Minimum Supply Voltage for Valid POR Signal |        |  | 1.2             | -    | -               | V                |
| Internal PGOOD Low Rising Threshold         |        | Percentage of nominal regulation voltage | 89.5            | 92   | 94.5            | %                |
| Internal PGOOD Low Falling Threshold        |        | Percentage of nominal regulation voltage | 85              | 88   | 91              | %                |
| Internal PGOOD High Rising Threshold        |        | Percentage of nominal regulation voltage | 108             | 112  | 114             | %                |
| Internal PGOOD High Falling Threshold       |        | Percentage of nominal regulation voltage | 104             | 107  | 110             | %                |
| Internal PGOOD Delay Time                   |        |  | -               | 6.5  | -               | $\mu\text{s}$    |
| <b>EN, SKIP, RSI</b>                        |        |  |                 |      |                 |                  |
| Logic Input Low                             |        |  | -               | -    | 0.4             | V                |
| Logic Input High                            |        |  | 1.4             | -    | -               | V                |
| Logic Input Leakage Current                 |        | Pulled up to 5.5V                        | -               | 0.1  | 1               | $\mu\text{A}$    |
| Thermal Shutdown                            |        |  | -               | 140  | -               | $^\circ\text{C}$ |
| Thermal Shutdown Hysteresis                 |        |  | -               | 25   | -               | $^\circ\text{C}$ |

## NOTES:

- Limits established by characterization and are not production tested.
- Parameters with MIN and/or MAX limits are 100% tested at  $+25^\circ\text{C}$ , unless otherwise specified. Temperature limits established by characterization and are not production tested.

## Pin Descriptions

### VIN

Input supply voltage. Connect a  $10\mu\text{F}$  ceramic capacitor to power ground.

### EN

Regulator enable pin. Enable the output when driven to high. Shutdown the chip and discharge output capacitor when driven to low. Do not leave this pin floating.

### POR

2ms timer output. At power-up or EN HI, this output is a 2ms delayed Power-Good signal for the output voltage. This output can be reset by a low RSI signal. 2ms starts when RSI goes to high.

### SKIP

Mode Selection pin. Connect to logic high or input voltage VIN for PFM mode; connect to logic low or ground for forced PWM mode. Do not leave this pin floating.

### LX

Switching node connection. Connect to one terminal of inductor.

### GND

System ground.

### VFB

Buck regulator output feedback. Connect to the output through a resistor divider for adjustable output voltage (ISL8009A-ADJ). For preset output voltage, connect this pin to the output.

### RSI

This input resets the 2ms timer. When the output voltage is within the PGOOD window, an internal timer is started and generates a POR signal 2ms later when RSI is low. A high RSI resets POR and RSI high to low transition restarts the internal counter if the output voltage is within the window, otherwise the counter is reset by the output voltage condition.

### Exposed Pad

The exposed pad must be connected to the GND pin for proper electrical performance. The exposed pad must also be connected to as much as possible for optimal thermal performance.

# Typical Operating Performance

(Unless otherwise noted, operating conditions are:  $T_A = +25^\circ\text{C}$ ,  $V_{IN} = 5\text{V}$ ,  $EN = V_{IN}$ ,  $RSI = SKIP = 0\text{V}$ ,  $L = 2.2\mu\text{H}$ ,  $C_1 = 20\mu\text{F}$ ,  $C_2 = 20\mu\text{F}$ ,  $I_{OUT} = 0\text{A}$ )

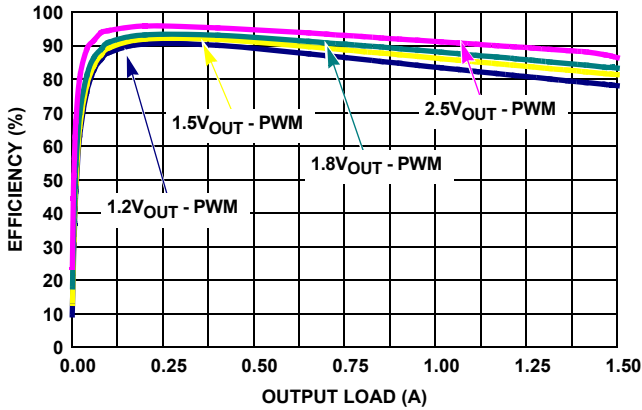


FIGURE 1. EFFICIENCY vs LOAD,  $V_{IN} = 3.3\text{V PWM}$

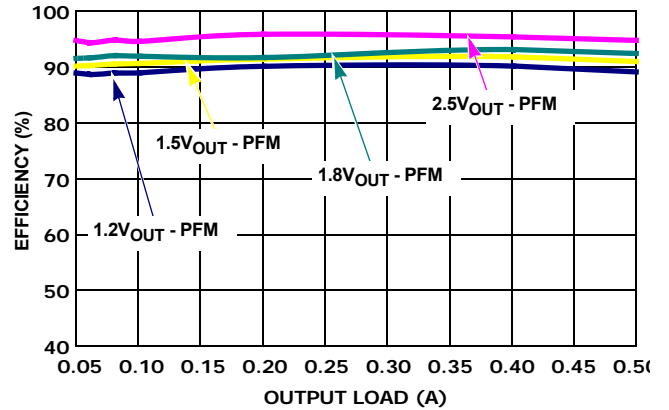


FIGURE 2. EFFICIENCY vs LOAD,  $V_{IN} = 3.3\text{V PFM}$

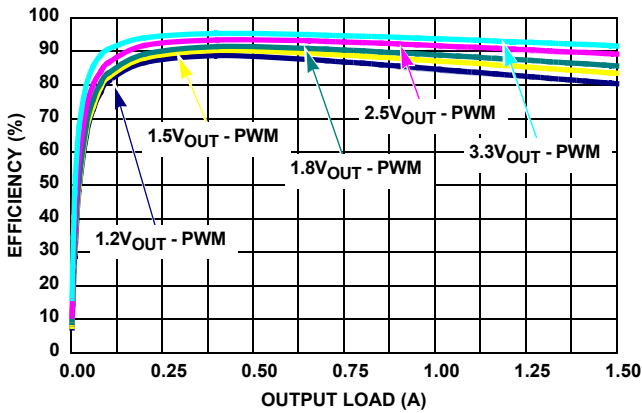


FIGURE 3. EFFICIENCY vs LOAD,  $V_{IN} = 5\text{V PWM}$

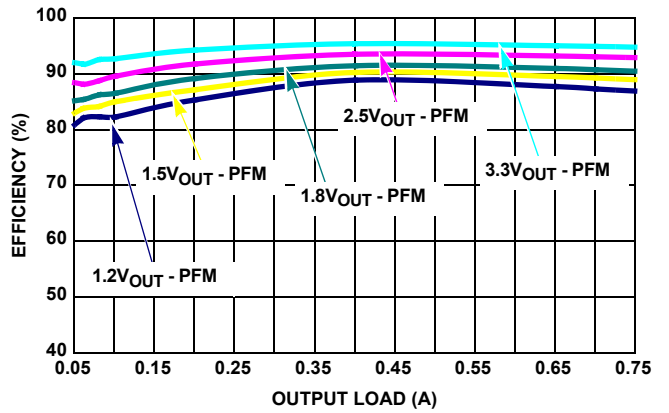


FIGURE 4. EFFICIENCY vs LOAD,  $V_{IN} = 5\text{V PFM}$

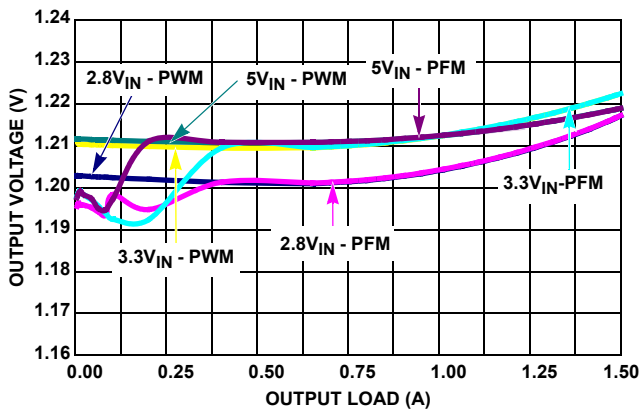


FIGURE 5.  $V_{OUT}$  REGULATION vs LOAD,  $V_{OUT} = 1.2\text{V}$

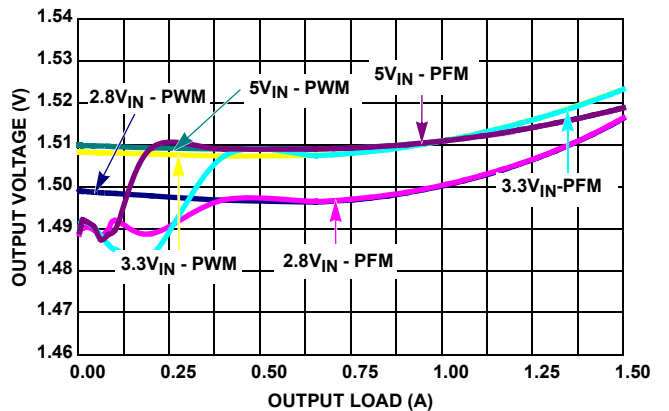


FIGURE 6.  $V_{OUT}$  REGULATION vs LOAD,  $V_{OUT} = 1.5\text{V}$

# Typical Operating Performance

(Unless otherwise noted, operating conditions are:  $T_A = +25^\circ\text{C}$ ,  $V_{IN} = 5\text{V}$ ,  $EN = V_{IN}$ ,  $RSI = \text{SKIP} = 0\text{V}$ ,  $L = 2.2\mu\text{H}$ ,  $C_1 = 20\mu\text{F}$ ,  $C_2 = 20\mu\text{F}$ ,  $I_{OUT} = 0\text{A}$ ) (Continued)

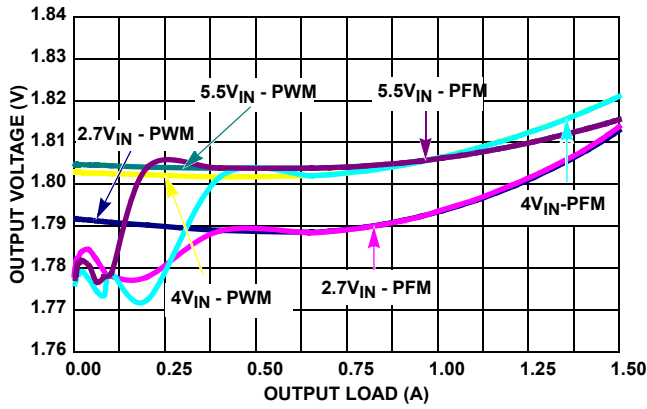


FIGURE 7.  $V_{OUT}$  REGULATION vs LOAD,  $V_{OUT} = 1.8\text{V}$

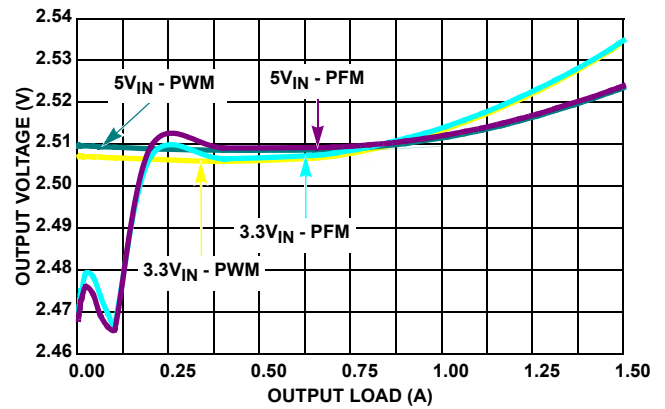


FIGURE 8.  $V_{OUT}$  REGULATION vs LOAD,  $V_{OUT} = 2.5\text{V}$

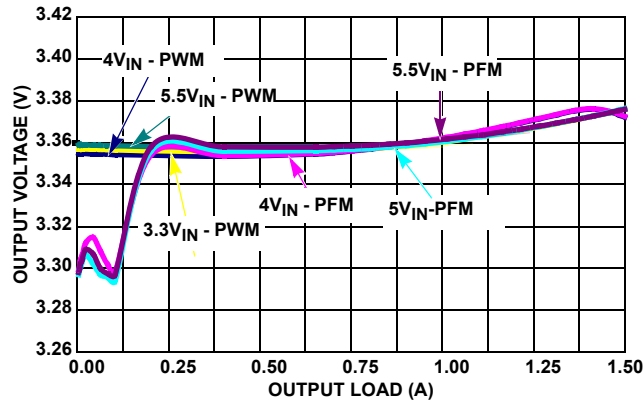


FIGURE 9.  $V_{OUT}$  REGULATION vs LOAD,  $V_{OUT} = 3.3\text{V}$

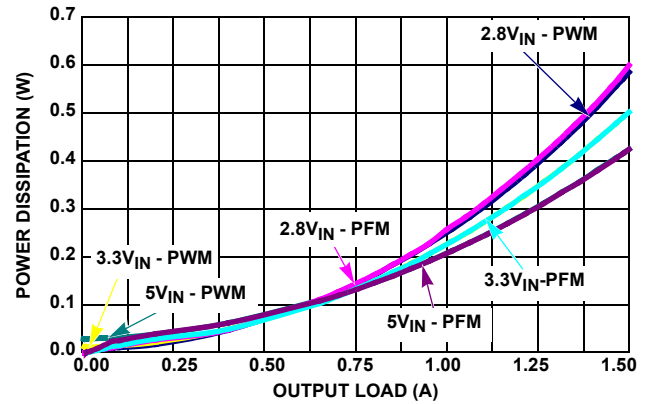


FIGURE 10. POWER DISSIPATION vs LOAD, 1.6 MHz,  $V_{OUT} = 1.8\text{V}$

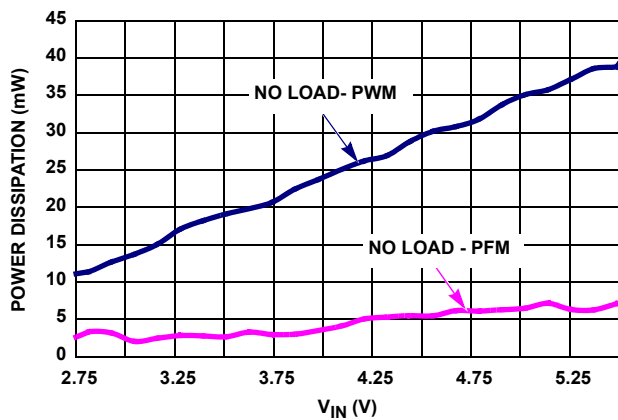


FIGURE 11. POWER DISSIPATION vs  $V_{IN}$  AT NO LOAD,  $V_{OUT} = 1.8\text{V}$

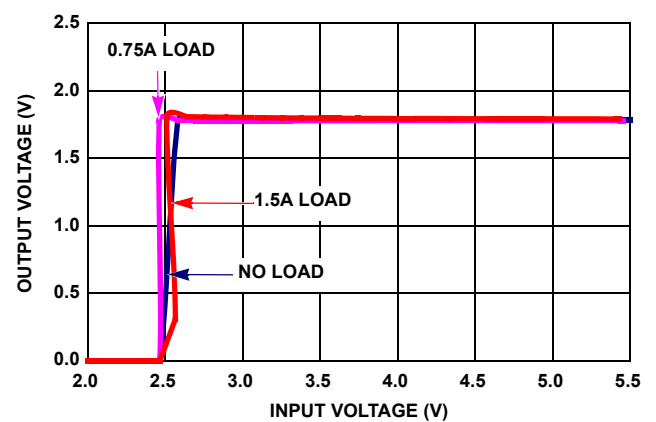


FIGURE 12. OUTPUT VOLTAGE REGULATION vs  $V_{IN}$  PWM MODE

# Typical Operating Performance

(Unless otherwise noted, operating conditions are:  $T_A = +25^\circ\text{C}$ ,  $V_{IN} = 5\text{V}$ ,  $EN = V_{IN}$ ,  $RSI = SKIP = 0\text{V}$ ,  $L = 2.2\mu\text{H}$ ,  $C_1 = 20\mu\text{F}$ ,  $C_2 = 20\mu\text{F}$ ,  $I_{OUT} = 0\text{A}$ ) (Continued)

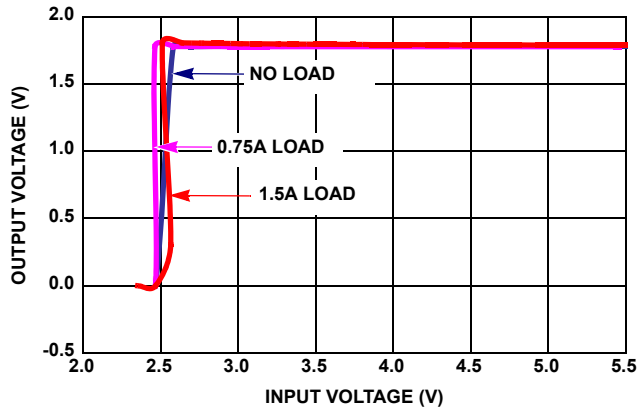


FIGURE 13. OUTPUT VOLTAGE REGULATION vs  $V_{IN}$  SKIP MODE

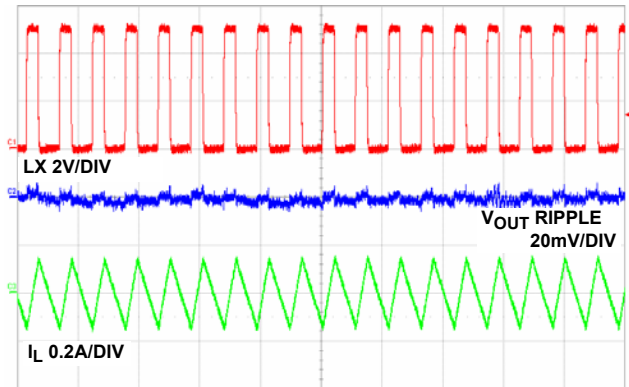


FIGURE 14. STEADY STATE OPERATION AT NO LOAD (PWM),  $1\mu\text{s}/\text{DIV}$

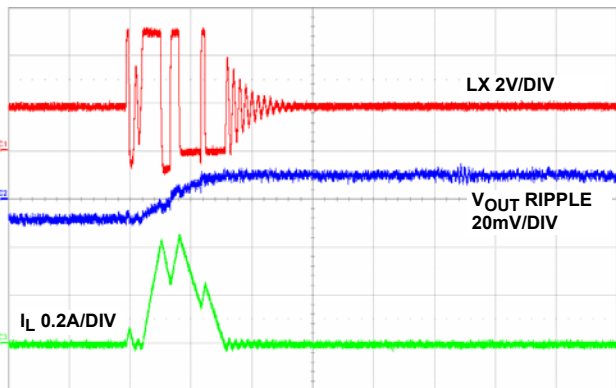


FIGURE 15. STEADY STATE OPERATION AT NO LOAD (PFM),  $1\mu\text{s}/\text{DIV}$

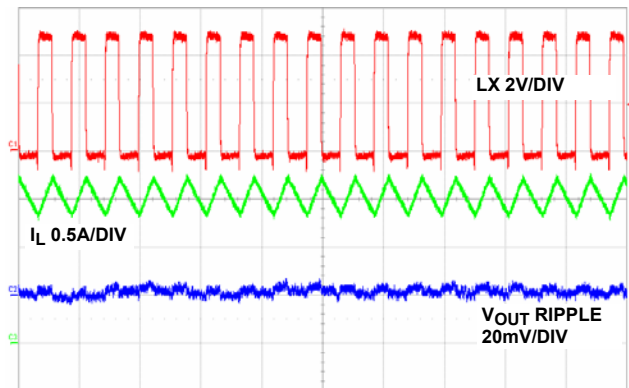


FIGURE 16. STEADY STATE OPERATION WITH FULL LOAD,  $1\mu\text{s}/\text{DIV}$

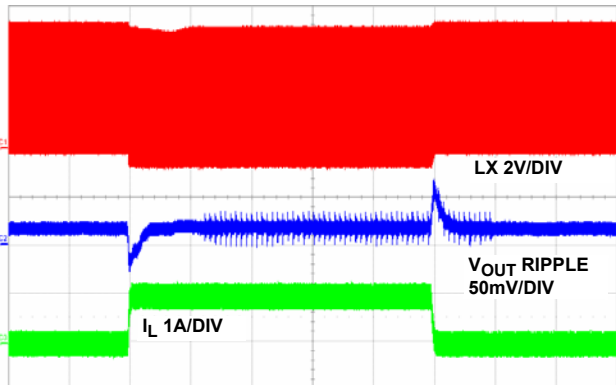


FIGURE 17. LOAD TRANSIENT (PWM),  $200\mu\text{s}/\text{DIV}$

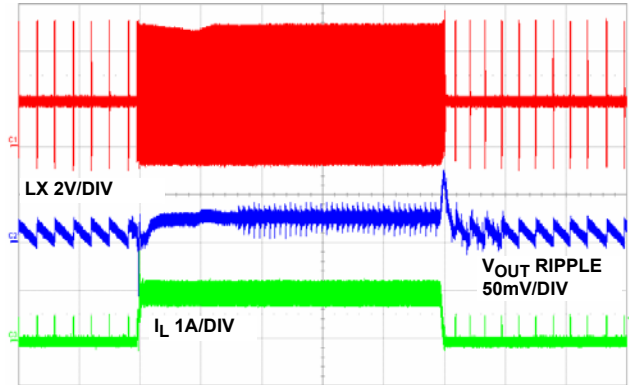


FIGURE 18. LOAD TRANSIENT (PFM),  $200\mu\text{s}/\text{DIV}$

# Typical Operating Performance

(Unless otherwise noted, operating conditions are:  $T_A = +25^\circ\text{C}$ ,  $V_{\text{VIN}} = 5\text{V}$ ,  $\text{EN} = \text{VIN}$ ,  $\text{RSI} = \text{SKIP} = 0\text{V}$ ,  $L = 2.2\mu\text{H}$ ,  $C_1 = 20\mu\text{F}$ ,  $C_2 = 20\mu\text{F}$ ,  $I_{\text{OUT}} = 0\text{A}$ ) (Continued)

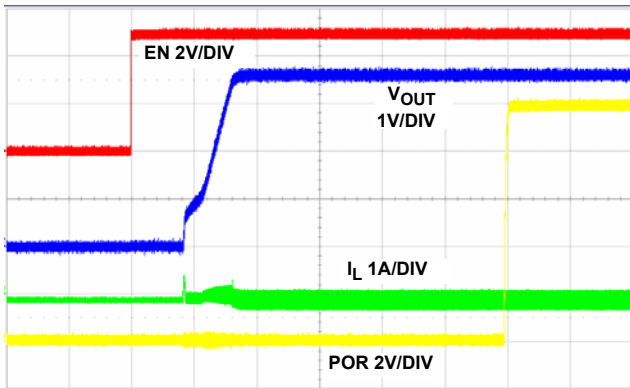


FIGURE 19. SOFT-START AT NO LOAD, 500 $\mu\text{s}$ /DIV

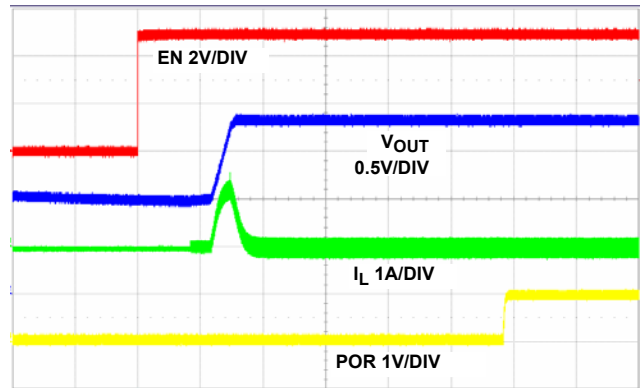


FIGURE 20. SOFT-START WITH PRE-BIASED 1V, 500 $\mu\text{s}$ /DIV

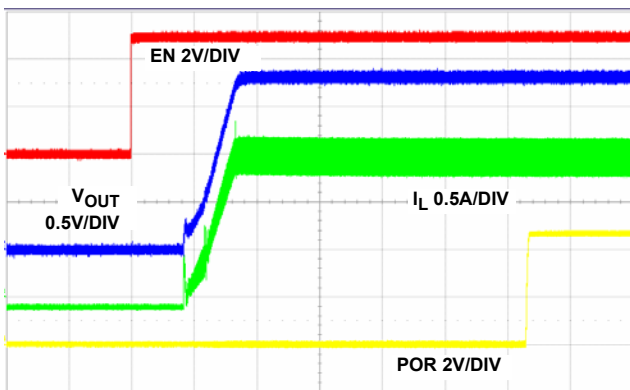


FIGURE 21. SOFT-START AT FULL LOAD, 500 $\mu\text{s}$ /DIV

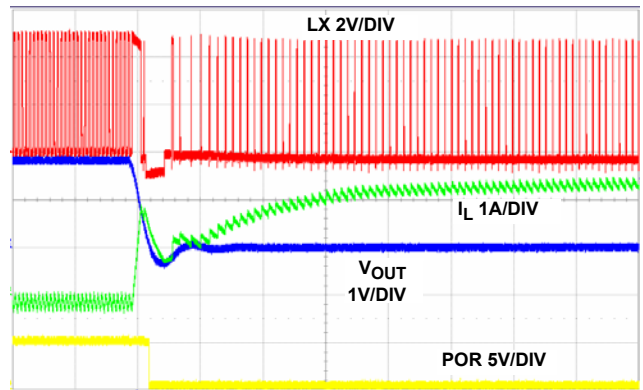


FIGURE 22. OUTPUT SHORT CIRCUIT, 10.0 $\mu\text{s}$ /DIV

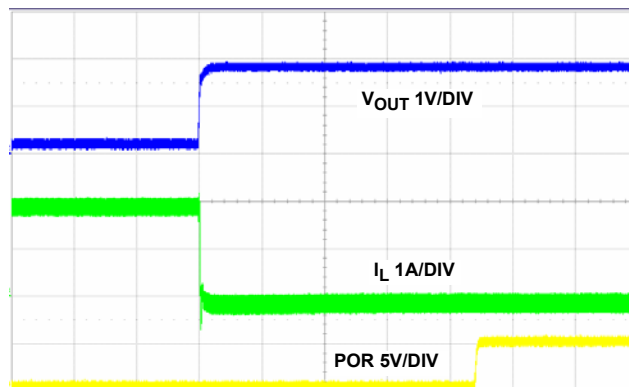


FIGURE 23. OUTPUT SHORT CIRCUIT RECOVERY, 500 $\mu\text{s}$ /DIV



# Typical Applications

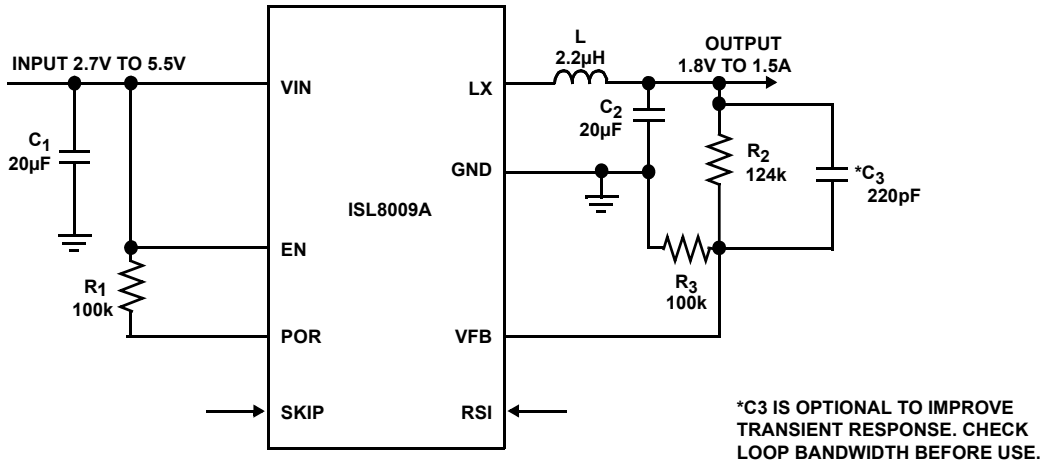


FIGURE 24. TYPICAL APPLICATION DIAGRAM

# Block Diagram

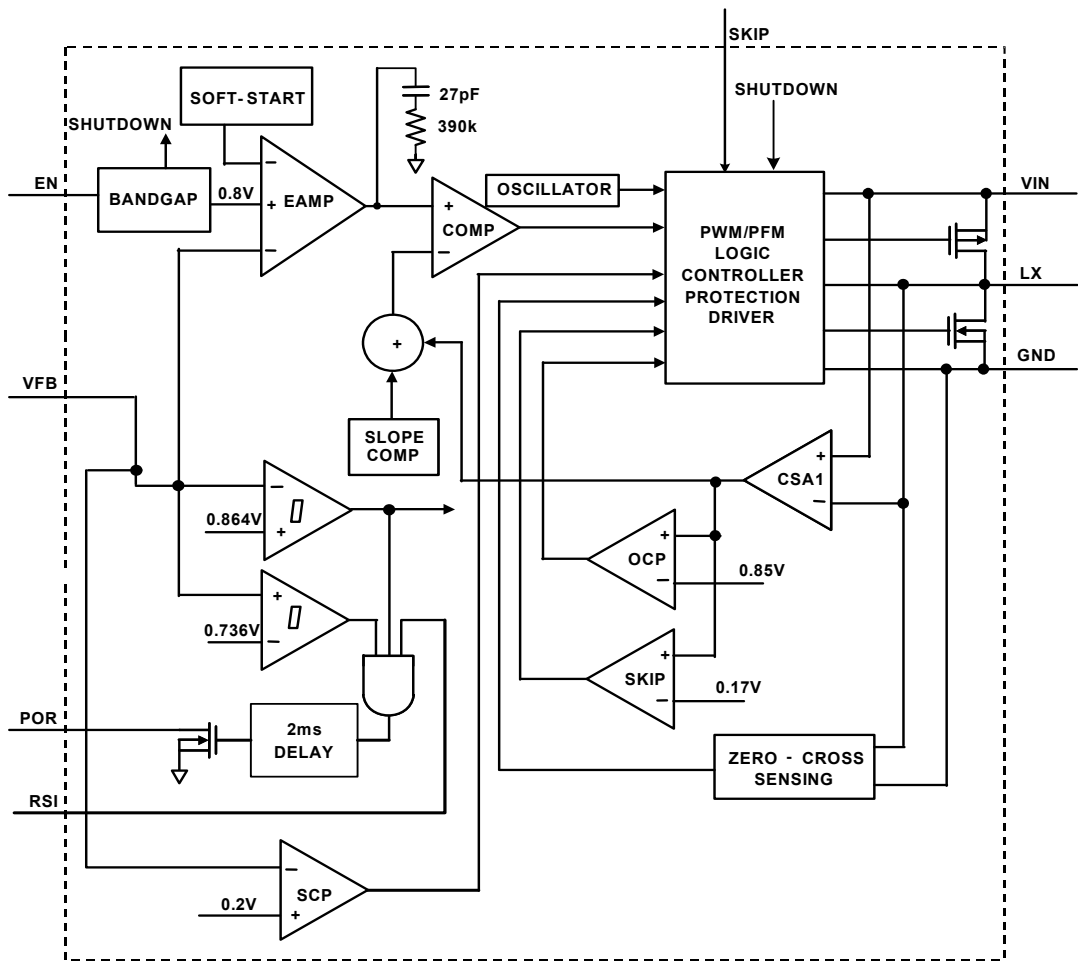


FIGURE 25. FUNCTIONAL BLOCK DIAGRAM

## Theory of Operation

The ISL8009A is a step-down switching regulator optimized for battery-powered handheld applications. The regulator operates at 1.6MHz fixed switching frequency under heavy load condition to allow small external inductor and capacitors to be used for minimal printed-circuit board (PCB) area. At light load, the regulator reduces the switching frequency, unless forced to the fixed frequency to minimize the switching loss and to maximize the battery life. The quiescent current when the output is not loaded is typically only 17 $\mu$ A. The supply current is typically only 0.1 $\mu$ A when the regulator is shutdown.

### PWM Control Scheme

The ISL8009A employs the current-mode pulse-width modulation (PWM) control scheme for fast transient response and pulse-by-pulse current limiting. Figure 25 shows the block diagram. The current loop consists of the oscillator, the PWM comparator COMP, the current sensing circuit, and the slope compensation for the current loop stability. The current sensing circuit consists of the resistance of the P-Channel MOSFET when it is turned on and the current sense amplifier CSA. The gain for the current sensing circuit is typically 0.4V/A. The control reference for the current loops comes from the error amplifier EAMP of the voltage loop.

The PWM operation is initialized by the clock from the oscillator. The P-Channel MOSFET is turned on at the beginning of a PWM cycle and the current in the MOSFET starts to ramp up. When the sum of the current amplifier CSA and the compensation slope (0.675V/ $\mu$ s) reach the control reference of the current loop, the PWM comparator COMP sends a signal to the PWM logic to turn off the P-MOSFET and to turn on the N-Channel MOSFET. The N-MOSFET stays on until the end of the PWM cycle. Figure 26 shows the typical operating waveforms during the PWM operation. The dotted lines illustrate the sum of the compensation ramp and the current-sense amplifier CSA output.

The output voltage is regulated by controlling the reference voltage to the current loop. The bandgap circuit outputs a 0.8V reference voltage to the voltage control loop. The feedback signal comes from the VFB pin. The soft-start block only affects the operation during the start-up and will be discussed separately. The error amplifier is a transconductance amplifier that converts the voltage error signal to a current output. The voltage loop is internally compensated with the 30pF and 300k $\Omega$  RC network. The maximum EAMP voltage output is precisely clamped to the bandgap voltage (1.172V).

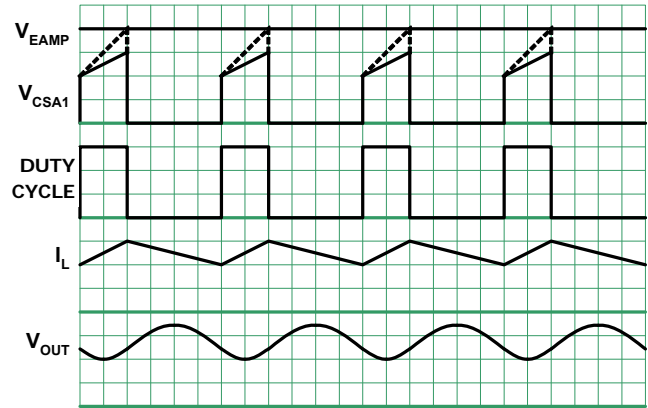


FIGURE 26. PWM OPERATION WAVEFORMS

### SKIP Mode

The ISL8009A enters a pulse-skipping mode at light load to minimize the switching loss by reducing the switching frequency. Figure 27 illustrates the skip-mode operation. A zero-cross sensing circuit shown in Figure 25 monitors the N-MOSFET current for zero crossing. When 8 consecutive cycles of the N-MOSFET crossing zero are detected, the regulator enters the skip mode. During the 8 detecting cycles, the current in the inductor is allowed to become negative. The counter is reset to zero when the current in any cycle does not cross zero.

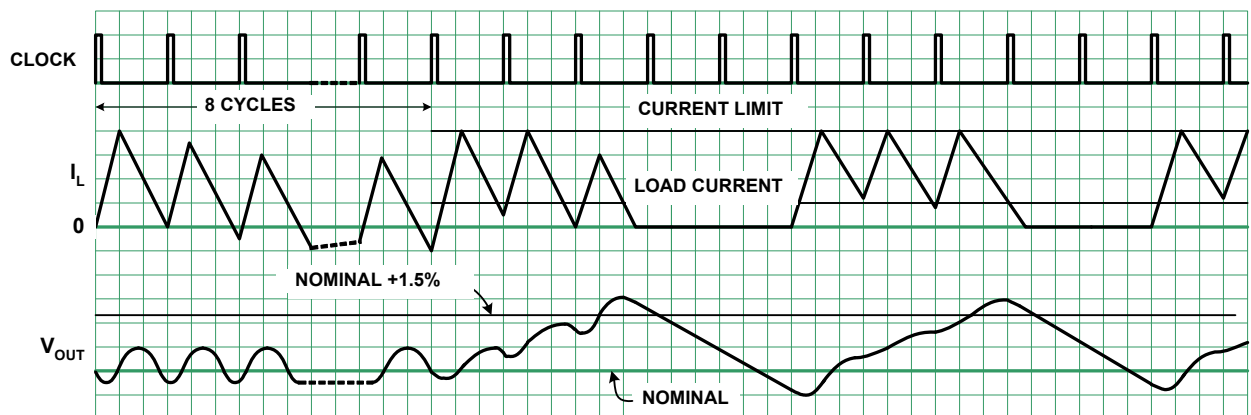


FIGURE 27. SKIP MODE OPERATION WAVEFORMS

Once the skip mode is entered, the pulse modulation starts being controlled by the SKIP comparator shown in Figure 25. Each pulse cycle is still synchronized by the PWM clock. The P-MOSFET is turned on at the clock and turned off when its current reaches 20% of the current limit value (0.2V at the CSA output). As the average inductor current in each cycle is higher than the average current of the load, the output voltage rises cycle over cycle. When the output voltage reaches 1.5% above the nominal voltage, the P-MOSFET is turned off immediately and the inductor current is fully discharged to zero and stays at zero. The output voltage reduces gradually due to the load current discharging the output capacitor. When the output voltage drops to the nominal voltage, the P-MOSFET will be turned on again at the clock, repeating the previous operations.

The regulator resumes normal PWM mode operation when the output voltage drops 1.5% below the nominal voltage.

### Mode Control

The ISL8009A has a SKIP pin that controls the operation mode. When the SKIP pin is driven to low or shorted to ground, the regulator operates in a forced PWM mode. The forced PWM mode remains the fixed PWM frequency at light load instead of entering the skip mode.

### Overcurrent Protection

The overcurrent protection is realized by monitoring the CSA output with the OCP comparator, as shown in Figure 25. The current sensing circuit has a gain of 0.4V/A, from the N-MOSFET current to the CSA output. When the CSA output reaches 0.8V, (which is equivalent to 2A for the switch current) the OCP comparator is tripped to turn off the P-MOSFET immediately.

### Short-Circuit Protection

A short-circuit protection SCP comparator monitors the VFB pin voltage for output short-circuit protection. When the VFB is lower than 0.2V, the SCP comparator forces the PWM oscillator frequency to drop to 1/3 of the normal operation value. This comparator is effective during start-up or an output short-circuit event.

### RSI/POR Function

When powering up, the open-collector Power-On-Reset output holds low for about 1ms after VO reaches the preset voltage. When the active-HI reset signal RSI is issued, POR goes to low immediately and holds for the same period of time after RSI comes back to LOW. The output voltage is unaffected (Figure 28). When the function is not used, connect RSI to ground and leave the pull-up resistor, R<sub>1</sub>, open at the POR pin.

The POR output also serves as a 1ms delayed Power-Good signal when the pull-up resistor, R<sub>1</sub>, is installed. The RSI pin needs to be directly or indirectly through another resistor connected to ground for this to function properly.

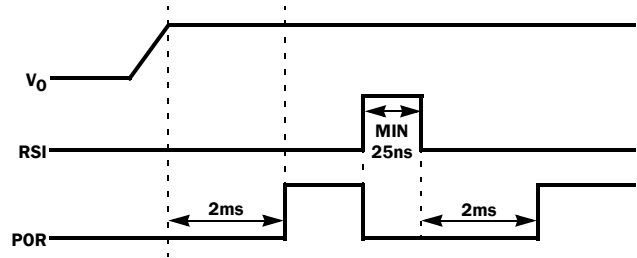


FIGURE 28. RSI AND POR TIMING DIAGRAM

### UVLO

When the input voltage is below the undervoltage lock out (UVLO) threshold, the regulator is disabled.

### Soft-Start-Up

The soft start-up eliminates the in-rush current during the start-up. The soft-start block outputs a ramp reference to both the voltage loop and the current loop. The two ramps limit the inductor current rising speed as well as the output voltage speed so that the output voltage rises in a controlled fashion. At the very beginning of the start-up, the output voltage is less than 0.2V; hence the PWM operating frequency is 1/3 of the normal frequency.

### Power MOSFETs

The power MOSFETs are optimized for best efficiency. The ON-resistance for the P-MOSFET is typically 120mΩ and the ON-resistance for the N-MOSFET is typically 110mΩ.

### Duty Cycle

The ISL8009A features duty cycle operation to maximize the battery life. When the battery voltage drops to a level that the ISL8009A can no longer maintain the regulation at the output, the regulator completely turns on the P-MOSFET. The maximum drop out voltage under the duty-cycle operation is the product of the load current and the ON-resistance of the P-MOSFET.

### Enable

The Enable (EN) input allows the user to control the turning on or off of the regulator for purposes such as power-up sequencing. When the regulator is enabled, there is typically a 600μs delay for waking up the bandgap reference, then the soft-start-up begins. When the regulator is disabled, the P-MOSFET and the N-MOSFET are turned off immediately. The 100Ω soft discharge resistor from LX to GDN is activated and pulls the output to 0V.

### Thermal Shutdown

The ISL8009A has built-in thermal protection. When the internal temperature reaches +140°C, the regulator is completely shutdown. As the temperature drops to +120°C, the ISL8009A resumes operation by stepping through a soft-start-up.

## Applications Information

### Output Inductor and Capacitor Selection

To consider steady state and transient operation, ISL8009A typically uses a 3.3μH output inductor. Higher or lower inductor values can be used to optimize the total converter system performance. For example, for higher output voltage 3.3V application, in order to decrease the inductor current ripple and output voltage ripple, the output inductor value can be increased. The inductor ripple current can be expressed in Equation 1:

$$\Delta I = \frac{V_O \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}{L \cdot f_S} \quad (\text{EQ. 1})$$

The inductor's saturation current rating needs to be at least larger than the peak current. The ISL8009A protects the typical peak current 2.1A. The saturation current needs to be over 2.4A for maximum output current application.

ISL8009A uses internal compensation network and the output capacitor value is dependant on the output voltage. The ceramic capacitor is recommended to be X5R or X7R. The recommended minimum output capacitor values are shown in Table 1.

TABLE 1. OUTPUT CAPACITOR VALUE vs V<sub>OUT</sub>

| V <sub>OUT</sub> (V) | C <sub>OUT</sub> (μF) | L (μH)  |
|----------------------|-----------------------|---------|
| 0.8                  | 10                    | 1.0~2.2 |
| 1.2                  | 10                    | 1.2~2.2 |
| 1.6                  | 10                    | 1.8~2.2 |
| 1.8                  | 10                    | 1.8~3.3 |
| 2.5                  | 10                    | 1.8~3.3 |
| 3.3                  | 10                    | 1.8~4.7 |
| 3.6                  | 10                    | 1.8~4.7 |

In Table 1, the minimum output capacitor value is given for different output voltages to make sure the whole converter system is stable. Maximum output capacitance should be limited to 50μF or less.

### Input Capacitor Selection

The main functions for the input capacitor are to provide decoupling of the parasitic inductance and to provide filtering function to prevent the switching current from flowing back to the battery rail. A 10μF, X5R or X7R ceramic capacitor is a good starting point for the input capacitor selection.

### Output Voltage Setting Resistor Selection

The resistors R<sub>2</sub> and R<sub>3</sub> shown in Figure 24 set the output voltage for the adjustable version. The output voltage can be calculated by Equation 2:

$$V_O = 0.8 \cdot \left(1 + \frac{R_2}{R_3}\right) \quad (\text{EQ. 2})$$

where the 0.8V is the reference voltage.

The voltage divider consists of R<sub>2</sub> and R<sub>3</sub> and increases the quiescent current by V<sub>O</sub>/(R<sub>2</sub> + R<sub>3</sub>), so larger resistance is desirable. On the other hand, the VFB pin has leakage current that will cause error in the output voltage setting. The leakage current has a typical value of 0.1μA. To minimize the accuracy impact on the output voltage, select the R<sub>3</sub> no larger than 200kΩ. For V<sub>O</sub> = 0.8V, it is recommended to short R<sub>2</sub> and open R<sub>3</sub>.

### Layout Recommendation

The layout is a very important converter design step to make sure the designed converter works well. For the ISL8009A buck converter, the power loop is composed of the output inductor L, the output capacitor C<sub>OUT</sub>, the LX pin and the GND pin. It is necessary to make the power loop as small as possible.

The heat of the IC is mainly dissipated through the thermal pad. Maximizing the copper area connected to the thermal pad is preferable. In addition, a solid ground plane is helpful for EMI performance. It is recommended to add 5 vias under the thermal pad connection to the solid ground plane.

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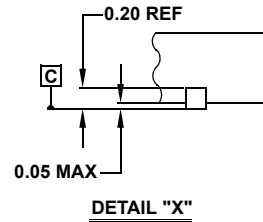
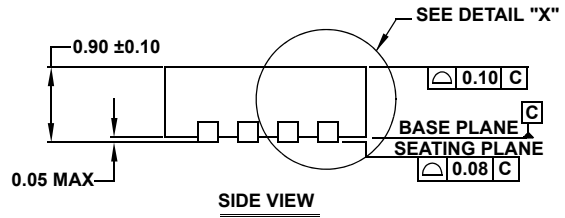
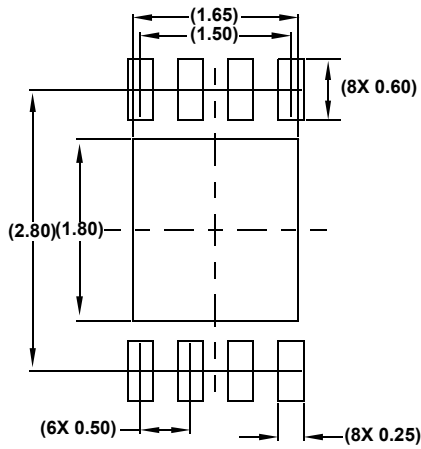
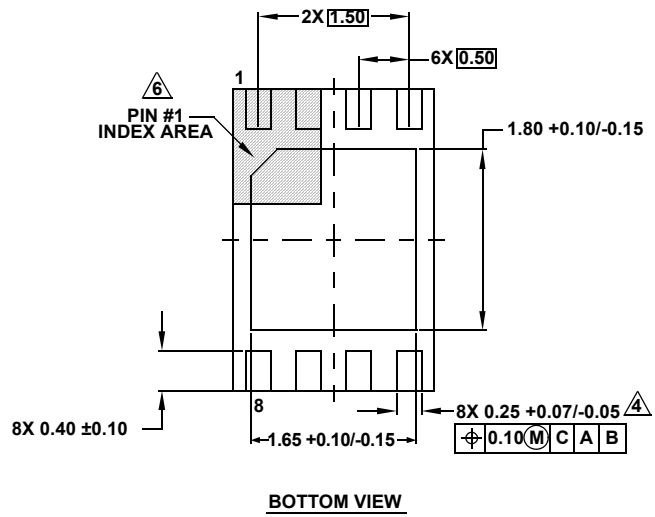
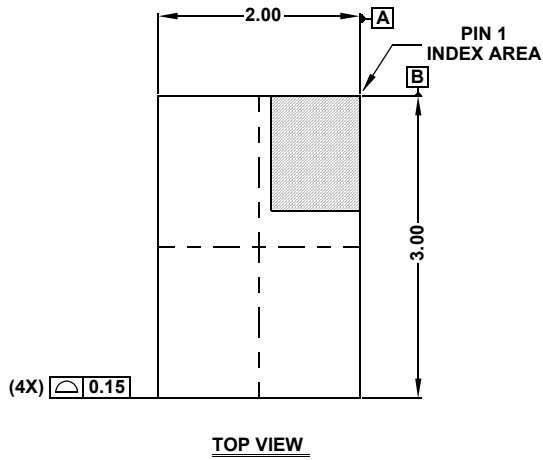
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# Package Outline Drawing

## L8.2x3

### 8 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE

Rev 1, 3/10



**NOTES:**

1. Dimensions are in millimeters.  
Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.25mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Complies to JEDEC MO-229 VCEd-2.