MP2940A

Digital Multi-phase Controller With PMBus Interface for IMVP8/9

DESCRIPTION

The MP2940A is a single rail, multi-phase digital VR controller compliant with IMVP8/IMVP9 for Intel microprocessors. It works with MPS's Intelli-Phase products to complete a multi-phase VR solution with minimum external components. It also can be configured to single phase operation.

The MP2940A provides on-chip MTP to store application configurations. Its configurations and fault information are easy to program or monitor through a PMBus interface. The MP2940A can monitor and report output current through Intelli-Phase CS output.

The MP2940A is based on a unique, digital multi-phase, non-linear control to provide fast load transient response with minimum output capacitors. With only one power loop control method for both steady state and load transient, the loop compensation parameter is very easy to configure.

FEATURES

- Configurable Phase Number
- Intel IMVP8 and IMVP9 Compliant
- PVID Interface to Support VccAUX
- PMBus Compliant
- Serial VID Interface for Programming and Monitoring
- Built-In MTP to Store Customer Configuration
- Automatic Loop Compensation
- Auto Phase-Shedding to Improve Overall Efficiency
- Phase-to-Phase Active Current Balancing
- Input/Output Voltage and Power, and Output Current Monitoring
- Regulator Temperature Monitoring
- UVLO/OVP/UVP/OCP/OTP/RVP with Options of No Action, Latch, Retry, or Hiccup
- Digital Programmable Load Line
- RoHS Compliant 4x4 TQFN-28

APPLICATIONS

- Ultra-Book Core
- High Performance Notebook Core
- Tablet Core

TYPICAL APPLICATION

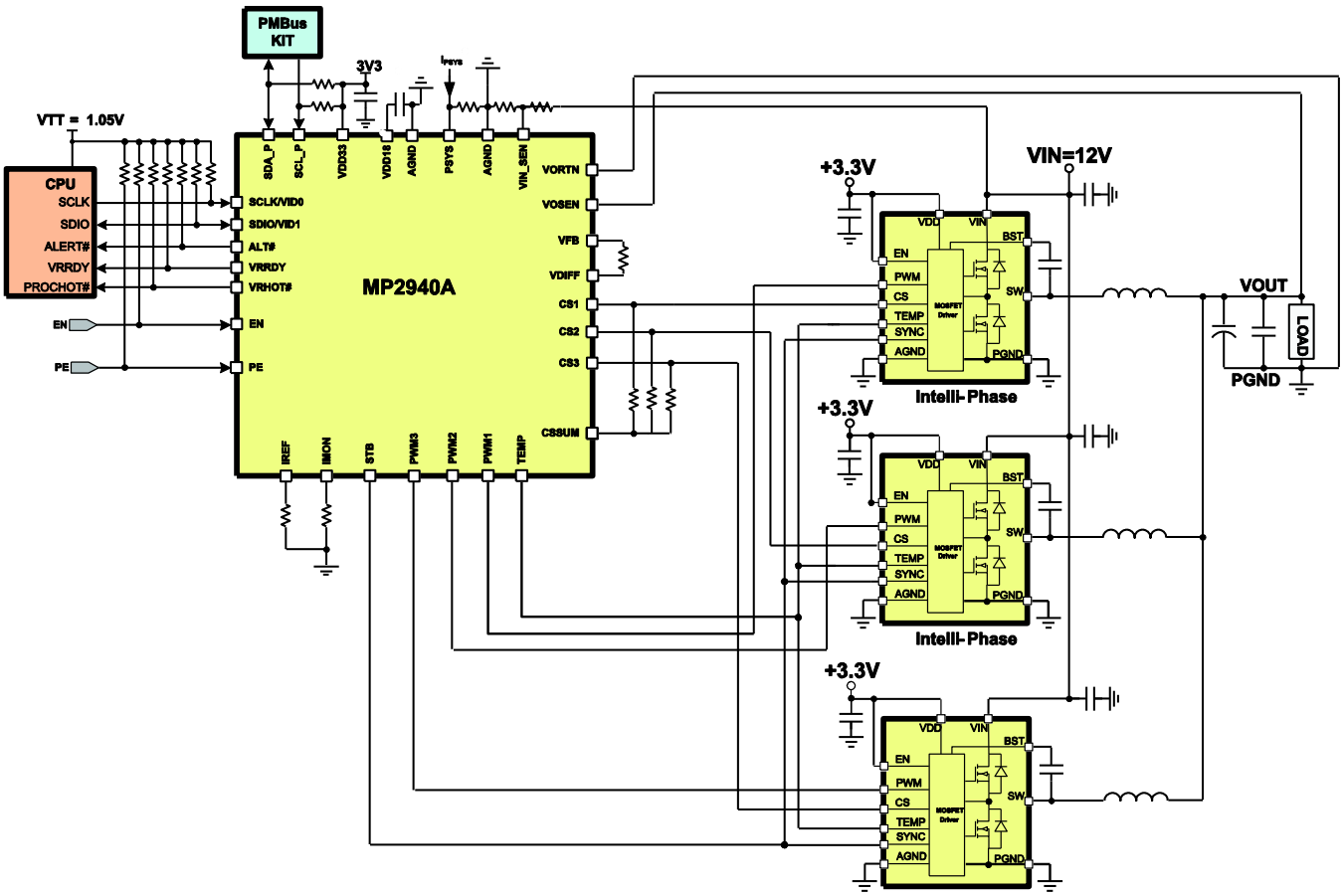


Figure 1: Three-phase Solution w/ Low-Height Inductor

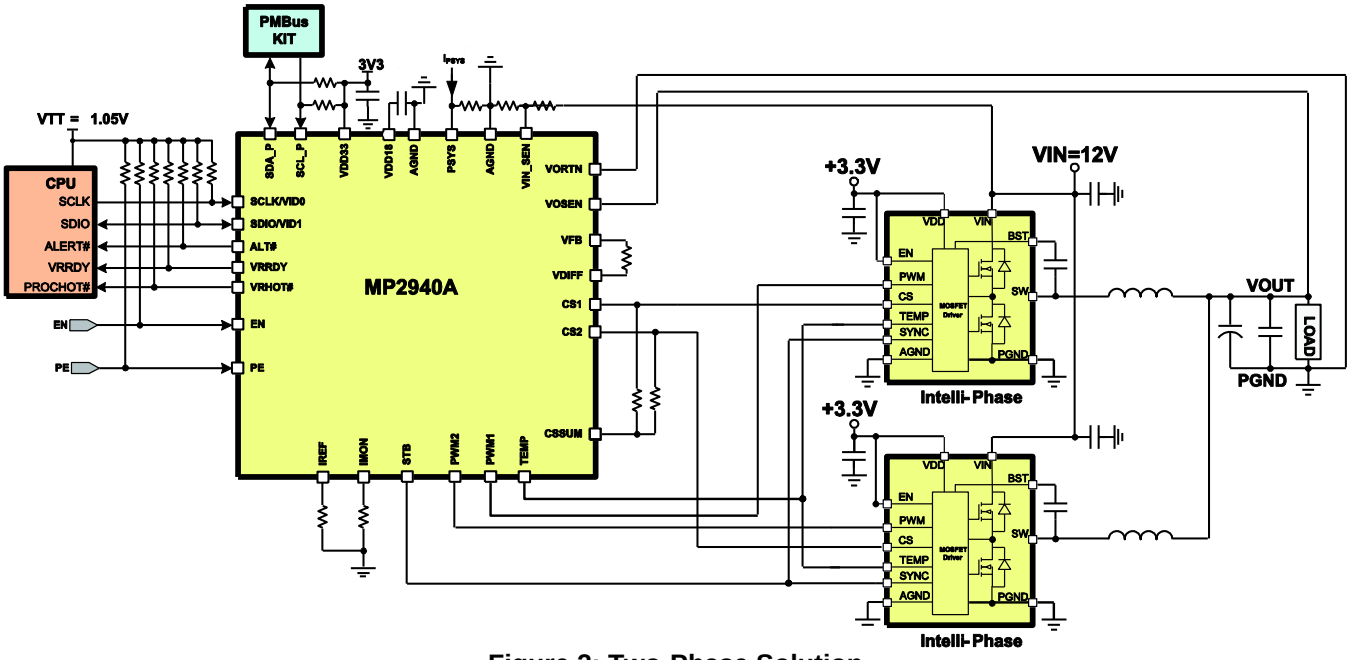


Figure 2: Two-Phase Solution

ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2940AGRT-xxxx**	TQFN-28 (4mmx4mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP2940AGRT-xxxx–Z);
** “xxxx” is the configuration code identifier for the register settings stored in the internal non-volatile memory (NVM). Each “x” can be a hexadecimal value between 0 and F. Please work with an MPS FAE to create this unique number.

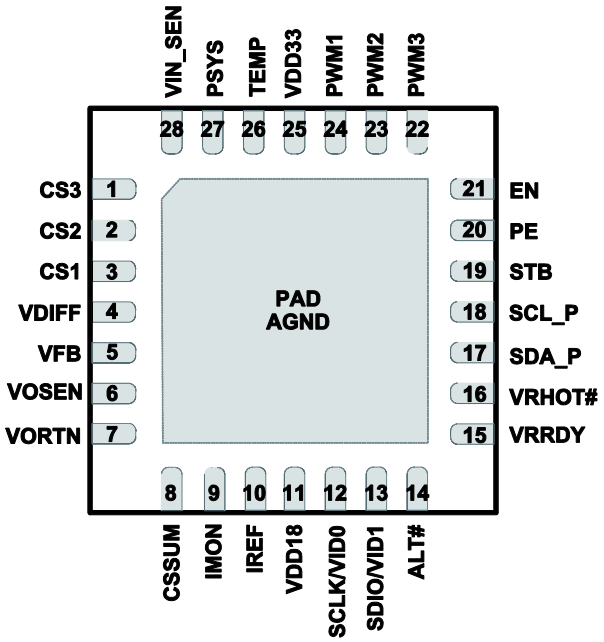
TOP MARKING

MPSYWW
M2940A
LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
M2940A: Part number
LLLLLL: Lot number

PACKAGE REFERENCE

TOP VIEW



TQFN-28 (4mmx4mm)

PIN FUNCTIONS OF MP2940A

Pin #	Name	I/O	Description
1	CS3	A [I]	**Phase3 current sense inputs.** Float CS of the unused phase.
2	CS2	A [I]	**Phase2 current sense inputs.** Float CS of the unused phase.
3	CS1	A [I]	**Phase1 current sense inputs.** Float CS of the unused phase.
4	VDIFF	A[O]	**Differential remote sense amplifier output.**
5	VFB	A [I/O]	**Feedback of VR.** VFB sources a current proportional to the sensed output current (I_{droop}). This current flows through the resistor between VFB and VDIFF to create a voltage drop proportional to the load current. Select a resistor between VDIFF and VFB to set a proper load line.
6	VOSEN	A[I]	**Positive remote voltage sense input.** VOSEN is connected directly to the VR output voltage at the load and should be routed differentially with VORTN.
7	VORTN	A[I]	**Remote voltage sensing return input of VR.** VORTN is connected directly to ground at the load and should be routed differentially with VOSEN.
8	CSSUM	A [I]	**Total phase current monitor for VR AVP.** Connect the active phase CS signal into CSSUM through current sense resistors.
9	IMON	A [I/O]	**Analog total load current signal of VR.** IMON sources a current proportional to the sensed total load current from CS_SUM. Connect an external resistor from IMON to AGND to program the gain.
10	IREF	A [I/O]	**Internal bias current set.** Connect an 61.9kΩ resistor from IREF to GND.
11	VDD18	A [I/O]	**1.8V LDO output for internal digital power supply.** Connect a 1µF bypass capacitor to AGND.
12	SCLK/VID0	D [I]	**Multi-functional pin.** When this pin is selected to support the SVID interface, this pin will source a synchronous clock from the CPU. The frequency range is from 10MHz to 26MHz. When this pin is selected to support the PVID for the VccAUX rail, it is VID0.
13	SDIO/VID1	D [I/O]	**Multi-functional pin.** When this pin is selected to support the SVID interface, it receives or drives the Data signal for the SVID bus. When it is selected to support the PVID for the VccAUX rail, it is VID1.
14	ALT#	D [O]	**Alert pin.** Open drain output. Alert signal from VID controller to CPU.
15	VRRDY	D [O]	**VR ready output of the controller.** Open drain output that signals when the output voltage is outside of the proper operating range. The VCCIO rail is expected for pull up; however, some systems may pull up to a maximum voltage of 3.3V, with external pull-up resistors.
16	VRHOT#	D [O]	**Voltage regulator thermal throttling logic output.** Open drain output. This pin actively pulls low if the monitored temperature exceeds the programmed VRHOT# temperature threshold.
17	SDA_P	D [I/O]	**Data signal between the PMBus controller and VID controller.**
18	SCL_P	D [I]	**Source synchronous clock from the PMBus Controller.**
19	STB	D[O]	**Digital output to indicate Intelli-Phase to enter low power mode.**
20	PE	D[I]	**Program enable.** Program the enable input for system configuration through the PMBus when EN is OFF, pull low to AGND with a 0Ω register if not used.
21	EN	D [I]	**Enable control for the controller.**
22	PWM3	D [O]	**Tri-state logic-level PWM outputs.** Each output is connected to the input of Intelli-Phase's PWM pin. The logic levels are 0V for low logic and 3.3V for high logic. The output is set to tri-state to shut down both the high-side MOSFET and low-side MOSFET of Intelli-Phase.
23	PWM2	D [O]	
24	PWM1	D [O]	

PIN FUNCTIONS OF MP2940A *(continued)*

Pin #	Name	I/O	Description
25	VDD33	A [I]	**3.3V power supply input.** Connect a 4.7µF bypass capacitor to the ground.
26	TEMP	A [I]	**Analog signal from VR to VID controller.** TEMP indicates the power stage temperature. Connect all of Intelli-Phase's VTEMP pins together to produce the maximum junction temperature and then connect to MP2940A's TEMP pin.
27	PSYS	A[I]	**Total system input power monitor.** A current proportional to the system power flows out from a sensor and goes to ground through an R_{PSYS}.
28	VIN_SEN	A[I]	**Input voltage sense.** Connect VIN_SEN to VIN through a 1/16 divider network.
PAD	AGND	I/O	**Analog ground.**

ABSOLUTE MAXIMUM RATINGS (1)

VDD33.....–0.3V to +4.0 V
VDD18.....–0.3V to +2.0 V
VORTN.....–0.3V to +0.3 V
CS1/2/3, PWM1/2/3, VFB, VDIFF, VOSEN, VRRDY, VRHOT#, SCL_P, SDA_P, PE, EN, SCLK/VID0, SDIO/VID1, TEMP .–0.3V to +3.6 V
All Other Pins.....–0.3V to +1.8 V
Continuous Power Dissipation (T_A = +25°C) (2)
…….…… ..2.9W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature..... –65°C to +150°C

Recommended Operating Conditions (3)

VDD33 .....+3.15V to +3.4V
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

TQFN-28(4mmX4mm) ..... 42 ..... 9.... °C/W

Notes:

1. Exceeding these ratings may damage the device.
2. The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature.
3. The device is not guaranteed to function outside of its operating conditions.
4. Measured on JESD51-7, 6-layer PCB.

ELECTRICAL CHARACTERISTICS

VDD33 = 3.3V, EN = 1V, T_J =25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
REMOTE SENSE AMPLIFIER						
Bandwidth(5)	$GBW_{(RSA)}$			20		MHz
VORTN current	$I_{RTN1,2}$	EN=1V; V_{OSEN}=3V; V_{ORTN}=0V		-25	-50	µA
VOSEN current	$I_{VOSEN1,2}$	EN=1V; V_{ORTN}=0V; V_{OSEN}=3V		50	100	µA
OSCILLATOR						
Frequency	f_{OSC}	I_{REF}=1.23V; R_{IREF}=61.9kΩ	1.5	1.5625		MHz
SYSTEM INTERFACE CONTROL INPUTS						
EN/PE						
Input low voltage	$VIL_{(EN)}$				0.4	V
Input high voltage	$VIH_{(EN)}$		0.8			V
Enable high leakage	$IIH_{(EN)}$	EN=2V			3.6	µA
Input low voltage	$VIL_{(PE)}$				0.8	V
Input high voltage	$VIH_{(PE)}$		2.4			V
PE high leakage	$IIH_{(PE)}$	PE=3.6V			2.0	µA
Enable delay	T_A	EN high to SVID ready		1.5		ms
THERMAL THROTTLING CONTROL						
VRHOT# low output impedance		$I_{VRHOT\#}$=20mA		8	12	Ω
VRHOT# high leakage current		V_{RHOT}=1.8V	-3		3	µA
IMON OUTPUT						
Current gain accuracy	I_{MON}/I_{CS_SUM}	Measured from I_{CS_SUM} to I_{MON}, I_{CS_SUM} =1.2mA		1:32		A/A
Digital Iout error				+/-1		%
COMPARATOR						
Propagation delay(5)	t_{PD}			10		ns
Common-mode range(5)			0		2.74	V
COMPARATOR (Protection)						
Under-voltage threshold	$V_{DIFF(UV)}$	Relative to reference DAC voltage		−150		mV
Over-voltage threshold	$V_{DIFF(OV2)}$	Relative to reference DAC voltage		200		mV
	$V_{DIFF(OV1)}$	OVP1 DAC voltage			2.54	V
PWM1~3, STB OUTPUTS						
Output low voltage	$V_{OL\ (PWM)}$	$I_{PWM(SINK)}$ = 400 µA		10	200	mV
Output high voltage	$V_{OH\ (PWM)}$	$I_{PWM(SOURCE)}$ = -400 µA	3.15			V
Rise and fall time(5)		C = 10pF		10		ns

ELECTRICAL CHARACTERISTICS *(continued)*

VDD33 = 3.3V, EN = 1V, T_J =25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
PWM/STB tri-state leakage		PWM = 1.5V; EN = 0V	-1		1	µA
INTERNAL LDO OUTPUT						
LDO output voltage	VDD18	Load = 0mA		1.8		V
LDO regulator load capability	I_{VDD18}	Voltage drop - 40mV	30	40		mA
VDD33 SUPPLY						
Supply voltage range	VDD33		3.15	3.3	3.4	V
Supply current	I_{VDD33}	EN=PE=high, VDD33=3.6V		7		mA
		EN= PE=low, VDD33=3.6V		100		µA
		EN=PE=high, VDD33=3.6V, PS4, T_A=25°C		140		µA
UVLO threshold voltage	$VDD33_{UVLO}$	VDD33 is rising		2.88		V
UVLO hysterisis(5)	$VDD33_{UVLO}$	VDD33 is falling		75		mV
SVID Interface(5)						
CPU interface voltage (SDIO, SCLK)	V_{IL}	Logic low			0.45	V
	V_{IH}	Logic high	0.65			V
Termination resistance (SDIO, SCLK, ALT#)	R_{PU}		50	55		Ω
Leakage current (SDIO, SCLK, ALT#)	IL	0V to VTT	-10		10	µA
Pad capacitance (SDIO, SCLK, ALT#)	C_{PAD}				4	pF
Pin capacitance (SDIO, SCLK, ALT#)	C_{PIN}				5	pF
Buffer on resistance (SDIO, SCLK, ALT#)	R_{ON}		4		13	Ω
Maximum voltage (SDIO, SCLK, ALT#)	V_{MAX}	Transient voltage including ringing	-0.3		2.1	V
Slew rate (SDIO, SCLK, ALT#)		2nH, 4pF load	0.5		2	V/ns
ADC						
Voltage range			0		1.6	V
ADC resolution(5)				10		Bits
DNL(5)				1		LSB
Sample rate(5)				780		kHz

ELECTRICAL CHARACTERISTICS *(continued)*

VDD33 = 3.3V, EN = 1V, T_J =25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
DAC (Reference Voltage for Vout)						
Range				1.6		V
Resolution/LSB(5)				5		mV
DAC (Vout Calibration)						
Range				320		mV
Resolution(5)				8		bit
DAC (Protection for Per Phase OCP)						
Range		Adjustable via PMBus	1.28		2.54	V
Resolution/LSB				10		mV
DAC (Protection for OVP1)						
Range		Adjustable via PMBus	0		2.54	V
Resolution/LSB				20		mV
PMBus DC Characteristics (SDA_P, SCL_P)						
Input high voltage	V_{IH}	SCL_P, SDA_P	2.3			V
Input low voltage	V_{IL}	SCL_P, SDA_P			0.8	V
Input leakage current		SCL_P, SDA_P, ALT_P	-10		10	µA
Output low voltage	V_{OL}	ALT_P sinks 2mA			400	mV
Maximum voltage(5)	V_{MAX}	Transient voltage including ringing	-0.3	3.3	3.6	V
Pin Capacitance(5)	C_{PIN}				10	pF
PMBus Timing Characteristics (5)						
Operating frequency range			10		2000	kHz
Bus free time		Between stop and start condition	0.5			µs
Holding time			0.26			µs
Repeated start condition setup time			0.26			µs
Stop condition setup time			0.26			µs
Data hold time			0			ns
Data setup time			50			ns
Clock low time out			25		35	ms
Clock low period			0.5			µs
Clock high period			0.26		50	µs
Clock/data fall time					120	ns
Clock/data rise time					120	ns

Notes:

5. Guaranteed by design or characterization data, not tested in production.

BLOCK DIAGRAM

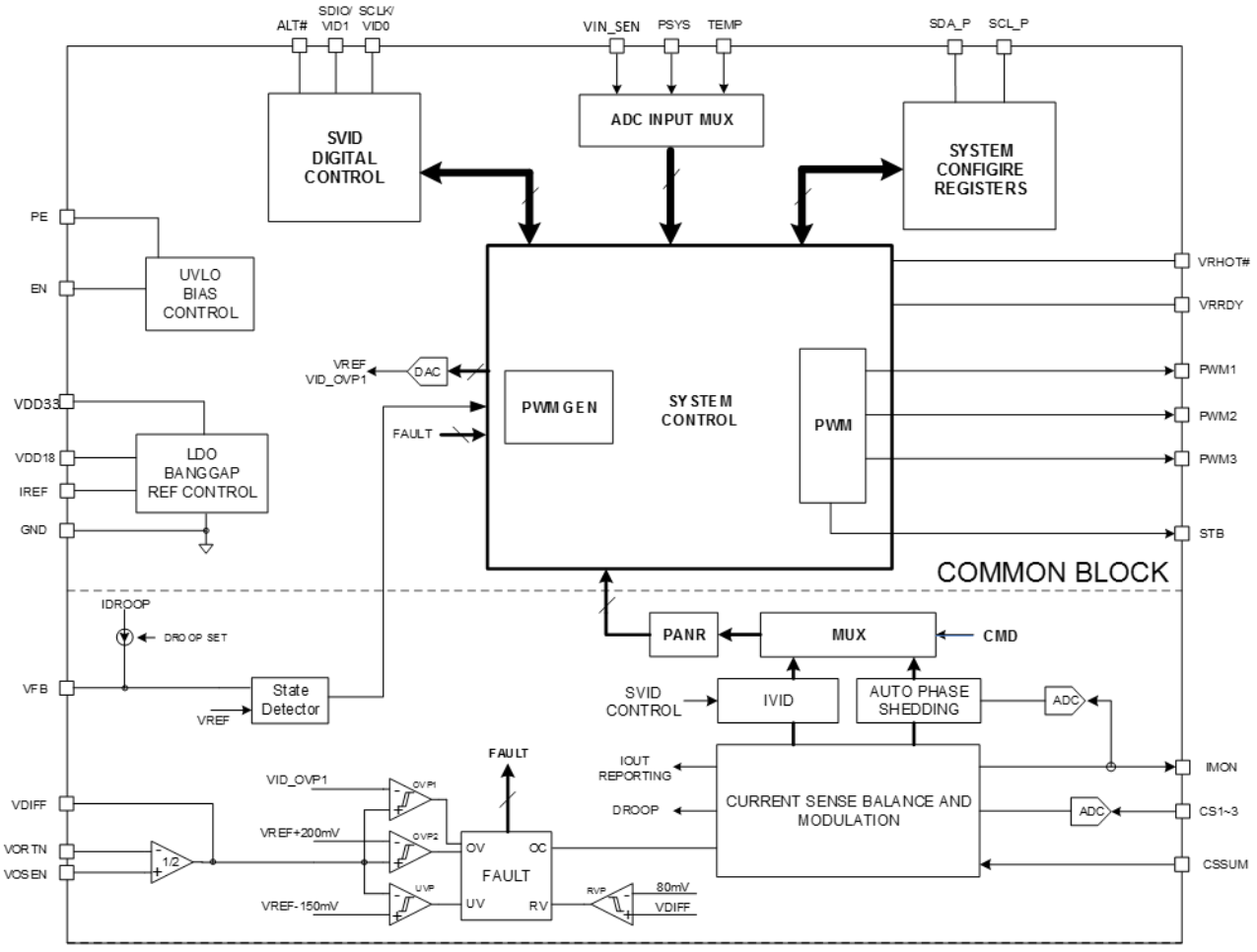


Figure 3: System Functional Block

OPERATION

The MP2940A is a single rail, multi-phase digital VR controller compliant with IMVP8/IMVP9 for Intel microprocessors. It can adaptively shed phases and add phases according to the load current to improve VR efficiency. It contains blocks of precision DAC and ADC, a differential remote voltage sense amplifier, a current sense amplifier, internal loop compensation, VR_READY monitoring, temperature monitoring, and a PMBus/SVID interface. MTP for custom configuration fault protection features include: Vin under-voltage lockout (UVLO), over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), over-temperature protection (OTP), and reverse voltage protection (RVP).

Phase Configuration

The MP2940A supports multiple phases depending on different applications/platforms; it can be configured up to 3 phases via the PMBus register MFR_PHASE_CFG (**CAh[2:0]**) See Table 1.

Table 1: Phase Configuration and Active PWM Pins

MFR_PHASE_ CFG [2:0]	Active PWM Pins
011	1,2,3
010	1,2
001	1
others	Not supported

PMBus Address

To support multiple VR devices used with the same PMBus interface, there is a PMBus address for every device. The PMBus address is a 7 bit code, which is setup by the register. The register SHUTLEVEL_ADDRPMBUS (**E1h[6:0]**) can be used to program the PMBus address.

Power On Sequence

The MP2940A is supplied by a +3.3V voltage for an analog circuit. The system will be reset by the internal power-on reset signal (POR). After the system comes out of POR, the data in MTP will be loaded to the registers to configure VR operation. The initialization process will take about 0.5ms + delay time Marked at T_A (see Figure 4), and then execute the soft-start process to charge the output capacitor with the SetVID_Slow slew rate until the reference reaches the target boot voltage. T_B (see Figure 4) is set by V_{BOOT}/Slow.

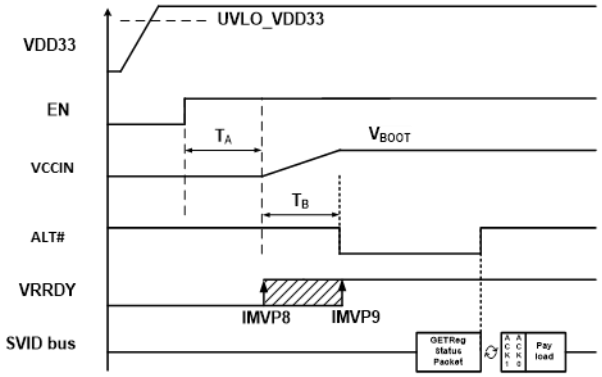


Figure 4: Start-Up Sequence

The MP2940A supports both IMVP8 and IMVP9 with different VRRDY assert time settings; the VRRDY signal will assert either when the SVID interface is ready to receive CPU commands (IMVP8), or when the VR reaches the boot voltage level (IMVP9).

The MP2940A also provides additional programmable EN delay by setting registers MFR_EN_DLY and MFR_EN_FILT_TIME. The T_A time can be set longer than the 0.5ms, T_A=0.5ms+MFR_EN_DLY+MFR_EN_FILT_TIME. See the register map for how to program the delay time.

When the boot voltage is set to 0, the PWM remains in tri-state until a valid SVID voltage is received. The controller then ramps the voltage to the target value and asserts ALERT#.

Steady State and Switching Frequency

The MP2940A applies a digital non-linear control to provide a fast transient response and easy loop compensation. The duty cycle of each active phase's PWM updates in real-time according to the input voltage and reference voltage under the set switching frequency. The active phases will be automatically interleaved during the steady state. At the steady state, the switching frequency is set at MFR_FS_VBOOT (**E5h[14:8]**).

The MP2940A adaptively changes the switching frequency of an individual phase during load transient to achieve super fast transient performance with minimum BOM cost.

Power State Change

The SVID bus can change the VR into different power states (PS0, PS1, PS2, PS3, and PS4) to achieve optimized efficiency on various load conditions. These states are entered by programming the power state register using SVID's SetPS command. The VR optimizes its power loss to flatten the efficiency curve over the operating current range, with the Power State commands issued by the processor. In PS0 mode, all phases run in CCM. In PS1 mode, only one phase runs in CCM; other phases are in tri-state. In PS2 mode, only one phase is running in the diode emulation mode, and the switching frequency falls down automatically to save the power loss at light load. See Table 2 for details on how the phases act at different power states.

During the dynamic VID transition issued by SVID commands like SetVID_Fast or SetVID_Slow, the power state will be changed to PS0 by default and runs in full-phase PWM mode. After the output is well regulated to the new target voltage, the power state will stay in PS0 mode until the processor sends a new command to change the power state.

Table 2: Power State and Phase Activities

PS State	Active Phase	CCM/DCM
PS0	All Phase PWM	CCM
PS1	One Phase PWM	CCM
PS2	One Phase PWM	DCM
PS3	One Phase PWM	DCM
PS4	All OFF	--

Reference

The MP2940A supports both 5mV VID step and 10mV VID step for IMVP8 and IMVP9 with only one DAC to generate REF. There is a control bit (MFR_STEP_SEL) in the E4h register that chooses the VID step. If this control bit is set to 1, then the output (VREF) of the DAC is shown as equation (1). Equation (2) shows how to get VREF when the control bit is written to 0.

$$VREF = (VID + 49)/2 * 5mV \quad (1)$$

$$VREF = (VID + 19)/2 * 10mV \quad (2)$$

Output Voltage Sense

The output voltages are remotely sensed with ½ gain differential amplifiers. The sensed output voltages are used for close loop compensation, OV/UV protection, and PMBus monitoring. A proper "package sense" (see Figure 5) is recommended to enclose the board parasitics within the feedback loop of the VR to achieve noise rejection and performance optimization. Two 0Ω resistors are placed close to the MP2940A.

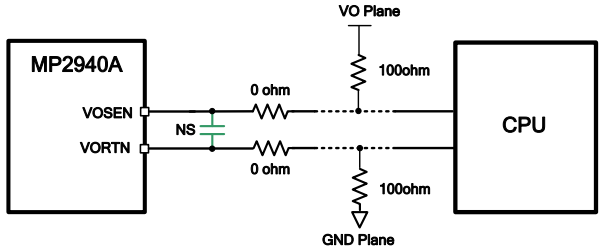


Figure 5: Output Remote Sense

To avoid errant operation or board damage when the CPU is absent, two 100Ω catch-up resistors are placed with connection to the Vo and PGND plane to get the output feedback even if the CPU is absent.

Input Voltage Sense

The input power supply voltage is sampled at the VIN_SEN pin and used for the output voltage regulation as the feed-forward control, Vin_UVLO, Vin_OVP fault protection, and monitoring via PMBus. Use two resistors connected to the input voltage and a 10nF bypass capacitor to get a 1/16 divider for VIN_SEN (see Figure 6). The default value is R_{VIN_1}=2MΩ and R_{VIN_2}=133KΩ.

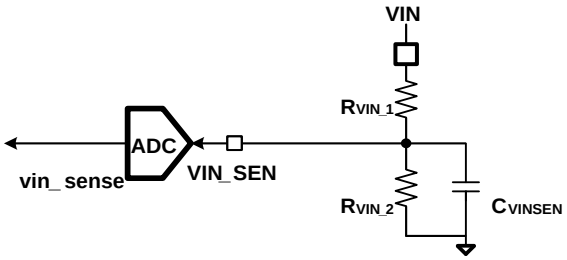


Figure 6: VIN Sense Network

Current Sense

The MP2940A works with the MPS Intelli-Phase to sense per phase inductor current and the total current (see Figure 7). The cycle-by-cycle current information is used for phase current balancing, over-current protection, and load line setting. The current sense gain is Kcs for Intelli-Phase products. The resistor R_{CS} is connected from CS to CS_SUM. CS_SUM is a 1.23V constant voltage, which is capable of sinking small currents to provide voltage shifts that meet the operating voltage range of CS.

Different Intelli-Phase products have different operating voltage ranges for CS: V_{CS_MIN} and V_{CS_MAX}. Refer to each Intelli-Phase's datasheet to determine the minimum and maximum operating voltage range. Use equation (3) to determine a proper R_{CS} value:

$$V_{CS\_MIN} < I_{CS} R_{CS} + 1.23V < V_{CS\_MAX}$$
$$I_{CS} = IL \times Kcs \quad (3)$$

By pairing with Intelli-Phase, the MP2940A doesn't need temperature compensation and impendence matching to achieve accurate current sensing.

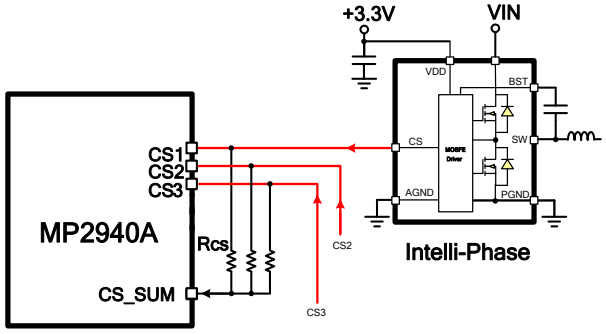


Figure 7: Phase Current Sense with 3-phase Configuration

IMON and IDROOP

The current flowing out from IMON is 1/32 of the filtered CS_SUM; it is named ISUM. Place a resistor from IMON to ground to generate a voltage proportional to the output current. The IMON voltage is sampled and converted by ADC and then stored in the Iout register, which is scaled to ICCMAX = ADC full range (FFh). The IMON voltage will get to its max data, V_{IMON_Max}, when the output current reaches ICCMAX.

The IMON voltage can be calculated with equation (4)

$$V_{IMON} = \frac{I_{OUT} \times K_{CS} \times R_{IMON}}{32} \quad (4)$$

Where:

Kcs is the current sense gain of Intelli-phase.

I_{OUT} is the output current.

R_{IMON} is the IMON resistor.

V_{IMON_Max}=1.6*8/11 V.

The R_{IMON} can be set with Iout=ICCMAX, and VIMON=V_{IMON_MAX}

$$R_{IMON} = \frac{32 \times V_{IMON\_Max}}{I_{CCMAX} \times K_{CS}} \quad (5)$$

Figure 8 shows the MP2940A IMON sense, and Idroop block diagram.

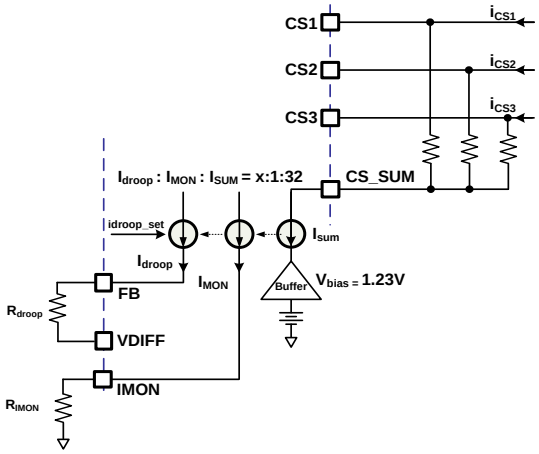


Figure 8: Current Sense Imon/ Idroop

Static Load Line Setting

The MP2940A uses a resistor between VFB and VDIFF to set the static load line. The droop current (default 1/8 of ISUM) flowing through the droop resistor from VFB to VDIFF generates the droop voltage. Given the application requirements for R_{LL} load line regulation, R_{droop} can be calculated according to equation (6) considering the 1/2 gain on the output remote sense.

$$R_{DROOP} = \frac{R_{LL}}{2 \times K_{CS} \times K_{Droop}} \quad (6)$$

Where K_{CS} is the current sense gain of the Intelli-Phase mentioned above. For the MP86901x series, the K_{CS} default value is 10μA/A. K_{Droop} is the gain of the droop current mirror, the default is 8/8*1/8.

Digital Programmable Load Line

Table 3: Digital Load Line Trim

IDROOP_SET [3:0]	Idroop Gain
0000 b	0
0001 b	4/8 * 1/8* I_{SUM}
0010 b	5/8 * 1/8* I_{SUM}
0011 b	6/8 * 1/8* I_{SUM}
0100 b	7/8 * 1/8* I_{SUM}
0101 b (Default)	**8/8 * 1/8* I_{SUM}**
0110 b	9/8 * 1/8* I_{SUM}
0111 b	10/8 * 1/8* I_{SUM}
1000 b	11/8 * 1/8* I_{SUM}
1001 b	12/8 * 1/8* I_{SUM}
1010 b	13/8 * 1/8* I_{SUM}
1011b	14/8 * 1/8* I_{SUM}
1100 b	15/8 * 1/8* I_{SUM}
1101 b	16/8 * 1/8* I_{SUM}
1110 b	17/8 * 1/8* I_{SUM}
1111 b	18/8 * 1/8* I_{SUM}

In addition to the load line setting from the external droop resistor, the MP2940A provides a digital programmable load line trim by register-idroop_set(1Bh[3:0]). The droop current mirror gain of the MP2940A is shown in Table 3. The load line can be changed through the PMBus and stored in MTP. With digital load line, users can change the droop without replacing the external droop resistor. The default value of idroop_set is 0001b, which presents a 1/8 gain to I_{SUM}.

IOUT Report

The Iout register 15h in the SVID register reports to the processor to avoid exceeding the thermal design point and maximum current capability of the system. The MP2940A applies a user-programmable register which contains the gain, MFR_IMON_SVID_GAIN (**FCh[7:0]**) and a signed current offset MFR_IMON_SVID_OFFSET (**FCh[14:8]**) on the SVID Iout reporting. The two programmable parameters allow users to match the IMON scaling to the design's Voltage Regulator Tolerance Band (VRTOB) calculation. This provides the most accurate current reporting across the entire load range and maximizes the performance of Intel turbo. Customers can reduce gain or offset to under report the total current to the CPU for better performance. Refer to the register map for details on how to configure the register **FCh**.

The PMBus Iout register **8Ch** is also used for total current protection. If the auto-phase shedding function is enabled via the PMBus, the total current report also will be used to determine whether to enter or exit the phase shedding mode to flatten the overall efficiency over the operating current range. Register IOUT_CAL_GAIN(**38h[10:0]**) and IOUT_CAL_OFFSET(**39h[5:0]**) are used to program the PMBus Iout report gain and offset to ensure the MP2940A tracks the load current efficiently (see Figure 9).

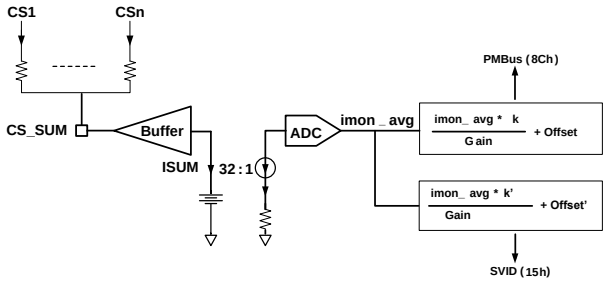


Figure 9: Total Current Sense and Report

Temperature Sense

The MP2940A measures the external temperature by connecting all the Intelli-Phase VTEMP pins (see Figure 10). The voltage of the MP2940A TEMP pin is the highest voltage among the Intelli-Phase, which indicates the highest temperature of the VR power system. The sensed temperature is used for an over-temperature fault protection, or asserting the SVID thermal alert or VRHOT# signal for the processor. A 49.9KΩ resistor in parallel with a 1μF capacitor from TEMP to GND is required to discharge TEMP.

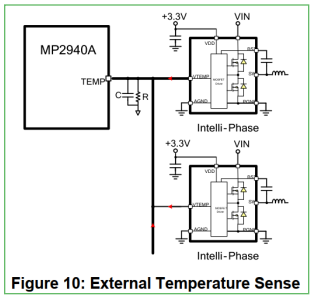


Figure 10: External Temperature Sense

VTEMP of Intelli-Phase is a voltage output proportional to the junction temperature. The junction temperature can be calculated using equation (7).

$$T_{JUNCTION} = \frac{V_{TEMP} + 100mV}{10mV / ^{\circ}C} \quad (7)$$

for $T_{JUNCTION} > 10^{\circ}C$

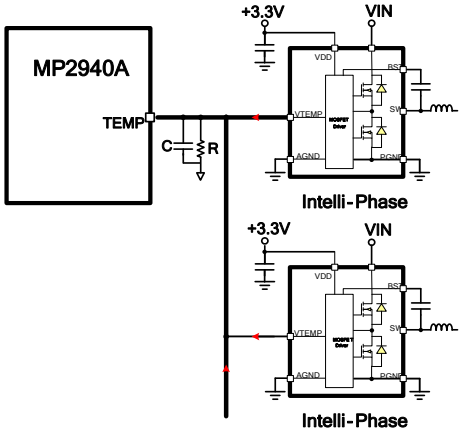


Figure 10: External Temperature Sense

For example, if the VTEMP voltage is 700mV, the junction temperature of that Intelli-Phase is 80°C. VTEMP cannot go below 0V, so it will read 0V for a junction temperature lower than 10°C.

Dynamic VID (DVID)

The MP2940A supports a Dynamic VID change when it receives SetVID (fast/slow/decay) commands.

The VID slew rate of SetVID_Fast is set by register VID_STEP_NUM (**FAh[7:6]**), which is equal to the VID increase or decrease per step. VID_SR_CNT(**FAh[5:0]**) defines the duration of time for the VID change one time. The fast slew rate can be calculated from the equation (8).

$$SlewRate = \frac{(VID\_STEP\_NUM + 1) \times VID\_STEP}{VID\_SR\_CNT \times 100ns} \quad (8)$$

Where VID_STEP_NUM is programmable from 0~3, VID_STEP is programmable to either 5mV or 10mV, according to the requirement of the CPU, and VID_SR_CNT is programmable in the range of 1 to 63. If VID_STEP_NUM is 1, VID_STEP is 5mV and VID_SR_CNT is 3, so the slew rate is 33.3mV/µs.

The SetVID_Slow slew rate is decided by register **F9h[3:0]**, which can be programmed to 1/2, 1/4, 1/8 or 1/16 of the SetVID_Fast. The slew rate for SetVID_Decay is determined by the load current and output capacitor bank.

FDh sets the Alert# assert time for DVID, a delay time can be added, which helps the MP2940A meet the Intel spec. Refer to the register map for details on how to configure the register **FDh**.

When DVID rises, the inductor current will rise to charge the output capacitors. This current will introduce a big positive droop voltage due to the load line, resulting in an output voltage lower than the target voltage, which may cause the output voltage to exceed the minimum regulation tolerance budget 1µs after Alert# asserts. The MP2940A can be programmed to ramp up more VID steps by register (**FAh[10:8]**). After VID ramps to the target voltage, it will keep this VID voltage for the time set by MFR_PLATFORM_TIME (**F1h[11:6]**). VID will fall back to the target VID voltage to cause the output voltage to rise into the regulation tolerance budget (TOB) as required by the Intel spec. Please refer to register map for the configuration.

When the output voltage is ramping down, the inductor current will become smaller to discharge the output capacitors, which will continue to discharge the output capacitors when the ramping ends. This may lead to output undershoot because of the droop voltage increase. It needs a duration of time for the inductance current to balance the load current, resulting in output voltage undershoot.

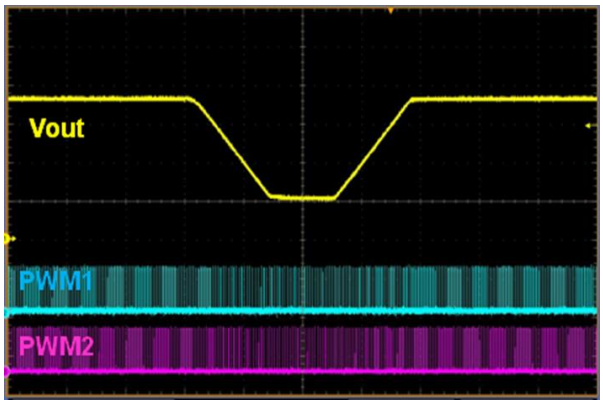


Figure 11. DVID Rise and Fall

The MP2940A applies a low-pass filter for the VID-DAC to smooth the reference voltage when the output voltage is ramping down.

Figure 11 shows the output voltage when SetVID_Fast rises after the previous SetVID_Fast fall is finished.

Programmable Audible Noise Reduction (PANR)

VR audible noise has been an issue for more than a decade. This issue is mainly caused by the capacitor flex with the voltage fluctuation at a certain frequency within the audible range. The MP2940A provides a control algorithm (PANR) to mitigate the voltage fluctuation within the range of audible frequency. This function can be activated by an enable bit. Two registers are available to program this function. If a SetVID down step is larger than a certain amplitude defined by register X, this command will be delayed for a certain time defined by register Y.

Auto-Phase Shedding (APS)

The MP2940A provides the auto-phase shedding function to improve the efficiency at PS0 state, according to the comparison between the total current report and the programmable threshold.

There are 3 types of registers to configure the auto-phase shedding function:

1. MFR_1PHL (**BBh[8:4]**) sets the phase shedding level. It is 1 phase at the CCM level. 2~3 phase CCM's level is MFR_1PHL * phase num. 1 phase DCM's level is fixed to 5A.
2. MFR_PHASE_HYS (**BBh[3:0]**) sets the hysteresis current value when phase adding.
3. phs_drop_dly (**30h[8:6]**) sets the delay time for the phase shedding action after the system's total current detected is smaller than the phase shedding threshold. Once the total current is higher than the phase adding threshold, idle phases will be added immediately. Please refer to the register map for the auto-phase shedding and adding configurations.

Table 4 and Table 5 list the phase shedding/adding entry conditions based on the current report.
In addition to the basic requirements listed in Table 4 and 5, the instructions below should be followed to improve the transient condition:

1. When the configured full phase number is smaller than the phase adding number, the system will run in full phase.
2. The DVID process will run in full phase if the VR receives the SetVID_Fast orSetVID_Slow command from the processor, regardless if the auto-phase shedding function is enabled or disabled. The phase shedding process starts after the VR is settled.
3. A load step up that causes VFB to fall below REFF – 15mV will trigger VR running in full phase to avoid the output voltage undershoot.

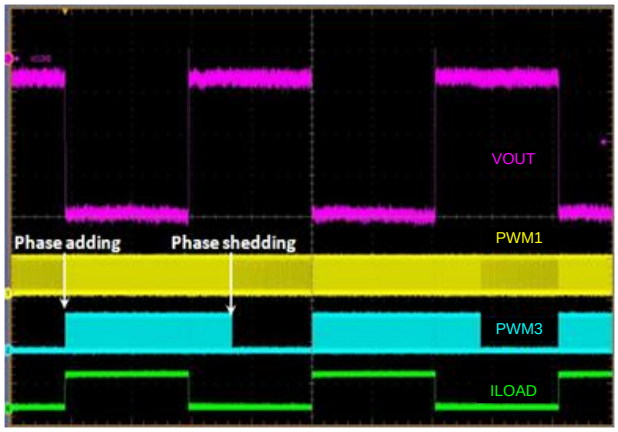


Figure 12: Phase Shedding and Adding Process

Table 4: Phase Number when Phase Adding Based on the Current Report (Iout)

Condition	Phase Number
2*MFR_1PHL + MFR_PHASE_HYS ≤ Iout	3 phase CCM or full(<3) phase CCM
1*MFR_1PHL + MFR_PHASE_HYS ≤ Iout < 2*MFR_1PHL+ MFR_PHASE_HYS	2 phase CCM or full(<2) phase CCM
5A + MFR_PHASE_HYS ≤ Iout < 1*MFR_1PHL+ MFR_PHASE_HYS	1 phase CCM
Iout < 5A + MFR_PHASE_HYS	1 phase DCM

Table 5: Phase Number when Phase Shedding Based on the Current Report (Iout)

Condition	Phase Number
2*MFR_1PHL < Iout	3 phase CCM or full(<3) phase CCM
1*MFR_1PHL < Iout≤ 2*MFR_1PHL	2 phase CCM or full(<2) phase CCM
5A < Iout≤ 1*MFR_1PHL	1 phase CCM
Iout ≤ 5A	1 phase DCM

IVID

The MP2940A supports an IVID function (defined in the IMVP8 spec) for automatic phase shedding and optimization, regardless if the PS state is required.

There are 2 types of registers for the IVID function:

1. IVIDx-VID: Only updated with the processor, which guarantees the current values are written in the IVIDx-I register.
2. IVIDx-I: Default setup by the VR vendor and can be rewritten by the processor. The registers reflect the maximum instantaneous current for the phase number being defined.

The IVID registers need to work with MFR_1PHL and MFR_PHASE_HYS registers to determine the active phase number. Table 6 lists the operation condition and the phase number.

In addition to the basic rules listed in Table 6, the VR also needs to follow the rules listed in the auto-phase shedding function section to improve the transient condition.

Figure 13 shows the IVID process. It uses the time set by register MFR_IVID_VALID_WAITTIME (**F9h[15:8]**) to start reducing the phase number after VR is settled, and phase adding immediately after receiving the SetVID command.

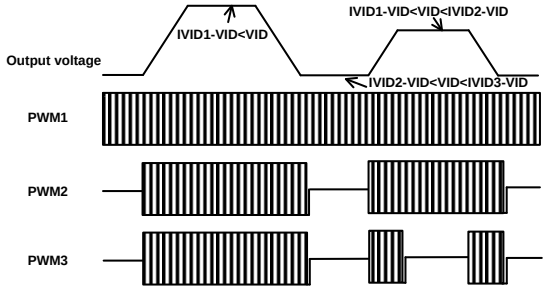


Figure 13: IVID Process when DVID

When the auto-phase shedding and IVID function are both enabled, the IVID function determines the phase number first, according to Table 6 based on the VID, then VR starts phase shedding according to Table 6 based on the current report.

To set up the auto-phase shedding and IVID functions, follow the steps below:

1. Set up the MFR_1PHL and MFR_PHASE_HYS according to the best efficiency performance of the Intelli-phase
2. Set up the IVID1-I, IVID2-I and IVID3-I according to the load application.

Table 6: Phase Shedding and Adding Based on the VID

Condition		Phase Number
VID> IVID1-VID		Full phase CCM
IVIDx-VID≥ VID> IVID(x+1)-VID(x=1,2) or IVID3-VID≥ VID	(n-1)*MFR_1PHL< IVIDx-I ≤ n*MFR_1PHL(n>1)	n phase CCMor Full(<n) phase CCM
IVIDx-VID≥ VID> IVID(x+1)-VID (x=1,2) or IVID3-VID≥ VID	5A< IVIDx-I ≤ 1*MFR_1PHL	1 phase CCM
IVIDx-VID≥ VID> IVID(x+1)-VID (x=1,2) or IVID3-VID≥ VID	IVIDx-I ≤ 5A	1 phase DCM

PMBus and SVID Communication

The MP2940A supports real time monitoring for the VR operation parameters and status monitoring with the PMBus and SVID interface. Table 7 lists the monitored parameters.

Table 7: PMBus and SVID Monitored Parameters

Parameter	PMBus	SVID
Output Voltage	×	×
Output Current	×	×
Temperature	×	×
Input Voltage	×	×
Input Power	×	×
Phase current	×	
OV	×	
OC	×	×
UV	×	
OT	×	×
CML	×	

Vin Protection:

The MP2940A adopts programmable Vin protection with the following protection thresholds programmed into the related PMBus registers.

The VR will tri-state shut off immediately if the sensed input voltage is below VIN_OFF （**36h[7:0]**. It restarts when the sensed input voltage is above VIN_ON (**35h[7:0]**) with Vin UVLO non-latch mode.

The VR will latch if the sensed input voltage is above VIN_OV_FAULT_LIMIT (**55h[7:0]**) when the Vin OVP is set to latch mode.

The VR is warned if the input voltage is below VIN_UV_WARNING_LIMIT (**58h[7:0]**).

Over-Voltage Protection (OVP)

The OVP circuit monitors the output voltage for an over-voltage condition. The over-voltage signals generation is shown in Figure 14.

There are two levels of over-voltage protection.

OVP2 is the first level of over-voltage protection. When the detected output voltage is 400mV higher than the reference voltage, the controller triggers OV protection after a certain delay time; the OVP2 action will latch PWM low on to discharge the output until the output drops below 160mV (RVP triggered). OVP2 is defined as REF+200mV for the 1/2 gain of the output voltage to VDIFF. Figure 15 shows the VR behavior when OVP2 is triggered.

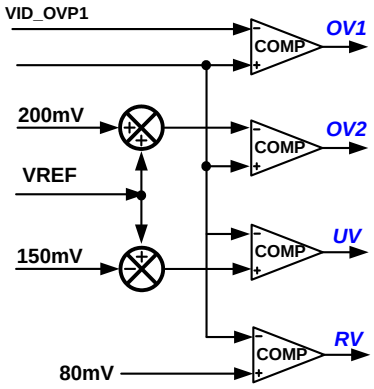


Figure 14: OVP and RVP Trigger Threshold

To avoid a false trigger, the OVP2 is blanked during soft start and shutdown, and the VID transition period (including SetVID Fast/Slow/ Decay). It sets PS4 as well.

The OVP2 default is latch off in normal IMVP8/9 applications. Additional modes like retry and hiccup mode are available to be set by register MFR_OVP2_SET_MODE **(F1h[5:4]).** The OVP delay time is set by register OVP2 DELAYTIME (**F7h[11:6]).**

OVP1 is the second level of over-protection protection. It is set by OVP_DA_LIMIT(**F6h[7:0]**). This is an absolute OV threshold, which is active whenever the controller is enabled, regardless of operation/fault conditions. In the event of an OVP1 condition, the PWMs are latched low to turn off the high-side MOSFETs and turn on the low-side MOSFETs to discharge the output voltage. The OVP1 latch can only be reset by EN or toggling VCC.

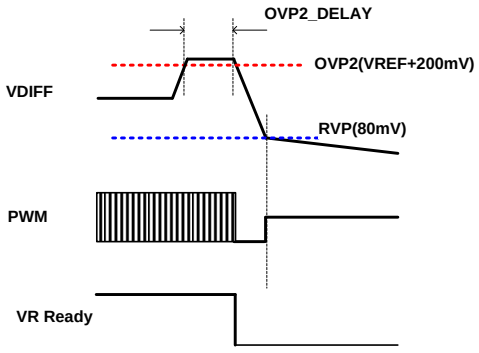


Figure 15: OVP and RVP Fault Protection

Reverse Voltage Protection (RVP)

During an OVP period, the LS will remain on to make the inductor current go negative. A large reverse inductor current may cause negative output voltages that harm the processor and other output components. In addition to OV protection, the MP2940A implements a reverse voltage protection (RVP) to avoid the negative voltage ringing after the OV logic is triggered. Once the VDIFF voltage drops below 80mV, the MP2940A will trigger the RVP by latching all PWM outputs to tri-state. The reverse inductor current can quickly reset to 0A by dissipating the energy in the inductor to the input DC voltage source through a forward-biased body diode of the high-side MOSFETs (see Figure 15).

Over-Current Protection (OCP)

The MP2940A provides a programmable total current protection to stop the VR from operating at an extremely heavy load; it will be triggered if the sensed average total output current is higher than the OC trigger level MFR_OCP_SET_LEVEL (**EEH[6:0]**). Once the sensed Iout is over the set OCP level, with a set delay time MFR_OCP_SET_DELAY_TIME (**EEH[13:8]**), the part will turn off both the HS and LS FETs by setting the PWM to tri-state. Figure 16 shows the diagram of the OCP process for total current protection.

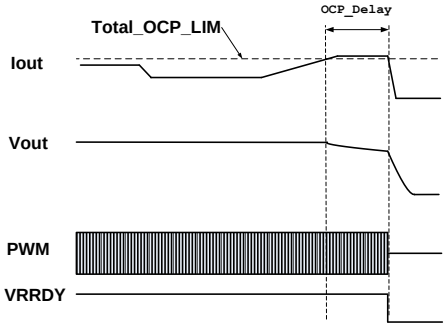


Figure 16: OC Protection for Total Current

The total OCP limit and delay time is set at register **EEh**. The OCP set point is recommended to be set around 130% of Iccmax. The OCP delay is recommended around 500µs.

Phase Current Limit Protection

In addition to the total over-current limit based on the sensed Iout, the MP2940A also utilizes a cycle-by-cycle valley point over-current limit method to limit each phase current. If the present phase current is higher than the setting valley point and remains for 80ns, this phase will not turn on, and the next phase will turn on when its own PWM is on, in order to regulate the output voltage at the set point. The phase current limit itself will not trigger latch off, latch off is triggered when the phase current limit is triggered by either the OCP or UVP.

The valley point over-current level can be programmed via the PMBus to limit the per phase current in register OCP_DA_LIMIT (**F6h[15:8]**) .

Figure 17 shows the process when the output is shorted to ground. During this process, the per phase OCP will limit the phase current immediately and after a certain time the VR will shut down.

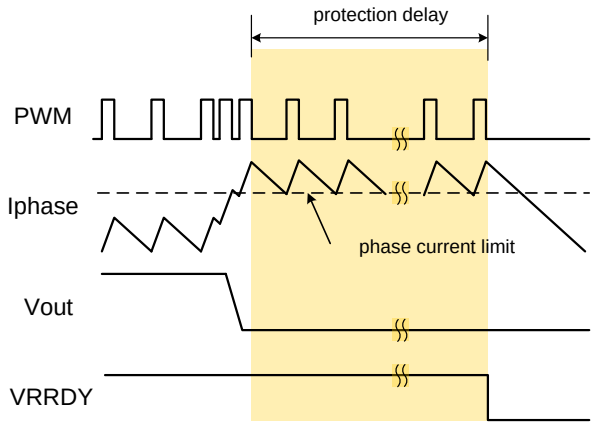


Figure 17: Phase Current Limit Protection when Output Dead Short

Under-Voltage Protection (UVP)

If the sensed output voltage (VDIFF) is low (below VREF-150mV) for a certain amount of time, the system will trigger UVP and immediately shut down and turn off all phases set by the PWM into tri-state (see Figure 18). Normally, UVP is triggered when OCP is reached. The UVP protection model (Default Latch) can be set through register MFR_UVP_SET_MODE (**F1h[7:6]).** The UVP delay time is set by register

UVP DELAYTIME (**F7h[5:0]).** Refer to the register list for more details.

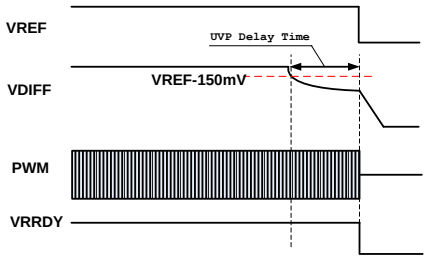


Figure 18: Under-Voltage Protection

VR_HOT#

The VR_HOT# fault is asserted when the sensed external temperature exceeds the temp max threshold. This is used for fault reporting only and it cannot shut down the system. VR_HOT# also has a fixed 3°C hysteresis when VR_HOT# asserts if the sensed temperature exceeds the temp max. The VR_HOT# pin will also assert when PSYS exceeds the critical value. VR_HOT# is initialized in tri-state when the device powers up.

Phase Current Balancing/Thermal Balancing

The phase current to the MP2940A is sensed and calculated with the current reference in the slow current PI loop. Each phase's PWM on time is adjusted individually to balance the currents by applying Σ-Δ modulation and delay line loop technology in the current balance modulation, so the current is balanced and the jitter is greatly reduced.

Each current balance loop can also include the programmable phase current offset to achieve the thermal balance among the phases. The phase that has the worst cooling capability can be set to take less phase current by adding an offset on the CS sample value. This keeps the phase thermals more balanced. Please refer to the register map for the phase current offset configuration.

SVID Interface

To support multiple VR devices used on the same SVID bus, the SVID address can be programmed independently through the register MFR_ADDR_SVID (E6h[11:0]). The SVID address is a 4 bit code. There are 14 addresses for up to 14 voltage regulator controllers. The final addresses 0Eh and 0Fh are "All Call" addresses, and all the VR controllers respond to those addresses.

The All Call address will only be used with SetVID or SetPS commands. It cannot be used with GET or SetRegADR and SetRegDAT commands. The VR will NAK those commands with an All Call address. The VR acknowledges an All Call address in the same manner as a single address.

Input Power Sense

The SVID address 0Dh domain is defined to report the system input power. When the voltage of PSYS reaches 0.8V, it means the platform input power has reached Pwr_in_Max and the report value for the CPU is FFh in the 1Bh SVID register.

The input power sensing device sends a current signal to the MP2940A, which is proportional to the input power. A resistor from PSYS to GND will convert the current into voltage. A bypass capacitor is required. Figure 19 shows the PSYS connection. The PSYS resistor value is calculated with Equation (9):

$$R_{PSYS} = \frac{0.8}{P_{wr\_in\_max} \times I_{sys}} \quad (9)$$

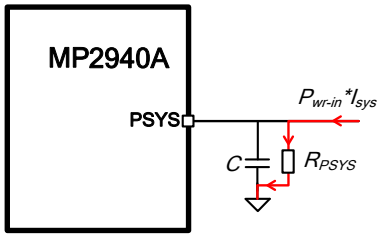


Figure 19: PSYS Connection

Where I_{sys} is the current gain of the input power sensor, with the unit of μA/W.

Pwr_in_Max is the maximum input power, with the unit of W.

The averaging interval of the input power sense is 1ms, and the register update interval is 500μs.

PS4 Enter/Exit Mechanism

The VR will enter PS4 mode after receiving a SETPS4 command, and VR changes the VID of the VR to 00h and

stops the PWM(s) of the VR immediately. ALERT# remains de-asserted in PS4, the chip turns off PLL and disables as many analog circuits as possible to save power (except the SVID interface).

The SetVID or SetPS0/1/2/3 commands are used to wake the VR from PS4 mode. When VR receives a SetVID or SetPS0/1/2/3 command, it enables the internal PLL and analog circuits. PS4 exit latency is less than 90µs, counted from ACK of the PS4 exit command to where VID is ready to ramp (SETPS) or (SETVID) starts ramping.

STB Function

STB is used to set MPS Intelli-Phase into standby mode by connecting STB to SYNC of the MPS Intelli-Phase. In PS4 mode, STB will go into tri-state, so Intelli-Phase will enter low power mode to save power. In normal operation mode, STB is logic high. Figure 20 shows the connection between the MP2940A STB pin and the MPS Intelli-Phase SYNC pin.

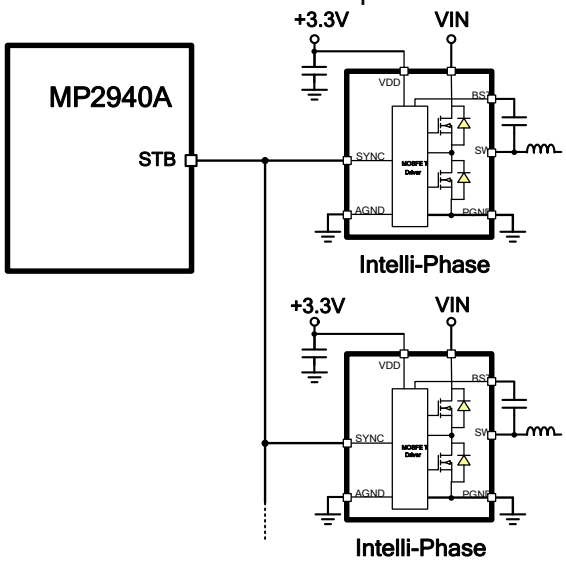


Figure 20: STB Connection between MP2940A and MPS Intelli-Phase

PVID Function for VccAUX

The MP2940A supports both a SVID interface, and a PVID interface. Pin 12 (SCLK/VID0) and pin 13 (SDIO/VID1) are multi-function pins and can be configured by the PMBUS register setting. When the MP2940A is configured to support the Intel CPU, pins 12 and 13 are selected as SCLK/SDIO to be the SVID interface. When the MP2940A is configured to support the VccAUX rail, pins 12 and 13 are selected as the PVID VID0 and VID1 input. When the PVID interface is selected, there are a total of 4 VID1/0 combinations to indicate 4 different output voltage levels. VID1/0=00 always means the output is 0V. For the other 3 combinations of VID1/0 (01, 10, 11), there are 3 corresponding PMBUS registers to set the output voltage level. By utilizing the MP2940A programmable function, the MP2940A is capable of supporting any combination of the target voltage level (see Table 8).

In PVID mode, Alert# (pin 14) is high and VRhot# (pin 16) is low.

Table 8: VID1/0 Output Voltage Selection

VID1/VID0	Output Voltage
00	**0V**
01	**Register Programmable Default 1.1V**
10	**Register Programmable Default 1.65V**
11	**Register Programmable Default 1.8V**

SVID REGISTERS

Table 9 shows the data and configuration registers for the SVID protocol.

Table 9: SVID Data and Configuration Registers

Index	Register Name	Access	Default	Note
00h	Vendor ID	Read Only by Master Write by Vendor	25h	Programmable through PMBus
01h	Product ID		0Bh	Programmable through PMBus
02h	Product Revision		00h	Programmable through PMBus
05h	Protocol ID		05h	Programmable through PMBus
06h	Capability		81h	Programmable through PMBus
10h	Status_1	Read by Master Write by PWM	00h	These registers are operation condition dependent. The register values vary with operating conditions.
11h	Status_2		00h	
12h	Temperature zone		00h	
15h	Output Current (Iout)		00h	
17h	VR Temperature		00h	
1Bh	Input Power		00h	
1Ch	Status2_last read		00h	
21h	ICC_MAX	Read Only Configured by the Platform	00h	Programmable through PMBus
24h	SR-fast		30mV/us	Programmable through PMBus
25h	SR-slow		15mV/us	Programmable through PMBus
30h	Vout max	Read & Write by Master	FFH	Can only be programmed by CPU
31h	VID setting		00H	Can only be programmed by CPU
32h	Pwr State		00H	Can only be programmed by CPU
34h	Multi VR configure	Read by Master Write by PWM	01H	Programmable through PMBus
42h	IVID1-VID	Read & Write by Master	00h	Programmable through PMBus
44h	IVID2-VID		00h	Programmable through PMBus
46h	IVID3-VID		00h	Programmable through PMBus
43h	IVID1-I		0Fh	CPU may program these registers during system boot.
45h	IVID2-I		0Fh	
47h	IVID3-I		05h	

VID RANGE

The MP2940A covers the full IMVP8/IMVP9 VID range. The IMVP8 VID is 0V, 0.25V~1.52V. Between 0.25V~1.52V, the voltage step is 5mV/step. The IMVP9 VID step is 5mV and 10mV; the voltage of the 5mV VID step matches the IMVP8. The 10mV/step of the IMVP9 VID is 0V, 0.2V~2.74V. Between 0.2V~2.74V, the voltage step is 10mV/step. See Table 10 and Table 11.

Table 10: IMVP8 5mVVID Step VID Table

VID(HEX)	VOUT(V)	VID(HEX)	VOUT(V)	VID(HEX)	VOUT(V)	VID(HEX)	VOUT(V)
00	0	40	0.565	80	0.885	C0	1.205
01	0.25	41	0.57	81	0.89	C1	1.21
02	0.255	42	0.575	82	0.895	C2	1.215
03	0.26	43	0.58	83	0.9	C3	1.22
04	0.265	44	0.585	84	0.905	C4	1.225
05	0.27	45	0.59	85	0.91	C5	1.23
06	0.275	46	0.595	86	0.915	C6	1.235
07	0.28	47	0.6	87	0.92	C7	1.24
08	0.285	48	0.605	88	0.925	C8	1.245
09	0.29	49	0.61	89	0.93	C9	1.25
0A	0.295	4A	0.615	8A	0.935	CA	1.255
0B	0.3	4B	0.62	8B	0.94	CB	1.26
0C	0.305	4C	0.625	8C	0.945	CC	1.265
0D	0.31	4D	0.63	8D	0.95	CD	1.27
0E	0.315	4E	0.635	8E	0.955	CE	1.275
0F	0.32	4F	0.64	8F	0.96	CF	1.28
10	0.325	50	0.645	90	0.965	D0	1.285
11	0.33	51	0.65	91	0.97	D1	1.29
12	0.335	52	0.655	92	0.975	D2	1.295
13	0.34	53	0.66	93	0.98	D3	1.3
14	0.345	54	0.665	94	0.985	D4	1.305
15	0.35	55	0.67	95	0.99	D5	1.31
16	0.355	56	0.675	96	0.995	D6	1.315
17	0.36	57	0.68	97	1	D7	1.32
18	0.365	58	0.685	98	1.005	D8	1.325
19	0.37	59	0.69	99	1.01	D9	1.33
1A	0.375	5A	0.695	9A	1.015	DA	1.335
1B	0.38	5B	0.7	9B	1.02	DB	1.34
1C	0.385	5C	0.705	9C	1.025	DC	1.345
1D	0.39	5D	0.71	9D	1.03	DD	1.35
1E	0.395	5E	0.715	9E	1.035	DE	1.355
1F	0.4	5F	0.72	9F	1.04	DF	1.36
20	0.405	60	0.725	A0	1.045	E0	1.365
21	0.41	61	0.73	A1	1.05	E1	1.37
22	0.415	62	0.735	A2	1.055	E2	1.375
23	0.42	63	0.74	A3	1.06	E3	1.38
24	0.425	64	0.745	A4	1.065	E4	1.385
25	0.43	65	0.75	A5	1.07	E5	1.39
26	0.435	66	0.755	A6	1.075	E6	1.395
27	0.44	67	0.76	A7	1.08	E7	1.4
28	0.445	68	0.765	A8	1.085	E8	1.405
29	0.45	69	0.77	A9	1.09	E9	1.41
2A	0.455	6A	0.775	AA	1.095	EA	1.415
2B	0.46	6B	0.78	AB	1.1	EB	1.42
2C	0.465	6C	0.785	AC	1.105	EC	1.425

2D	0.47	6D	0.79	AD	1.11	ED	1.43
2E	0.475	6E	0.795	AE	1.115	EE	1.435
2F	0.48	6F	0.8	AF	1.12	EF	1.44
30	0.485	70	0.805	B0	1.125	F0	1.445
31	0.49	71	0.81	B1	1.13	F1	1.45
32	0.495	72	0.815	B2	1.135	F2	1.455
33	0.5	73	0.82	B3	1.14	F3	1.46
34	0.505	74	0.825	B4	1.145	F4	1.465
35	0.51	75	0.83	B5	1.15	F5	1.47
36	0.515	76	0.835	B6	1.155	F6	1.475
37	0.52	77	0.84	B7	1.16	F7	1.48
38	0.525	78	0.845	B8	1.165	F8	1.485
39	0.53	79	0.85	B9	1.17	F9	1.49
3A	0.535	7A	0.855	BA	1.175	FA	1.495
3B	0.54	7B	0.86	BB	1.18	FB	1.5
3C	0.545	7C	0.865	BC	1.185	FC	1.505
3D	0.55	7D	0.87	BD	1.19	FD	1.51
3E	0.555	7E	0.875	BE	1.195	FE	1.515
3F	0.56	7F	0.88	BF	1.2	FF	1.52

Table 11: IMVP9 10mV VID Step VID Table

VID(HEX)	VOUT(V)	VID(HEX)	VOUT(V)	VID(HEX)	VOUT(V)	VID(HEX)	VOUT(V)
00	0	40	0.83	80	1.47	C0	2.11
01	0.2	41	0.84	81	1.48	C1	2.12
02	0.21	42	0.85	82	1.49	C2	2.13
03	0.22	43	0.86	83	1.5	C3	2.14
04	0.23	44	0.87	84	1.51	C4	2.15
05	0.24	45	0.88	85	1.52	C5	2.16
06	0.25	46	0.89	86	1.53	C6	2.17
07	0.26	47	0.9	87	1.54	C7	2.18
08	0.27	48	0.91	88	1.55	C8	2.19
09	0.28	49	0.92	89	1.56	C9	2.2
0A	0.29	4A	0.93	8A	1.57	CA	2.21
0B	0.3	4B	0.94	8B	1.58	CB	2.22
0C	0.31	4C	0.95	8C	1.59	CC	2.23
0D	0.32	4D	0.96	8D	1.6	CD	2.24
0E	0.33	4E	0.97	8E	1.61	CE	2.25
0F	0.34	4F	0.98	8F	1.62	CF	2.26
10	0.35	50	0.99	90	1.63	D0	2.27
11	0.36	51	1	91	1.64	D1	2.28
12	0.37	52	1.01	92	1.65	D2	2.29
13	0.38	53	1.02	93	1.66	D3	2.3
14	0.39	54	1.03	94	1.67	D4	2.31
15	0.4	55	1.04	95	1.68	D5	2.32
16	0.41	56	1.05	96	1.69	D6	2.33
17	0.42	57	1.06	97	1.7	D7	2.34
18	0.43	58	1.07	98	1.71	D8	2.35
19	0.44	59	1.08	99	1.72	D9	2.36
1A	0.45	5A	1.09	9A	1.73	DA	2.37
1B	0.46	5B	1.1	9B	1.74	DB	2.38
1C	0.47	5C	1.11	9C	1.75	DC	2.39
1D	0.48	5D	1.12	9D	1.76	DD	2.4
1E	0.49	5E	1.13	9E	1.77	DE	2.41
1F	0.5	5F	1.14	9F	1.78	DF	2.42
20	0.51	60	1.15	A0	1.79	E0	2.43
21	0.52	61	1.16	A1	1.8	E1	2.44
22	0.53	62	1.17	A2	1.81	E2	2.45
23	0.54	63	1.18	A3	1.82	E3	2.46
24	0.55	64	1.19	A4	1.83	E4	2.47
25	0.56	65	1.2	A5	1.84	E5	2.48
26	0.57	66	1.21	A6	1.85	E6	2.49
27	0.58	67	1.22	A7	1.86	E7	2.5
28	0.59	68	1.23	A8	1.87	E8	2.51
29	0.6	69	1.24	A9	1.88	E9	2.52
2A	0.61	6A	1.25	AA	1.89	EA	2.53
2B	0.62	6B	1.26	AB	1.9	EB	2.54
2C	0.63	6C	1.27	AC	1.91	EC	2.55
2D	0.64	6D	1.28	AD	1.92	ED	2.56
2E	0.65	6E	1.29	AE	1.93	EE	2.57
2F	0.66	6F	1.3	AF	1.94	EF	2.58
30	0.67	70	1.31	B0	1.95	F0	2.59
31	0.68	71	1.32	B1	1.96	F1	2.6
32	0.69	72	1.33	B2	1.97	F2	2.61

33	0.7	73	1.34	B3	1.98	F3	2.62
34	0.71	74	1.35	B4	1.99	F4	2.63
35	0.72	75	1.36	B5	2	F5	2.64
36	0.73	76	1.37	B6	2.01	F6	2.65
37	0.74	77	1.38	B7	2.02	F7	2.66
38	0.75	78	1.39	B8	2.03	F8	2.67
39	0.76	79	1.4	B9	2.04	F9	2.68
3A	0.77	7A	1.41	BA	2.05	FA	2.69
3B	0.78	7B	1.42	BB	2.06	FB	2.7
3C	0.79	7C	1.43	BC	2.07	FC	2.71
3D	0.8	7D	1.44	BD	2.08	FD	2.72
3E	0.81	7E	1.45	BE	2.09	FE	2.73
3F	0.82	7F	1.46	BF	2.1	FF	2.74

Selected PMBus Register Map

The PMBus registers are distributed into Page 0. This section contains most of the functional resistors for all of the rails with details on how to program the register data.

PMBUS COMMANDS/REGISTERS (PAGE 0)

Command Code	Command Name	Type	Bytes	Page 0
00h	PAGE	r/w	1	✓
01h	OPERATION	r/w	1	✓
03h	CLEAR_FAULTS	send	0	✓
07h	LAST_FAULT_BLOCK	r/w	2	✓
08h	CLEAR_LAST_FAULT	send	0	✓
15h	STORE_USER_ALL	send	0	✓
16h	RESTORE_USER_ALL	send	0	✓
1Bh	IDROOP_CTRL	r/w	2	✓
1Dh	MFR_MTP CTRL	r/w	2	✓
1Eh	PSYS_WARN_FILT_CNT	r/w	1	✓
21h	VOUT_COMMAND	r/w	2	✓
22h	MFR_VOUT_TRIM	r/w	2	✓
23h	VOUT_CAL_OFFSET	r/w	2	✓
24h	MFR_VOUT_MAX	r/w	2	✓
25h	VOUT_MARGIN_HIGH	r/w	2	✓
26h	VOUT_MARGIN_LOW	r/w	2	✓
2Bh	MFR_IMMEDIATE_SET	r/w	2	✓
2Eh	MFR_PLATFORM_TIME	r/w	2	✓
30h	MFR_APSI_CTRL	r/w	2	✓
35h	VIN_ON	r/w	2	✓
36h	VIN_OFF	r/w	2	✓
38h	IOUT_CAL_GAIN	r/w	2	✓
39h	IOUT_CAL_OFFSET	r/w	2	✓
3Ah	MFR_IMON_SVID1	r/w	2	✓
3Bh	MFR_IMON_SVID2	r/w	2	✓
3Ch	MFR_IMON_SVID3	r/w	2	✓
50h	MFR_SYS_PASSWORD	r/w	1	✓
51h	MFR_INPUT_PASSWORD	r/w	1	✓
55h	VIN_OV_FAULT_LIMIT	r/w	2	✓
58h	VIN_UV_WARNING_LIMIT	r/w	2	✓
72h	SVID_REG_80H_81H	r	2	✓
73h	SVID_REG_82H	r	1	✓
74h	SLAVE_ADDR	r	1	✓
75h	MFR_CS_1_2	r	2	✓
76h	MFR_CS_3	r	2	✓
7Ah	STATUS_VOUT	r	1	✓
7Bh	STATUS_IOUT	r	1	✓
7Ch	STATUS_INPUT	r	1	✓
7Dh	STATUS_TEMPERATURE	r	1	✓
7Eh	STATUS_CML	r	1	✓
88h	READ_VIN	r	2	✓
8Bh	READ_VOUT	r	2	✓
8Ch	READ_IOUT	r	2	✓
8Dh	READ_TEMPERATURE	r	2	✓
96h	READ_POUT	r	2	✓
97h	READ_PIN	r	2	✓
B8h	MFR_VIN_HYS	r/w	1	✓

PMBUS COMMANDS/REGISTERS (PAGE 0) *(continued)*

Command Code	Command Name	Type	Bytes	Page0
BBh	MFR_1PHL_HYS	r/w	1	✓
BDh	PROTOCOL_ID_SVID_RDY_VR	r/w	2	✓
BEh	PS3_ PS4_EXIT_DELAY	r/w	2	✓
BFh	VENDOR_ID_PRODUCT_ID	r/w	2	✓
C0h	PRODUCT_DATA_CODE_VR	r/w	2	✓
C1h	LOT_CODE_VR	r/w	2	✓
C2h	DECAY_CFG_34H_06H	r/w	2	✓
C3h	TOLERANCE_SR_FAST	r/w	2	✓
C4h	MFR_VOUT_MAX_9BIT	r/w	2	✓
C5h	IVID2_1_I_DEF	r/w	2	✓
C6h	PIN_MAX_IVID3_I_DEF	r/w	2	✓
CAh	MFR_PHASE_NUM	r/w	1	✓
CCh	DC_CTRL_DYNAMIC_FLT	r/w	2	✓
CDh	MFR_SW_HF_SET	r/w	2	✓
CEh	MIN_ON_OFF_BLANK_TIME	r/w	2	✓
CFh	MFR_SW_LF_SET	r/w	2	✓
D6h	MFR_SLOPE_SR_3P	r/w	2	✓
D7h	MFR_SLOPE_CNT_3P	r/w	2	✓
D8h	MFR_SLOPE_SR_2P	r/w	2	✓
D9h	MFR_SLOPE_CNT_2P	r/w	2	✓
DAh	MFR_SLOPE_SR_1P	r/w	2	✓
DBh	MFR_SLOPE_CNT_1P	r/w	2	✓
DCh	MFR_SLOPE_SR_DCM	r/w	2	✓
DDh	MFR_SLOPE_CNT_DCM	r/w	2	✓
DEh	MFR _TRIM_2_1_DCM	r/w	2	✓
DFh	MFR_TRIM_3	r/w	2	✓
E1h	SHUTLEVEL_ADDRPMBUS	r/w	2	✓
E2h	MFR_CB_SATU_PI	r/w	2	✓
E3h	MFR_VCAL_PI	r/w	2	✓
E4h	MFR_VR_CONFIG	r/w	2	✓
E5h	MFR_FS _VBOOT	r/w	2	✓
E6h	MFR_ADDR_SVID	r/w	2	✓
E8h	TEMPERATURE_GAIN_OFFSET	r/w	2	✓
E9h	MFR_CUR_GAIN	r/w	2	✓
EAh	MFR_CUR_OFFSET	r/w	1	✓
EBh	MFR_CS_OFFSET1_2	r/w	2	✓
ECh	MFR_CS_OFFSET3	r/w	2	✓
EEh	MFR_OCP_SET	r/w	2	✓
EFh	MFR_ICC_MAX	r/w	2	✓
F0h	MFR_VOUT_CMPS_MAX	r/w	1	✓
F1h	MFR_PROTECT_CFG	r/w	2	✓
F2h	MFR_OTP_SET	r/w	2	✓
F3h	MFR_TEMP_MAX	r/w	2	✓
F5h	MFR_AUDIBLE_REDUCE	r/w	2	✓
F6h	OCP_OVP_DA_LIMIT	r/w	1	✓
F7h	MFR_OVP_UVP_SET	r/w	2	✓
F8h	MFR_VID_DOWN_DELAY	r/w	2	✓
F9h	MFR_FILTER_SET	r/w	2	✓
FAh	MFR_TRANS_FAST	r/w	2	✓
FBh	MFR_EN_SEQUENCE_CFG	r/w	2	✓

PMBUS COMMANDS/REGISTERS (PAGE 0) *(continued)*

Command Code	Command Name	Type	Bytes	Page0
FCh	MFR_PSYS_SVID	r/w	2	✓
FDh	MFR_ALT_SET	r/w	2	✓
FEh	CLEAR_EEPROM_FAULTS	send	0	✓

PAGE 0 REGISTER MAP

PAGE (00h)

The PAGE command provides the ability to configure, control, and monitor through only one physical address for the three rails and test mode.

Command	PAGE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r/w	r/w
Function	X	X	X	X	X	X	PAGE	

Bits	Bit Name	Description
[7:1]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[0]	PAGE	1’b0: Page 0 for register configuration 1’b1: Page 1 for the test mode

OPERATION (01h)

The OPERATION command on Page 0 is used to turn the output on or off in conjunction with input from EN. OPERATION is also used to set the output voltage to the upper or lower margin voltages. The unit stays in the commanded operating mode until a subsequent OPERATION command or a change in the state of EN instructs the device to change to another mode.

Command	OPERATION							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	OPERATION_MODE							

Bit[7:6]	Bit[5:4]	Bit[3:2]	Bit[1:0]	On/off	Margin state
0x	xx	xx	xx	Immediate off	N/A
10	00	xx	xx	on	off
10	01	01	xx	on	Margin low (ignore fault)
10	01	10	xx	on	Margin low (act on fault)
10	10	01	xx	on	Margin high (ignore fault)
10	10	10	xx	on	Margin high (act on fault)

CLEAR_FAULTS (03h)

The CLEAR_FAULTS command is used to clear any fault bits that have been set on Rail A. This command clears all bits in all status registers simultaneously. This command is write only. There is no data byte for this command.

LAST_FAULT_BLOCK (07h)

This command is used to record any protection, regardless of the rail when OVP1, OVP2, OCP, UVP, VIN_OVP, VIN_UVLO, OTP, or TEMP_FAULT occurs.

Command	LAST_FAULT_BLOCK															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	X	X	X	X	X	X	X	X								

Bits	Bit Name	Description
[7]	OVP1	Flag of OVP1. Read only.
[6]	OVP2	Flag of OVP2. Read only.
[5]	OCP	Flag of OCP. Read only.
[4]	UVP	Flag of UVP. Read only.
[3]	VIN_OVP	Flag of V_{IN} OVP. Read only.
[2]	VIN_UVLO	Flag of V_{IN} UVLO. Read only.
[1]	OTP	Flag of OTP. Read only.
[0]	TEMP_FAULT	Flag of TEMP fault. Read only.

When VR restarts after a protection shutdown, the data of the flag in MTP is restored to memory 07h. If any bit of 07h is 1'b1, protect_fault_record_en = 1, and register 1Dh[6] is equal to 1'b1, the VR will not start up after sending the CLEAR_EEPROM_FAULTS (FEh) command until the CLEAR_LAST_FAULT command (08h) is sent.

CLEAR_LAST_FAULT (08h)

See the LAST_FAULT_BLOCK (07h) section above.

STORE_USER_ALL (15h)

The STORE_USER_ALL command instructs the PMBus device to copy the Page 0 ~ Page 1 contents (not including read-only registers) of the operating memory to the matching locations in the MTP, regardless of the current PMBus register page. This command can be used while the device is outputting power. This command is write only. There is no data byte for this command.

RESTORE_USER_ALL (16h)

The RESTORE_USER_ALL command instructs the PMBus device to copy the Page 0 ~ Page 1 contents of the MTP to the matching locations in the operating memory. The values in the operating memory are overwritten by the value retrieved from the user store. Any items in the user store that do not have matching locations in the operating memory are ignored. It is *not* permitted to use this command while the device is outputting power unless MFR_EEPROM_COPY_EN (register 1Dh[1] on Page 0) is set to 1. This command is write only. There is no data byte for this command.

IDROOP_CTRL (1Bh)

The IDROOP_CTRL command on Page 0 is used to set the IDROOP bandwidth for all rails and the IDROOP DC gain for Rail A.

Command	IDROOP_CTRL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	MFR_GATECLK_DIS						droop_comp						IDROOP_DC_SET			

Bits	Bit Name	Description
[15]	MFR_GATECLK_DIS[5]	Disable gate clk for all calculation module, high effective.
[14]	MFR_GATECLK_DIS[4]	Disable gate clk for PMBUS communication, high effective.
[13]	MFR_GATECLK_DIS[3]	Disable gate clk for clk_mem, high effective.
[12]	MFR_GATECLK_DIS[2]	Disable gate clk for rail_ctrl module, high effective.
[11]	MFR_GATECLK_DIS[1]	Disable gate clk for analog_ctrl module, high effective.
[10]	MFR_GATECLK_DIS[0]	Disable gate clk for clk_reg_slave, high effective.
[9:7]	droop_comp	It is used to select bandwidth and bias current for ac droop.
[6]	dac_cmp_en	It is used to enable dac_cmp. 1'b0 : disable 1'b1 : enable
[5]	idroop_bw_set	It is used to select the bandwidth of Idroop. 1'b0 : low bandwidth 1'b1 : high bandwidth
[4]	idroop_en	It is used to enable DC Idroop or AC Idroop. 1'b0 : enable DC Idroop 1'b1 : enable AC Idroop
[3:0]	idroop_set	Set the Idroop DC gain to set digital load line gain. The default value of 'Idroop_set' is 4'h5 Idroop_set[3:0] Gain Idroop_set[3:0] Gain 1'h 0 0 1'h 8 11/8 * 1/8 1'h 1 4/8 * 1/8 1'h 9 12/8 * 1/8 1'h 2 5/8 * 1/8 1'h A 13/8 * 1/8 1'h 3 6/8 * 1/8 1'h B 14/8 * 1/8 1'h 4 7/8 * 1/8 1'h C 15/8 * 1/8 1'h 5 8/8 * 1/8 1'h D 16/8 * 1/8 1'h 6 9/8 * 1/8 1'h E 17/8 * 1/8 1'h 7 10/8 * 1/8 1'h F 18/8 * 1/8

MFR_MTP_CTRL (1Dh)

The MFR_MTP_CTRL command on Page 0 is used to control the operation of the MTP and LAST_FAULT_BLOCK function.

Command	MFR_EEPROM_CTRL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	MFR_MTP_PASSWORD															

Bits	Bit Name	Description
[15:8]	MFR_MTP_PASSWRD	If bit[15]=0 or reg_2d[6:0](page1) = reg_1d[14:8](page0), the user can write the special register or store them to MTP. Otherwise, the user can't write and store them to the MTP special register. These include : 1Dh,2Fh,B0h-B7h,C7h-C9h,F1h
[7]	reg_1dh_b7	Enable bit to clear memory 07h after the CLEAR_LAST_FAULT command takes effect. 1'b0: disable 1'b1: enable
[6]	reg_1dh_b6	Enable bit to block start-up if a protection occurred during the last operating cycle. 1'b0: disable 1'b1: enable
[5]	ignore_no_vin_temp_fault	Ignore Vin or Temp fault
[4]	clr_eeprom_last_fault_en	Enable bit of the CLEAR_LAST_FAULT command (08h). 1'b0: disable 1'b1: enable
[3]	protect_fault_record_en	Enable bit to record protection information into MTP. 1'b0: disable 1'b1: enable when protection occurs. VR records protection information into MTP automatically
[2]	reg_1dh_b2	It is used to disable the function that doesn't store some special register to MTP when 1Dh[15]=1 and the password is wrong.
[1]	MFR_MTP_COPY_EN	Enable bit to read (restore) MTP while outputting power. 1'b0: disable 1'b1: enable
[0]	MFR_CRC_PROTECT_EN	Enable bit of CRC protection. 1'b0: disable 1'b1: enable

PSYS_WARN_FILT_CNT (1Eh)

The PSYS_WARN_FILT_CNT command on Page 0 is used to set the filter time of PSYS.

Command	PSYS_WARN_FILT_CNT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r/w	r/w	r/w
Function	X	X	X	X	X	PSYS_WARN_FILT_CNT		

Bits	Bit Name	Description
[7:3]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[2:0]	PSYS_WARN_FILT_CNT	Used to set the filter time of psys_warn2 and psys_warn1. If [2:0] = 0, use the ordinary 2-level FF synchronization, or the psys_warn2/1 positive edge delays ([2:1] + 1)*100ns, and a negative edge delays 100ns based on the 2FFs sync.

VOUT_COMMAND (21h)

The VOUT_COMMAND command on Page 0 sets the Rail A output voltage when the PMBus controls the output.

Command	VOUT_COMMAND															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	MFR_VREF_DIS_FSLOW								VOUT_COMMAND							

Bits	Bit Name	Description
[15:8]	MFR_VREF_DIS_FSLOW	It is used to set the VID to turn the DC loop on, regardless of how low frequency is detected. 5mV/LSB when MFR_STEP_SEL = 1 and 10mV/LSB when MFR_STEP_SEL = 0. Input the target voltage on the right box.
[7:0]	VOUT_COMMAND	Set the Rail A reference voltage (VID_DAC output voltage) in PMBus mode. In 5mV mode (E4h[5] = 1'b1): VREF = (VID + 49) / 2 * 5mV In 10mV mode (E4h[5] = 1'b0): VREF = (VID + 19) / 2 * 10mV

MFR_VOUT_TRIM (22h)

This MFR_VOUT_TRIM command on Page 0 is used to apply a fixed offset voltage to the output voltage command value for different power states. This command is most typically used by the end user to trim the output voltage at the time the PMBus device is assembled into the end user's system.

Command	MFR_VOUT_TRIM															
Format	Signed binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	VOUT_TRIM_3_CCM				VOUT_TRIM_2_CCM				VOUT_TRIM_1_CCM				VOUT_TRIM_1_DCM			

Bits	Bit Name	Description
[15:12]	VOUT_TRIM_3_CCM	Applies a fixed offset voltage to the output voltage at 3--phase CCM. 3.12mV/LSB. For example: 4'h1: 3.12mV; 4'h7: 21.84mV; 4'h8: -24.96mV; 4'hF: -3.12mV.
[11:8]	VOUT_TRIM_2_CCM	Applies a fixed offset voltage to the output voltage at 2-phase CCM. 3.12mV/LSB. For example: 4'h1: 3.12mV; 4'h7: 21.84mV; 4'h8: -24.96mV; 4'hF: -3.12mV.
[7:4]	VOUT_TRIM_1_CCM	Applies a fixed offset voltage to the output voltage at 1-phase CCM. 3.12mV/LSB. For example: 4'h1: 3.12mV; 4'h7: 21.84mV; 4'h8: -24.96mV; 4'hF: -3.12mV.
[3:0]	VOUT_TRIM_1_DCM	Applies a fixed offset voltage to the output voltage at 1-phase DCM. 3.12mV/LSB. For example: 4'h1: 3.12mV; 4'h7: 21.84mV; 4'h8: -24.96mV; 4'hF: -3.12mV.

VOUT_CAL_OFFSET (23h)

The VOUT_CAL_OFFSET command on Page 0 offers an offset VID to the Rail A target determined by VOUT_COMMAND, VOUT_MARGIN_HIGH, and VOUT_MARGIN_LOW. This command is the initial value of the SVID offset.

Command	VOUT_CAL_OFFSET															
Format	Signed binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	VOUT_CAL_OFFSET							

Bits	Bit Name	Description
[15:8]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[7:0]	VOUT_CAL_OFFSET	Sets the VID offset in PMBus mode. It is also the initial value for the SVID offset register (33h). 5mV/LSB or 10mV/LSB according to E4h[5], -80h ~ +7Fh.

MFR_VOUT_MAX (24h)

The MFR_VOUT_MAX command on Page 0 is the initial value of SVID VOUT_MAX (SVID 30h), which sets an upper limit on the VID target (not including the offset) of SVID to provide a safeguard against an accidental setting of the output voltage to a possibly destructive level. If an attempt is made to program the VID target higher than VOUT_MAX, the command is rejected. The PMBus VID target is not constrained by MFR_VOUT_MAX.

Command	MFR_VOUT_MAX															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	MFR_VOUT_MAX							

Bits	Bit Name	Description
[15:8]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[7:0]	MFR_VOUT_MAX	Sets an upper limit on the Rail A VID target (not including the offset) of SVID.

VOUT_MARGIN_HIGH (25h)

The VOUT_MARGIN_HIGH command is used to set the reference voltage (VID_DAC output voltage) at the command MARGIN HIGH state. Bit[7:0] is used to set target VID @ PVID =2'b10 when PVID enabled

Command	VOUT_MARGIN_HIGH															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	Vfb buf trim without idroop						VOUT_MARGIN_HIGH							

Bits	Bit Name	Description
[13:8]	Vfb buf trim without idroop	It is used for customer to record Vfb buf trim without idroop
[7:0]	VOUT_MARGIN_HIGH	Sets the reference voltage (VID_DAC output voltage) at the command MARGIN HIGH state. Target VID @ PVID =2'b10 when PVID enabled.

VOUT_MARGIN_LOW (26h)

The VOUT_MARGIN_LOW command is used to set the reference voltage (VID_DAC output voltage) at the command MARGIN LOW state. Bit[7:0] is used to set target VID @ PVID =2'b01 when PVID enabled. Bit[15:8] is used to record DC load line.

Command	VOUT_MARGIN_LOW															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	DC load line, 0.1mohm/LSB								VOUT_MARGIN_LOW							

Bits	Bit Name	Description
[15:8]	DC load line	It is used for customer to record DC load line, 0.1mohm/LSB
[7:0]	VOUT_MARGIN_LOW	Sets the reference voltage (VID_DAC output voltage) at the command MARGIN LOW state. Target VID @ PVID =2'b01 when PVID enabled.

MFR_IMMEDIATE_SET (2Bh)

The MFR_IMMEDIATE_SET command on Page 0 sets the Rail A slew rate, alert time, and bit[0] of STATUS1 when SVID sends VID within ±2LSB in 5mV mode.

Command	MFR_IMMEDIATE_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X										

Bits	Bit Name	Description
[15:10]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[9:8]	MFR_IMMED_REF_ STEP	Sets the VID (output reference) step when SVID sends VID within ±2LSB in 5mV mode of Rail A.
[7:5]	MFR_IMMED_ALT_ TIME	Sets the length of time of the ALTER slewing one step (FD[13:12] + 1) when SVID sends VID within ±2LSB in 5mV mode of Rail A. 100ns/LSB.
[4:2]	MFR_IMMED_REF_ TIME	Sets the length of time of the VID slewing one step ([9:8]) when the SVID sends VID within ±2LSB in 5mV mode of Rail A. 100ns/LSB.
[1]	MFR_IMMEDIATE_SVID _EN	Enable bit of Rail A to force the STATUS bit[0] to 1'b1. 1'b0: disable. STATUS bit[0] remains at 1'b0 until it settles normally. 1'b1: enable. Forces STATUS bit[0] to 1'b1 when the SetVID command is received within ±2LSB.
[0]	MFR_IMMEDIATE_REF _EN	Enable bit of Rail A using bit[9:2]. 1'b0: disable 1'b1: enable

MFR_ PLATFORM_TIME (2Eh)

MFR_PLATFORM_TIME is the period after vid_pres has added the rising_step and before vid_pres starts to subtract rising_step.

Command	MFR_PLATFORM_TIME															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	X	X	MFR_PLATFORM_TIME					

Bits	Bit Name	Description
[5:0]	MFR_PLATFORM_TIME	It is used to set the VREF hold time from VREF rise to target VID+more step*VID step, FAh[7:6] to VREF begins to decrease, when DVID rises. 1us/LSB

MFR_APSI_CTRL (30h)

This command is used to control the auto-phase shedding.

Command	MFR_APSI_CTRL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X			phs_drop_dly						APS_DELAY_TIME		

Bits	Bit Name	Description
[10]	MFR_ADP_PSI_BYPASS	Disable the SetPS command of the auto-phase shedding (not including IVID) enabled rail, high active
[9]	MFR_ADP_OC_EXIT_EN	Enable the 1PH CCM/DCM rail exit to full phase when per-phase oc appears, high active
[8:6]	phs_drop_dly	The delay time of the phase dropping action after detecting the total current is smaller than the phase shedding threshold; one whole sample period/LSB.
[5]	load_step_cmp_det	Hold the auto-phase shedding for a given time if n25=0 or p20=0
[4]	vid_psi_chg	Hold the auto-phase shedding for a given time after DVID/Decay
[3]	load_step_fsw_det	Hold the auto-phase shedding for a given time if frequency is high or low
[2:0]	APS_DELAY_TIME	Delay time to enable the auto-phase shedding after load transient

VIN_ON (35h)

The VIN_ON command on Page 0 is used to set the V_{IN} UVLO rising threshold.

Command	VIN_ON															
Format	Linear, two's complement binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	FIXED					X	X	X	VIN_ON							

Bits	Bit Name	Description
[15:11]	FIXED	Read only, fixed at -3 (dec) = 11101 (bin).
[10:8]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[7:0]	VIN_ON	Used to set the V_{IN} on level when V_{IN} is rising. 0.125V/LSB. For example, to set V_{IN} on at 5V, write 35h to E828h.

VIN_OFF (36h)

The VIN_OFF command on Page 0 is used to set the V_{IN} UVLO falling threshold.

Command	VIN_OFF															
Format	Linear, two's complement binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	FIXED					X	X	X	VIN_OFF							

Bits	Bit Name	Description
[15:11]	FIXED	Read only, fixed at -3 (dec) = 11101 (bin).
[10:8]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[7:0]	VIN_OFF	Sets the V_{IN} off level when V_{IN} is falling. 0.125V/LSB. For example, to set V_{IN} off at 4V, write 35h to E820h.

IOUT_CAL_GAIN (38h)

The IOUT_CAL_GAIN command on Page 0 is used to set the Rail A PMBus I_{OUT} report gain and can be calculated with Equation (10):

$$\text{IOUT\_CAL\_GAIN} = \frac{K_{CS} * R_{imon} * 2\text{^}15}{32*1000*k} \quad (10)$$

Where K_{CS} is the CS gain of the Intelli-Phase (in µA/A) (e.g.: MP86901C K_{CS} = 10µA/A), R_{imon} is the resistor connected to IMON (in kΩ), and *k* is a coefficient according to ICCMAX.

Command	IOUT_CAL_GAIN															
Format	Linear, two's complement binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	*k*					IOUT_CAL_GAIN										

Bits	Bit Name	Description
[15:11]	*k*	*k* = 1, IOUT_CAL_GAIN[15:11] = 5'b10001, when 20A ≤ ICCMAX, *k* = 2, IOUT_CAL_GAIN[15:11] = 5'b10010, when 10A ≤ ICCMAX < 20A *k* = 4, IOUT_CAL_GAIN[15:11] = 5'b10011, when 5A ≤ ICCMAX < 10A
[10:0]	IOUT_CAL_GAIN	Sets the Rail A PMBus I_{OUT} report gain.

IOUT_CAL_OFFSET (39h)

The IOUT_CAL_OFFSET command on Page 0 is used to set the Rail A PMBus I_{OUT} report offset.

Command	IOUT_CAL_OFFSET															
Format	Linear, two's complement binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w

Function	FIXED	X	X	X	X	X	IOUT_CAL_OFFSET

Bits	Bit Name	Description
[15:11]	FIXED	Fixed to -1 (dec) = 11111 (bin).
[10:6]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[5:0]	IOUT_CAL_OFFSET	Assigned value to set the PMBus I_{OUT} report offset. 0.5A/LSB. Default value is 0. Bit[5] is the sign bit. For example, write 1111100000111110b = F83Eh to 39h to add -1A offset on the PMBus I_{OUT} report.

MFR_IMON_SVID1 (3Ah)

The MFR_IMON_SVID1 command on Page 0 is used to set the gain and offset of the I_{OUT} report from the VR to the SVID processor for one phase condition. R_{imon} can be calculated with Equation (12):

$$R_{imon} = \frac{1.6*8*32}{11*Kcs*MFR\_ICC\_MAX} \quad (12)$$

Where K_{CS} is the Intelli-Phase current sense gain (in μA/A).

Command	MFR_IMON_SVID1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	MFR_IMON_SVID_OFFSET							MFR_IMON_SVID_GAIN							

Bits	Bit Name	Description
[15]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[14:8]	MFR_IMON_SVID_OFFSET	Sets the Rail A I_{OUT} SVID report offset, which is added to the value directly to the SVID I_{OUT} report register (15h). The default value is 0. Bit[14] is the sign bit. If setting the offset to -1, set [14:8] = 7'h7F If setting the offset to -2, set [14:8] = 7'h7E
[7:0]	MFR_IMON_SVID_GAIN	Sets the gain of the Rail A I_{OUT} SVID report. The default value is 128.

MFR_IMON_SVID2 (3Bh)

The MFR_IMON_SVID1 command on Page 0 is used to set the gain and offset of the I_{OUT} report from the VR to the SVID processor for a two phase condition. The calculation is the same as register 3Ah.

Command	MFR_IMON_SVID1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	MFR_IMON_SVID_OFFSET							MFR_IMON_SVID_GAIN							

Bits	Bit Name	Description
[15]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.

[14:8]	MFR_IMON_SVID_OFFSET	Sets the Rail A I_{OUT} SVID report offset, which is added to the value directly to the SVID I_{OUT} report register (15h). The default value is 0. Bit[14] is the sign bit. If setting the offset to -1, set [14:8] = 7'h7F If setting the offset to -2, set [14:8] = 7'h7E
[7:0]	MFR_IMON_SVID_GAIN	Sets the gain of the Rail A I_{OUT} SVID report. The default value is 128.

MFR_IMON_SVID3 (3Ch)

The MFR_IMON_SVID1 command on Page 0 is used to set the gain and offset of the I_{OUT} report from the VR to the SVID processor for a three phase condition. The calculation is the same as register 3Ah.

Command	MFR_IMON_SVID1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	MFR_IMON_SVID_OFFSET							MFR_IMON_SVID_GAIN							

Bits	Bit Name	Description
[15]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[14:8]	MFR_IMON_SVID_OFFSET	Sets the Rail A I_{OUT} SVID report offset, which is added to the value directly to the SVID I_{OUT} report register (15h). The default value is 0. Bit[14] is the sign bit. If setting the offset to -1, set [14:8] = 7'h7F If setting the offset to -2, set [14:8] = 7'h7E
[7:0]	MFR_IMON_SVID_GAIN	Sets the gain of the Rail A I_{OUT} SVID report. The default value is 128.

MFR_SYS_PASSWORD (50h)

50h is used to store the system password. This register can be stored to MTP.

Command	MFR_SYS_PASSWORD							
Format	Linear							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	MFR_SYS_PASSWORD							

MFR_INPUT_PASSWORD (51h)

51h is used as an input port; this register can't be stored to MTP, only when 51h[7:0] = 50h[7:0], the user can change other register values via the PMBus.

Command	MFR_ INPUT _PASSWORD							
Format	Linear							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	MFR_ INPUT _PASSWORD							

VIN_OV_FAULT_LIMIT (55h)

The VIN_OV_FAULT_LIMIT command on Page 0 is used to set the V_{IN} OVP threshold. Once the sensed input voltage exceeds the limit, the system takes action according to the V_{IN} OVP mode.

Command	VIN_OV_FAULT_LIMIT (0.125V/LSB)															
Format	Linear, two's complement binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	FIXED					X	X	X	VIN_OV_FAULT_LIMIT							

Bits	Bit Name	Description
[15:11]	FIXED	Fixed to -3 (dec) = 11101 (bin).
[10:8]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[7:0]	VIN_OV_FAULT_LIMIT	Sets the V_{IN} OVP level. 0.125V/LSB. For example, to set V_{IN} on at 24V, write 55h to 1110100011000000b = E8C0h.

VIN_UV_WARNING_LIMIT (58h)

The VIN_UV_WARNING_LIMIT command on Page 0 is used to set the V_{IN} UV warning threshold. Once the sensed input voltage is under the limit, the system indicates that V_{IN} is too low.

Command	VIN_UV_WARN_LIMIT (0.125V/LSB)															
Format	Linear, two's complement binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	FIXED					X	X	X	VIN_UV_WARNING_LIMIT							

Bits	Bit Name	Description
[15:11]	FIXED	Fixed to -3 (dec) = 11101 (bin).
[10:8]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[7:0]	VIN_UV_WARNING_ LIMIT	Sets the V_{IN} UV warning level. 0.125V/LSB. For example, to set V_{IN} on at 4.5V, write 55h to 1110100000100100b = E824h.

SVID_REG_80H_81H (72h)

The SVID_REG_80H_81H command on Page 0 stores part of the SVID command (not including GetReg 80h/81h/82h), which is stored in the SVID addresses of 80h and 81h.

Command	SVID_REG_80H_81H															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	X	X	X	X	SVID_REG_80H				SVID_REG_81H							

Bits	Bit Name	Description
[15:12]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[11:8]	SVID_REG_80H	Stores the address of the received SVID command.
[7:0]	SVID_REG_81H	Bit[7] is used to store the frame error flag. Bit[6] is used to store the parity error flag. Bit[5] is used to store the parity in the command. Bit[4:0] is used to store the 5-bit CMD in the SVID command.

SVID_REG_82H (73h)

The SVID_REG_82H command on Page 0 stores part of the SVID command (not including GetReg 80h/81h/82h), which is stored in the SVID addresses of 82h.

Command	SVID_REG_82H							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	SVID_REG_82H							

Bits	Bit Name	Description
[7:0]	SVID_REG_82H	Stores the received SVID command payload.

SLAVE_ADDR (74h)

The WRFAIL command on Page 0 is the latched WRFAIL signal from the MTP, which can only be reset by writing the MTP. The SLAVE_ADDR command on Page 0 is the final address of the PMBus.

Command	SLAVE_ADDR							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r	r
Function	WRFAIL	SLAVE_ADDR						

Bits	Bit Name	Description
[7]	WRFAIL	Flag that indicates the internal write operation is out of time or not when written to MTP.
[6:0]	SLAVE_ADDR	Final slave address of the PMBus.

MFR_CS_1_2 (75h)

The MFR_CS_1_2 command on Page 0 is for phase 1/2 current monitoring via the PMBus.

Command	MFR_CS_1_2															
Format	Linear															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	MFR_CS_1								MFR_CS_2							

Bits	Bit Name	Description
[15:8]	MFR_CS_1	Shows the monitored current connected to CS1. 0.5A/LSB.
[7:0]	MFR_CS_2	Shows the monitored current connected to CS2. 0.5A/LSB.

MFR_CS_3 (76h)

The MFR_CS_3 command on Page 0 is for phase 3 current monitoring via the PMBus.

Command	MFR_CS_3															
Format	Linear															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Reserved								MFR_CS_3							

Bits	Bit Name	Description
[7:0]	MFR_CS_3	Shows the monitored current connected to CS4. 0.5A/LSB.

MFR_CS_4_5 (77h)

The MFR_CS_4_5 command Page 0 is for phase 4/5 current monitoring via the PMBus.

Command	MFR_CS_4_5															
Format	Linear															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	MFR_CS_4								MFR_CS_5							

Bits	Bit Name	Description
[15:8]	MFR_CS_4	Shows the monitored current connected to CS4. 0.5A/LSB.
[7:0]	MFR_CS_5	Shows the monitored current connected to CS5. 0.5A/LSB.

STATUS_VOUT (7Ah)

The STATUS_VOUT command on Page 0 is a combined register of the output voltage fault flags for Rail A.

Command	STATUS_VOUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function						x	x	x
Default	0	x	x	0	0	x	x	x

Bits	Bit Name	Description
[7]		Ovp1 || ovp2, the final protect signal, “1” means vr will enter protection and shut down;
[6]		Ov1 || ov2, ov1=vout>vout_max+400mv, ov2=vout>vref+400mv; Ovp1 = ov1&& ovp1_en or latched ovp1; Ovp2 = ovp2_en && (ov2 lasts enough delay);
[5]		Uv_sync10MHz;
[4]		Uvp, uv_sync10MHz lasts enough delay and uvp is enabled;
[3]		Vout_max_warining, value written into PMBUS 21h25h/26h is larger than MFR_VOUT_MAX
[2:0]		Reserved.

STATUS_IOUT (7Bh)

The STATUS_IOUT command on Page 0 is a combined register of the output current fault flags for Rail A.

Command	STATUS_IOUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function		x		x	x	x	x	x
Default	0	x	0	x	x	x	x	x

Bits	Bit Name	Description
[7]		OCP flag. This bit is 1 if OCP is tripped.
[6]		Phase current limit flag && UVP
[5]		Phase current limit flag. This bit is 1 if the per-phase current limit is reached.
[4:0]		Reserved.

STATUS_INPUT (7Ch)

The STATUS_INPUT command on Page 0 is a combined register of the input voltage fault flags for the complete regulator.

Command	STATUS_INPUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function		x	x		x	x	x	x
Default	0	x	x	0	x	x	x	x

Bits	Bit Name	Description
[7]		V_{IN} OVP flag. This bit is 1 if VIN OVP is tripped.
[6]		Reserved.
[5]		V_{IN} UVLO flag. This bit is 1 if VIN UVLO is tripped.
[4:0]		Reserved.

STATUS_ TEMPERATURE (7Dh)

The STATUS_ TEMPERATURE command on Page 0 is a combined register of the temperature fault flags for the complete regulator.

Command	STATUS_INPUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function			x	x	x	x	x	x
Default	0	0	x	x	x	x	x	x

Bits	Bit Name	Description
[7]		OTP flag.
[6]		OTP flag || DrMos fault
[5:0]		Reserved.

STATUS_ CML (7Eh)

Command	STATUS_CML							
Format	Unsigned binary							
BIT	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	Invalid unsupported command	Invalid / unsupported data		Memory fault detected	x	x	Other fault	Memory busy

Bits	Bit Name	Description
[7]	CML_invalid_command	The I2C command isn't supported.
[6]	CML_invalid_data	I2C communication error when transmitting data.
[5]	PEC error	PEC error during PMBus communication
[4]	MTP fault	CRC_error || WRfail_flag.

[3:2]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[1]	CML_other_fault.	Start/stop bit during I2C communication.
[0]	MTP signature fault	Data in {000h, 001h} of MTP isn't 16'h1234.

READ_VIN (88h)

The READ_VIN command on Page 0 is used to monitor the input voltage.

Command	READ_VIN (0.125V/LSB)															
Format	Linear, two's complement binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	FIXED					X	X	X	READ_VIN							

Bits	Bit Name	Description
[15:11]	FIXED	Fixed to 11101 (bin) = -3 (dec).
[10:8]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[7:0]	READ_VIN	Monitors the input voltage. 0.125V/LSB.

READ_VOUT (8Bh)

The READ_VOUT command on Page 0 is used to return the sensed VDIFF voltage.

Command	READ_VOUT															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	X	X	X	X	X	X	ADC Sampled Vout value									

Bits	Bit Name	Description
[15:10]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[7:0]	READ_VOUT	Shows ADC sampled Vout value. 3.125mV/LSB

READ_IOUT (8Ch)

The READ_IOUT command on Page 0 reflects the PMBus monitor total average output current.

Command	READ_IOUT (0.25A/LSB)															
Format	Linear, two's complement binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	FIXED					READ_IOUT										

Bits	Bit Name	Description
[15:11]	FIXED	Fixed to 11110 (bin) = -2 (dec).
[10:0]	READ_IOUT	Shows the total average output current of Rail A monitored by the PMBus. 0.25A/LSB.

READ_TEMPERATURE (8Dh)

The READ_TEMPERATURE command on Page 0 is used to monitor the power stage temperature. The MP2949A monitors the power stage temperature by sensing the voltage on TEMP.

Command	READ_TEMPERATURE															
Format	Linear															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	X	X	X	X	X	X	X	X	READ_TEMPERATURE							

Bits	Bit Name	Description
[15:8]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[7:0]	READ_TEMPERATURE	Shows the sensed temperature from TEMP. 1°C/LSB.

READ_POUT (96h)

The READ_POUT command on Page 0 is used to monitor the Rail A output power.

Command	READ_POUT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	X	X	X	X	X	X	X	READ_POUT								

Bits	Bit Name	Description
[15:9]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[8:0]	READ_POUT	Shows the monitored output power of Rail A by the PMBus. 1W/LSB.

READ_PIN (97h)

The READ_PIN command on Page 0 is used to monitor the system total input power. It monitors the input power by sensing the voltage on PSYS.

Command	READ_PIN															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	X	X	X	X	X	X	X	READ_PIN								

Bits	Bit Name	Description
[15:9]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[8:0]	READ_PIN	Shows the monitored system total input power. 1W/LSB.

MFR_VIN_HYS (B8h)

The MFR_VIN_HYS command on Page 0 is used to set the V_{IN} sense hysteresis and V_{IN} sense offset. The V_{IN} sample result is equal to the ADC result plus the MFR_VIN_SENSE_OFFSET. MFR_VIN_HYS is the threshold for the input voltage sample result variation to trigger on-time calculation.

Command	MFR_VIN_HYS							
Format	HYS: unsigned binary; OFFSET: signed binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	MFR_VIN_HYS				MFR_VIN_SENSE_OFFSET			

Bits	Bit Name	Description
[7:4]	MFR_VIN_HYS	Sets the threshold for the V_{IN} sample result variation to trigger on-time calculation. The on time is refreshed when the V_{IN} sample variation is larger than MFR_VIN_HYS. 6.25mV/LSB.
[3:0]	MFR_VIN_SENSE_ OFFSET	Sets the V_{IN} sample offset. Bit[3] is the sign bit. 25mV/LSB.

MFR_1PHL_HYS (BBh)

The MFR_1PHL command on Page 0 is used to set the phase shedding level of the total current. MFR_1PHL is 1-phase CCM's level. 2- to 6-phase CCM's level is MFR_1PHL * phase number. 1-phase DCM's level is fixed at 5A.

Command	MFR_1PHL/MFR_PHASE_HYS															
format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x	MFR_1PHL					MFR_PHASE_HYS			

Bits	Bit Name	Description
[15:9]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[8:4]	MFR_1PHL	Sets the phase shedding level of 1-phase CCM. 1A/LSB.
[3:0]	MFR_PHASE_HYS	It is used to set the hysteresis value during phase adding. 1A/LSB.

For example, if MFR_1PHL (BBh[8:5]) = 11h (17A) and MFR_PHASE_HYS (BBh[3:0]) = 05h (5A), then the phase shedding threshold is 51A, and the phase adding threshold is 56A from 4-phase to 3-phase (see Figure 19).

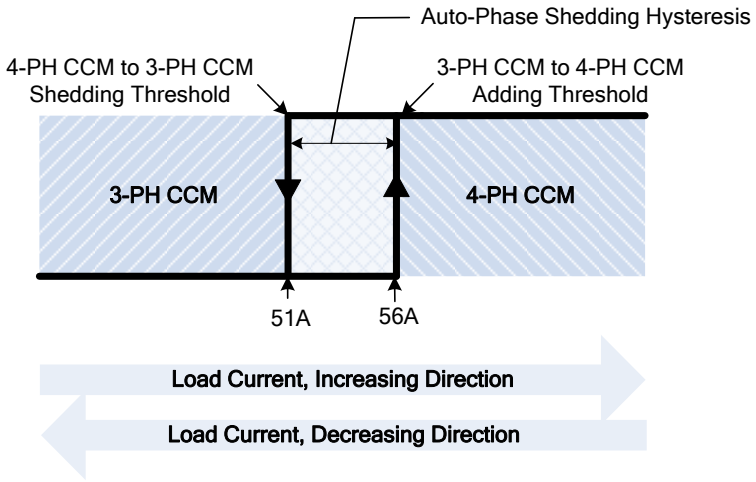


Figure 19: Phase Shedding and Adding Operation

PROTOCOL_ID_SVID_RDY_VR (BDh)

PROTOCOL_ID_R4[15:8] is used to set the lower four bits of PROTOCOL_ID of rail 4 and VR. PROTOCOL_ID_R4 = {4'h0, PROTOCOL_ID_VR_R4}; PROTOCOL_ID = {4'h0, PROTOCOL_ID_VR};

The ENABLE_TO_SVID_RDY_VR command on Page 0 is used to set the time length from EN's positive edge to the time VR is ready to receive the SVID command according to the Intel spec. Its format is the same as the SVID spec.

Command	PROTOCOL_ID_RD_RC_TA															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	PROTOCOL_ID RD				PROTOCOL_ID RC				ENABLE_TO_SVID_RDY_VR							

Bits	Bit Name	Description
[15:12]	PROTOCOL_ID_R4	Provides Rail D's lower four bits of PROTOCOL_ID, which show what version of the SVID protocol Rail 4 can support.
[11:8]	PROTOCOL_ID	Provides VR's lower four bits of PROTOCOL_ID, which show what version of the SVID protocol VR can support.
[7:0]	ENABLE_TO_SVID_ RDY_VR	Sets the length of time (in µs) from EN's positive edge to the time when VR is ready to receive the SVID command. The time length is equal to [3:0] / 16 * 2 ^ [7:4].

PS3_PS4_EXIT_DELAY (BEh)

The PS3_PS4_EXIT_DELAY command on Page 0 is used to set the length of time for the VR to exit PS3/4. The format is the same as the SVID spec.

Command	PS3_PS4_EXIT_DELAY															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	PS3_EXIT_LATENCY_VR								PS4_EXIT_LATENCY_VR							

Bits	Bit Name	Description
[15:8]	PS3_EXIT_LATENCY_VR	Sets the time length (in µs) for Rail A to exit PS3. The time length is equal to [11:8] / 16 * 2 ^ [15:12].
[7:0]	PS4_EXIT_LATENCY_VR	Sets the time length (in µs) that VR takes to exit PS4. The time length is equal to [3:0] / 16 * 2 ^ [7:4].

VENDOR_ID_PRODUCT_ID (BFh)

The VENDOR_ID_VR command on Page 0 provides the unique identification for the VR vendor. The vendor ID is assigned by Intel. This register is mandatory, and the VR must return the assigned vendor ID. The PRODUCT_ID_VR command on Page 0 provides the unique identification for the VR product. The VR vendor assigns this number.

Command	VENDOR_ID_PRODUCT_ID															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	VENDOR_ID_VR								PRODUCT_ID_VR							

Bits	Bit Name	Description
[15:8]	VENDOR_ID_VR	Provides the unique identification assigned by Intel for the VR vendor.
[7:0]	PRODUCT_ID_VR	Provides the unique identification assigned by the VR vendor for the VR product.

PRODUCT_DATA_CODE (C0h)

The PRODUCT_DATA_CODE command on Page 0 provides the unique four-digit hex code identifier for different customers or different projects for the VR controller. The vendor assigns this data.

Command	PRODUCT_DATA_CODE															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	PRODUCT_DATA_CODE															

Bits	Bit Name	Description
[15:0]	PRODUCT_DATA_CODE	Provides the unique four-digit hex code identifier assigned by the vendor for different customers and different projects.

LOT_CODE_VR (C1h)

The LOT_CODE_VR command on Page 0 identifies the code revision. PROTOCOL_ID_RB/A are the lower four bits of PROTOCOL_ID of Rail B and Rail A, respectively. These commands identify what version of the SVID protocol the controller supports.

Command	LOT_CODE_VR							
Format	Direct							
BIT	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	CODE_REV							

Bits	Bit Name	Description
[7:0]	CODE_REV	Provides the digital code revision assigned by the VR vendor.

DECAY_CFG_34H_06H (C2h)

The DECAY_CFG identifies the SVID VR capabilities and which of the optional telemetry registers are supported.

Command	MFR_STORE_MTP_STATE, DECAY_CFG, MFR_MULTI_VR_CONFIG, CAPABILITY_VR							
Format	Direct							
BIT	15	14	13	12	11	10	9	8
Access	r	r	r/w	r/w	r/w	r/w	r/w	r/w
Function	DVID_SETPS4_PS0_EN			MFR_STORE_MTPSTATE	DECAY_CFG		Lock VID/PS	VR_ready_ 0V

Command	MFR_STORE_MTP_STATE, DECAY_CFG, MFR_MULTI_VR_CONFIG, CAPABILITY_VR							
Format	Direct							
BIT	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Icc_max Format	Tamped Enable	Pin ADC Enable	Vin ADC Enable	Iin ADC Enable	Pout ADC Enable	Vout ADC Enable	Iout ADC Enable

Bits	Bit Name	Description
[15]		Enable bit to reject SetReg_VoutMax payload<Vid_setting command
[14]		Enable bit of ACK SETPS4 CMD when DVID.
[13]		Enable bit of ACK SETPS0 CMD when DVID.
[12]	STORE MTP FSM	Enable bit to store the mtp_wr state to the SVID registers for debugging. 1b'0: disable 1b'1: enable
[11:10]	DECAY_CFG	Configures the decay slew rate. 2b'00 or 2b'11: normal decay, Hi-Z PWM, or output discharge slew rate depending on output caps and output current. 2b'01: decay with fast slew rate, VREF discharge with fast slew rate when the decay command is received. 2b'10: decay with slow slew rate, VREF discharge with slow slew rate when the decay command is received.
[9:8]	MUTI_VR_CONFIG	Initial value of the lower two bits of SVID MUTI_VR_CONFIG (34h).

[7:0]	CAPABILITY_VR	Shows which of the telemetry registers are supported. A 1 in any bit indicates that an optional function is supported by the slave. Bit[7]: I_{OUT}/J_{OUT} format (15h) Bit[6]: temperature (17h) Bit[5]: input P (1Bh) Bit[4]: input V (1Ah) Bit[3]: input I (19h) Bit[2]: P_{OUT} (18h) Bit[1]: V_{OUT} (16h) Bit[0]: I_{OUT} (15h)

TOLERANCE_SR_FAST (C3h)

The MFR_VR_TOLERANCE command on Page 0 is used to set the output tolerance (binary format in mV). The SR_FAST_VR command on Page 0 is used to set the data register containing the Rail A fast slew rate capability of the slew rate the platform VR can sustain (binary format in mV/µs).

Command	TOLERANCE_SR_FAST															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	SR_FAST_VR								MFR_VR_TOLERANCE							

Bits	Bit Name	Description
[15:8]	SR_FAST_VR	Shows the fast slew rate that supports. 1mV/µs per LSB.
[7:0]	MFR_VR_TOLERANCE	Shows the output tolerance. 1mV/LSB.

MFR_VOUT_MAX_9BIT (C4h)

The MFR_VOUT_MAX_9BIT command on Page 0 is used to set the upper limit of VID + OFFSET. In PMBus mode, if VID + OFFSET is higher than this limit, the command is acknowledged, and the output is clamped at this limit. In SVID mode, if VID + OFFSET is higher than this limit, this command is rejected, and the output holds the voltage before the command.

Command	MFR_VOUT_MAX_9BIT															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	MFR_VOUT_MAX_9BIT								

Bits	Bit Name	Description
[15:9]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[8:0]	MFR_VOUT_MAX_9BIT	Sets the Rail A upper limit of VID + OFFSET.

IVID2_1_I_DEF (C5h)

The ivid2_i_def command on Page 0 is the default value of the maximum current (1A/bit) expected when VID is set as IVID2 - VID ≥ VID > IVID3 - VID. The ivid1_i_def command on Page 0 is the Rail A default value of the maximum current (1A/bit) expected when VID is set as IVID1 - VID ≥ VID > IVID2 - VID.

Command	IVID2_1_I_DEF															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	ivid2_i_def								ivid1_i_def							

Bits	Bit Name	Description
[15:8]	ivid2_i_def	Sets the Rail A default value of the maximum current expected when VID is set as IVID2 - VID ≥ VID > IVID3 - VID. 1A/LSB.
[7:0]	ivid1_i_def	Sets the Rail A default value of the maximum current expected when VID is set as IVID1 - VID ≥ VID > IVID2 - VID. 1A/LSB.

PIN_MAX_IVID3_I_DEF (C6h)

The MFR_PIN_MAX command on Page 0 is the input power sensor scaling for the SVID 1Bh (PSYS) register, programmed by the platform designer to the rating of the input power sensor (1W/LSB). The SVID PIN_MAX register (2Eh) is half of MFR_PIN_MAX. ivid3_i_def is the default value of the Rail A maximum current (1A/bit) expected when VID is set as IVID3 - VID ≥ VID.

Command	PIN_MAX_IVID3_I_DEF															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	MFR_PIN_MAX								Ivid3_i_def (1A/LSB)							

Bits	Bit Name	Description
[15:8]	MFR_PIN_MAX	Sets the system input power senor scaling. 1W/LSB.
[7:0]	ivid3_i_def	Sets the Rail A default value of the maximum current expected when VID is set as IVID3 - VID ≥ VID. 1A/LSB.

MFR_PHASE_NUM (CAh)

The MFR_PHASE_NUM (CAh) command on Page 0 is used to set the phase configuration of the VR. The PWM can be active only when both the rail and MFR_PHASE_NUM are enabled. The PWM distribution shown below is under CBh[15] = 1.

Command	MFR_PHASE_NUM							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r/w	r/w
Function	X	X	X	X	X	X	MFR_PHASE_NUM	

Bits	Bit Name	Description
[7:2]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[1:0]	MFR_PHASE_NUM	2b'01: one phase 2b'10: two phase; 2b'11: three phase

DC_CTRL_DYNAMIC_FLT (CCh)

The MFR_PANR_RAND_BW is used to select the range of random numbers. MFR_DYNAMIC_FLT register controls how to hold the current balance. MFR_DC_CTRL is used to control the DC calibration function.

Command	DC_CTRL, MFR_DYNAMIC_FLT															
format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	MFR_PANR_RAND_BW			MFR_DC_CTRL							MFR_DYNAMIC_FLT					

Bits	Bit Name	Description
[15:13]	MFR_PANR_RAND_BW	It is valid when PANR enabled (F5h[8] = 1) and random delay enabled (F5h[9] = 1). rand_a = F5h[15:10] rand_c = F8h[15: 0] rand_x0 = FAh[15:0] rand_delay = rem(rand_a*rand_x0 + rand_c, 65536) rem : strives for the remainder used_rand_delay is acturally used delay time for PANR. 3'b000:used_rand_delay={10'd0,rand_delay[5:0]}; 3'b001:used_rand_delay={8'd0,rand_delay[7:0]}; 3'b010:used_rand_delay={6'd0,rand_delay[9:0]}; 3'b011:used_rand_delay={4'd0,rand_delay[11:0]}; 3'b100:used_rand_delay={2'd0,rand_delay[13:0]}; 3'b101:used_rand_delay={4'd0,rand_delay[15:4]}; 3'b110:used_rand_delay={2'd0,rand_delay[15:2]}; 3'b111:used_rand_delay={rand_delay[15:0]};
[12:10]	MFR_DC_CAL_CNT	It is used to set the delay time to hold the DC loop. ADC sample period/LSB
[9]	MFR_DC_CAL_CTRL[3]	It used to hold the DC loop for a given time, CCh[12:10], when fs is low, CFh[8:0], and vid is low, 21h[15:8], under ps0/ps1 1'b0 - enable dc loop if [6]=1, enable dc loop if [6]=0; 1'b1 - hold dc loop if [6]=1, enable dc loop if [6]=0;
[8]	MFR_DC_CAL_CTRL[2]	Enable bit to hold the DC loop for a given time, CCh[12:10], when N20 or P25 is detected. When VFB>VREF+25mV or VFB<VREF-20mV, the VR holds the DC loop calibration for a given time. 1'b0: enable dc loop 1'b1: hold dc loop
[7]	MFR_DC_CAL_CTRL[1]	It is used to hold the DC loop for a given time, CCh[12:10], when VR dvid or change PS 1'b0:enable dc loop 1'b1:hold dc loop
[6]	MFR_DC_CAL_CTRL[0]	It is used to hold the DC loop for a given time, CCh[12:10], when fsw is high, CDh[7:0], or low, CFh[8:0] 1'b0: enable dc loop 1'b1:hold dc loop

[5]	MFR_DYNAMIC_FLT[5]	Enable bit to hold the current balance for a given time, CCH[2:0], when N20 or P25 is detected. When VFB>VREF+25mV or VFB<VREF-20mV, the VR holds the current balance for a given time. 1'b0: enable current balance 1'b1: hold current balance
[4]	MFR_DYNAMIC_FLT[4]	It is used to hold the DC loop for a given time, CCH[2:0], when VR DVID or a change to PS 1'b0: enable current balance 1'b1: hold current balance
[3]	MFR_DYNAMIC_FLT[3]	It is used to hold the DC loop for a given time, CCH[2:0], when fsw is high, CDh[7:0], or low, CFh[8:0] 1'b0: enable current balance 1'b1: hold current balance
[2:0]	MFR_DYNAMIC_FLT [2:0]	It is used to set the delay time to hold the current balance. One whole sample period/LSB. Input the delay time in the right box.

MFR_SW_HF_SET (CDh)

MFR_SW_HF_SET defines the frequency detection high level. If the pwm1 period is shorter than the frequency low level, then the switch frequency is high.

Command	MFR_SW_HF_SET															
format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x		MFR_SW_ HF_CYCLE							

Bits	Bit Name	Description
[8]	Enable bit	Enable bit of frequency detection high;
[7:0]	MFR_SW_ HF_CYCLE	Switch period(10ns/LSB),

MIN_ON_OFF_BLANK_TIME (CEh)

The MFR_MINON_TIME command on Page 0 is to control the minimum PWM on pulse for the three rails. The MFR_MINOFF_TIME command on Page 0 is to control the minimum interval time between the adjacent PWM on pulse of the same phase for the three rails. The MFR_BLANK_TIME command on Page 0 is used to control the minimum interval time between the adjacent phases in the same rail for the three rails.

Command	MINOFF_BLANK_TIME															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	MFR_MINON_ TIME			MFR_MINOFF_TIME							MFR_BLANK_TIME					

Bits	Bit Name	Description
[15:13]	MFR_MINON_TIME	Sets the minimum PWM width for three rails. 5ns/LSB.
[12:6]	MFR_MINOFF_TIME	Sets the minimum time between the last PWM falling edge and the next PWM rising edge of the same phase for three rails. 10ns/LSB.
[5:0]	MFR_BLANK_TIME	Sets the minimum time between the adjacent phase PWM of the same rail for the three rails. 10ns/LSB.

MFR_SW_LF_SET (CFh)

The MFR_SW_LF_CYCLE command on Page 0 defines the low PWM frequency threshold. If the length of time between the adjacent PWM of the same phase is longer than that set by MFR_SW _LF_CYCLE, then the switching frequency is low. PFM_LOW/HIGH_EN_Rx on Page 0 controls the low/high switch frequency function for the three rails.

Command	MFR_PFM_SET															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X		MFR_SW_LF_CYCLE								

Bits	Bit Name	Description
[15:10]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[9]	Enable bit	Enable bit of frequency detection low
[8:0]	MFR_LF_CYCLE	Sets the detected switch low frequency threshold. 10ns/LSB.

MFR_SLOPE_SR_3P (D6h)

The MFR_SLOPE_SR_3P command on Page 0 is used to set the slew rate of the slope ramp compensation during 3-phase operation.

Command	MFR_SLOPE_SR_3P															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	CAP_3P			CURRENT_SOURCE_3P					

Bits	Bit Name	Description
[15:9]	RESERVED	Unused. X indicates writes are ignored and always read as 0.
[8:6]	CAP_3P	It is used to set the cap number for slope voltage generation at 3-phase CCM operation. The capacitance is equal to (8 - DEC (CAP_2P)) x 3.7pF.
[5:0]	CURRENT_SOURCE_3P	It is used to set the current source for slope voltage generation at 3-phase CCM operation. 0.25μA/LSB (design value, subject to change after bench data collection).

MFR_SLOPE_SR_2P (D8h)

The MFR_SLOPE_SR_2P command on Page 0 is used to set the slew rate of the slope ramp compensation during 2-phase operation.

Command	MFR_SLOPE_SR_2P															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	CAP_2P			CURRENT_SOURCE_2P					

Bits	Bit Name	Description
[15:9]	RESERVED	Unused. X indicates writes are ignored and always read as 0.
[8:6]	CAP_2P	It is used to set the cap number for slope voltage generation at 2-phase CCM operation. The capacitance is equal to (8 - DEC (CAP_2P)) x 3.7pF.
[5:0]	CURRENT_SOURCE_2P	It is used to set the current source for slope voltage generation at 2-phase CCM operation. 0.25μA/LSB (design value, subject to change after bench data collection).

MFR_SLOPE_CNT_2P (D9h)

The MFR_SLOPE_CNT_2P command on Page 0 is used to set the saturation value of the slope ramp compensation during 2-phase operation.

Command	MFR_SLOPE_CNT_2P															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	MFR_SLOPE_CNT_2P									

Bits	Bit Name	Description
[15:10]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[9:0]	MFR_SLOPE_CNT_2P	Sets the slope compensation saturation time for 2-phase CCM. 10ns/LSB. Generally, this time is set at 1.3 x (Ts/2-Tblank) time, where Ts is the switching period time, and Tblank is the PWM blanking time.

Figure 20 shows a slope voltage curve at 2-phase CCM.

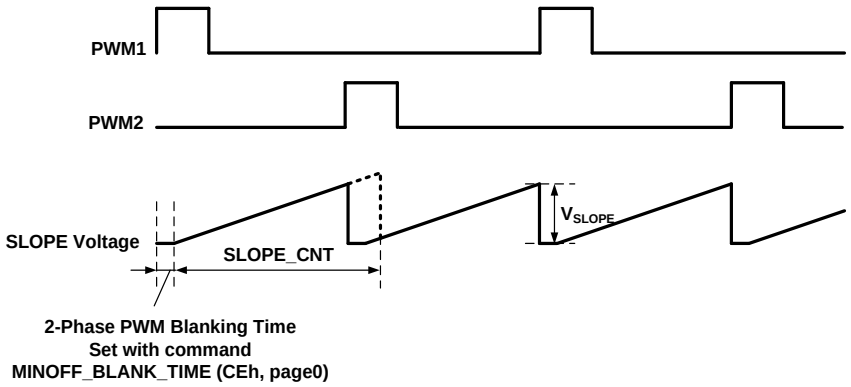


Figure 20: Slope Voltage at 2-Phase CCM Power State

MFR_SLOPE_SR_1P (DAh)

The MFR_SLOPE_SR_1P command on Page 0 is used to set the slew rate of the slope ramp compensation during 1-phase operation.

Command	MFR_SLOPE_SR_1P															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	CAP_1P			CURRENT_SOURCE_1P					

Bits	Bit Name	Description
[15:9]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[8:6]	CAP_1P	Sets the cap number for slope voltage generation at 1-phase CCM operation. The capacitance is equal to (8 - DEC (CAP_1P)) x 3.7pF.
[5:0]	CURRENT_SOURCE_1P	Sets the current source for slope voltage generation at 1-phase CCM operation. 0.25μA/LSB (design value, subject to change after bench data collection).

MFR_SLOPE_CNT_1P (DBh)

The MFR_SLOPE_CNT_1P command on Page 0 is used to set the saturation value of the slope ramp compensation during 1-phase operation.

Command	MFR_SLOPE_CNT_1P															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	MFR_SLOPE_CNT_1P									

Bits	Bit Name	Description
[15:10]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[9:0]	MFR_SLOPE_CNT_1P	Sets the slope compensation saturation time for 1-phase CCM. 10ns/LSB. Generally, this time is set at 1.3 x (Ts - Tblank) time, where Ts the switching period time, and Tblank is the PWM blanking time.

MFR_SLOPE_SR_DCM (DCh)

The MFR_SLOPE_SR_ DCM command on Page 0 is used to set the slew rate of the slope ramp compensation during 1-phase DCM operation.

Command	MFR_SLOPE_SR_ DCM															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	CAP_DCM			CURRENT_SOURCE_DCM					

Bits	Bit Name	Description
[15:9]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[8:6]	CAP_DCM	Sets the cap number for slope voltage generation at 1-phase DCM operation. The capacitance is equal to (8 - DEC (CAP_DCM)) x 3.7pF.
[5:0]	CURRENT_SOURCE_DCM	Sets the current source for slope voltage generation at 1-phase DCM operation. 0.25μA/LSB (design value, subject to change after bench data collection).

MFR_SLOPE_CNT_ DCM (DDh)

The MFR_SLOPE_CNT_DCM command on Page 0 is used to set the saturation value of the slope compensation during 1-phase DCM operation.

Command	MFR_SLOPE_CNT_ DCM															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function					X	X	X	MFR_SLOPE_CNT_ DCM								

Bits	Bit Name	Description
[15]	MFR_SLOPE_LEAKAGE	Enable bit to turn off the switch in the slope charging loop when the slope is saturated in ps2 state. 1'b0 : disable 1'b1 : enable
[14:12]	SLOPE_DISCHARGE_TIME	It is used to set the slope discharge time. Slope discharge time =([14:12]+1)*10 10ns/LSB
[11:9]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[8:0]	MFR_SLOPE_CNT_ DCM	Sets the slope compensation saturation time for 1-phase DCM. 10ns/LSB. Generally, this time is set at 2 x (Ts - Tblank) time, where Ts is the switching period time, and Tblank is the PWM blanking time.

MFR_TRIM_2_1_DCM (DEh)

The MFR_TRIM_2_1_DCM command on Page 0 is used to trim the output voltage during 1-phase ~ 2-phase CCM and 1-phase DCM.

Command	MFR_TRIM_2_1_DCM															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	MFR_TRIM_2					MFR_TRIM_1					MFR_TRIM_DCM				

Bits	Bit Name	Description
[15]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[14:10]	MFR_TRIM_2	Sets the Rail A V_{OUT} trim for 2-phase CCM operation. 2.73mV/LSB.
[9:5]	MFR_TRIM_1	Sets the Rail A V_{OUT} trim for 1-phase CCM operation. 2.73mV/LSB.
[4:0]	MFR_TRIM_DCM	Sets the Rail A V_{OUT} trim for 1-phase DCM operation. 2.73mV/LSB.

MFR_TRIM_2 (DFh)

The MFR_TRIM_2 command on Page 0 is used to trim the output voltage during 3 phase CCM.

Command	MFR_TRIM_2_1_DCM															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	X	X	X	X	MFR_TRIM_3				

Bits	Bit Name	Description
[15:5]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[4:0]	MFR_TRIM_3	Sets the V_{OUT} trim for 3-phase operation. 2.73mV/LSB.

SHUTLEVEL_ADDRPMBUS (E1h)

SHUTLEVEL_ADDRPMBUS is the shut level set by MFR_SHUTDOWN_LEVEL, where VREF is lower than the moment V_{OUT} (VREF) is slewing downward. The VR stops switching and starts to decay for the three rails. The MFR_ADDR_PMBUS command on Page 0 is used to configure the PMBus address of the device.

Command	SHUTLEVEL_ADDRPMBUS															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	MFR_SHUTDOWN_LEVEL						X		ADDRPMBUS						

Bits	Bit Name	Description
[15]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[14:9]	MFR_SHUTDOWN_ LEVEL	5mV/LSB (5mV mode), 10mV/LSB (10mV mode). For example, to set the shutdown level at 0.16V, set this bit as 6'h20h (5mV/LSB) or 6'h10 (10mV/LSB).
[8]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[7]	4_LOW_ADDR_REG	Selection bit to choose the four lower bits of the PMBus address set by the register or pin. 1'b0: set PMBus address bit[3] ~ [0] from the pin 1'b1: set PMBus address bit[3] ~ [0] from the register
[6:0]	MFR_ADDR_PMBUS	Sets the four lower bits of the PMBus address.

MFR_CB_SATU_PI (E2h)

The TUNE_NSATU_PSATU command on Page 0 is used to define the negative and positive saturation level of the current balance calculation. The MFR_CB_PI command is used to set the proportion integrate (PI) value for the current balance.

Command	MFR_CB_SATU_PI															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	TUNE_NSATU				TUNE_PSATU				MFR_CB_PI							

Bits	Bit Name	Description
[15:12]	TUNE_NSATU	Defines the negative saturation level of the current balance calculation. 10ns/LSB, range from -80ns ~ 0ns. bit[15] is the sign bit. For example, to set the negative saturation level as -50ns, set E2h [15:12] = 4'hB.
[11:8]	TUNE_PSATU	Defines the positive saturation level of the current balance calculation. 10ns/LSB, range from 0ns ~ 70ns. For example, to set the negative saturation level as 50ns, set E2h [11:8] = 4'h5.
[7:0]	MFR_CB_PI	Sets the Rail A PI parameter value for the current balance.

VTRIM_VCAL_PI (E3h)

The MFR_VCAL_PI command is used to set the Rail PI value for DC calibration.

command	MFR_VCAL_PI							
format	Direct							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	MFR_VCAL_PI					

Bits	Bit Name	Description
[7:6]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[5:0]	MFR_VCAL_PI	Sets the PI parameter for DC loop calibration.

MFR_VR_CONFIG (E4h)

The MFR_VR_CONFIG command on Page 0 is used to enable the function of VR, such as DC loop calibration, auto-phase shedding, etc.

Command	MFR_VR_CONFIG															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function																

Bits	Bit Name	Description
[15]	PVID_MODE_SEL	Enable bit of PVID mode. 1b'0: disable 1b'1: enable
[14]	MFR_PMBUS_SR_SEL	Selection bit of Rail A for the VID slew rate when the PMBus controls V_{OUT}. 1b'0: V_{OUT} changes with fast slew rate when the PMBus controls V_{OUT}. 1b'1: V_{OUT} changes with slow slew rate when the PMBus controls V_{OUT}.
[13]	MFR_WAIT_SETTLE_ SEL	Selection bit of the three rails for the time VRRDY moves slowly from high when DVID rises from 0V (not include VBOOT), if SVID 34h is written to 00. 1b'0: VRRDY turns high when DVID rises from 0V (not include VBOOT) and starts. 1b'1: VRRDY turns high after DVID rises from 0V (not include VBOOT) and finishes.
[12]	IMVP9_SEL	Selection bit for the three rails to choose IMVP8 or IMVP9. Only affects the VRRDY assignment. 1b'0: IMVP8 1b'1: IMVP9
[11]	DC LOOP_DCM_EN	Enable bit for Rail A DC's calibration during PS2. Only active when DC_LOOP_EN is enabled. 1b'0: disable 1b'1: enable when bit[10] = 1
[10]	DC_LOOP_EN	Enable bit for Rail A DC calibration. 1b'0: disable 1b'1: enable DC calibration in CCM. Must enable bit[11] for PS2 DC calibration.
[9]	PMBUS_PS_EN	Enable bit for PMBus to control the power state of Rail A in PMBus mode. 1'b0: disable 1'b1: enable
[8:7]	PMBUS_PS	Sets the Rail A power state when the PMBus controls the power state. 2'b00: PS0 2'b01: PS1 2'b10: PS2 2'b11: PS3
[6]	TON_REDUCTION_ DCM_EN	Enable bit of Rail A to reduce the PS2 on time to 75% of that in PS0. 1'b0: disable 1'b1: enable
[5]	VID_STEP	Selection bit of the VID step for Rail A. 1'b1: 5mV/LSB 1'b0: 10mV/LSB
[4]	IPHASE_BALNCE_EN	Enable bit of the Rail A current balance. 1'b0: disable 1'b1: enable
[3]	PVID_PS4_ENABLE	Enable bit of whether VR enter PS4 @ PVID = 2'b00 when PVID mode enabled 1'b0: disable 1'b1: enable
[2]	APS_EN	Enable bit of the Rail A auto-phase shedding function. 1'b0: disable 1'b1: enable
[1]	IVID_EN	Enable bit of the Rail A IVID function. 1'b0: disable 1'b1: enable
[0]	PMBUS_MODE_SEL	Selection bit of Rail A controlled by the SVID PMBus or SVID when [15]=0. [15] has a higher priority. 1'b0: SVID 1'b1: PMBus

MFR_FS_VBOOT (E5h)

The MFR_FS command on Page 0 is used to set the frequency for all the rails. The MFR_VBOOT command on Page 0 is used to set the boot-up voltage for Rail A.

Command	MFR_FS_VBOOT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	MFR_FS (50kHz/LSB)							MFR_VBOOT							

Bits	Bit Name	Description
[15]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[14:8]	MFR_FS	Sets the operation frequency for all rails. 50kHz/LSB.
[7:0]	MFR_VBOOT	Sets the boot-up voltage for Rail A (VID format). For example, to set the output voltage at 0.9V, set E5h[7:0] = 8'h83 (5mV VID mode) or 8'h47 (10mV VID mode).

MFR_ADDR_SVID (E6h)

The MFR_ADDR_SVID command on Page 0 is used to set the SVID address for the controller.

Command	MFR_ADDR_SVID															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x	x	x	x	ALLCALL_CTRL		SVID ADDR			

Bits	Bit Name	Description
[15:6]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[5:4]	ALLCALL_CTRL	Sets the All Call address. 2'b 00: no All Call address 2'b 01: set 0Eh to be All Call address 2'b 10: set 0Fh to be All Call address 2'b 11: set both 0Eh and 0Fh to be All Call addresses
[3:0]	RAIL_SVID_ADDRESS	Sets the SVID address of Rail . 4'b 0000: set Rail address to 00h 4'b 0001: set Rail address to 01h 4'b 0010: set Rail address to 10h 4'b 0011: set Rail address to 11h

TEMPERATURE_GAIN_OFFSET (E8h)

The TEMPERATURE_GAIN_OFFSET command on Page 0 is used to set the gain and offset of the temperature sense.

Command	TEMPERATURE_GAIN_OFFSET															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	MFR_TEMP_GAIN								MFR_TEMP_OFFSET							

Bits	Bit Name	Description
[15:8]	MFR_TEMP_GAIN	Sets the temperature (T(°C)) and temperature sense voltage (V_{TEMP_SENSE}) relationship. T(°C) = A x V_{TEMP_SENSE} + B, where A is MFR_TEMP_GAIN/0.8, and B is MFR_TEMP_OFFSET.
[7:0]	MFR_TEMP_OFFSET	The offset is used to set the offset of the temperature sense. Signed value, 1°C/LSB. For example, to set MFR_TEMP_OFFSET as -2°C, set MFR_TEMP_OFFSET to 8'hFE.

MFR_CUR_GAIN (E9h)

The MFR_CUR_GAIN command on Page 0 is used to set the per-phase current sense gain of Rail A. Calculate I_{READ} with Equation (11):

$$I\_READ = \frac{I_{CS} * K_{CS} * R_{CS} + 1.23}{32 * MFR\_CUR\_GAIN} * 1023 - MFR\_CUR\_OFFSET \quad (11)$$

Where K_{CS} is in μA/A, and R_{CS} is in Ω.

Command	MFR_CUR_GAIN															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	MFR_CUR_GAIN									

Bits	Bit Name	Description
[15:10]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[9:0]	MFR_CUR_GAIN	Sets the gain of the per-phase current sense of Rail A. MFR_CUR_GAIN is used to calculate the current from per-phase current sample results.

MFR_CUR_OFFSET (EAh)

The MFR_CUR_OFFSET command on Page 0 is used to set the offset for the Rail 1.23V bias voltage of the per-phase current sense.

Command	MFR_CUR_OFFSET							
Format	signed binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	MFR_CUR_OFFSET							

Bits	Bit Name	Description
[7:0]	MFR_CUR_OFFSET	Sets the offset for the 1.23V bias voltage of the per-phase current sense.

MFR_CS_OFFSET1_2 (EBh)

The MFR_CS_OFFSET1_2 command on Page 0 is used to set the phase 1/2 current bias for thermal offset.

Command	MFR_CS_OFFSET1_2															
Format	signed binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	MFR_CS_OFFSET1								MFR_CS_OFFSET2							

Bits	Bit Name	Description
[15:8]	MFR_CS_OFFSET1	Sets the CS1 offset in the current balance loop. 3.125mV/LSB.
[7:0]	MFR_CS_OFFSET2	Sets the CS2 offset in the current balance loop. 3.125mV/LSB.

MFR_CS_OFFSET3 (ECh)

The MFR_CS_OFFSET3 command on Page 0 is used to set the phase 3 current bias for thermal offset.

Command	MFR_CS_OFFSET3															
Format	signed binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	MFR_CS_OFFSET3								Reserved							

Bits	Bit Name	Description
[15:8]	MFR_CS_OFFSET3	Sets the CS3 offset in the current balance loop. 3.125mV/LSB.

MFR_OCP_SET_LEVEL (EEh)

The MFR_OCP_SET_LEVEL command on Page 0 is used to set the Rail A OC limit level and the OCP delay time for the three rails.

Command	MFR_OCP_SET_DELAYTIME, MFR_OCP_SET_LEVEL															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	MFR_OCP_SET_DELAYTIME						X	MFR_OCP_SET_LEVEL						

Bits	Bit Name	Description
[15:14]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[13:8]	MFR_OCP_SET_DELAY TIME	Sets the average OCP delay time for the three rails. 20µs/LSB.
[7]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[6:0]	MFR_OCP_SET_LEVEL	Sets the Rail A over-current limit value (1A/LSB). The total OCP limit is set at [6:0]*phase number, which is compared with READ_IOUT(8Ch)/4.

MFR_ICC_MAX (EFh)

The MFR_ICC_MAX command on Page 0 is used to set the ICCMAX of Rail.

command	MFR_ICC_MAX							
format	Direct							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	1A/LSB							

Bits	Bit Name	Description
[7:0]	MFR_ICC_MAX	Sets the ICCMAX for Rail A. 1A/LSB. 00h indicates that this value is not programmed and the platform will not boot.

MFR_VOUT_CMPS_MAX (F0h)

The MFR_VOUT_CMPS_MAX command on Page 0 is the maximum level of V_{OUT} compensation of all rails.

command	MFR_VOUT_CMPS_MAX															
format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	MFR_VOUT_CMPS_MAX															

Bits	Bit Name	Description
[15:8]	MFR_VOUT_CMPS_ MAX	Sets all rails' max level of VOUT compensation. 0.34mV/LSB.
[7:6]	5mV_VO_COMP_SETP	It is used to set the VOUT compensation COMP adding step by counting the PWM number when SetVID_Fast/Slow, it updates every ([7:6]+1) PWM1.
[5]	5mV_VO_COMP_SETP _EN	Enable bit to count PWM1 when adding VOUT compensation, effective when [4]=1. 1b'0 : Disable 1b'1 : Enable
[4]	5mV_VO_COMP_EN	Enable bit to add 5mV VOUT compensation under 5mV mode for VR. 1b'0 : Disable 1b'1 : Enable
[3:1]	VO_COMP_SETP_EXIT _DECAY	It is used to set the VOUT compensation COMP adding step by counting the PWM number after decay, it update every [3: 1] PWM1.
[0]	VO_COMP_SETP_EXIT _DECAY_EN	Enable for VR to add VOUT compensation COMP by counting the PWM after DECAY finishes, or VOUT compensation will add once after DECAY finishes. 1b'0 : VOUT compensation COMP add once. 1b'1 : VOUT compensation COMP add by counting PWM.

MFR_PROTECT_CFG (F1h)

This command is used to set the OTP/ Vin OVP/ UVP/OVP1/OVP2/OCP mode.

Command	MFR_PROTECT_CFG															
format	Linear, Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x								UVP		OVP2		OVP1		OCP	

Bits	Bit Name	Description
[15]	RESERVED	Reserved. Fixed to 0.
[14]	ss_oc_en	Enable bit of phase OC turn-off switch at soft start. 1’b0:disable 1’b1: enable
[13]	temp_fault_en	Temp fault enable bit 1’b0:disable 1’b1: enable
[12]	ot_flag_en	Over-temperature protection enable bit. 1’b0:disable 1’b1: enable
[11]	vin_flag_en	Vin under-voltage and over-voltage protection enable bit. 1’b0:disable 1’b1: enable
[10]	otp_latch	Over-temperature protection mode selection. 1’b0:hiccup 1’b1:latch
[9]	vin_uvlo_latch	Vin under-voltage protection mode selection. 1’b0:hiccup 1’b1:latch
[8]	vin_ovp_latch	Vin over voltage protection mode selection. 1’b0:hiccup 1’b1:latch
[7:6]	MFR_UVP_SET_MODE	Sets the Rail A UVP mode. 2’b00: no action 2’b01: latch 2’b01: hiccup 2’b11: retry six times and then latch off
[5:4]	MFR_OVP2_SET_MODE	00: no action 01: latch 10: hiccup 11: retry 6 times and then latch off
[3:2]	MFR_OVP1_SET_MODE	bit[2] : ovp1 mode: ‘1’ latch, ‘0’ hiccup bit[3] : ovp1 enable :
[1:0]	MFR_OCP_SET_MODE	Sets the Rail A OCP mode. 2’b00: no action 2’b01: latch 2’b01: hiccup 2’b11: retry six times and then latch off

MFR_OTP_SET (F2h)

The MFR_OTP_SET command on Page 0 is used to set the OTP level for the VR.

Command	MFR_OTP_SET															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	MFR_OTP_LIMIT								MFR_OTP_HYS						

Bits	Bit Name	Description
[15]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[14:7]	MFR_OTP_LIMIT	Sets the OTP limit. When the junction temperature monitored on TEMP is higher than OTP_LIMIT, the VR shuts off and disables the output. 1°C/LSB.
[6:0]	MFR_OTP_HYS	Sets the temperature hysteresis of OTP if OTP is in no-latch mode. When the junction temperature monitored on TEMP is lower than MFR_OTP_LIMIT - MFR_OTP_HYS, the PWM initiates a soft start as it would during a normal power-on. 1°C/LSB.

MFR_TEMP_MAX (F3h)

The MFR_TEMP_MAX command on Page 0 is used to set the max temperature the platform supports and the level VRHOT# asserts.

Command	MFR_TEMP_MAX															
format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x			MFR_TEMP_MAX							

Bits	Bit Name	Description
[9]	psys_ast_hot_en	It is used to decide whether psys over critical level asserts vr_hot or not . 1'b0 : not assert 1'b1: assert
[8]	vsysmode	It is used to select vsys mode or psys mode for VR . 1'b0 : psys mde 1'b1 : vsys mode
[7:0]	MFR_TEMP_MAX	Sets the over-temperature warning limit setting. VRHOT# asserts when the sensed temperature reaches this threshold. 1°C/LSB.

MFR_AUDIBLE_REDUCE (F5h)

MFR_AUDIBLE_REDUCE configures the audible noise reduction function parameters.

command	MFR_AUDIBLE_REDUCE															
format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	rand_a															

Bits	Bit Name	Description
[15:10]	rand_a	rand_a. a parameter for random number algorithm.

[9:8]	AUDIBLE_REDUCE_EN	It is used to select the mode of audible noise reduction 2'bX0 : Disable the function of PANR 2'b01 : Enable PANR and use fixed delay time for delayed DVID down 2'b11 : Enable PANR and use random delay time for delayed DVID down, random delay time range can be set by CCh[15:13].
[7:0]	vid_target_delta	VID Delta threshold to delay dynamic VID, if VID_present - VID_target>MFR_AUDIBLE_REDUCE[7:0], delay DVID for a duration

OCP_OVP_DA_LIMIT (F6h)

Ocp_da_limit sets the ocp max limit. Ovp_da_limit sets the ovp max limit. It outputs to DAC directly. The OCP DAC is 10mV/LSB. The OVP DAC is 40mV/LSB. The minimum value of ocp/ovp DACs is 1.28V.

command	OCP_OVP_DA_LIMIT															
format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	ocp_da_limit								x	ovp_da_limit						

Bits	Bit Name	Description
[15:8]	OCP_DA_LIMIT	Sets the valley limitation level of the current sense (CS) of a single phase for Rail A. 10mV/LSB. VR will not latch when it reaches the limit and usually ends in UVP.
[7]	RESERVED	Reserved. Fixed to 1.
[6:0]	OVP_DA_LIMIT	It is used to set the threshold of the VR output voltage limit. Once vout is over this level, VR will be protected. 40mV/LSB

MFR_OVP_UVP_SET (F7h)

The MFR_OVP_UVP_SET command on Page 0 is used to set the delay time of OVP2 and UVP for all the rails.

Command	MFR_OVP_UVP_SET															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	OVP2 DELAYTIME (200ns/LSB)						UVP DELAYTIME (20µs/LSB)					

Bits	Bit Name	Description
[15:12]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[11:6]	OVP2 DELAYTIME	Sets the OVP2 delay time for the three rails. 200ns/LSB.
[5:0]	UVP DELAYTIME	Sets the UVP delay time for the three rails. 20µs/LSB.

MFR_VID_DOWN_DELAY (F8h)

MFR_VID_DOWN_DELAY(F8h) configures the delay time of delayed downward DVID.

Command	MFR_VID_DOWN_DELAY															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	1us/LSB															

MFR_FILTER_SET (F9h)

The MFR_FILTER_SET on Page 0 is used to set the parameters of the VID filter and slow the slew rate for Rail A.

Command	MFR_FILTER_SET															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	MFR_IVID_VALID_WAITTIME (100ns/LSB)												SLOW_SR_SEL			

1B1B Bits	Bit Name	Description
[15:8]	MFR_IVID_VALID_ WAITTIME	Sets the IVID phase shedding delay time. 100ns/LSB.
[7]	MFR_DAC_CMP_EN	Enable bit of DAC_CMP_FILTER from the analog of Rail A, which is used to filter the VID_DAC output until the filtered VID_DAC output level equals the VID_DAC output when SetVID_down is interrupted by SetVID_up. 1’b0: disable 1’b1: enable
[6]	MFR_VID_FILTER_EN	Enable bit of the VID filter for Rail A, which is the VID_DAC output filter for SetVID_fast/slow_down transitions. There is no VID filter when VID is up or VID is down by decay. Set PS4 CMD. 1’b0: disable 1’b1: enable
[5:4]	MFR_VID_FILTER	Sets Rail A VID_DAC output filter. 2’b00: 1µs added filter at VID ramping down or steady V_{OUT} 2’b01: 3µs added filter at VID ramping down or steady V_{OUT} 2’b10: 5µs added filter at VID ramping down or steady V_{OUT} 2’b11: 7µs added filter at VID ramping down or steady V_{OUT}
[3:0]	SLOW_SR_SEL	Selection bit of the slew rate when Rail A receives the SetVID_Slow command. 4’b1xxx: 1/16 of the fast slew rate 4’b01xx: 1/8 of the fast slew rate 4’b001x: 1/4 of the fast slew rate 4’b0001: 1/2 of the fast slew rate

MFR_TRANS_FAST (FAh)

The MFR_TRANS_FAST command on Page 0 is used to set the Rail reference fast slew rate when Rail A receives the SetVID_Fast_Up command. The REF down slew rate is set by the FDh register. Figure 21 shows the definition of the slew rate of VREF up and down (5mV/LSB). VID_STEP: FAh[7:6], VID_SR_CNT: FAh[5:0], ALERT_STEP_NUM: FDh[13:12], ALERT_SR_CNT: FDh[5:0].

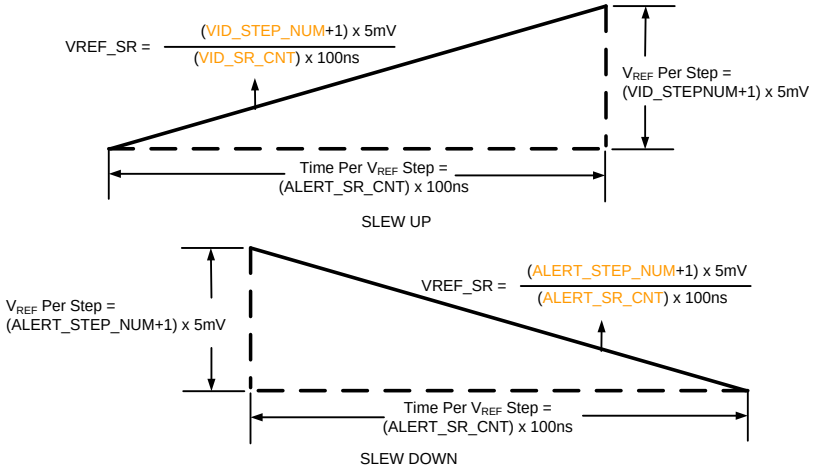


Figure 21: Slew Rate Definition

Normal slew rate = ([7:6] + 1) * 5mV / ([5:0] * 100ns) * 10 ^ 3 (mV/µs), in 5mV mode.

Normal slew rate = ([7:6] + 1) * 10mV / ([5:0] * 100ns) * 10 ^ 3 (mV/µs), in 10mV mode.

Command	MFR_TRANS_FAST															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function			X	X												

Bits	Bit Name	Description
[15:14]	VID_STEP_DECAY	Sets the Rail A reference minus the step during decay. The step = 2 * bit[15:14] + 1.
[13:12]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[11]	VID_SUBTRACT	Selection bit of the Rail A slew rate when the reference removes the additional rising step. 1'b0: 1/4 of the fast slew rate 1'b1: 1/8 of the fast slew rate
[10:8]	MORE_RISING_STEP	Sets the number of additional rising steps of Rail A after the VID reaches the target to increase the output voltage. Rising step = [10:8] * 2 + 1 in 5mV mode Rising step = [10:8] in 10mV mode
[7:6]	VID_STEP_NUM	Sets the Rail A reference step at one VID_SR_CNT period when slewing up. The step is equal to DEC([7:6]) + 1.
[5:0]	VID_SR_CNT	Sets the time length of Rail A that VREF changes once. 100ns/LSB.

MFR_EN_SEQUENCE_CFG (FBh)

The MFR_EN_DLY command on Page 0 is used to set the Rail EN delay time. MFR_EN_FILTER_TIME is used to set the EN filter time for the three rails.

Command	MFR_EN_DLY															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X		MFR_EN_FILTER_TIME				MFR_EN_DLY						

Bits	Bit Name	Description
[15:12]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[11]	MFR_COPYMTP_ENPIN_RESTART	Enable bit of copying MTP when EN pulls up again (PE = 1). 1'b0: disable 1'b1: enable
[10:7]	MFR_EN_FILTER_TIME	It is used to set the synchronized EN pulse length to be high for EN start-up or EN re-start-up for the three rails. 100µs/LS.
[6:0]	MFR_EN_DLY	Sets the delay for Rail A to wait to output power after FBh[10:7] (on Page 0) passes, and there is no V_{IN} or temp fault. 20µs/LSB. This is the second delay for the start, and it is also the delay of hiccup, retry, and PMBus off and on.

MFR_IMON_SVID (FCh)

The MFR_IMON_SVID command on Page 0 is used to set the gain and offset of the Rail A I_{OUT} report from the VR to the SVID processor. R_{imon} can be calculated with Equation (12):

$$R_{imon} = \frac{1.6*8*32}{11*Kcs*MFR\_ICC\_MAX} \quad (12)$$

Where K_{CS} is the Intelli-Phase current sense gain (in µA/A).

Command	MFR_IMON_SVID															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	MFR_IMON_SVID_OFFSET							MFR_IMON_SVID_GAIN							

Bits	Bit Name	Description
[15]	RESERVED	Unused. X indicates that writes are ignored and always read as 0.
[14:8]	MFR_IMON_SVID_OFFSET	Sets the Rail A I_{OUT} SVID report offset, which is added to the value directly to the SVID I_{OUT} report register (15h). The default value is 0. Bit[14] is the sign bit. If setting the offset to -1, set [14:8] = 7'h7F If setting the offset to -2, set [14:8] = 7'h7E
[7:0]	MFR_IMON_SVID_GAIN	Sets the gain of the Rail A I_{OUT} SVID report. The default value is 128.

MFR_ALT_SET (FDh)

The MFR_ALT_SET command on Page 0 is used to set the Rail alert timing.

Slew rate of the alert reference: ([13:12] + 1) * 5mV / ([5:0] * 100ns) * 10 ^ 3 (mV/µs), in 5mV mode.

Slew rate of the alert reference: ([13:12] + 1) * 10mV / ([5:0] * 100ns) * 10 ^ 3 (mV/µs), in 10mV mode.

Command	MFR_ALT_SET															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function																

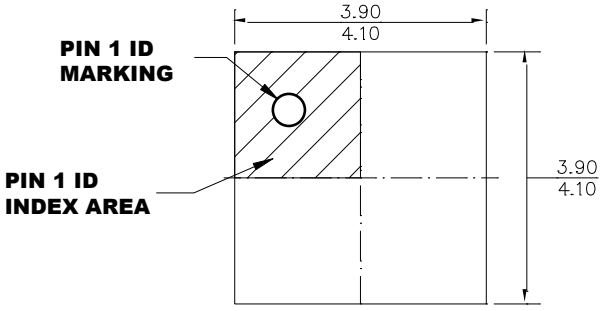
Bits	Bit Name	Description
[15:13]	ALERT_FIRST_STEP	The number of VID changes with the first change of VID_ALERT. The first VID change = FDh[15:13]
[12:11]	ALERT_STEP_NUM	Sets the decreasing step for Rail A at a non-decay DVID. The step is set to DEC ([13:12]) + 1.
[10:6]	ALERT_DELAY_TIME	Sets the Rail delay time to pull the VR_settle signal high after the alert reference reaches the target VID. 100ns/LSB.
[5:0]	ALERT_SR_CNT	Sets the Rail time length of the alert reference changing one step. 100ns/LSB.

CLEAR_EEPROM_FAULTS (FEh)

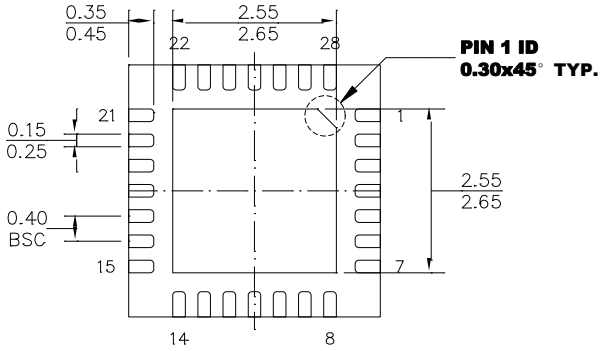
The CLEAR_EEPROM_FAULTS command is used to clear the EEPROM fault bits. The VR starts ramping and outputs power if no other protection exists. This command is write only. There is no data byte for this command.

PACKAGE INFORMATION

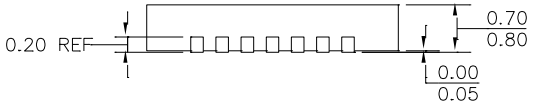
TQFN-28 (4mm X 4mm)



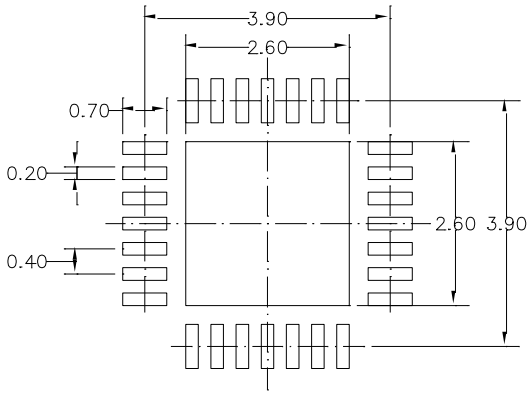
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) DRAWING CONFORMS TO JEDEC MO-220.
5) DRAWING IS NOT TO SCALE.