FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-27247-2E

ASSP for Power Supply Applications (Secondary battery)

DC/DC Converter IC of Synchronous Rectification for charging Li-ion battery

MB39A119

■ DESCRIPTION

The MB39A119 is the N-ch MOS drive of the synchronous rectification type DC/DC converter IC using pulse-width modulation (PWM) type that can charge Li-ion battery from 1 cell to 4 cells and suitable for down-conversion.

This IC integrates built-in comparator for the voltage detection of the AC adapter and switches the power supply to the AC adapter or battery automatically, enabling supply it to system. In addition, the constant voltage control state detection function is built in, which prevents mis-detecting the full charge. The MB39A119 provides a wide range of power supply voltage and low standby current, high efficiency, making it ideal for use as a built-in charge device in products such as notebook PC.

■ FEATURES

- High efficiency : 97 % (Max)
- High-frequency operation : 1 MHz (Max)
- Built-in off time control function
- Built-in voltage detection function of AC adapter (ACOK, XACOK terminal)
- Preventing mis-detection for the full charge by the constant voltage control state detection function (CVM terminal)

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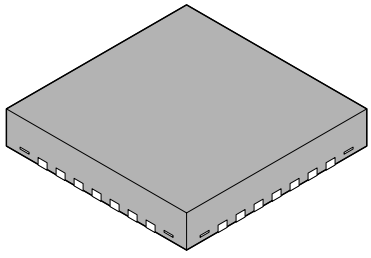
■ PACKAGE

28-pin plastic QFN



(LCC-28P-M10)

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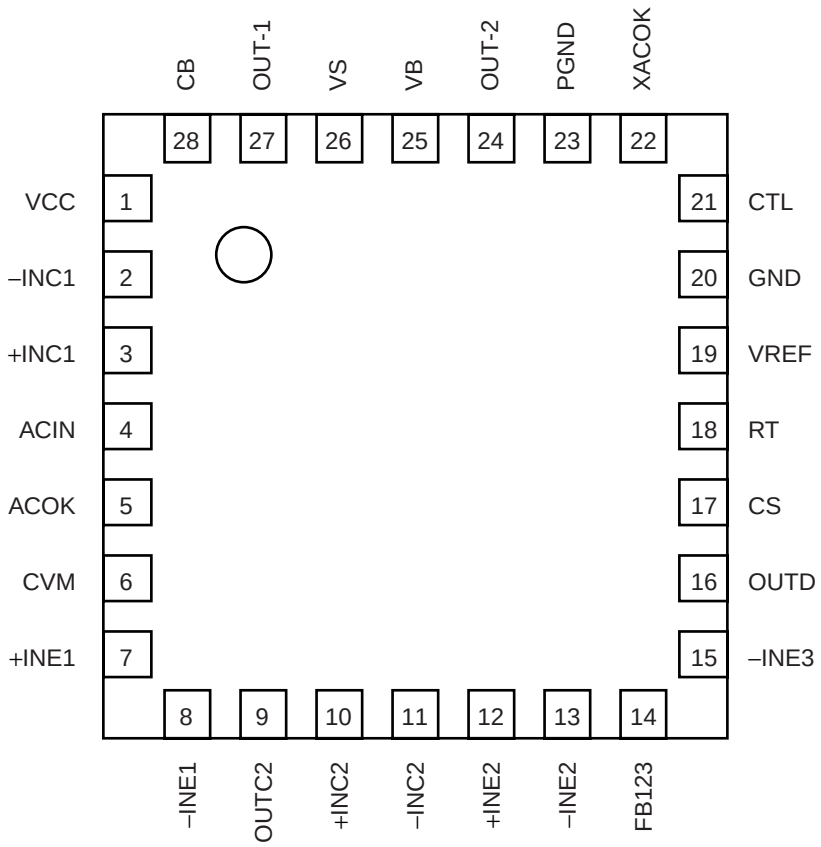
- Built-in two constant current control circuits
- Analog control of constant current value is possible (+ INE1, + INE2 terminal)
- Built-in output stage for N-ch MOS FET synchronous rectification
- Built-in charge stop function at low input voltage
- Output voltage setting accuracy : 4.2 V ± 0.74 % (Ta= – 10 °C to + 85 °C)
- Built-in high accuracy charge current detection amplifier : ± 4 %
  (At input voltage difference 100 mV with Voltage gain 24.5 (V/V)
- Built-in high accuracy input current detection amplifier : ± 3 %
  (At input voltage difference 100 mV with Voltage gain 25 (V/V)
- Arbitrary output voltage can be set by external resistor
- In IC standby mode, output voltage setting resistor is made to be open to prevent inefficient current loss
- Quiescent current : 1.9 mA (Typ)
- Standby current : 0 μA (Typ)
- Package : QFN28

■ PIN ASSIGNMENT

(TOP VIEW)



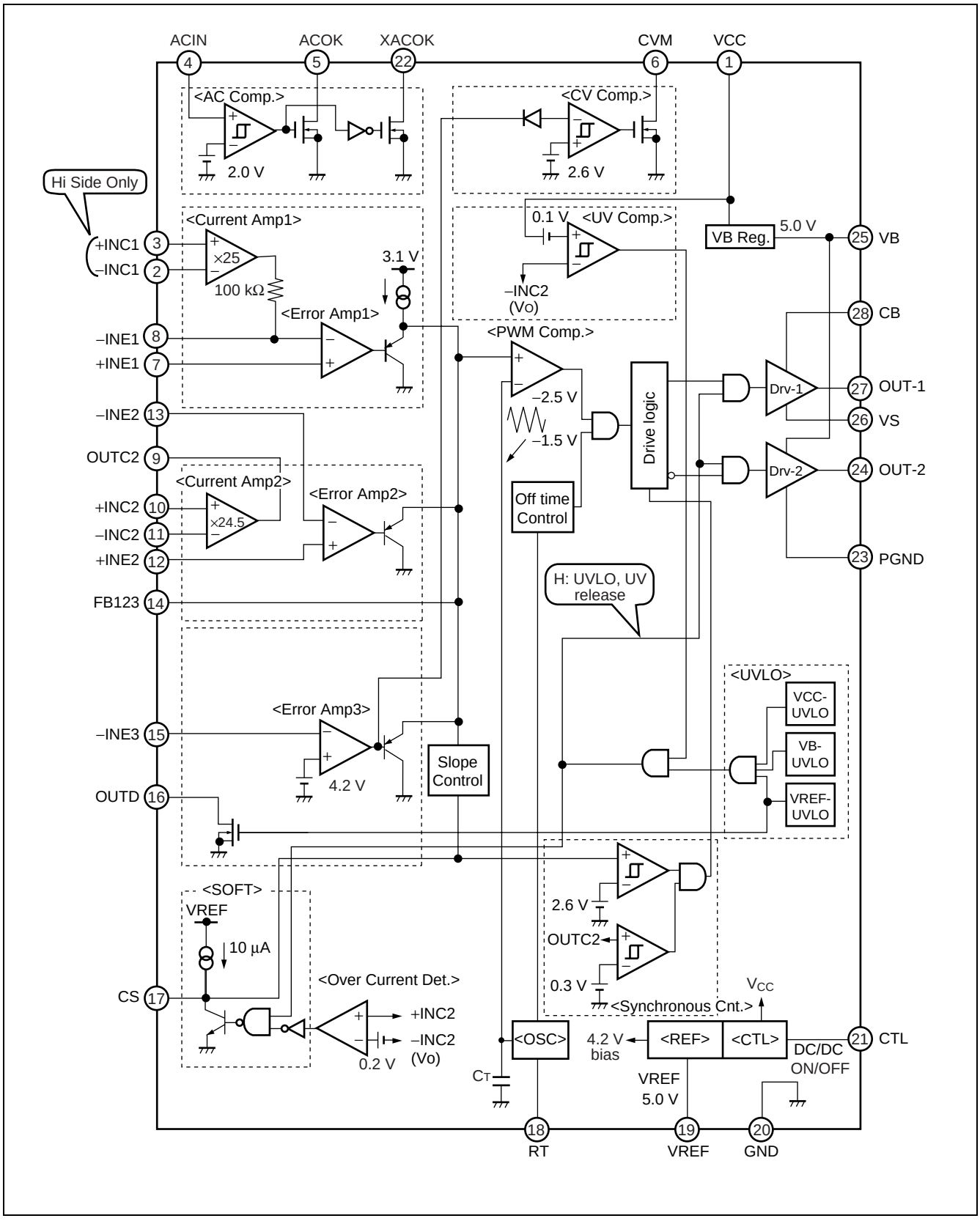
(LCC-28P-M10)

Note : Connect IC's radiation board at bottom side to potential of GND.

■ PIN DESCRIPTION

Pin No.	Pin Name	I/O	Description
1	VCC	—	Power supply terminal for reference voltage and control circuit.
2	–INC1	I	Input current detection amplifier (Current Amp1) input terminal.
3	+ INC1	I	Input current detection amplifier (Current Amp1) input terminal.
4	ACIN	I	AC adapter voltage detection block (AC Comp.) input terminal.
5	ACOK	O	AC adapter voltage detection block (AC Comp.) output terminal. ACOK = L when ACIN = H, ACOK = Hi-Z when ACIN = L, ACOK = Hi-Z when CTL = L
6	CVM	O	Constant voltage control state detection block (CV Comp.) output terminal.
7	+ INE1	I	Error amplifier (Error Amp1) non-inverted input terminal.
8	–INE1	I	Error amplifier (Error Amp1) inverted input terminal.
9	OUTC2	O	Charge current detection amplifier (Current Amp2) output terminal.
10	+ INC2	I	Charge current detection amplifier (Current Amp2) input terminal.
11	–INC2	I	Charge current detection amplifier (Current Amp2) and low input voltage detection comparator (UV Comp.) input terminal.
12	+ INE2	I	Error amplifier (Error Amp2) non-inverted input terminal.
13	– INE2	I	Error amplifier (Error Amp2) inverted input terminal.
14	FB123	O	Error amplifier (Error Amp1, 2, 3) output terminal.
15	–INE3	I	Error amplifier (Error Amp3) inverted input terminal.
16	OUTD	O	This terminal is set to Hi-Z to prevent loss of current through the output voltage setting resistor when IC is standby mode. OUTD = Hi-Z when CTL = L OUTD = L when CTL = H
17	CS	—	Soft-start capacitor connection terminal.
18	RT	—	Triangular wave oscillation frequency setting resistor connection terminal.
19	VREF	O	Reference voltage output terminal.
20	GND	—	Ground terminal.
21	CTL	I	Power supply control terminal for DC/DC converter block.
22	XACOK	O	AC adapter voltage detection block (AC Comp.) output terminal. XACOK = Hi-Z when ACIN = H, XACOK = L when ACIN = L, XACOK = Hi-Z when CTL = L
23	PGND	—	Ground terminal.
24	OUT-2	O	External synchronous rectification side FET gate drive output terminal.
25	VB	O	Bias output terminal for output circuit.
26	VS	—	External main side FET source conneciton terminal.
27	OUT-1	O	External main side FET gate drive output terminal.
28	CB	—	Boot strap capacitor connection terminal. The capacitor is connected between the CB terminal and the VS terminal.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating		Unit
			Min	Max	Unit
Power supply voltage	V_{CC}	VCC terminal	—	27	V
CB terminal input voltage	V_{CB}	CB terminal	—	32	V
Control input voltage	V_{CTL}	CTL terminal	—	27	V
Input voltage	V_{INE}	+ INE1, + INE2, − INE1, − INE2, − INE3 terminal	—	V_{CC} + 0.3	V
	V_{INC1}	+ INC1, − INC1 terminal	—	V_{CC} + 0.3	V
	V_{INC2}	+ INC2, − INC2 terminal	—	20	V
OUTD terminal output voltage	V_{OUTD}	OUTD terminal	—	20	V
ACIN input voltage	V_{ACIN}	ACIN terminal	—	V_{CC}	V
ACOK terminal output voltage	V_{ACOK}	ACOK terminal	—	27	V
XACOK terminal output voltage	V_{XACOK}	XACOK terminal	—	27	V
CVM terminal output voltage	V_{CVM}	CVM terminal	—	27	V
Output current	I_{OUT}	—	—	60	mA
Power dissipation	P_D	Ta ≤ +25 °C	—	4400*1,*2	
			—	1900*1,*3	mW
Storage temperature	T_{STG}	—	−55	+ 125	°C

*1 : The packages are mounted on the dual-sided epoxy board (10 cm × 10cm) .

*2 : With connection of exposed pad and with thermal via.

*3 : With connection of exposed pad and without thermal via.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power supply voltage	V_{CC}	VCC terminal	8	—	25	V
CB terminal input voltage	V_{CB}	CB terminal	—	—	30	V
Reference voltage output current	I_{REF}	VREF terminal	–1	—	0	mA
Bias output current	I_{VB}	VB terminal	–1	—	0	mA
Input voltage	V_{INE}	+ INE1, + INE2, – INE1, – INE2, – INE3 terminal	0	—	5	V
	V_{INC1}	+ INC1, –INC1 terminal	7	—	V_{CC}	V
	V_{INC2}	+ INC2, –INC2 terminal	0	—	19	V
Input voltage difference	D_{VINC}	Current detection voltage range	0	—	140	mV
OUTD terminal output voltage	V_{OUTD}	OUTD terminal	0	—	19	V
OUTD terminal output current	I_{OUTD}	OUTD terminal	0	—	2	mA
CTL terminal input voltage	V_{CTL}	CTL terminal	0	—	25	V
ACIN input voltage	V_{ACIN}	ACIN terminal	0	—	V_{CC}	V
ACOK terminal output voltage	V_{ACOK}	ACOK terminal	0	—	25	V
XACOK terminal output voltage	V_{XACOK}	XACOK terminal	0	—	25	V
CVM terminal output voltage	V_{CVM}	CVM terminal	0	—	25	V
Peak output current	I_{OUT}	Duty ≤ 5 % (t=1/f_{OSC} × Duty)	–1200	—	+1200	mA
Oscillation frequency	f_{OSC}	—	200	500	1000	kHz
Timing resistor	R_T	RT terminal	—	39	—	kΩ
Soft-start capacitor	C_S	CS terminal	—	0.22	—	µF
CB terminal capacitor	C_B	CB terminal	—	0.1	—	µF
Bias output capacitor	C_{VB}	VB terminal	—	1.0	—	µF
Reference voltage output capacitor	C_{REF}	VREF terminal	—	0.1	1.0	µF
Operating ambient temperature	Ta	—	–30	+25	+85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

(VCC = 19 V, VB = 0 mA, VREF = 0 mA, Ta = +25 °C)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min	Typ	Max	
Reference voltage block [REF]	Output voltage	V_{REF1}	19	Ta = +25 °C	4.963	5.000	5.037	V
		V_{REF2}	19	Ta = –10 °C to + 85 °C	4.95	5.00	5.05	V
	Input stability	Line	19	VCC = 8 V to 25 V	—	1	10	mV
	Load stability	Load	19	VREF = 0 mA to –1 mA	—	1	10	mV
	Short-circuit output current	Ios	19	VREF = 1 V	–60	–30	–15	mA
Under voltage lockout protection circuit block [UVLO]	Threshold voltage	V_{TLH}	1	VCC	—	7.5	7.9	V
		V_{THL}	1	VCC	7.0	7.4	—	V
	Hysteresis width	V_H	1	VCC	—	0.1	—	V
	Threshold voltage	V_{TLH}	25	VB	3.8	4.0	4.2	V
		V_{THL}	25	VB	3.1	3.3	3.5	V
	Hysteresis width	V_H	25	VB	—	0.7	—	V
	Threshold voltage	V_{TLH}	19	VREF	2.5	2.7	2.9	V
		V_{THL}	19	VREF	2.3	2.5	2.7	V
	Hysteresis width	V_H	19	VREF	—	0.2	—	V
Soft-start block [SOFT]	Charge current	I_{CS}	17	—	–14	–10	–6	µA
Triangular wave oscillator block [OSC]	Oscillation frequency	fosc	27	RT = 39 kΩ	450	500	550	kHz
	Frequency temperature stability	Δf/fdt	27	Ta = –30 °C to + 85 °C	—	1*	—	%
Error amplifier block [Error Amp1]	Input offset voltage	V_{IO}	7, 8	—	—	1	5	mV
	Input bias current	I_B	7, 8	—	–50	–15	—	nA
	Voltage gain	A_V	7, 8, 14	DC	—	100*	—	dB
	Frequency bandwidth	BW	7, 8, 14	A_V = 0 dB	—	1.2*	—	MHz
	Output voltage	V_{FBH}	14	—	2.9	3.1	—	V
		V_{FBL}	14	—	—	0.8	0.9	V
	Output source current	I_{SOURCE}	14	FB123 = 2 V	—	–60	–30	µA
	Output sink current	I_{SINK}	14	FB123 = 2 V	2.0	4.0	—	mA

* : Standard design value

(Continued)

(VCC = 19 V, VB = 0 mA, VREF = 0 mA, Ta = +25 °C)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min	Typ	Max	
Error amplifier block [Error Amp2]	Input offset voltage	V_{IO}	12, 13	—	—	1	5	mV
	Input bias current	I_B	12, 13	—	–50	–15	—	nA
	Voltage gain	A_V	12, 13, 14	DC	—	100*	—	dB
	Frequency bandwidth	BW	12, 13, 14	A_V = 0dB	—	1.2*	—	MHz
	Output voltage	V_{FBH}	14	—	2.9	3.1	—	V
		V_{FBL}	14	—	—	0.8	0.9	V
	Output source current	I_{SOURCE}	14	FB123 = 2 V	—	–60	–30	µA
	Output sink current	I_{SINK}	14	FB123 = 2 V	2.0	4.0	—	mA
Error amplifier block [Error Amp3]	Threshold voltage	V_{TH1}	14, 15	FB123 = 2 V	4.179	4.200	4.221	V
		V_{TH2}	14, 15	FB123 = 2 V, Ta = –10 °C to + 85 °C	4.169	4.200	4.231	V
	Voltage gain	A_V	14, 15	DC	—	100*	—	dB
	Frequency bandwidth	BW	14, 15	A_V = 0 dB	—	1.2*	—	MHz
	Output voltage	V_{FBH}	14	—	2.9	3.1	—	V
		V_{FBL}	14	—	—	0.8	0.9	V
	Output source current	I_{SOURCE}	14	FB123 = 2 V	—	–60	–30	µA
	Output sink current	I_{SINK}	14	FB123 = 2 V	2.0	4.0	—	mA
	OUTD terminal leak current	I_{LEAK}	16	OUTD = 19 V	—	0	1	µA
	OUTD terminal output ON resistance	R_{ON}	16	OUTD = 1 mA	—	35	50	Ω
Current detection amplifier block [Current Amp1]	Current detection voltage	V_{OUTC1}	8	+ INC1 = − INC1 = 7 V to 19 V, ΔV_{IN} = 100 mV	2.425	2.5	2.575	V
		V_{OUTC2}	8	+ INC1 = − INC1 = 7 V to 19 V, ΔV_{IN} = 20 mV	0.425	0.5	0.575	V
	Voltage gain	A_V	2, 3, 8	+ INC1 = − INC1 = 7 V to 19 V, ΔV_{IN} = 100 mV	24.25	25	25.75	V/V
	Input offset voltage	V_{IO}	2, 3, 8	+ INC1 = − INC1 = 7 V to 19 V	–3	—	+3	mV
	Input current	I_{INC1}	2, 3	+ INC1 = − INC1 = 7 V to 19 V	—	20	30	µA
		I_{INC2}	2, 3	+ INC1 = − INC1 = 7 V to 19 V, CTL = 0 V	—	0	1	µA
	Frequency bandwidth	BW	2, 3, 8	A_V = 0 dB	—	3.0*	—	MHz
	Output voltage	V_{OUTCH}	8	—	3.7	4.0	—	V
		V_{OUTCL}	8	—	—	0.04	0.2	V
	Output source current	I_{SOURCE}	8	-INE1 = 2 V	—	–1.2	–0.6	mA
	Output sink current	I_{SINK}	8	-INE1 = 2 V	100	200	—	µA

* : Standard design value

(Continued)

(VCC = 19 V, VB = 0 mA, VREF = 0 mA, Ta = +25 °C)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min	Typ	Max	
Current detection amplifier block [Current Amp2]	Current detection voltage	V_{OUTC1}	9	+ INC2 = − INC2 = 3 V to 19 V, ΔV_{IN} = 100 mV	2.38	2.48	2.58	V
		V_{OUTC2}	9	+ INC2 = − INC2 = 3 V to 19 V, ΔV_{IN} = 20 mV	0.44	0.52	0.60	V
		V_{OUTC3}	9	+ INC2 = − INC2 = 0 V to 3 V, ΔV_{IN} = 100 mV	2.24	2.45	2.66	V
		V_{OUTC4}	9	+ INC2 = − INC2 = 0 V to 3 V, ΔV_{IN} = 20 mV	0.30	0.5	0.70	V
	Voltage gain	A_V	9, 10, 11	+ INC2 = − INC2 = 3 V to 19 V, ΔV_{IN} = 100 mV	23.76	24.5	25.24	V/V
	Input offset voltage	V_{IO}	9, 10, 11	+ INC2 = − INC2 = 3 V to 19 V	−1.5	+1.5	+4.5	mV
	Input current	I_{+INCH}	10	+ INC2 = − INC2 = 3 V to 19 V, ΔV_{IN} = 100 mV	—	30	45	µA
		I_{-INCH}	11	+ INC2 = − INC2 = 3 V to 19 V, ΔV_{IN} = 100 mV	—	0.1*	—	µA
		I_{INCL}	10, 11	+ INC2 = − INC2 = 0 V	−300	−200	—	µA
	Frequency bandwidth	BW	9, 10, 11	A_V = 0 dB	—	3.0*	—	MHz
	Output voltage	V_{OUTCH}	9	—	3.9	4.2	—	V
		V_{OUTCL}	9	—	—	0.04	0.2	V
	Output source current	I_{SOURCE}	9	OUTC2 = 2 V	—	−1.2	−0.6	mA
	Output sink current	I_{SINK}	9	OUTC2 = 2 V	100	200	—	µA
PWM comparator block [PWM Comp.]	Threshold voltage	V_{TL}	14	Duty cycle = 0%	—	1.5	—	V
		V_{TH}	14	Duty cycle = 100%	—	2.5	—	V
Output block [Drv-1, 2]	Output ON resistance	R_{OH}	24, 27	OUT-1, OUT-2 = −100 mA	—	4	7	Ω
		R_{OL}	24, 27	OUT-1, OUT-2 = 100 mA	—	1	3.5	Ω
Under input voltage detection comparator block [UV Comp.]	Threshold voltage	V_{TLH}	11	−INC2 = 12.6 V	12.6	12.8	13.0	V
		V_{THL}	11	−INC2 = 12.6 V	12.5	12.7	12.9	V
	Hysteresis width	V_H	11	—	—	0.1	—	V

* : Standard design value

(Continued)

(Continued)

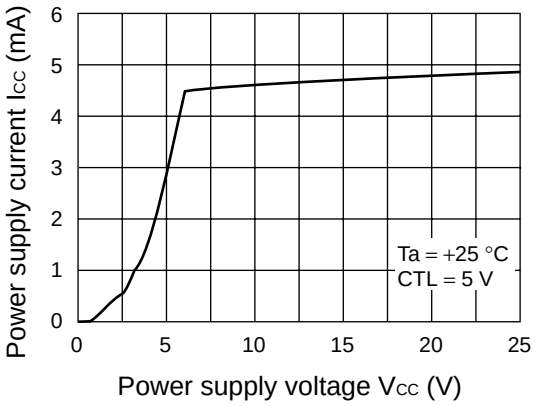
(VCC = 19 V, VB = 0 mA, VREF = 0 mA, Ta = +25 °C)

Parameter		Symbol	Pin No.	Conditions	Value			Unit
					Min	Typ	Max	
Overcurrent detection block [Over Current Det.]	Threshold voltage	V_{TLH}	11	–INC2 = 12.6 V	12.75	12.8	12.85	V
AC adapter voltage detection block [AC Comp.]	Threshold voltage	V_{TLH}	4	—	2.056	2.12	2.184	V
		V_{THL}	4	—	1.959	2.02	2.081	V
	Hysteresis width	V_H	4	—	—	0.1	—	V
	ACOK terminal output leak current	I_{LEAK}	5	ACOK = 25 V	—	0	1	µA
	ACOK terminal output ON resistance	R_{ON}	5	ACOK = 1 mA	—	200	400	Ω
	XACOK terminal output leak current	I_{LEAK}	22	XACOK = 25 V	—	0	1	µA
	XACOK terminal output ON resistance	R_{ON}	22	XACOK = 1 mA	—	200	400	Ω
Constant voltage control state detection block [CV Comp.]	Threshold voltage	V_{TLH}	14	—	—	2.7*	—	V
		V_{THL}	14	—	—	2.6*	—	V
	Hysteresis width	V_H	14	—	—	0.1*	—	V
	CVM terminal output leak current	I_{LEAK}	6	CVM = 25 V	—	0	1	µA
	CVM terminal output ON resistance	R_{ON}	6	CVM = 1 mA	—	200	400	Ω
Synchronous rectification control block [Synchronous Cnt.]	CS threshold voltage	V_{TLH}	17	—	2.55	2.6	2.65	V
		V_{THL}	17	—	2.50	2.55	2.60	V
	Hysteresis width	V_H	17	—	—	0.05	—	V
	Light load detection threshold voltage	V_{TLH}	9	—	0.35	0.4	0.45	V
		V_{THL}	9	—	0.25	0.3	0.35	V
	Hysteresis width	V_H	9	—	—	0.1	—	V
Bias voltage block [VB]	Output voltage	V_B	25	—	4.9	5.0	5.1	V
	Load stability	Load	25	VB = 0 mA to − 10 mA	—	10	50	mV
Control block [CTL]	CTL input voltage	V_{ON}	21	IC operating state	2	—	25	V
		V_{OFF}	21	IC standby state	0	—	0.8	V
	Input current	I_{CTLH}	21	CTL = 5 V	—	25	40	µA
		I_{CTLL}	21	CTL = 0 V	—	0	1	µA
General	Standby current	I_{CCS}	1	CTL = 0 V	—	0	10	µA
	Power supply current	I_{CC}	1	CTL = 5 V	—	1.9	2.9	mA

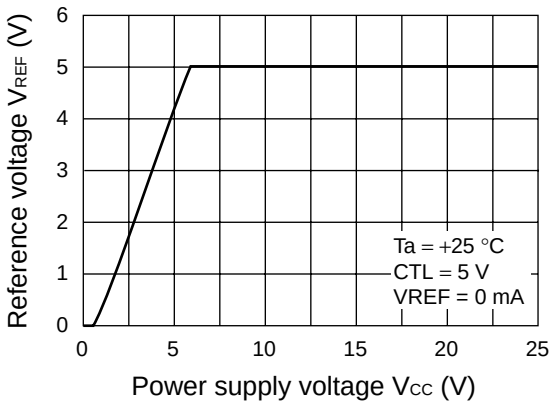
* : Standard design value

■ TYPICAL CHARACTERISTICS

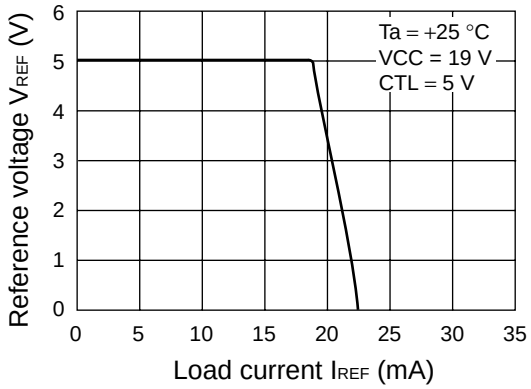
Power Supply Current vs. Power Supply Voltage



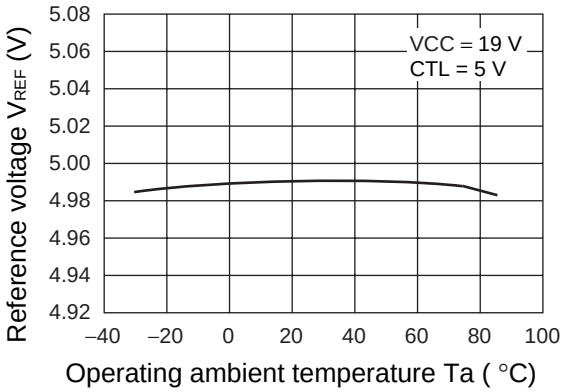
Reference Voltage vs. Power Supply Voltage



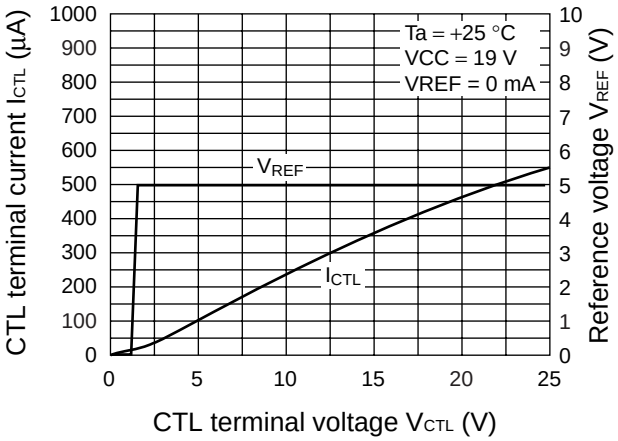
Reference Voltage vs. Load Current



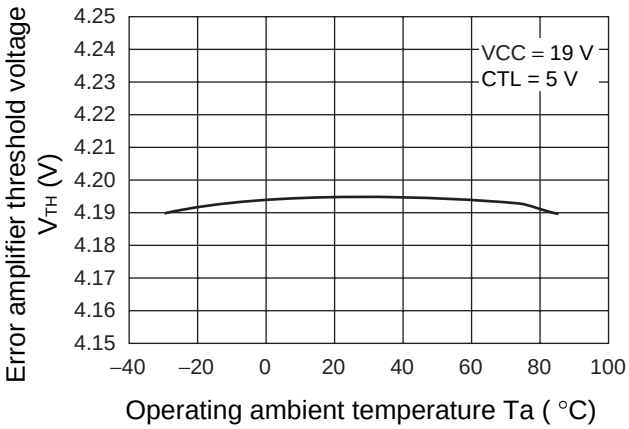
Reference Voltage vs. Operating Ambient Temperature



CTL Terminal Current, Reference Voltage vs. CTL Terminal Voltage



Error Amplifier Threshold Voltage vs. Operating Ambient Temperature



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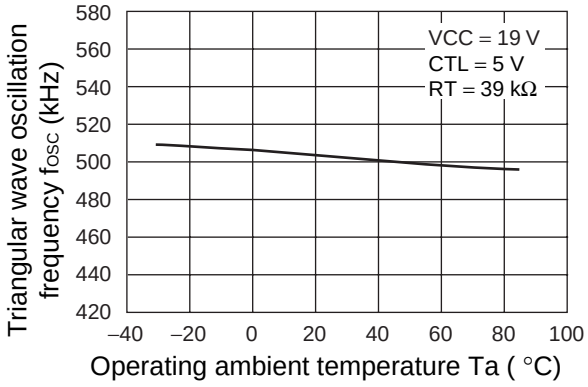
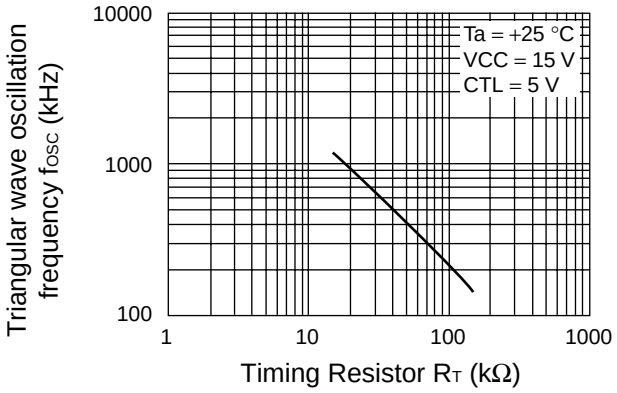
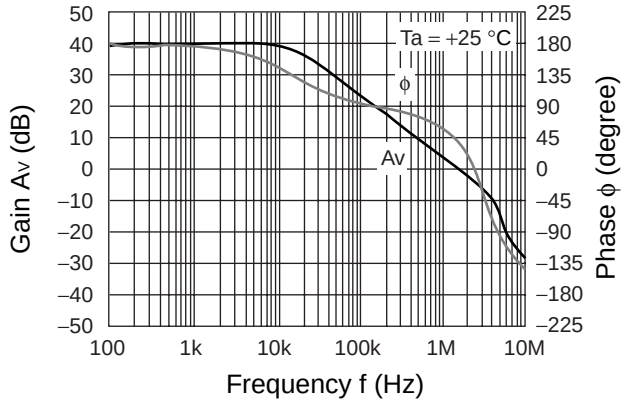
Triangular Wave Oscillation Frequency vs. Operating Ambient Temperature

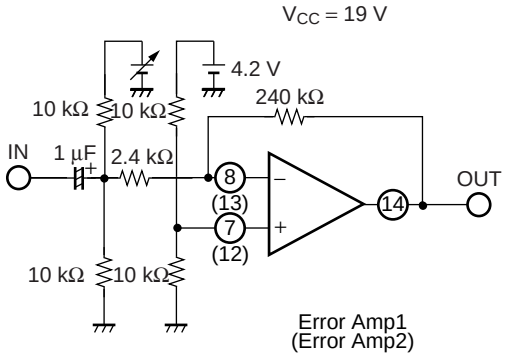


Triangular Wave Oscillation Frequency vs. Timing Resistor

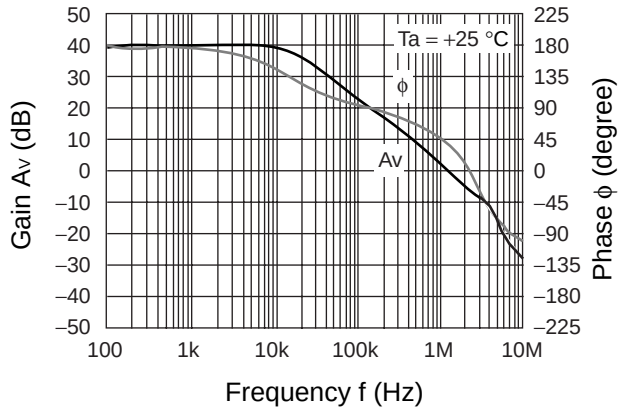


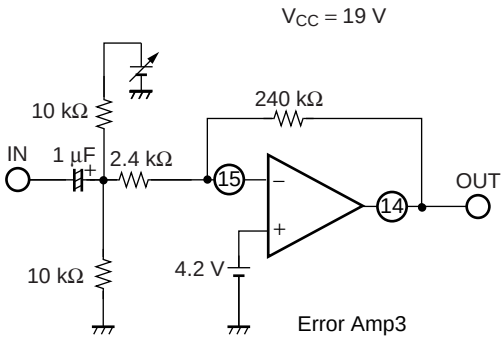
Error Amplifier Gain, Phase vs. Frequency (ERR1, 2)





Error Amplifier Gain, Phase vs. Frequency (ERR3)





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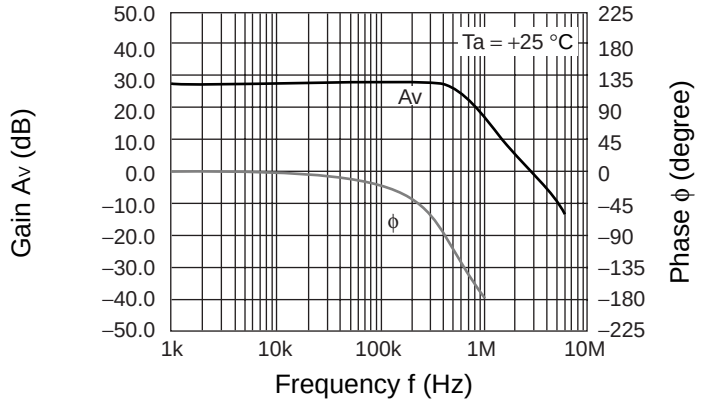
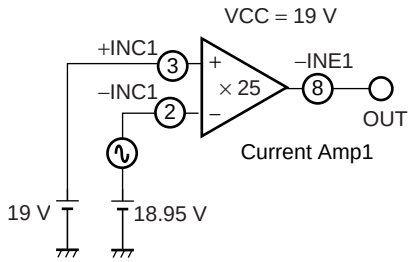
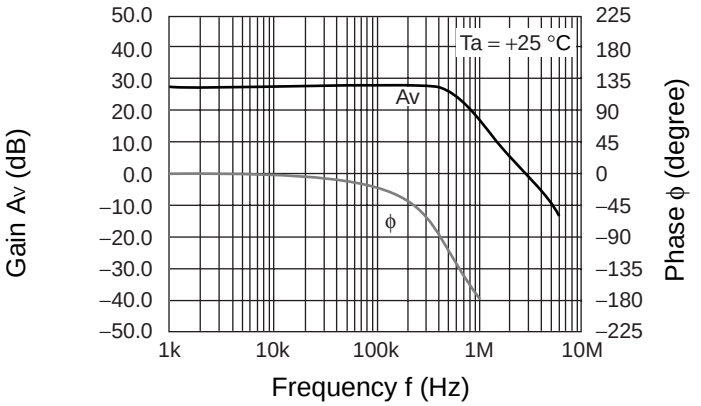
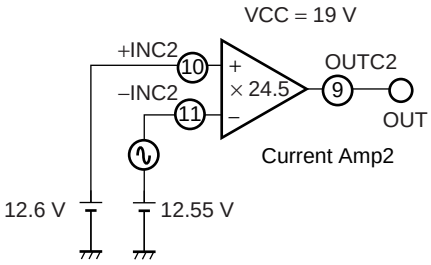
Current Detection Amplifier Gain, Phase vs. Frequency



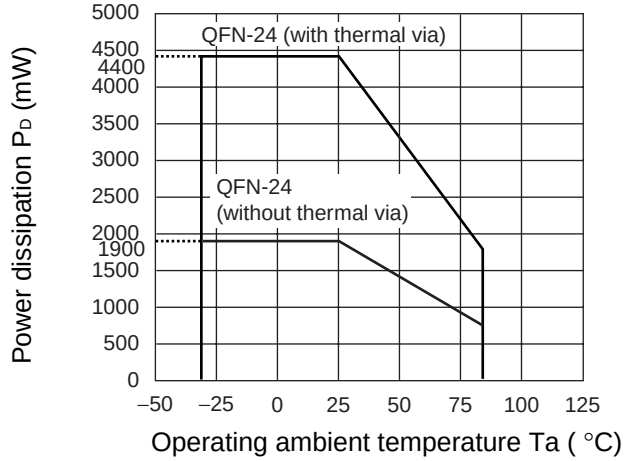


Current Detection Amplifier Gain, Phase vs. Frequency





Power Dissipation vs. Operating Ambient Temperature



■ FUNCTION DESCRIPTION

1. DC/DC Converter Block

(1) Reference voltage block (REF)

The reference voltage circuit uses the voltage supplied from the VCC terminal (pin 1) to generate a temperature compensated, stable voltage (5.0 V Typ) used as the reference power supply voltage for the IC's internal circuitry. This block can also be used to obtain a load current to a maximum of 1 mA from the reference voltage VREF terminal (pin 19) .

(2) Triangular wave oscillator block (OSC)

The triangular wave oscillator block has built-in capacitor for frequency setting and generates the triangular wave oscillation waveform by connecting the triangular wave oscillation frequency setting resistor with the RT terminal (pin 17) .

The triangular wave is input to the PWM comparator circuits on the IC.

(3) Error amplifier block (Error Amp1)

This amplifier detects the output signal from the current detection amplifier (Current Amp1) , compares this to the +INE1 terminal (pin 7) , and outputs a PWM control signal to be used in controlling the charge current.

In addition, an arbitrary loop gain can be set up by connecting a feedback resistor and capacitor between the FB123 terminal (pin 14) and -INE1 terminal (pin 8) , providing stable phase compensation to the system.

(4) Error amplifier block (Error Amp2)

This amplifier detects the output signal from the current detection amplifier (Current Amp2) , compares this to the +INE2 terminal (pin 12) , and outputs a PWM control signal to be used in controlling the charge current.

In addition, an arbitrary loop gain can be set up by connecting a feedback resistor and capacitor between the FB123 terminal (pin 14) and -INE2 terminal (pin 13) , providing stable phase compensation to the system.

(5) Error amplifier block (Error Amp3)

This error amplifier (Error Amp3) detects the output voltage from the DC/DC converter and outputs the PWM control signal. External output voltage setting resistors can be connected to the error amplifier inverted input terminal to set the desired level of output voltage from 1 cell to 4 cells.

In addition, an arbitrary loop gain can be set by connecting a feedback resistor and capacitor from the FB123 terminal (pin 14) to the -INE3 terminal (pin 15) of the error amplifier, enabling stable phase compensation to the system.

(6) Current detection amplifier block (Current Amp1)

The current detection amplifier (Current Amp1) detects a voltage drop which occurs between both ends of the output sense resistor (R_{S2}) due to the flow of the AC adapter current, using the +INC1 terminal (pin 3) and -INC1 terminal (pin 2) . The AC adapter current control signal is amplified to 25 times and output to the inverse input terminal of Error Amp1 through the internal 100 kΩ.

This amplifier cannot use for detecting the charge current.

(7) Current detection amplifier block (Current Amp2)

The current detection amplifier (Current Amp2) detects a voltage drop which occurs between both ends of the output sense resistor (R_{S1}) due to the flow of the charge current, using the +INC2 terminal (pin 10) and -INC2 terminal (pin 11) . The signal amplified to 24.5 times is output to the OUTC2 terminal (pin 9) .

(8) PWM comparator block (PWM Comp.)

The PWM comparator circuit is a voltage-pulse width converter for controlling the output duty of the error amplifiers (Error Amp1 to Error Amp3) depending on their output voltage.

The PWM comparator circuit compares with either of low voltages between the triangular wave voltage generated by the triangular wave oscillator and the error amplifier output voltage, turns on the main side output transistor

and turns off on the synchronous rectification side output transistor, during the interval in which the triangular wave voltage is lower than the error amplifier output voltage.

(9) Output block (Drv-1, 2)

The output circuit uses a CMOS configuration capable of driving an external N-ch MOS FET both main side and synchronous rectification side.

(10) Control block (CTL)

Setting the CTL terminal (pin 21) "L" level places in the standby mode.

CTL function table

CTL	Power	OUTD
L	OFF (Standby)	Hi-Z
H	ON (Active)	L

(11) Bias voltage block (VB)

Bias voltage block outputs 5 V (Typ) for the power supply of the output circuit and for setting the bootstrap voltage.

(12) Off time control block (Off time Control)

When MB39A119 operates by high on-duty, voltage difference of both ends of boot strap capacitor C_B is decreasing gradually. In such the case, off time control block charges with C_B by compulsorily generating off time (0.3 μs Typ) .

(13) Overcurrent detection block (Over Current Det.)

Overcurrent detection block detects the 0.2 V (Typ) or more potential difference between +INC2 terminal (pin 10) and -INC2 terminal (pin 11) . When excessive current flows to the charge direction due to load-sudden change, it determines the overcurrent, makes CS terminal (pin 17) "L" level, and makes the on duty 0 %. After finishing the overcurrent, MB39A119 restarts with the soft-start operation.

(14) Synchronous rectification control block (Synchronous Cnt.)

CS terminal (pin 17) and 2.6 V (Typ) are compared. Output OUT-2 terminal (pin 24) for synchronous rectification side FET drive in the soft-start is fixed at "L" level.

Output OUTC2 terminal of current detection amplifier block (Current Amp2) (pin 9) and 0.3 V (Typ) are compared, and output OUT-2 terminal (pin 24) for synchronous rectification side FET drive is fixed at "L" level at light-load.

2. Protection Function

(1) Under voltage lockout protection circuit block (VREF-UVLO)

A momentary decrease in internal reference voltage (VREF) may cause malfunctions in the control IC, resulting in breakdown or degradation of the system.

To prevent such malfunction, the under voltage lockout protection circuit detects internal reference voltage drop and fixes the OUT-1 terminal (pin 27) and the OUT-2 terminal (pin 24) to the “L” level. The system restores voltage supply when the internal reference voltage reaches the threshold voltage of the under voltage lockout protection circuit.

Protection circuit (VREF-UVLO) operation function table

When UVLO is operating (VREF voltage is lower than UVLO threshold voltage) , the logic of the following terminal is fixed.

OUTD	OUT-1	OUT-2	CS	VB
Hi-Z	L	L	L	L

(2) Under voltage lockout protection circuit block (VCC-UVLO, VB-UVLO)

The transient state or a momentary decrease in power supply voltage, which occurs when the bias voltage (VB) for output circuit is turned on, may cause malfunctions in the control IC, resulting in breakdown or degradation of the system.

To prevent such malfunction, the under voltage lockout protection circuit detects a bias voltage drop and fixes the OUT-1 terminal (pin 27) and the OUT-2 terminal (pin 24) to the “L” level. The system restores voltage supply when the power supply voltage or internal reference voltage reaches the threshold voltage of the under voltage lockout protection circuit.

Protection circuit (VCC-UVLO, VB-UVLO) operation function table

When UVLO is operating (VCC voltage or VB voltage is lower than UVLO threshold voltage) , the logic of the following terminal is fixed.

OUT-1	OUT-2	CS
L	L	L

(3) Under input voltage detection comparator block (UV Comp.)

VCC terminal (pin 1) voltage and -INC2 terminal (pin 11) voltage are compared, and VCC voltage is lower than the battery voltage +0.1 V (Typ) and fixes the OUT-1 terminal (pin 27) and OUT-2 terminal (pin 24) to the “L” level.

The system restores voltage supply when the input voltage reaches the threshold voltage of the under input voltage detection comparator.

Protection circuit (UV Comp.) operation function table

When under input voltage is detected (Input voltage is lower than UV Comp. threshold voltage) , the logic of the following terminal is fixed.

OUT-1	OUT-2	CS
L	L	L

3. Detection Functions

(1) AC adapter voltage detection block (AC Comp.)

When ACIN terminal (pin 4) voltage is lower than 2.0 V (Typ) , AC adapter voltage detection block (AC Comp.) outputs “Hi-Z” level to the ACOK terminal (pin 5) and outputs “L” level to the XACOK terminal (pin 22) . When CTL terminal (pin 21) is set to “L” level, ACOK terminal (pin 5) and XACOK terminal (pin 22) are fixed to “Hi-Z” level.

AC adapter detection function table

The logic of the following terminal is fixed according to the connection state of the AC adapter.

ACIN	ACOK	XACOK
H	L	Hi-Z
L	Hi-Z	L

(2) Constant voltage control state detection block (CV Comp.)

When CV Comp. detects that the FB123 terminal (pin 14) voltage of the error amplifier (Error Amp3) output terminal becomes 2.6 V (Typ) or less, “L” level is output to constant voltage control state detection block output terminal CVM terminal (pin 6) .

Charge control state function table

Error Amp3 output (FB123)	CVM	Status
$>$ 2.6 V	Hi-Z	Constant current control
$\leq$ 2.6 V	L	Constant voltage control

■ CONSTANT CHARGING VOLTAGE AND CURRENT OPERATION

The MB39A119 is DC/DC converter IC with the pulse width modulation method (PWM method) .

In the output voltage control loop, the output voltage of the DC/DC converter is detected, and the Error Amp3 compares internal reference voltage 4.2 V and DC/DC converter output to output the PWM controlled signal.

In the charging current control loop, the voltage drop generated at both ends of charging current sense resistor (R_{S1}) is sensed by +INC2 terminal (pin 10) , -INC2 terminal (pin 11) of Current Amp2, and the signal is output to OUTC2 terminal (pin 9) , which is amplified by 24.5 times. Error Amp2 compares the OUTC2 terminal (pin 9) voltage, which is the output of Current Amp2, and +INE2 terminal (pin 12) to output the PWM control signal, and it regulates the charging current.

In AC adapter current control loop, the voltage drop generated at both ends of AC adapter current sense resistor (R_{S2}) is sensed by +INC1 terminal (pin 3) , -INC1 terminal (pin 2) of Current Amp1, and the signal is output to -INE1 terminal (pin 8) , which is amplified by 25 times. Error Amp1 compares -INE1 terminal (pin 8) voltage, which is output of Current Amp1, and +INE1 terminal (pin 7) to output PWM controlled signal, and it limits the charging current due to the AC adapter current not to exceed the setting value.

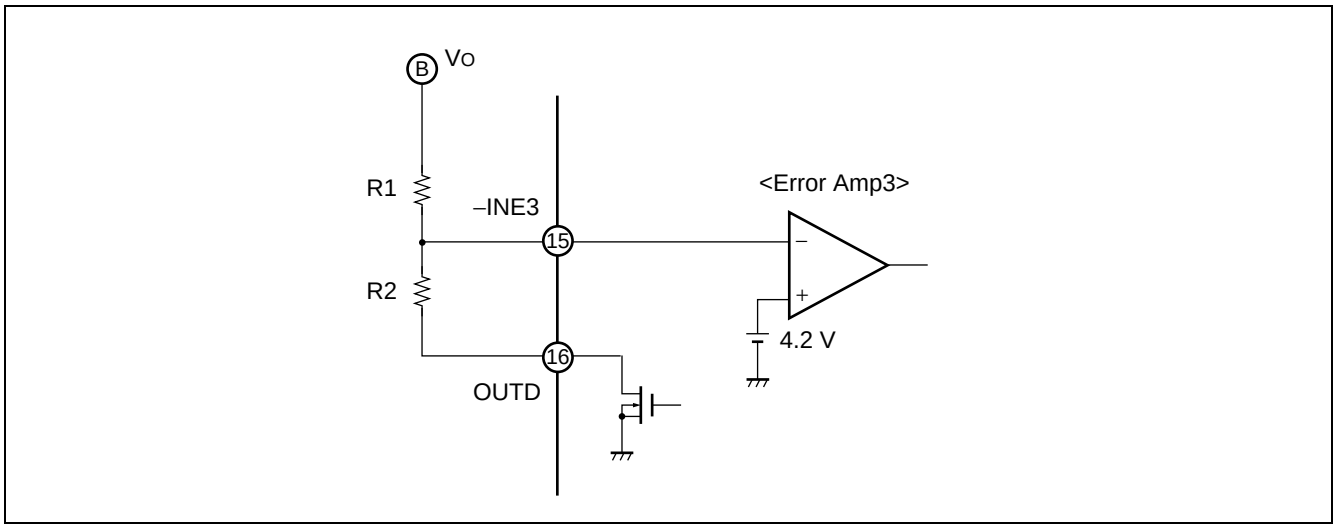
The PWM comparator compares the triangular wave to the smallest terminal voltage among the Error Amplifier output voltage (Error Amp1 to Error Amp3) . And the triangular wave voltage generated by the triangular wave oscillator. When the triangular wave voltage is smaller than the error amplifier output voltage, the main side output transistor is turned on and the synchronous rectification side output transistor is turned off.

■ SETTING THE CHARGE VOLTAGE

The charge voltage (DC/DC output voltage) can be set by connecting external output voltage setting resistors (R1 and R2) to the -INE3 terminal (pin 15) . Be sure to select a resistor value that allows you to ignore the on-resistance (35 Ω at 1 mA) of internal FET connected to the OUTD terminal (pin 16).

Battery charge voltage : V_O

$$V_O\ (V) = \frac{R1 + R2}{R2} \times -INE3\ (V)$$



■ SETTING THE CHARGE CURRENT

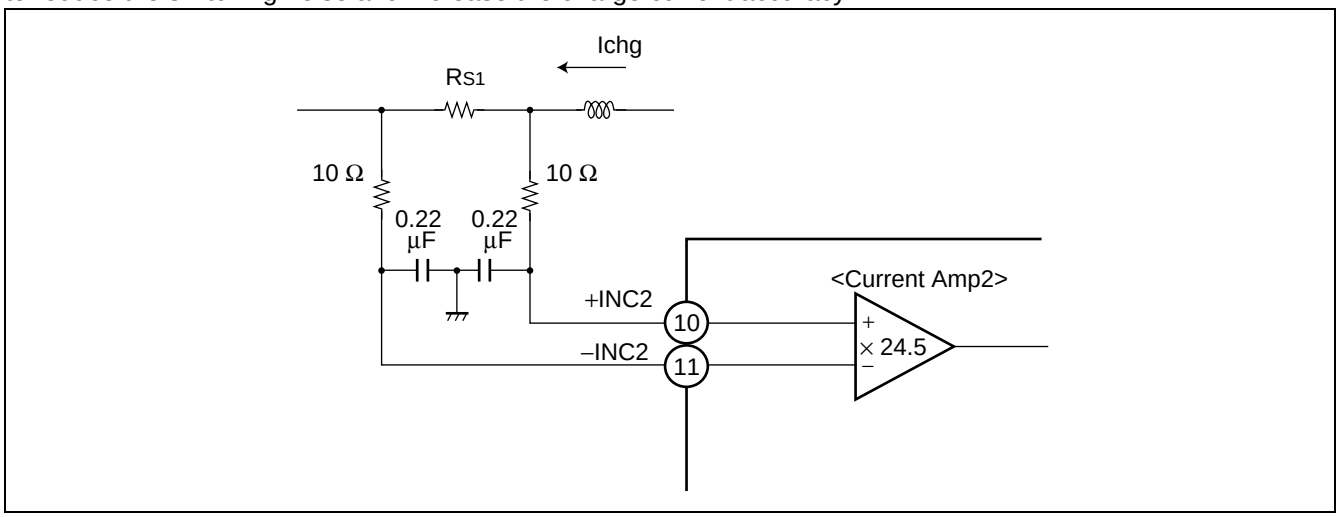
The charge current value can be set at the analog voltage value of the +INE2 terminal (pin 12) .

Charge current formula : $Ichg\ (A) = \frac{+INE2\ (V)}{24.5 \times R_{S1}\ (\Omega)}$

Battery charge current setting voltage : + INE2

$+INE2\ (V) = 24.5 \times Ichg\ (A) \times R_{S1}\ (\Omega)$

It is recommended that the filter should be connected to an input terminal of Current Amp2 as shown below in order to reduce the switching noise and increase the charge current accuracy.



■ SETTING THE INPUT CURRENT

The input limit current value can be set at the analog voltage value of the +INE1 terminal (pin 7) .

Input current formula : I_{IN} (A) $=$ $\dfrac{+\text{INE1 (V)}}{25 \times R_{S2}\ (\Omega)}$

Input current setting voltage : + INE1

+ INE1 (V) $= 25 \times I_{IN}$ (A) $\times R_{S2}$ (Ω)

■ SETTING THE OVERCURRENT DETECTION VALUE

The overcurrent is detected when the voltage difference is more than 0.2 V (Typ) between +INE2 terminal (pin 10) voltage and -INE2 terminal (pin 11) voltage.

Charge overcurrent detection value : Iocdet (A) $=$ $\dfrac{0.2\ (V)}{R_{S1}\ (\Omega)}$

Charge current and overcurrent detection value by R_{S1} value (example)

R_{S1}	+INE2	Ichg	OCDet
33 mΩ	0.5 V to 3.5 V	0.6 A to 4.2 A	6 A
15 mΩ	0.5 V to 3.5 V	1.3 A to 9.3 A	13 A

■ SETTING THE TRIANGULAR WAVE OSCILLATION FREQUENCY

The triangular wave oscillation frequency can be set by the timing resistor (R_T) connected to the RT terminal (pin 18) .

Triangular wave oscillation frequency : f_{OSC}

fosc (kHz) $\fallingdotseq$ $\dfrac{19500}{R_T\ (k\Omega)}$

■ SETTING THE SOFT-START TIME

To prevent rush current at start-up of IC, the soft-start time can be set by connecting soft-start capacitor (C_S) to the CS terminal (pin 17) .

When the CTL terminal (pin 21) is set to “H” level and IC is started ($V_{CC} \geq$ UVLO threshold voltage) , external soft-start capacitor (C_S) connected to the CS terminal (pin 17) is charged at 10 μA.

ON duty depends PWN comparator output, which compares the FB123 terminal (pin 14) voltage and the triangular wave oscillator output voltage.

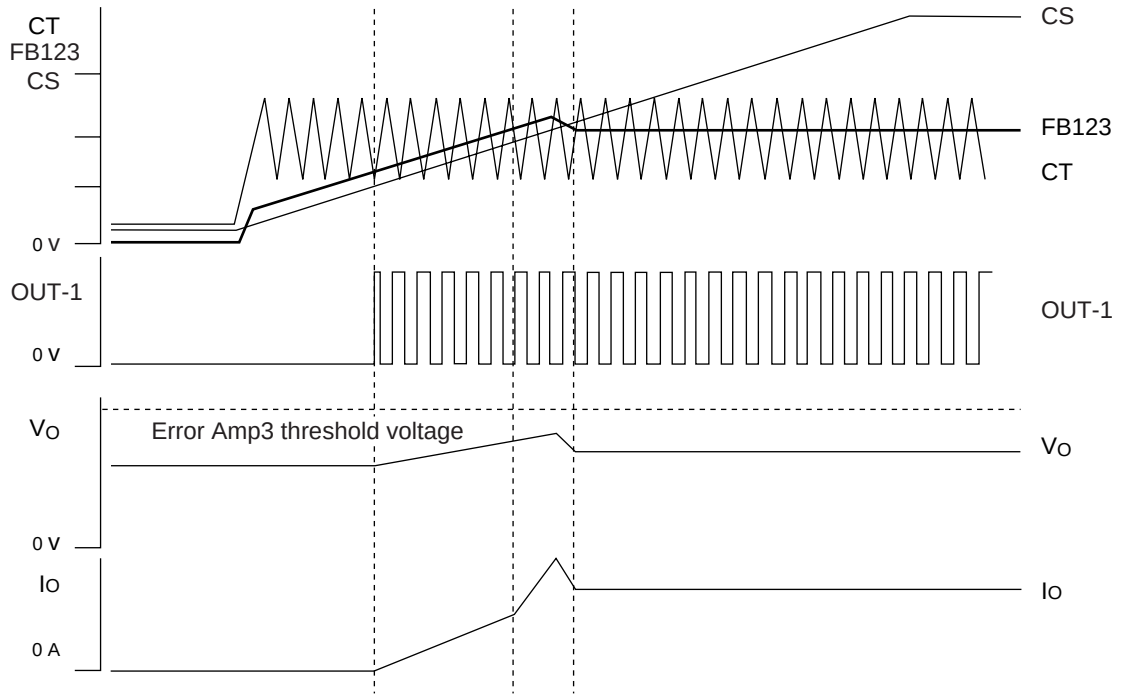
During soft-start, FB123 terminal (pin14) voltage increases with sum voltage of CS terminal (pin 17) and diode voltage. Therefore, the output voltage of the DC/DC converter and current increase can be set by output ON duty in proportion to rise of the CS terminal (pin 17) voltage. The ON duty is affected by the ramp voltage of FB123 terminal (pin 14) until an output voltage of one Error Amp reaches the DC/DC converter loop controlled voltage.

Soft-start time is obtained from the following formula. :

Soft-start time : t_S (time to output on duty 80 %)

t_S (s) ≒ 0.13 × C_S (μF)

• Soft-start timing chart



■ TRANSIENT RESPONSE AT LOAD-STEP

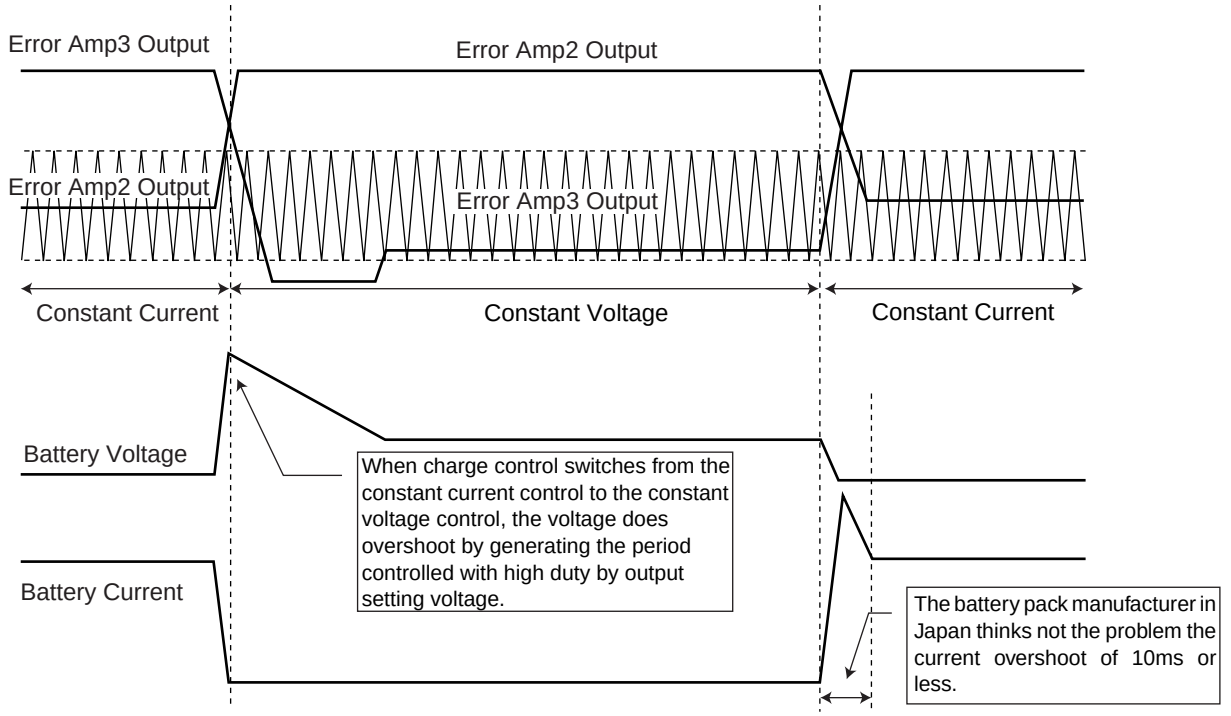
The constant voltage control loop and the constant current control loop are independent. With the load-step, these two control loops change.

The battery voltage and current overshoot are generated by the delay time of the control loop when the mode changes. The delay time is determined by phase compensation constant. When the battery is removed if the charge control is switched from the constant current control to the constant voltage control, and the charging voltage does overshoot by generating the period controlled with high duty by output setting voltage. The excessive voltage is not applied to the battery because the battery is not connected.

When the battery is connected if the charge control is switched from the constant voltage control to the constant current control, and the charging current does overshoot by generating the period controlled with high duty by output setting voltage.

The battery pack manufacturer in Japan thinks not the problem the current overshoot of 10ms or less.

• Operation at step-load



■ AC ADAPTER DETECTION FUNCTION

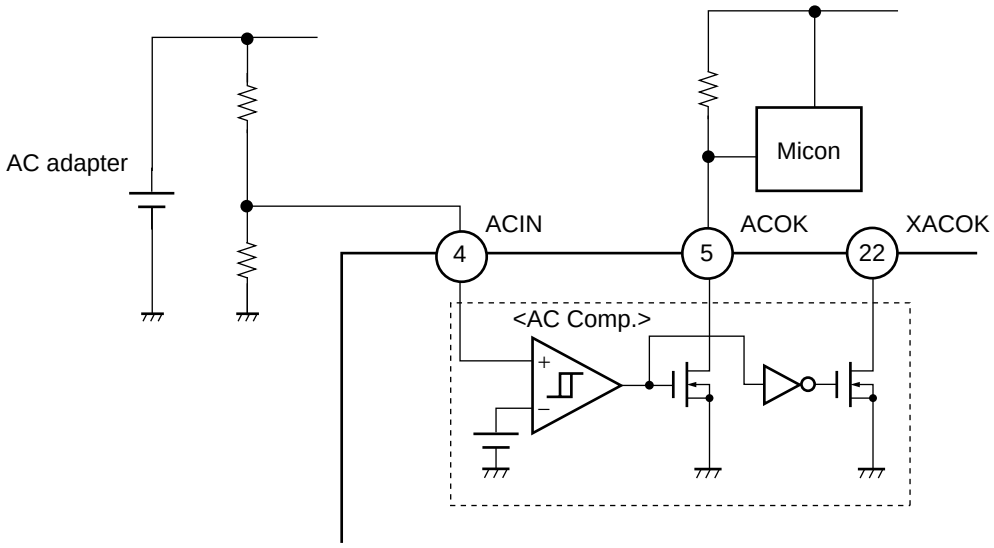
When ACIN terminal (pin 4) voltage is lower than 2.0 V (Typ) , AC adapter voltage detection block (AC Comp.) outputs “Hi-Z” level to the ACOK terminal (pin 5) and outputs “L” level to the XACOK terminal (pin 22) . When CTL terminal (pin 21) is set to “L” level, ACOK terminal (pin 5) and XACOK terminal (pin 22) are fixed to “Hi-Z” level.

(1) AC adapter presence

The presence of AC adapter can be easily detected because the signal is output from the ACOK terminal (pin 5) to microcomputer etc.

In this case, if CTL terminal (pin 21) is set in “L” level, IC become the standby state (I_{CC} = 0 μA Typ) .

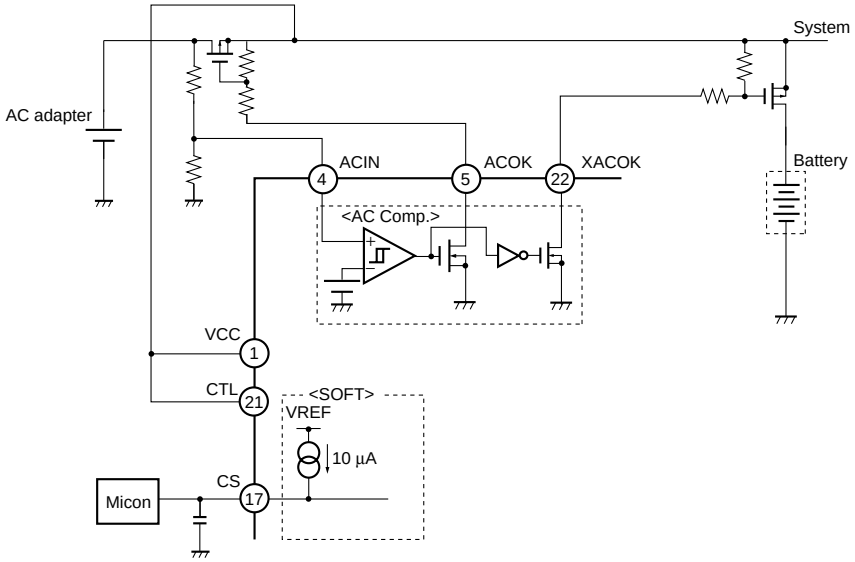
• Connection example of detecting AC adapter presence



(2) Automatic changing system power supply between AC adapter and battery

The AC adapter voltage is detected, and the external switch at input side and battery side is changed automatically with the connection as follows. Connect CTL terminal (pin 21) to VCC terminal (pin 1) for this function. OFF duty cycle becomes 100 % when CS terminal (pin 17) voltage is made to be 0 V, if it is needed after full charge.

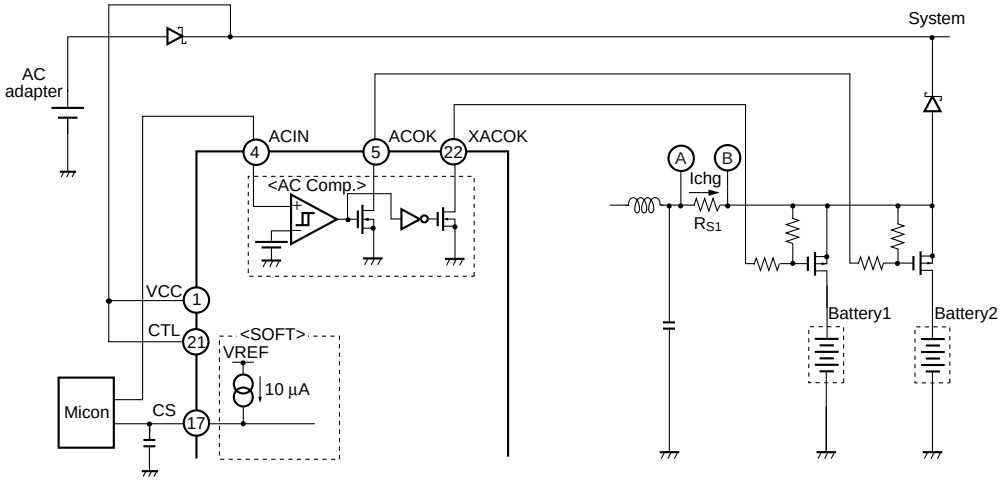
• Connection example of automatic changing system power supply between AC adapter and battery



(3) Battery selector function

When control signal from microcomputer etc. is input to ACIN terminal (pin 4) below, ACOK terminal (pin 5) output voltage and XACOK terminal (pin 22) output voltage are controlled to select one of the two batteries for charge. Connect CTL terminal (pin 21) to VCC terminal (pin 1) for this function. OFF duty cycle becomes 100 % when CS terminal (pin 17) voltage is made to be 0 V, if it is needed after full charge.

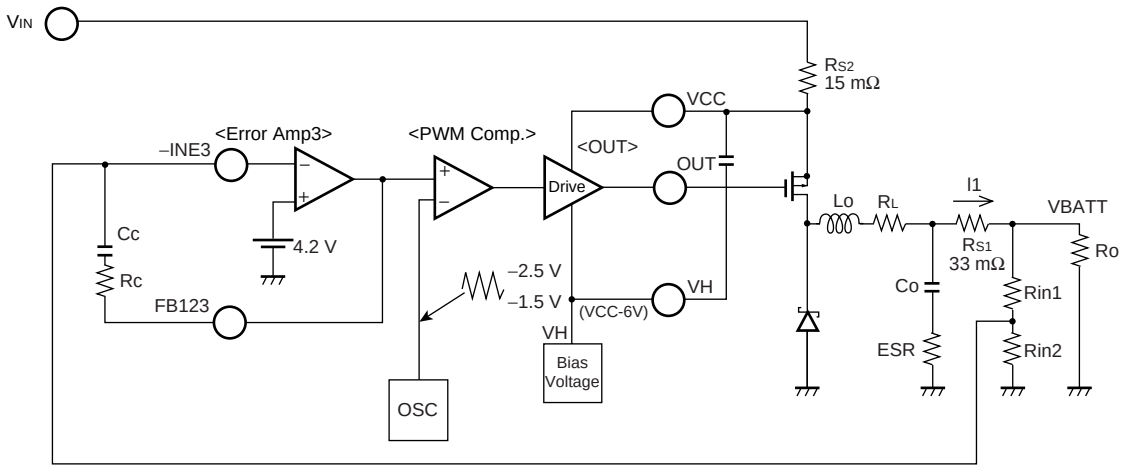
• Connection example of battery selector function



■ PHASE COMPENSATION

Circuit example of phase compensation is shown below.

• Circuit example of phase compensation



Lo : Inductance

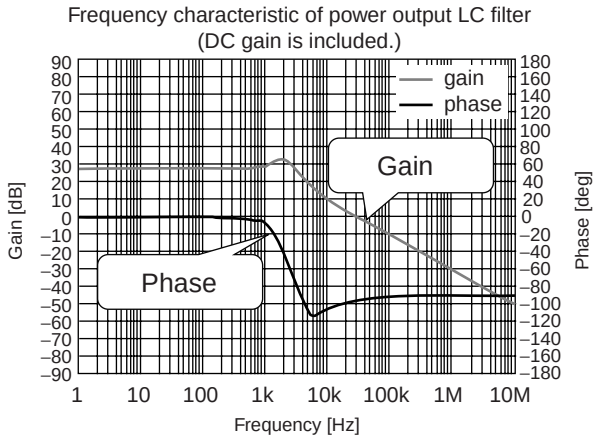
R_L : Equivalent series resistance of inductance

Co : Capacity of condenser

ESR : Equivalent series resistance of condenser

Ro : Load resistance

• Method to obtain frequency characteristic of LC filter

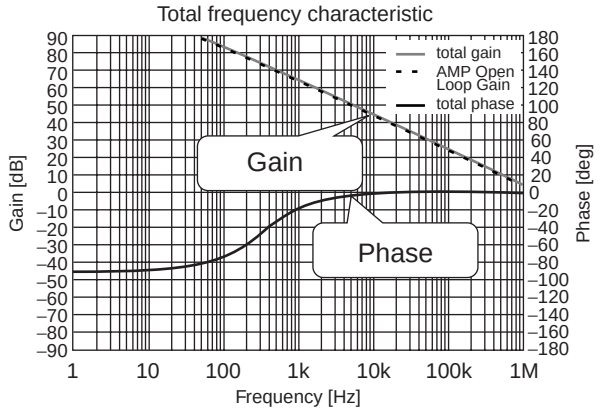


Cut-off frequency

$$f1\ (Hz) = \frac{1}{2\pi\sqrt{Lo \times Co \times \frac{(Ro + ESR)}{(Ro + R_L)}}}$$

Lo = 15 µH
Co = 14.1 µF
Ro = 4.2 Ω
R_L = 30 mΩ
ESR = 100 mΩ

• Method to obtain frequency characteristic of Error Amp

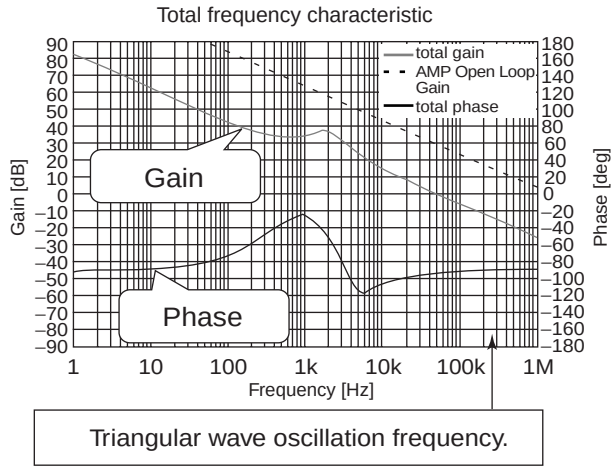


Cut-off frequency

$$f2\ (Hz) = \frac{1}{2\pi \times Rc \times Cc}$$

Rc = 150 kΩ
Cc = 3300 pF

• Method to obtain frequency characteristic of DC/DC converter

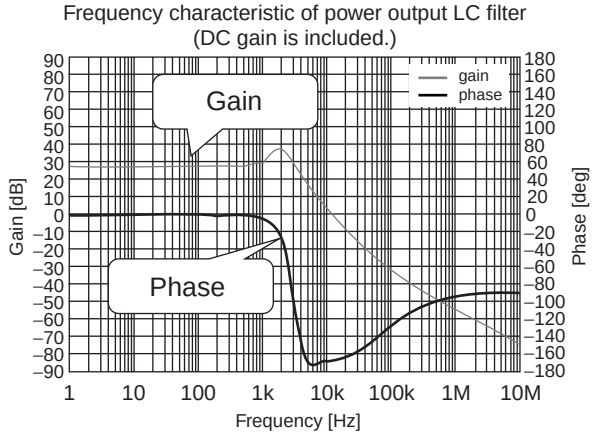


The overview of frequency characteristic for DC/DC converter can be obtained in combination between LC filter and frequency characteristic of Error Amp as mentioned above.
Note the following point in order to stabilize frequency characteristic of DC/DC converter.
Cut-off frequency of DC/DC converter should be set to half or less of the triangular wave oscillator frequency.

Note1) Review frequency characteristic of Error Amp when LC filter constant is changed.

Note2) When the ceramic capacitor is used as smoothing capacitor C_O, phase margin is reduced because ESR of the ceramic capacitor is extremely small as frequency characteristic of LC filter at low ESR. Therefore, change phase compensation of Error Amp or create resistance equivalent to ESR using pattern.

• Method to obtain frequency characteristic of LC filter at low ESR



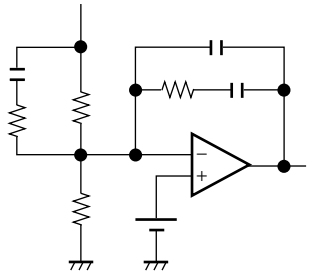
Cut-off frequency

$$f1\ (Hz) = \frac{1}{2\pi \sqrt{Lo \times Co \times \frac{(Ro + ESR)}{(Ro + R_L)}}}$$

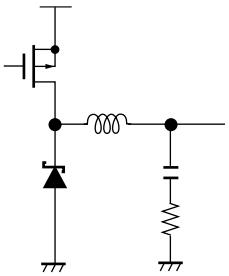
Lo = 15 µH
Co = 14.1 µF
Ro = 4.2 Ω
R_L = 30 mΩ
ESR = 100 mΩ

- 3Pole2Zero

DC/DC output



- Additional ESR

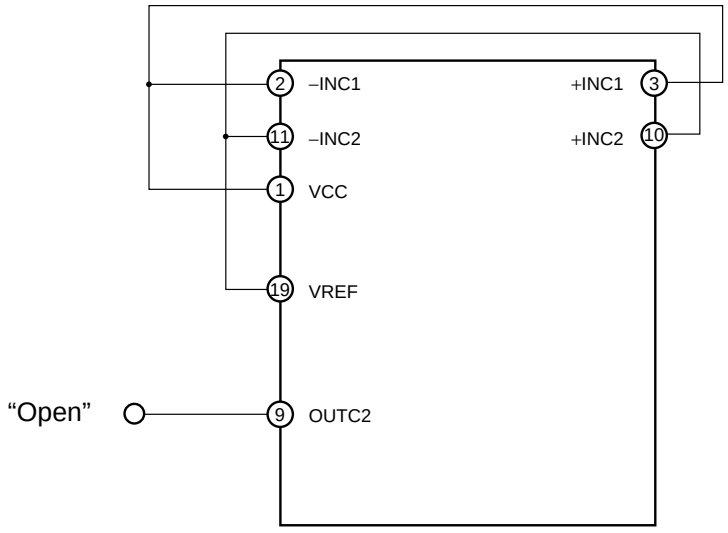


Board Pattern or connected resistor

■ PROCESSING WITHOUT USING OF THE CURRENT AMP1 AND AMP2

When Current Amp is not used, connect +INC1 terminal (pin 3) and –INC1 terminal (pin 2) to VCC terminal (pin 1) , connect +INC2 terminal (pin 10) and –INC2 terminal (pin 11) to VREF terminal (pin 19) , and then leave OUTC2 terminal (pin 9) open.

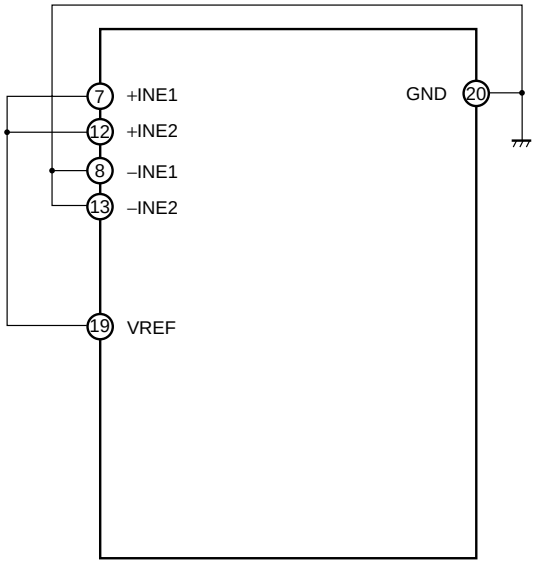
• Connection when Current Amp is not used



■ PROCESSING WITHOUT USING OF THE ERROR AMP1 AND AMP2

When Error Amp1 and Amp2 are not used, connect –INE1 terminal (pin 8) and –INE2 terminal (pin 13) to GND (pin 20) , and connect +INE1 terminal (pin 7) and +INE2 terminal (pin 12) to VREF terminal (pin 19) .

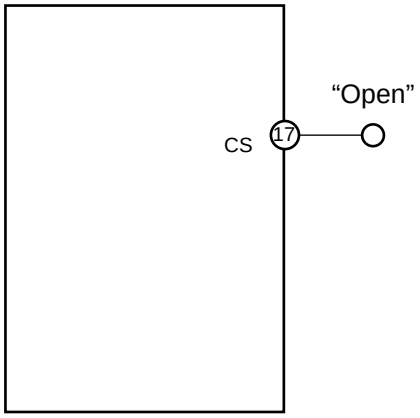
• Connection when Error Amp is not used



■ PROCESSING WITHOUT USING OF THE CS TERMINAL

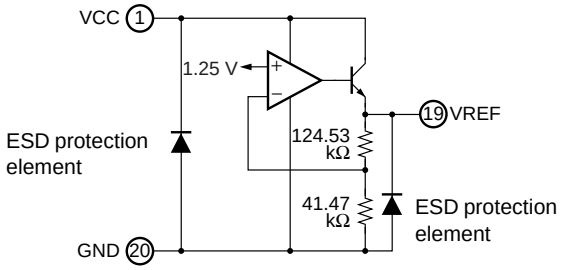
When soft-start function is not used, leave the CS terminal (pin 17) open.

- Connection when no soft-start time is specified

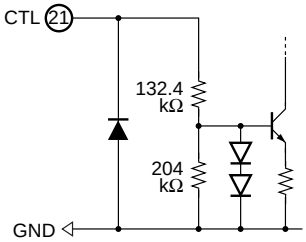


■ I/O EQUIVALENT CIRCUIT

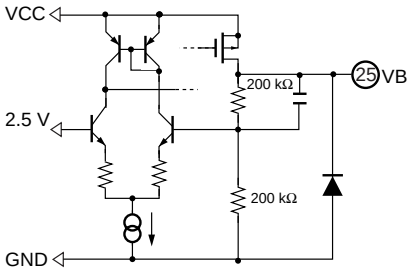
• Reference voltage block



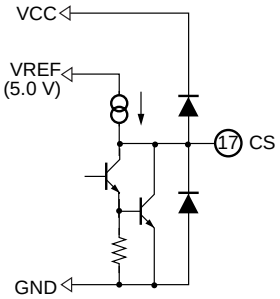
• Control block



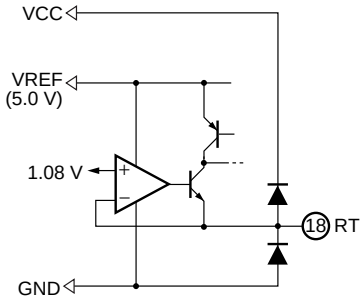
• Bias voltage block



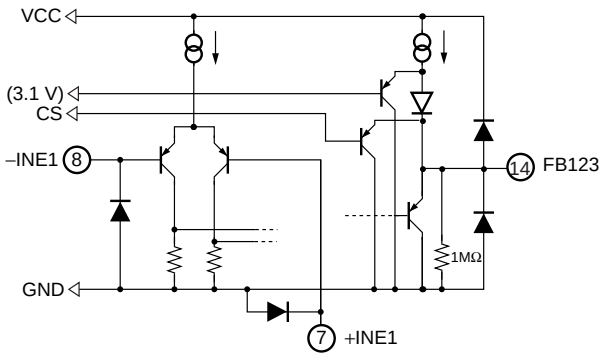
• Soft-start block



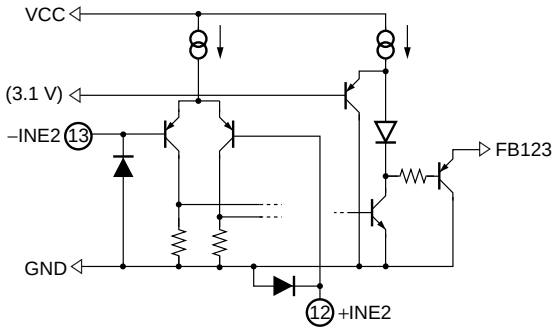
• Triangular wave oscillator block



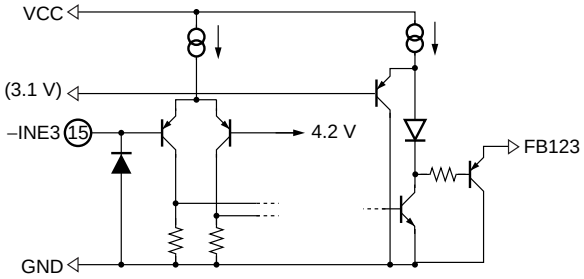
• Error amplifier block (Error Amp1)



• Error amplifier block (Error Amp2)



• Error amplifier block (Error Amp3)



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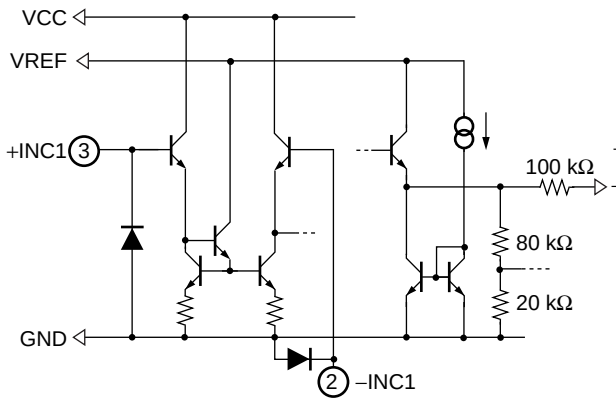
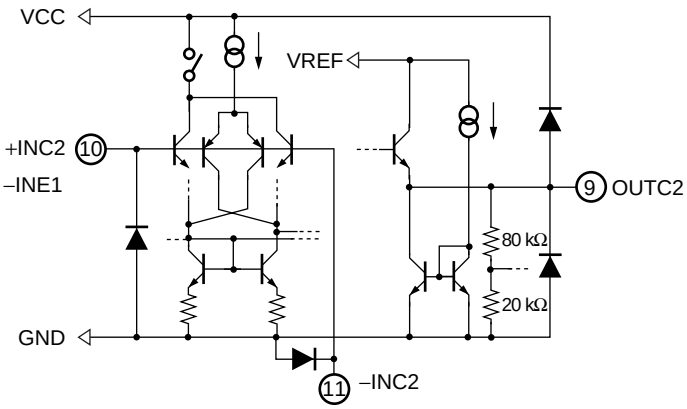
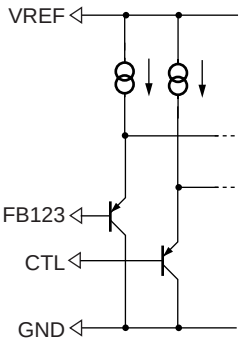
• Current detection amplifier block (Current Amp1)



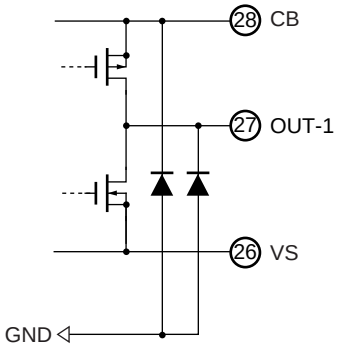
• Current detection amplifier block (Current Amp2)



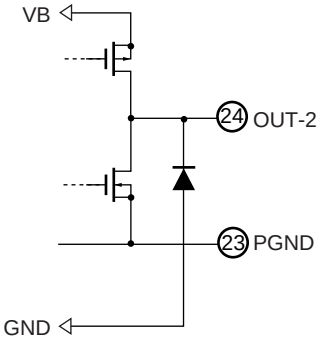
• PWM comparator block



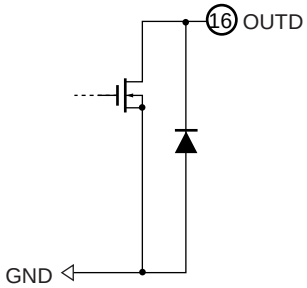
• Output block (Main side)



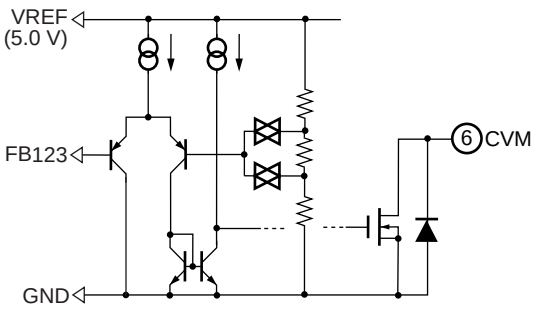
• Output block (synchronous rectification side)



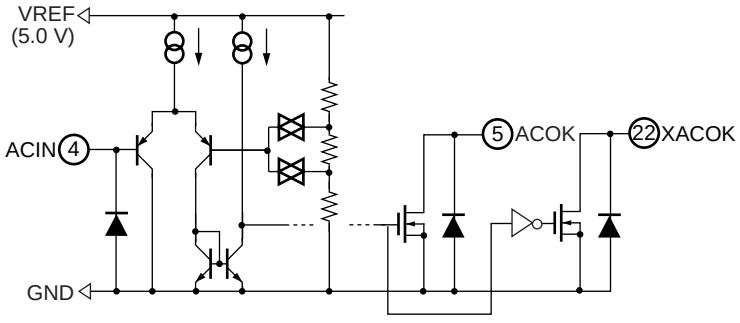
• Invalidity current prevention block



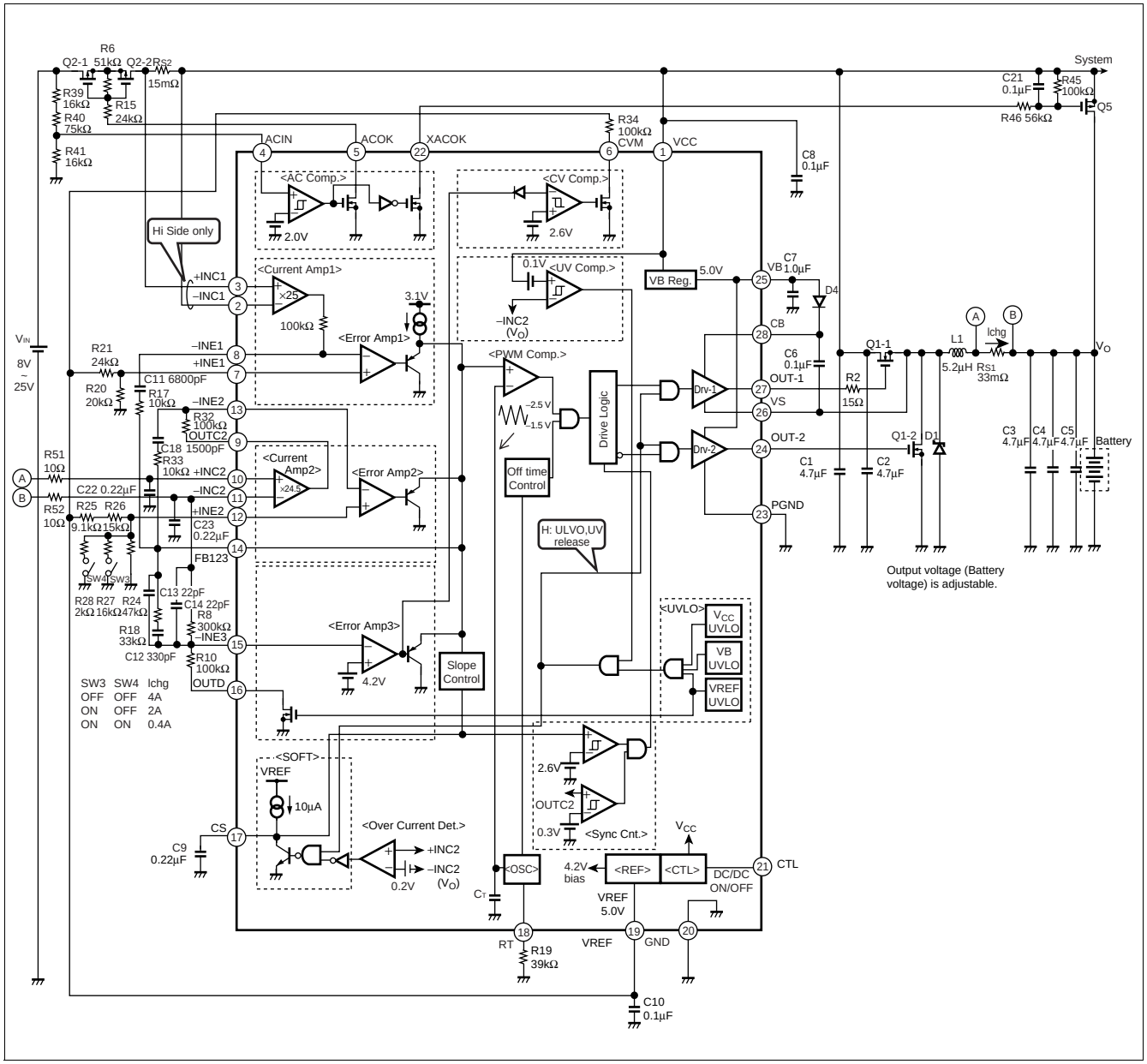
• Constant voltage control state detection block



• AC adapter voltage detection block



■ APPLICATION EXAMPLE



■ PARTS LIST

Component	Item	Specification	Vendor	Package	Parts No.
M1	IC	MB39A119	Fujitsu	QFN-28P	MB39A119QN-G
Q1-1, Q1-2	N-ch FET	VDS = − 30 V, ID = 8 A (Max)	NEC	SO-8	μPA2752
Q2-1, Q2-2	P-ch FET	VDS = − 30 V, ID = 8 A (Max)	NEC	SO-8	μPA1772
Q5	P-ch FET	VDS = − 30 V, ID = 6 A (Max)	TOSHIBA	SO-8	TPC8102
D1	Diode	VF = 0.35 V (Max) at IF = 0.5 A	ROHM	TUMD2	RSX051VA-30
D4	Diode	VF = 0.4 V (Max) at IF = 0.3 A	SANYO	1197A	SBS006
L1	Inductor	5.2 μH, 22 mΩ, 5.5 A	SUMIDA	SMD	CDRH104R-5R2
C1	Ceramic condenser	4.7 μF (25 V)	TDK	3216	C3216JB1E475K
C2	Ceramic condenser	4.7 μF (25 V)	TDK	3216	C3216JB1E475K
C3	Ceramic condenser	4.7 μF (25 V)	TDK	3216	C3216JB1E475K
C4	Ceramic condenser	4.7 μF (25 V)	TDK	3216	C3216JB1E475K
C5	Ceramic condenser	4.7 μF (25 V)	TDK	3216	C3216JB1E475K
C6	Ceramic condenser	0.1 μF (50 V)	TDK	1608	C1608JB1H104K
C7	Ceramic condenser	1.0 μF (25 V)	TDK	3216	C3216JB1E105K
C8	Ceramic condenser	0.1 μF (50 V)	TDK	1608	C1608JB1H104K
C9	Ceramic condenser	0.22 μF (25 V)	TDK	1608	C1608JB1E224K
C10	Ceramic condenser	0.1 μF (50 V)	TDK	1608	C1608JB1H104K
C11	Ceramic condenser	6800 pF (50 V)	TDK	1608	C1608JB1H682K
C12	Ceramic condenser	330 pF (50 V)	TDK	1608	C1608CH1H331J
C13	Ceramic condenser	22 pF (50 V)	TDK	1608	C1608CH1H220J
C14	Ceramic condenser	22 pF (50 V)	TDK	1608	C1608CH1H220J
C18	Ceramic condenser	1500 pF (50 V)	TDK	1608	C1608CH1H152J
C21	Ceramic condenser	0.1 μF (50 V)	TDK	1608	C1608JB1H104K
C22	Ceramic condenser	0.22 μF (25 V)	TDK	1608	C1608JB1E224K
C23	Ceramic condenser	0.22 μF (25 V)	TDK	1608	C1608JB1E224K
R_{S1}	Resistor	33 mΩ	KOA	SL1	SL1TTE33L0D
R_{S2}	Resistor	15 mΩ	KOA	SL1	SL1TTE15L0D
R2	Resistor	15 Ω	ssm	1608	RR0816P150D
R6	Resistor	51 kΩ	ssm	1608	RR0816P513D
R8	Resistor	300 kΩ	ssm	1608	RR0816P304D
R10	Resistor	100 kΩ	ssm	1608	RR0816P104D
R15	Resistor	24 kΩ	ssm	1608	RR0816P243D
R17	Resistor	10 kΩ	ssm	1608	RR0816P103D
R18	Resistor	33 kΩ	ssm	1608	RR0816P333D
R19	Resistor	39 kΩ	ssm	1608	RR0816P393D
R20	Resistor	20 kΩ	ssm	1608	RR0816P203D
R21	Resistor	24 kΩ	ssm	1608	RR0816P243D
R24	Resistor	47 kΩ	ssm	1608	RR0816P473D
R25	Resistor	9.1 kΩ	ssm	1608	RR0816P912D
R26	Resistor	15 kΩ	ssm	1608	RR0816P153D
R27	Resistor	16 kΩ	ssm	1608	RR0816P163D

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Component	Item	Specification	Vendor	Package	Parts No.
R28	Resistor	2 kΩ	ssm	1608	RR0816P202D
R32	Resistor	100 kΩ	ssm	1608	RR0816P104D
R33	Resistor	10 kΩ	ssm	1608	RR0816P103D
R34	Resistor	100 kΩ	ssm	1608	RR0816P104D
R39	Resistor	16 kΩ	ssm	1608	RR0816P163D
R40	Resistor	75 kΩ	ssm	1608	RR0816P753D
R41	Resistor	16 kΩ	ssm	1608	RR0816P163D
R45	Resistor	100 kΩ	ssm	1608	RR0816P104D
R46	Resistor	56 kΩ	ssm	1608	RR0816P563D
R51	Resistor	10 Ω	ssm	1608	RR0816P100D
R52	Resistor	10 Ω	ssm	1608	RR0816P100D

Note : NEC : NEC corporation
TOSHIBA : TOSHIBA CORPORATION
ROHM : ROHM CO., LTD.
SUMIDA : Sumida Corporation
TDK : TDK Corporation
KOA : KOA Corporation
ssm : SUSUMU CO., LTD.
SANYO : SANYO Electric Co., Ltd.

■ SELECTION OF COMPONENTS

• N-ch MOS FET

The N-ch MOS FET for switching use should be rated for at least +20% more than the input voltage. To minimize continuity loss, use a FET with low $R_{DS\ (ON)}$ between the drain and source. For high input voltage and high frequency operation, on-cycle switching loss will be higher so that power dissipation must be considered. In this application, the NEC μPA2752 is used. Continuity loss, on/off switching loss and total loss are determined by the following formulas. The selection must ensure that peak drain current does not exceed rated values.

Continuity loss : Pc

$$P_C = I_{D2} \times R_{DS\ (ON)} \times Duty$$

On-cycle switching loss : $P_{S\ (ON)}$

$$P_{S\ (ON)} = \frac{V_{D\ (Max)} \times I_D \times tr \times fosc}{6}$$

Off-cycle switching loss : $P_{S\ (OFF)}$

$$P_{S\ (OFF)} = \frac{V_{D\ (Max)} \times I_{D\ (Max)} \times tf \times fosc}{6}$$

Total loss : P_T

$$P_T = P_C + P_{S\ (ON)} + P_{S\ (OFF)}$$

• Inductor

In selecting inductors, it is of course essential not to apply more current than the rated capacity of the inductor, but also to note that the lower limit for ripple current is a critical point that if reached will cause discontinuous operation and a considerable drop in efficiency. This can be prevented by choosing a higher inductance value, which will enable continuous operation under light loads. Note that if the inductance value is too high, however, direct current resistance (DCR) is increased and this will also reduce efficiency. The inductance must be set at the point where efficiency is greatest.

Note also that the DC superimposition characteristics become worse as the load current value approaches the rated current value of the inductor, so that the inductance value is reduced and ripple current increases, causing loss of efficiency. The selection of rated current value and inductance value will vary depending on where the point of peak efficiency lies with respect to load current. Inductance values are determined by the following formulas.

The L value for all load current conditions is set so that the peak to peak value of the ripple current is 1/2 the load current or less.

16.8 V output

V_{IN} = 24 V (Max) , V_O = 16.8 V, I_O = 4.0 A, fosc = 500 kHz

1. N-ch MOS FET (μPA2752 : NEC product)

Main side

V_{DS} = 30 V, V_{GS} = ± 20 V, I_D = 8 A, R_{DS} (ON) = 25 mΩ (Typ) , Qg = 10 nC (Typ)

Synchronous rectification side

V_{DS} = 30 V, V_{GS} = ± 20 V, I_D = 8 A, R_{DS} (ON) = 25 mΩ (Typ) , Qg = 10 nC (Typ)

Drain current : Peak value

The peak drain current of this FET must be within its rated current.
If the FET's peak drain current is I_D, it is obtained by the following formula.

Main side

$$I_D \geq Io + \frac{V_{IN}-Vo}{2L} t_{ON}$$

$$\geq 4.0 + \frac{24-16.8}{2 \times 5.2 \times 10^{-6}} \times \frac{1}{500 \times 10^3} \times 0.7$$

$$\geq \underline{4.97\ A}$$

Synchronous rectification side

$$I_D \geq Io + \frac{Vo}{2L} t_{OFF}$$

$$\geq 4.0 + \frac{16.8}{2 \times 5.2 \times 10^{-6}} \times \frac{1}{500 \times 10^3} \times (1 - 0.7)$$

$$\geq \underline{4.97\ A}$$

2. Inductor (CDRH104R-5R2 : SUMIDA product)

5.2 μH (tolerance ± 30%) , rated current = 5.5 A

$$L \geq \frac{2\,(V_{IN}-Vo)}{Io} t_{ON}$$

$$\geq \frac{2 \times (24-16.8)}{4.0} \times \frac{1}{500 \times 10^3} \times 0.7$$

$$\geq \underline{5.04\ \mu H}$$

The load current satisfying the continuous current condition

$$Io \geq \frac{Vo}{2L} t_{OFF}$$

$$\geq \frac{16.8}{2 \times 5.2 \times 10^{-6}} \times \frac{1}{500 \times 10^{-3}} \times (1-0.7)$$

$$\geq \underline{0.97\ A}$$

Ripple current : Peak value

The peak ripple current must be within the rated current of the inductor.

If the peak ripple current is I_L, it is obtained by the following formula.

$$I_L \geq Io \frac{V_{IN}-Vo}{2L} t_{ON}$$

$$\geq 4.0 + \frac{24-16.8}{2 \times 5.2 \times 10^{-6}} \times \frac{1}{500 \times 10^{3}} \times 0.7$$

$$\geq \underline{4.97\ A}$$

Ripple current : peak-to-peak value

If the peak-to-peak ripple current is ΔI_L, it is obtained by the following formula.

$$\Delta I_L = \frac{V_{IN}-Vo}{L} t_{ON}$$

$$= \frac{24-16.8}{5.2 \times 10^{-6}} \times \frac{1}{500 \times 10^{3}} \times 0.7$$

$$\fallingdotseq \underline{1.94\ A}$$

12.6 V output

V_{IN} = 20 V (Max) , V_O = 12.6 V, I_O = 4.0 A, fosc = 500 kHz

1. N-ch MOS FET (μPA2752 : NEC product)

Main side

V_{DS} = 30 V, V_{GS} = ± 20 V, I_D = 8 A, R_{DS} (ON) = 25 mΩ (Typ) , Qg = 10 nC (Typ)

Synchronous rectification side

V_{DS} = 30 V, V_{GS} = ± 20 V, I_D = 8 A, R_{DS} (ON) = 25 mΩ (Typ) , Qg = 10 nC (Typ)

Drain current : Peak value

The peak drain current of this FET must be within its rated current.
If the FET's peak drain current is I_D, it is obtained by the following formula.

Main side

$$I_D \geq Io + \frac{V_{IN}-Vo}{2L} t_{ON}$$

$$\geq 4.0 + \frac{20-12.6}{2 \times 5.2 \times 10^{-6}} \times \frac{1}{500 \times 10^3} \times 0.63$$

$$\geq \underline{4.90\ A}$$

Synchronous rectification side

$$I_D \geq Io + \frac{Vo}{2L} t_{OFF}$$

$$\geq 4.0 + \frac{12.6}{2 \times 5.2 \times 10^{-6}} \times \frac{1}{500 \times 10^3} \times (1 - 0.63)$$

$$\geq \underline{4.90\ A}$$

2. Inductor (CDRH104R-5R2 : SUMIDA product)

5.2 µH (tolerance ± 30%) , rated current = 5.5 A

$$L \geq \frac{2\,(V_{IN}-Vo)}{Io}\,t_{ON}$$

$$\geq \frac{2\times\,(24-12.6)}{4.0}\times\frac{1}{500\times10^{3}}\times\;0.63$$

$$\geq \underline{4.67\ \mu H}$$

The load current satisfying the continuous current condition

$$Io \geq \frac{Vo}{2L}\,t_{OFF}$$

$$\geq \frac{12.6}{2\times5.2\times10^{-6}}\times\frac{1}{500\times10^{3}}\times\quad(1-0.63)$$

$$\geq \underline{897.0\ mA}$$

$$I_L \geq \quad I_O\quad\frac{V_{IN}-Vo}{2L}\;t_{ON}$$

$$\geq\ 4.0+\frac{20-12.6}{2\times5.2\times10^{-6}}\times\frac{1}{500\times10^{3}}\times\;0.63$$

$$\geq\ \underline{4.90\ A}$$

Ripple current : Peak-to-peak value

If the peak-to-peak ripple current is ΔI_L, it is obtained by the following formula.

$$\Delta I_L = \frac{V_{IN}-Vo}{L}\;t_{ON}$$

$$=\frac{20-12.6}{5.2\times^{-6}}\times\frac{1}{500\times10^{3}}\times\;0.63$$

$$\fallingdotseq\ \underline{1.79\ A}$$

3. Diode for bootstrap (SBS006 : SANYO product)

V_R (DC reverse voltage) = 30 V, Average output current = 500 mA, peak surge current = 10 A

V_F (forward voltage) = 0.35 V, at I_F = 300 mA

V_R : value that satisfies input voltage

Efficiency is somewhat rising in low leak Schottky diode by the use but even if the signal diode is used, it is enough. It is recommended to use low V_F. Also, capacitor for bootstrap must be very large than gate capacity of FET at main side. It is recommended to use the capacity of approximately 0.1 µF to 1.0 µF.

4. Charging current setting sense resistor (SL1TTE33L0F : KOA product)

33 mΩ

When + INE2 terminal (pin 12) voltage is 3.3 V, and the charging current (I_O) is 4.0 A, R4 is obtained by the following formula.

$$R4 = \frac{+\,INE2}{24.5 \times I_O}$$

$$= \frac{3.3}{24.5 \times 4.0}$$

$$\fallingdotseq \underline{33.0\ m\Omega}$$

5. Input current setting sense resistor (SL1TTE15L0F : KOA product)

15 mΩ

When + INE1 terminal (pin 7) voltage is 2.25 V, and the input current is 6.0 A, R1 is obtained by the following formula.

$$R1 = \frac{+\,INE1}{25 \times I1}$$

$$= \frac{2.25}{25 \times 6.0}$$

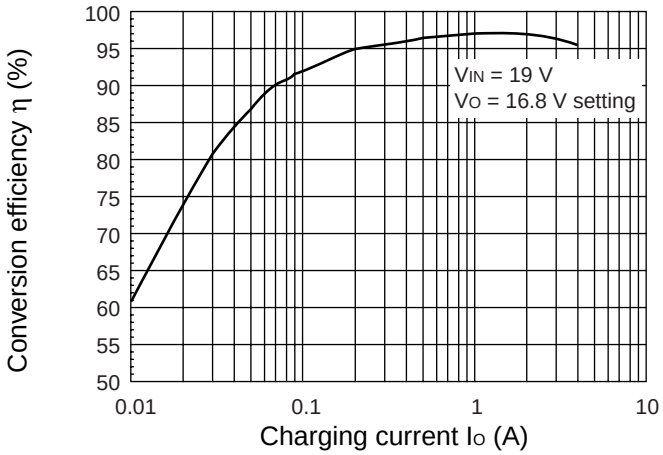
$$\fallingdotseq \underline{15.0\ m\Omega}$$

6. Switching P-ch FET (μPA1772 : NEC product, TPC8102 : TOSHIBA product)

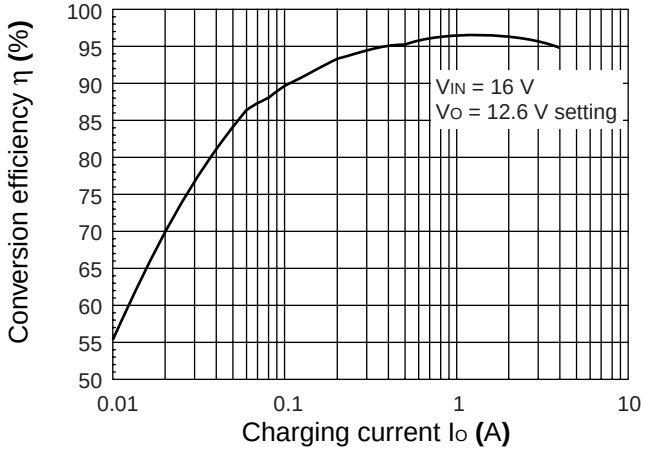
Q2-1, Q2-2, and Q5 must select an appropriate device according to the input current.

■ REFERENCE DATA

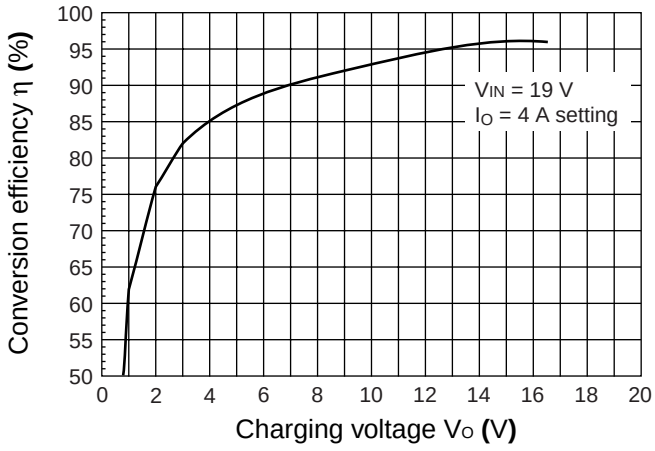
Conversion efficiency vs. Charging current (constant voltage mode)



Conversion efficiency vs. Charging current **(**constant voltage mode**)**



Conversion efficiency vs. Charging voltage **(**constant current mode**)**



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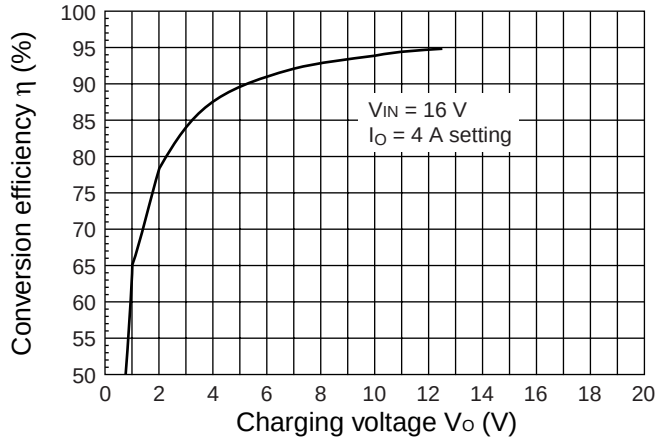
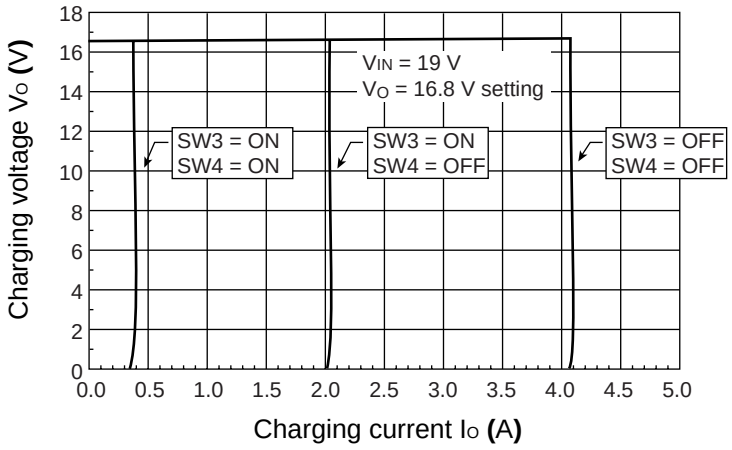
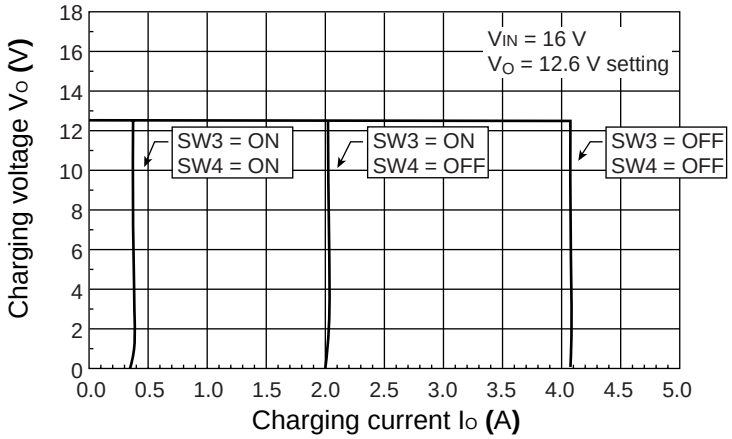
Conversion efficiency vs. Charging voltage (constant current mode)



Charging voltage vs. Charging current

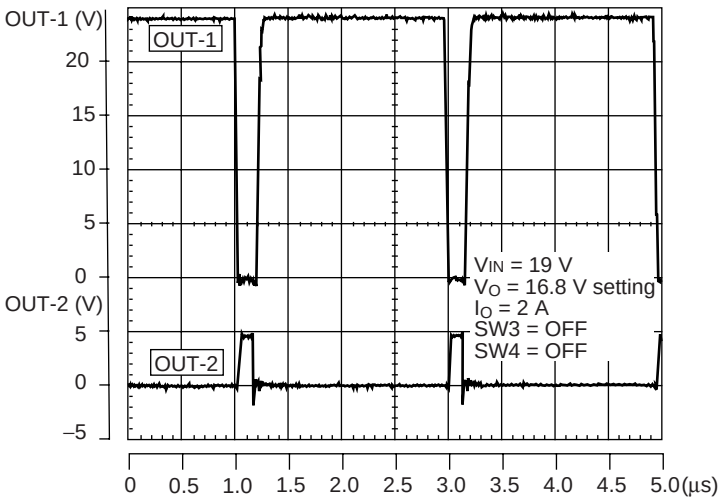


Charging voltage vs. Charging current

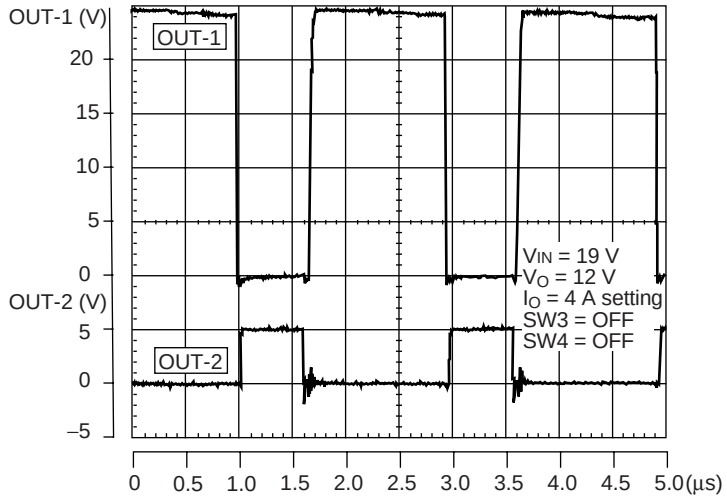


(Continued)

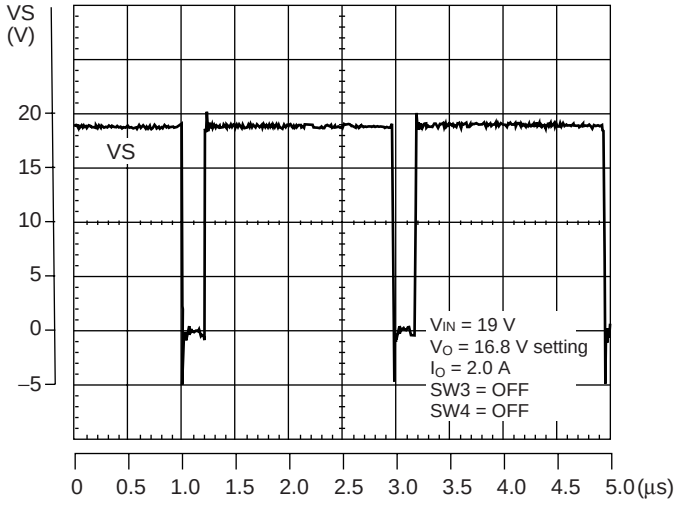
Switching waveform (constant voltage mode)



Switching waveform **(**constant current mode**)**

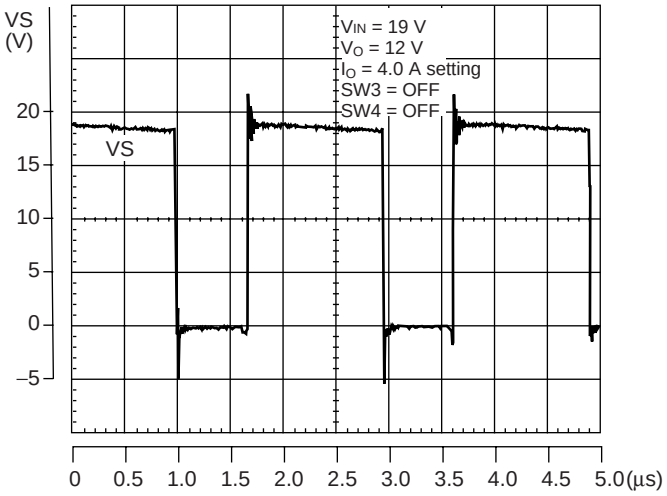


Switching waveform **(**constant voltage mode**)**

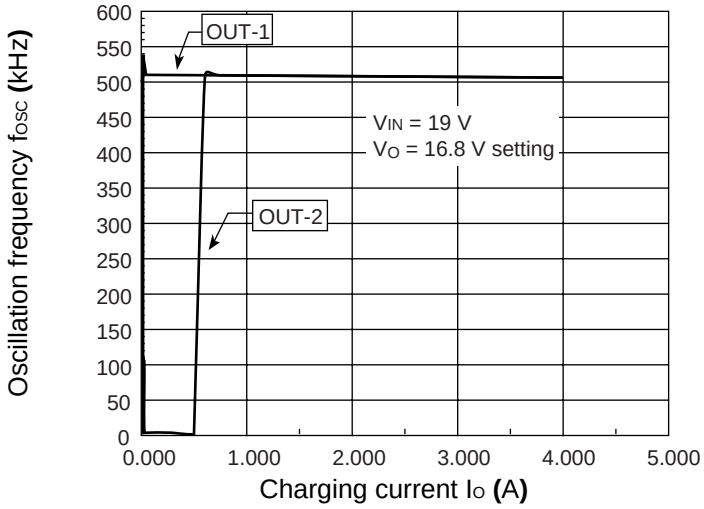


(Continued)

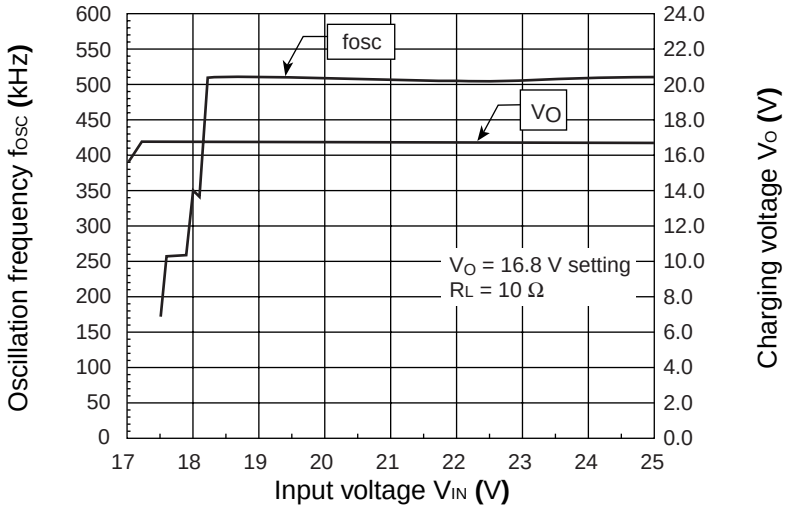
Switching waveform (constant current mode)



Oscillation frequency vs. Charging current

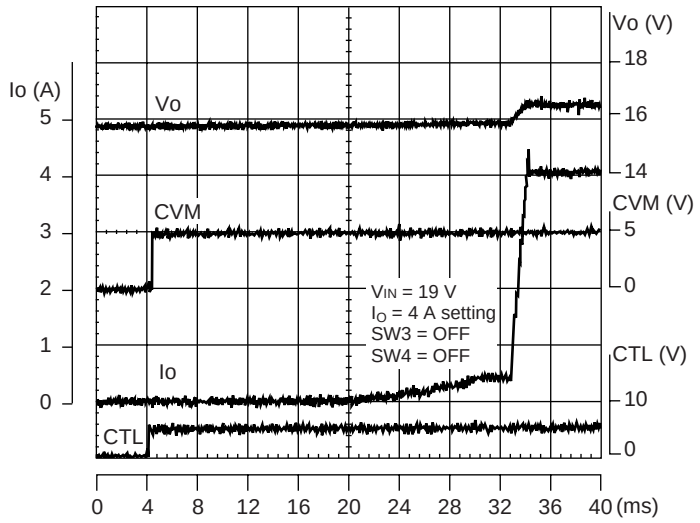


Oscillation frequency charging voltage vs. Input voltage

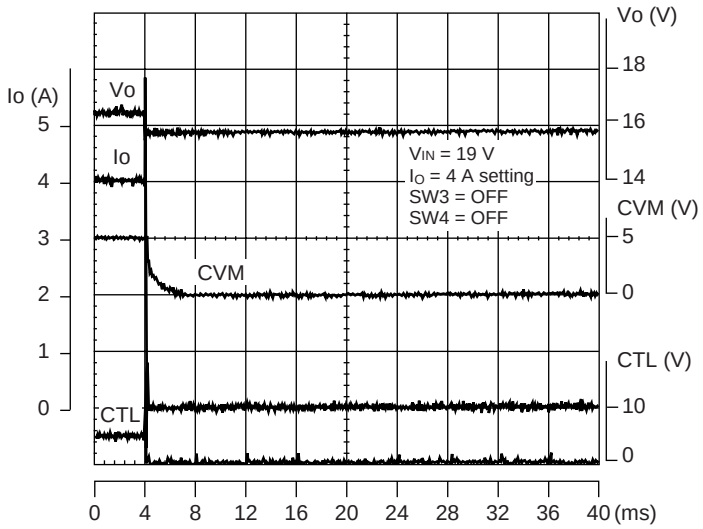


(Continued)

Soft-start operating waveform (constant current mode)

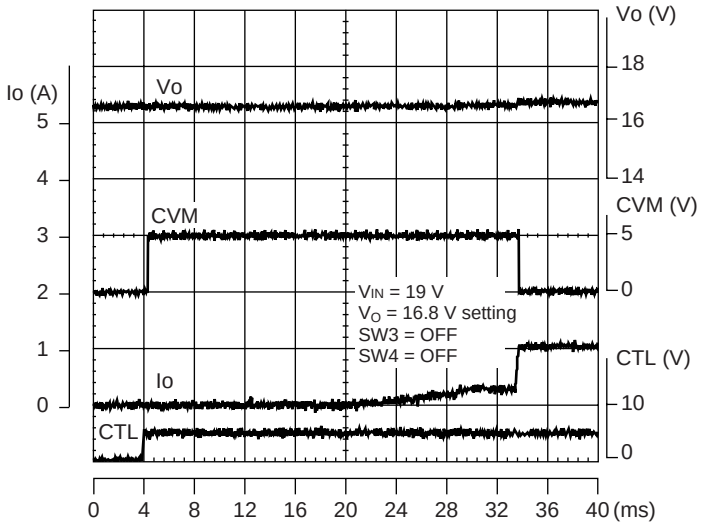


Soft-start operating waveform (constant current mode)

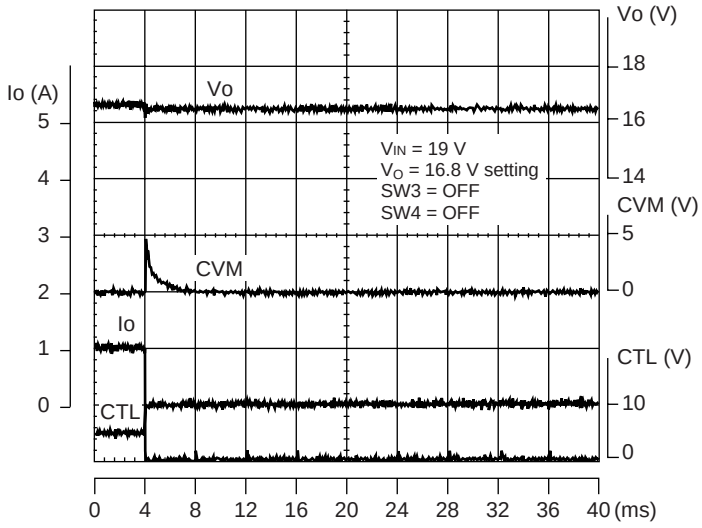


(Continued)

Soft-start operating waveform (constant voltage mode)

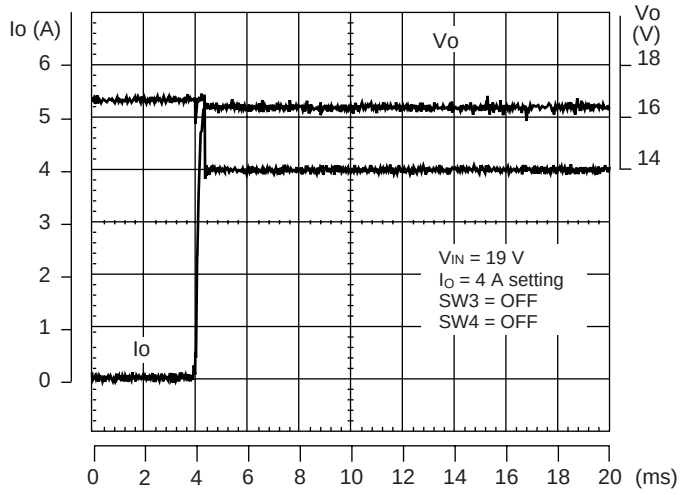


Soft-start operating waveform (constant voltage mode)

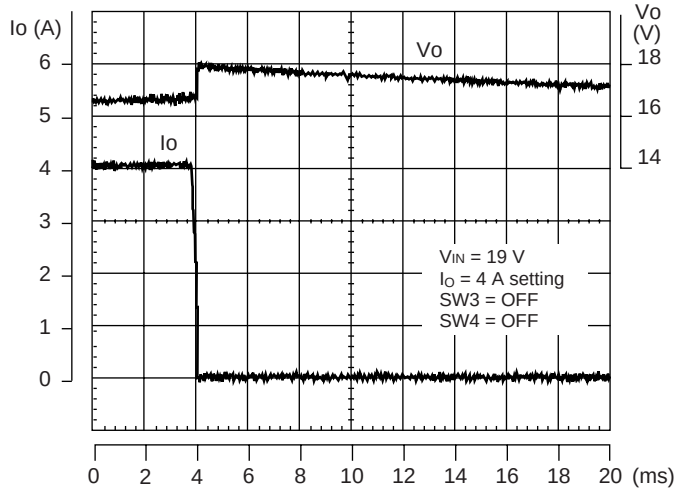


(Continued)

Load-step response operation waveform (C.V mode→C.C mode)



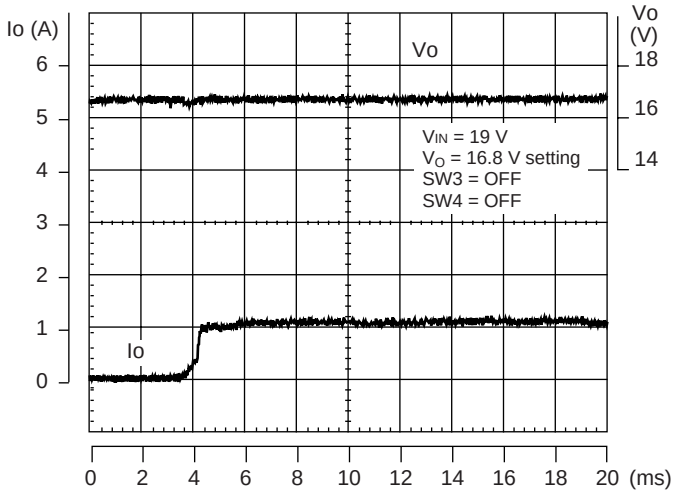
Load-step response operation waveform (C.C mode→C.V mode)



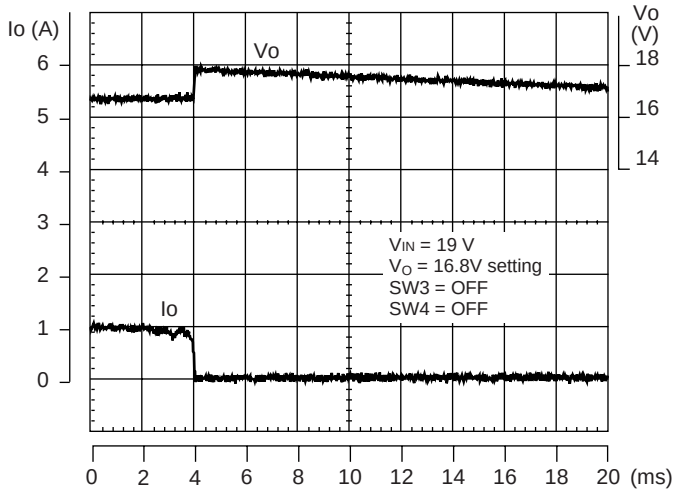
(Continued)

(Continued)

Load-step response operation waveform (C.V mode→C.V mode)



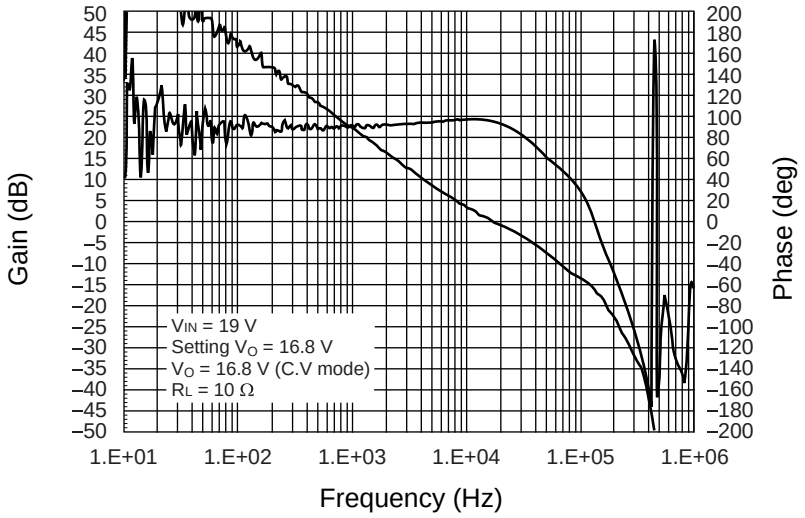
Load-step response operation waveform (C.V mode→C.V mode)



■ LOOP CHARACTERISTICS

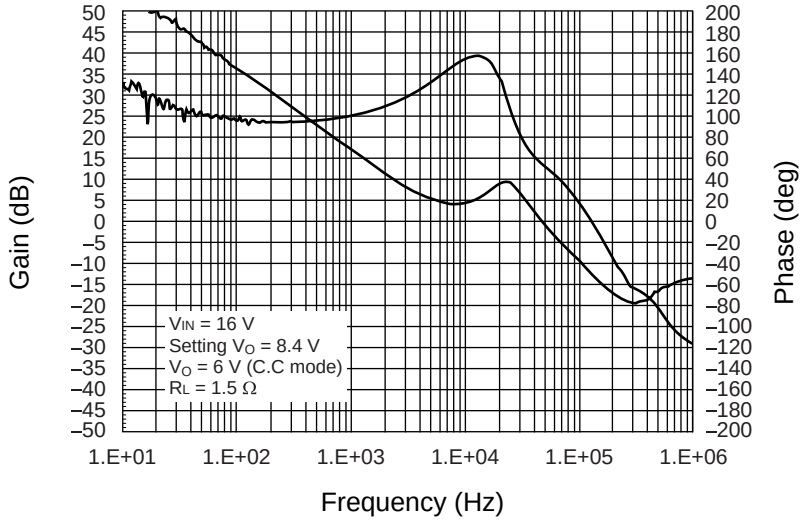
<Voltage mode>

Gain, phase vs. Frequency



<Current mode>

Gain, phase vs. Frequency



■ USAGE PRECAUTIONS

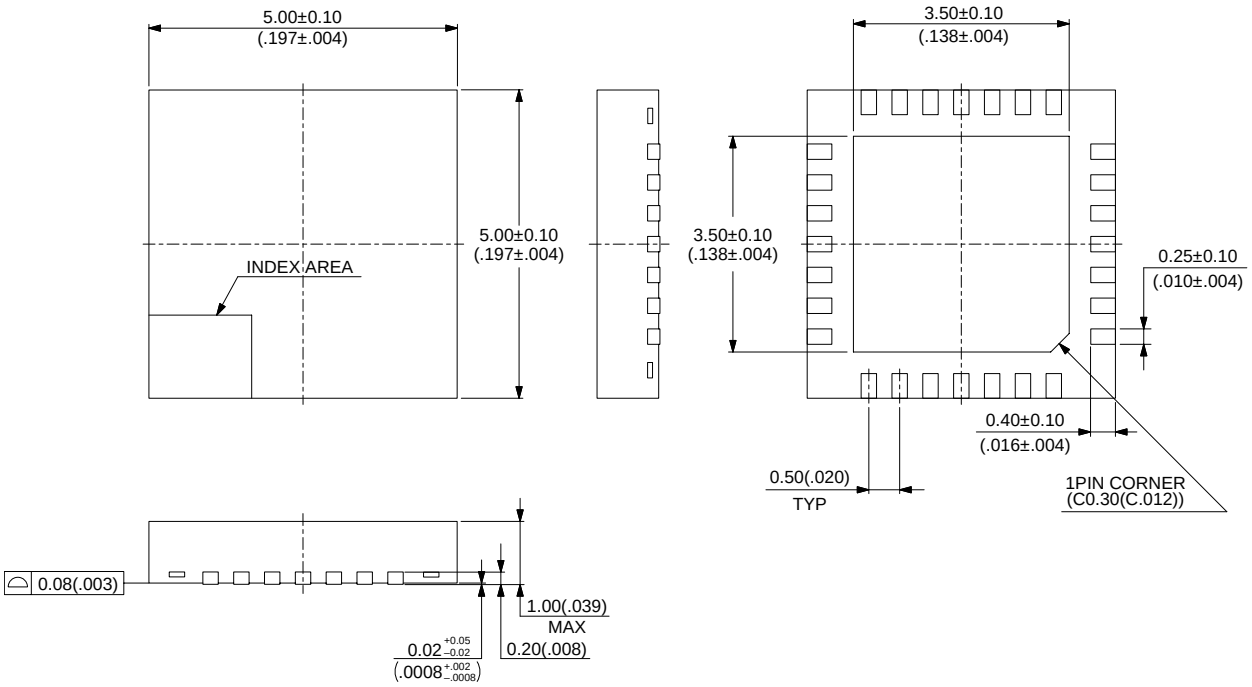
- Printed circuit board ground lines should be set up with consideration for common impedance.
- Take appropriate static electricity measures.
  - Containers for semiconductor materials should have anti-static protection or be made of conductive material.
  - After mounting, printed circuit boards should be stored and shipped in conductive bags or containers.
  - Work platforms, tools, and instruments should be properly grounded.
  - Working personnel should be grounded with resistance of 250 kΩ to 1 MΩ between body and ground.
- Do not apply negative voltages.
  - The use of negative voltages below –0.3 V may create parasitic transistors on LSI lines, which can cause abnormal operation.

■ ORDERING INFORMATION

Part number	Package	Remarks
MB39A119QN	28-pin plastic QFN (LCC-28P-M10)	

■ PACKAGE DIMENSION

28-pin plastic QFN
(LCC-28P-M10)



Dimensions in mm (inches) .
Note : The values in parentheses are reference values.

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